2016 IEEE Radio Frequency Integrated Circuits Symposium

San Francisco, California, USA
22–24 May 2016

IEEE

PROGRAM

San Francisco Marriott Marquis
and
Moscone Center

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
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IEEE Solid-State Circuits Society

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RFIC Plenary, Reception, Joint Industry Showcase & Interactive Forum

Sunday Evening, 22 May 2016
San Francisco Marriott Marquis
Yerba Buena Ballroom, Salons 7–15

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in San Francisco Marriott Marquis (Marriott), Yerba Buena Ballroom, Salons 7–15.

17:30–19:00, Marriott, Yerba Buena Ballroom, Salons 7–8 — The Plenary Session kicks off the evening with the Student Paper Awards, RFIC Industry Best Paper Award, and RFIC Tina Quach Service Award ceremony followed by two outstanding plenary speakers, Dr. Craig Barratt, Senior Vice President of Google Access, and Dr. K. Lawrence Loh, Corporate Senior Vice President of MediaTek.

19:00–21:00, Marriott, Yerba Buena Ballroom, Salons 9–15 — "Hot Chips and Cold Drinks" Reception and Joint Industry Showcase & Interactive Forum: Immediately following the Plenary Session is the RFIC Reception held in the foyer just outside the ballroom in Marriott. Drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest news in the wireless industry.

The Industry Showcase session, held concurrently with the plenary reception, will highlight 12 selected papers submitted by authors from the industry. Jointly with the Industry Showcase, the Interactive Forum Session will present 11 papers in poster format. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and Superpass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss these great events. Please see http://rfic-ieee.org/ for more details.

The RFIC Reception is sponsored by the RFIC Steering Committee, and through generous support of our corporate sponsors:

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RFIC Symposium Schedule (21–24 May 2016)

Event	Location	Sat 21 May	Sun 22 May	Mon 23 May	Tue 24 May
Registration	Marriott, Yerba Buena Foyer	08:00–19:00	07:00–19:00	07:00–19:00	07:00–12:00
Workshop Speakers' Breakfast	Moscone, Room 309		07:00–08:00		
Workshops & Short Courses	Moscone, Rooms 301–310		08:00–17:00		
Workshop Lunch	Moscone, Esplanade Foyer		12:00–13:00		
Plenary Session	Marriott, Salons 7–8		17:30–19:00		
Reception, Joint Industry Showcase & Interactive Forum	Marriott, Salons 9–15		19:00–21:00		
Workshop Breakfast	Moscone, Esplanade Foyer			07:00–08:00	
Speakers' Breakfast	Marriott, Nob Hill A–D			07:00–08:00	
Technical Sessions	Marriott, Salons 1–15			08:00–09:40 10:10–11:50 13:30–15:10 15:40–17:15	08:00–09:40 10:10–11:50
Panel Sessions	Marriott, Nob Hill A–D (Mon) Moscone, Room 310 (Tue)			12:00–13:00	

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The RFIC Symposium is the premier IC conference focused exclusively on the latest developments in RF, Microwave, and mm-Wave Integrated Circuit technology and innovation from both industry and academia.

Welcome Message from Chairs

We invite you to participate in the 2016 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held in San Francisco, California, on 22–24 May 2016. RFIC Symposium is the premier IC design conference focused exclusively on the latest advances in RF, Microwave and Millimeter Wave integrated circuit (IC) technologies and designs, as well as innovations in high frequency analog/mixed-signal ICs. We cordially invite you to participate in this global event!

As in past years, the RFIC Symposium, the International Microwave Symposium (IMS), ARFTG and the Industry Exhibition make up the "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. Come to Microwave Week to learn from the world's experts through a variety of technical sessions, interactive forums, panel sessions, workshops, short courses, industrial exhibits, application seminars and historical exhibits. Share your knowledge with others, expand your networks, catch up with old friends and colleagues, and return invigorated with new ideas and enthusiasm.

RFIC 2016 will continue to offer a number of initiatives: The 2-page industry brief format, allowing the latest state-of-the-art RF IC design results to be presented without requiring die photos and detailed schematics, will continue in 2016. The popular Industry Showcase Session, featuring poster presentations (and optional demos) of the most innovative and highly-rated industrial papers (both two and four page formats), will be the highlight during the RFIC Reception in the evening of Sunday, 22 May 2016. This year, the Industry Showcase will be held jointly with the Interactive Forum (IF) Session during the RFIC Reception, which will offer the attendees an enhanced interactive experience in a relaxed environment. To improve academic submissions, all of the RFIC student paper finalists will receive complimentary RFIC registration. Students may volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complimentary conference registration, meals, T-shirts, and other benefits. The joint RFIC/IMS PhD Student Sponsorship Initiative Program will continue to involve selected first and second-year PhD students to complete technical assignments during the conference in exchange for complimentary conference registrations, lodging and meals.

RFIC 2016 will open on Sunday, 22 May 2016, with ten workshops (four full-day and seven half-day), seven of which will be joint RFIC/IMS workshops. These workshops cover a wide range of topics including: "Phased arrays for handsets and cellular/integrated circuit, system and antenna realization of millimeter-wave front-ends for 5G radios", "Highly efficient 5G PA design", "How mm-wave systems reshape the future of telecom and sensing applications", "Circuit techniques and system architectures for carrier aggregation and multi-band radios", "Calibration and correction techniques for CMOS radios", "Enhanced IC design and waveform control techniques for wireless power transfer, energy harvesting, and RFIDs", "Frequency synthesizers of multi-band, multi-standard radios and Internet of Things (IoT)", "RF/analog IC design challenges in advanced CMOS technology", "High-efficiency broadband multimode multi standards amplifier design, high efficiency transmitters", "Millimeter-wave electronics: from applications to manufacturing" and "e-Health: implantable systems and communications in the human body". These workshops cover some of the hottest topics in RFIC designs.

The Plenary Session will be held on Sunday, 2 May 2016 in the evening. It will begin with conference highlights, followed by presentation of the Student Paper Awards and the Industry Best Paper Award. The Plenary continues with two outstanding keynote talks to be given by two renowned leaders in the RF/Microwave community. The first speaker is Dr. Craig Barratt, Senior Vice President of Google Access. The topic of his talk is *"*Innovations for Enabling Scalable Wireless Capacity*".* The second speaker is Dr. Lawrence Loh, Corporate Senior Vice President of MediaTek Inc. and President of MediaTek USA. His talk is titled "RFIC under Big Digital Semiconductor Companies: Challenges and Opportunities". Be sure not to miss these engaging presentations!

Immediately following the Plenary Session is the joint Industry Showcase Session and Interactive Session embedded in the RFIC Reception, providing a mixed experience of "hot chips" with cold drinks.

Technical papers will be presented during oral sessions throughout Monday and on Tuesday morning. The Interactive Forum, jointly with the Industry Showcase on Sunday evening, features carefully selected papers presented in poster format, allowing the attendees to speak directly with the authors. Two Panel Sessions will be featured during lunchtime on both Monday and Tuesday. The two controversial panel topics will be "Bio-Electronics: Silicon in MY Body?!" and "Patents — The Good, the Bad and the Ugly". These are certainly "sizzling" topics that are sure to spark lively debates among the panelists and audience. Make sure to bring your own opinions and questions to the panels.

This year, to enhance the experiences of the attendees, a new feature is added to allow onsite download of papers by registered audience during the Symposium.

San Francisco is trendy, artistic, progressive and tech-savvy. It is close to the Silicon Valley, and offers many attractions for visitors including the Golden Gate Bridge, Fisherman's Wharf, beaches, museums, excellent restaurants and close-by wineries.

On behalf of the RFIC 2016, we warmly welcome you to the 2016 RFIC Symposium! We are looking forward to an exciting program and hope you can join us in San Francisco, California! Please visit the RFIC 2016 website (http://rfic-ieee.org) for more details and update.

Albert Wang
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UC Riverside

Kevin Kobayashi
TPC Chair
Qorvo

Walid Ali-Ahmad
TPC Co-Chair
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Li-Wu Yang, *RF Integrated*
Gary Zhang, *Guangdong University of Technology*
Yuxiang Zheng, *Intel*

RFIC 2016 Schedule

Saturday, 21 May 2016

08:00–19:00 Registration — San Francisco Marriott Marquis (Marriott), Yerba Buena Foyer

Sunday, 22 May 2016

07:00–19:00 Registration — Marriott, Yerba Buena Foyer
07:00–08:00 Workshop Speakers' Breakfast — Moscone Center, Room 309
08:00–17:00 Workshops and Short Courses, Moscone Center, Rooms 301–310
12:00–13:00 Workshops Lunch — Moscone Center, Esplanade Foyer
17:30–19:00 RFIC Plenary — Marriott, Salons 7–8
19:00–21:00 Reception, Joint Industry Showcase & Interactive Forum — Marriott, Salons 9–15

Monday, 23 May 2016

07:00–19:00 Registration — Marriott, Yerba Buena Foyer
07:00–08:00 Speakers' Breakfast — Marriott, Nob Hill A–D
07:00–08:00 Workshop Breakfast — Moscone Center, Esplanade Foyer
08:00–17:00 Workshops and Short Courses, Moscone Center, Rooms 301–310
08:00–09:40 RMO1A — Marriott, Salons 1–3: *Advanced Passive, Switch and Active Device Modeling*
RMO1C — Marriott, Salons 10–12: *Next Generation Cellular and Wireless Connectivity Transceivers*
RMO1D — Marriott, Salons 13–15: *Advanced Techniques for RF Receivers*
09:40–10:10 Break — Marriott, Yerba Buena Foyer
10:10–11:50 RMO2A — Marriott, Salons 1–3: *Advances in Processing and Materials for RF Applications*
RMO2C — Marriott, Salons 10–12: *High-Performance Fractional-N Frequency Synthesizers*
RMO2D — Marriott, Salons 13–15: *High Performance RF Components*
12:00–13:00 Workshops Lunch — Moscone Center, Esplanade Foyer
12:00–13:00 RFIC Panel Session — Marriott, Nob Hill A–D
13:00–14:30 RFIC Steering Committee Lunch Meeting — Marriott, Foothill D
13:30–15:10 RMO3A — Marriott, Salons 1–3: *Mixed-Signal/RF Circuits for Wideband Transceivers*
RMO3C — Marriott, Salons 10–12: *Millimeter-Wave and THz Signal Sources*
RMO3D — Marriott, Salons 13–15: *Mixed-Signal Power Amplifiers*
15:10–15:40 Break — Marriott, Yerba Buena Foyer
15:40–17:15 RMO4A — Marriott, Salons 1–3: *Low-Power Transceivers*
RMO4B — Marriott, Salons 4–6: *Interferer Resilient Receivers*
RMO4D — Marriott, Salons 13–15: *Wideband Power Amplifiers*

Tuesday, 24 May 2016

07:00–12:00 Registration — Marriott, Yerba Buena Foyer
07:00–08:00 Speakers' Breakfast — Marriott, Nob Hill A–D
08:00–09:40 RTU1A — Marriott, Salons 1–3: *Spectrum Sensing*
RTU1C — Marriott, Salons 10–12: *Millimeter-Wave Systems and Components for W-band and Above*
RTU1D — Marriott, Salons 13–15: *Advanced PA Design Techniques*
09:40–10:10 Break — Marriott, Yerba Buena Foyer
10:10–11:50 RTU2A — Marriott, Salons 1–3: *Innovative Reconfigurable Transceiver Architectures*
RTU2C — Marriott, Salons 10–12: *5G Millimeter-Wave Components and Integrated Systems*
12:00–13:00 Joint RFIC/IMS Panel Session — Moscone Center, Room 310
13:30–15:00 RFIC TPC Lunch Meeting — Marriott, Nob Hill

Schedule: Plenary, Reception, Joint Industry Showcase & Interactive Forum

Sunday Evening, 22 May 2016
San Francisco Marriott Marquis

17:30–19:00
RFIC Plenary
Yerba Buena Ballroom, Salons 7–8

Chair: Albert Wang, University of California, Riverside

Co-Chair: Kevin Kobayashi, Qorvo

Co-Chair: Walid Ali-Ahmad, Qualcomm

17:30 Welcome Message from General Chair and TPC Chairs, Student Paper Awards, Industry Best Paper Award, Tina Quach Service Award

18:00 *Innovations for Enabling Scalable Wireless Capacity*
Craig Barratt, Google Access

18:30 *RFIC under Big Digital Semiconductor Companies: Challenges and Opportunities*
K. Lawrence Loh, MediaTek

19:00–21:00
"Hot Chips and Cold Drinks":
Reception, Joint Industry Showcase & Interactive Forum
Yerba Buena Ballroom, Salons 9–15

RFIC Reception starts immediately after the Plenary Session. The new Joint Industry Showcase and Interactive Forum sessions, held concurrently with the Reception, will highlight 12 selected industry papers and 11 interactive papers. Authors of these papers will be present to discuss their innovative work, summarized in poster format, good for interactions between the authors and the audience. Some industry showcase papers will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Best Student Paper Award Finalists

One of the missions of RFIC Symposium is to promote academic research and education. As part of the Best Student Paper Award program, several finalists are nominated every year by RFIC Technical Program Committee to enter the final contest where the top-three best papers are selected. All finalists benefit from a complimentary RFIC registration. The top-three Best Student Papers will be announced during the RFIC Plenary Session on 22 May 2016 in San Francisco. Each winner will receive an honorarium and a plaque. This year's Best Student Paper Award finalists are:

A Multiphase Switched Capacitor Power Amplifier in 130nm CMOS
Wen Yuan, Jeffrey S. Walling
University of Utah, USA
RMO3D-4 14:30

An Efficient 210GHz Compact Harmonic Oscillator with 1.4dBm Peak Output Power and 10.6% Tuning Range in 130nm BiCMOS
Chen Jiang[1], Andreia Cathelin[2], Ehsan Afshari[1]
[1]Cornell University, USA, [2]STMicroelectronics, France
RMO3C-5 14:50

A Mixer Frontend for a Four-Channel Modulated Wideband Converter with 62dB Blocker Rejection
Douglas Adams[1], Yonina Eldar[2], Boris Murmann[1]
[1]Stanford University, USA, [2]Technion, Israel
RTU1A-4 09:00

A 2.22–2.92GHz LC-VCO Demonstrated with an Integrated Magnetic-Enhanced Inductor in 180nm SOI CMOS
Rui Ma[1], Fei Lu[1], Qi Chen[1], Chenkun Wang[1], Feng Liu[2], Wanghui Zou[3], Albert Wang[1]
[1]University of California, Riverside, USA, [2]Wuhan University, China, [3]Hunan University, China
RMO2A-3 10:50

An 802.11 a/b/g/n Digital Fractional-N PLL with Automatic TDC Linearity Calibration for Spur Cancellation
Dongyi Liao[1], Hechen Wang[1], Fa Foster Dai[1], Yang Xu[2], Roc Berenguer[3]
[1]Auburn University, USA, [2]Illinois Institute of Technology, USA, [3]Innophase, USA
RMO2C-5 11:30

A Wideband Voltage Mode Doherty Power Amplifier
Voravit Vorapipat, Cooper Levy, Peter M. Asbeck
University of California, San Diego, USA
RMO4D-4 16:40

A Fully Integrated Software-Defined FDD Transceiver Tunable from 0.3-to-1.6GHz
Dong Yang[1], Hazal Yüksel[2], Christopher Newman[2], Changhyuk Lee[3], Zachariah Boynton[2], Noman Paya[4], Miles Pedrone[5], Alyssa Apsel[2], Alyosha Molnar[2]
[1]Broadcom, USA, [2]Cornell University, USA, [3]Columbia University, USA, [4]Texas Instruments, USA, [5]IBM, USA
RTU2A-3 10:50

Sunday, 22 May 2016 **17:30–18:00** **Marriott Salons 7–8**

A Fully Integrated 320pJ/b OOK Super-Regenerative Receiver with -87dBm Sensitivity and Self-Calibration

Vahid Dabbagh Rezaei[1], Stephen J. Shellhammer[2], Mohamed Elkholy[1], Kamran Entesari[1]
[1]Texas A&M University, USA, [2]Qualcomm, USA
RMO4A-2 16:00

A 28GHz Quadrature Fractional-N Synthesizer for 5G Mobile Communication with Less Than 100fs Jitter in 65nm CMOS

W. El-Halwagy[1], A. Nag[1], P. Hisayasu[2], F. Aryanfar[2], P. Mousavi[1], M. Hossain[1]
[1]University of Alberta, Canada, [2]Samsung, USA
RMO2C-1 10:10

A 5GHz All-Passive Negative Feedback Network for RF Front-End Self-Steering Beam-Forming with Zero DC Power Consumption

Min-Yu Huang, Taiyun Chi, Hua Wang
Georgia Institute of Technology, USA
RMO1D-3 08:40

A 42mW 26–28GHz Phased-Array Receive Channel with 12dB Gain, 4dB NF and 0dBm IIP3 in 45nm CMOS SOI

Umut Kodak, Gabriel M. Rebeiz
University of California, San Diego, USA
RTU2C-3 10:50

A 28-GHz 4-Channel Dual-Vector Receiver Phased Array in SiGe BiCMOS Technology

Yi-Shin Yeh[1], Benjamin Walker[2], Ed Balboni[2], Brian A. Floyd[1]
[1]North Carolina State University, USA, [2]Analog Devices, USA
RTU2C-4 11:10

0.84-THz Imaging Pixel with a Lock-In Amplifier in CMOS

Rui Xu[1], Ja-Yol Lee[2], Dae Yeon Kim[1], Shinwoong Park[3], Zeshan Ahmad[1], Kenneth K. O[1]
[1]University of Texas at Dallas, USA, [2]ETRI, Korea, [3]Virginia Tech, USA
RMO3A-3 14:10

Student Paper Contest Eligibility: The student must have been a full time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must be the lead author of the paper and must present the paper at the Symposium. A memorandum will be automatically sent to the advisor to certify that the work was done by the student.

Judging Procedure: Student papers are reviewed and admitted to the conference in the same manner as all other conference papers. After the paper review process is completed, each technical program subcommittee recommends a maximum of two student papers as finalists. A student paper contest committee consisting of one representative from each subcommittee is then formed to review all the finalists and select the top three papers. Papers accepted for the competition are judged on content.

Stefano Pellerano
Student Programs Chair
Intel

Plenary Speaker 1

Craig Barratt
Senior Vice President, Google Access

Innovations for Enabling Scalable Wireless Capacity

Abstract: Wireless technologies are steadily approaching Shannon limits. Network densification (reuse), unlocking swathes of new spectrum, and spatial multiplexing gains via multiple antennas are key to delivering higher network capacity. Enabling these concepts to coherently work together — while also achieving practical, lower cost networks — is itself a key challenge. Dr. Barratt will share perspectives on technologies that enable more efficient use of spectrum and greater network capacity to support the future growth of the wireless Internet.

About Craig Barratt

Craig Barratt is an industry leader in wireless technology and communications. He joined Google in 2013, and oversees its Access division, which includes Google Fiber, the gigabit-speed internet service, OnHub, Google's smart Wi-Fi router, and Railtel, its project to provide Wi-Fi service at up to 400 railway stations across India. The co-inventor of 34 US patents, Craig was previously President and CEO of Atheros, one of the semiconductor pioneers of Wi-Fi, where he led its public offering in 2004 and sale to Qualcomm for US$3.6 billion in 2011. He is sometimes referred to in the industry as "the other Craig Barratt" to avoid confusion with former Chairman and CEO of Intel, Craig Barrett. Craig holds PhD and Master's degrees in electrical engineering from Stanford University, and B.Eng. and B.Sc. degrees from the University of Sydney. He is the co-author of a book on Linear Controller Design and several open source projects.

Plenary Speaker 2

K. Lawrence Loh
Corporate Senior Vice President, MediaTek
President, MediaTek USA

RFIC under Big Digital Semiconductor Companies: Challenges and Opportunities

Abstract: In recent years the semiconductor industry has entered a massive wave of consolidation due to slowing growth and rising costs. Semiconductor companies, excluding foundries, memory makers and vertically integrated companies, have been gradually divided into two categories: larger-scale SOC platforms based "big-digital" companies and moderate-to-smaller scale IC components based "non-big-digital" companies. For roughly over 15 years, RFIC designers of "big digital" companies have demonstrated increasingly digitized RF circuits and systems to take advantage of continually shrinking process technologies. Nevertheless these designers are also facing unprecedented challenges to share bulk substrates of sensitive RF/analog circuits with increasingly noisy digital high speed and high switching-current circuits. When Moore's Law is reaching its plateaus of frequency walls and per-transistor costs, RF designers would need to further deal with sophisticated cost/performance tradeoffs to decide on the right technologies and partitions between RFICs and SOCs. Although RFIC has played its traditional role as the "enabler" of wireless SOC platforms, opportunities have continued to grow to motivate more innovations to differentiate from other SOC platform providers. In this talk, we will address potential opportunities and associated technical challenges from a "big-digital" company's RFIC designers' views.

About K. Lawrence Loh

Dr. Kou-Hung Lawrence Loh is a Corporate Senior Vice President of MediaTek Inc., responsible for centralized corporate R&D and engineering functions including RF, analog/mixed-signal and circuits/hardware engineering and technology development for all MediaTek's product lines including wireless communication, mobile application processors, wireless connectivity, home entertainment, optical storage and broadband/networking business. He is also President of MediaTek USA overseeing the company's global operations in Europe and America. Dr. Loh started his first circuit design position at IMP and later he joined Cirrus Logic, where his last position was Director of Analog IC Engineering. In 1998, Dr. Loh founded Silicon Bridge Inc. Before joining MediaTek in 2004, Dr. Loh had contributed to IC design industry in areas of read/write channels for magnetic and optical storage, high-performance analog filters, solid-state fingerprint sensors, high-speed SERDES and wireline transceivers for various business applications.

Dr. Loh received his Ph.D. degree in Electrical Engineering from Texas A&M University, College Station, Texas. He has authored/co-authored dozens of technical papers/patents on IC/system designs. Dr. Loh served on ISSCC Technical Program Committee. He is on Steering Committee of A-SSCC and Board of Directors for Global Semiconductor Alliance (GSA).

Sunday, 22 May 2016 **18:30–19:00** **Marriott Salons 7–8**

"Hot Chips and Cold Drinks" Industry Showcase

Chair: Nick Cheng, Skyworks Solutions

The Industry Showcase session, held concurrently with the plenary reception and the Interactive Forum, will highlight 12 selected papers submitted by authors from the industry. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. A Best Industry Paper Award will be awarded to the author of one selected paper among these. This year's Industry Showcase papers are:

Experimental Characterization of Packaged Switch Devices for RF and Millimeter-Wave Applications
[1]CRISMAT, France, [2]NXP Semiconductors, France
Thanh Vinh Dinh[1], Philippe Descamps[1], Daniel Pasquet[1], Dominique Lesénéchal[1], Sidina Wane[2]
RMO1A-1 08:00

On the Characterization of Thermal Coupling Resistance in a Current Mirror
Skyworks Solutions, USA
Tianbing Chen, Bhuvaneshwaran Vijayakumar, Tzung-Yin Lee, Chun-Wen Paul Huang, Mike McPartlin
RMO1A-4 09:00

A Direct-Conversion Transmitter for Small-Cell Cellular Base Stations with Integrated Digital Predistortion in 65nm CMOS
Analog Devices, USA
Chris Mayer, David J. McLaurin, Jason Fan, Steve Bal, Christopher Angell, Oliver E. Gysel, Martin McCormick, Manish J. Manglani, Richard P. Schubert, Brian Reggiannini, John Kornblum, Lu Wu, Lex Leonard, Shipra Bhal, Alex Kagan, Tony Montalvo
RMO1C-1 08:00

A Direct-Conversion Receiver for Multi-Carrier 3G/4G Small-Cell Base Stations in 65nm CMOS
Analog Devices, USA
David J. McLaurin, Kevin G. Gard, Richard P. Schubert, Robert Glenn, David Alldred, Trevor C. Caldwell, Zhao Li, Steve Bal, Christopher Angell, Jianxun Fan, Manish J. Manglani, Brian Reggiannini, John Kornblum, Lu Wu, Chris Mayer, Oliver E. Gysel, Wei An, Shipra Bhal, Bruce E. Wilcox, Tony Montalvo
RMO1C-3 08:40

Single Crystal AlGaN Bulk Acoustic Wave Resonators on Silicon Substrates with High Electromechanical Coupling
Akoustis Technologies, USA
Jeffrey B. Shealy, Michael D. Hodge, Pinal Patel, Ramakrishna Vetury, Alexander Yu. Feldman, Shawn R. Gibb, Mark D. Boomgarden, Michael P. Lewis, James B. Shealy, James R. Shealy
RMO2A-1 10:10

A 28GHz SiGe BiCMOS Phase Invariant VGA
IBM, USA
B. Sadhu, J.F. Bulzacchelli, Alberto Valdes-Garcia
RMO2D-4 11:10

A 28nm, 475mW, 0.4-to-1.7GHz Embedded Transceiver Front-End Enabling High-Speed Data Streaming Within Home Cable Networks

[1]Broadcom, USA, [2]Broadcom, Taiwan, [3]imec, Belgium, [4]Broadcom, The Netherlands, [5]Apple, USA

S. Spiridon[1], D. Koh[1], J. Xiao[1], M. Brandolini[1], B. Shen[1], C.-M. Hsiao[2], H. Huang[2], D. Guermandi[3], S. Bozzola[4], H. Yan[4], M. Introini[4], L. Krishnan[1], K. Raviprakash[5], Y. Shin[1], R. Gomez[1], J. Chang[1]

RMO3A-5 14:50

A 20dBm Configurable Linear CMOS RF Power Amplifier for Multi-Standard Transmitters

DSP Group, Israel

Eli Schwartz, Sergey Anderson, Alex Mostov, Ilya Sima, Udi Suissa, Ron Pongratz, Amit Ezer, Avi Cohen, Michael Gulko, Nadav Snir, Asaf Elazari, Avi Bauer

RTU1D-3 08:40

Single Die Broadband CMOS Power Amplifier and Tracker with 37% Overall Efficiency for TDD/FDD LTE Applications

Skyworks Solutions, USA

Florinel Balteanu

RTU1D-4 09:00

A 30-MHz-to-3-GHz CMOS Array Receiver with Frequency and Spatial Interference Filtering for Adaptive Antenna Systems

NEC, Japan

Naoki Oshima, Masaki Kitsunezuka, Kenta Tsukamoto, Kazuaki Kunihiro

RTU2A-1 10:10

A Wideband Single-PLL RF Receiver for Simultaneous Multi-Band and Multi-Channel Digital Car Radio Reception

[1]NXP Semiconductors, The Netherlands, [2]NXP Semiconductors, Germany

Jan van Sinderen[1], Lucien Breems[1], Hans Brekelmans[1], Frank Leong[1], Nenad Pavlovic[1], Robert Rutten[1], Jan Niehof[1], Raf Roovers[1], Bernard Burdiek[2], Jochen Rudolph[2], Ulrich Moehlmann[2], Peter Blinzer[2], Manfred Biehl[2], Niels Gabriel[2], Andreas Wichern[2], Gerd Schippmann[2], Frank Rethmeier[2], Janusz Klimczak[2], Joerg Wenzel[2], Ralf-Gero Pilaski[2]

RTU2A-2 10:30

A 60GHz Packaged Switched Beam 32nm CMOS TRX with Broad Spatial Coverage, 17.1dBm Peak EIRP, 6.1dB NF at <250mW

IBM, USA

B. Sadhu, Alberto Valdes-Garcia, J.-O. Plouchart, H. Ainspan, A.K. Gupta, M. Ferriss, M. Yeck, M. Sanduleanu, X. Gu, C. Baks, D. Liu, D . Friedman

RTU2C-1 10:10

Sunday, 22 May 2016
19:00–21:00
Marriott Salons 9–15
Session RSUIF: Interactive Forum
Chair: Brian Floyd, North Carolina State University
Co-Chair: Hua Wang, Georgia Tech

RSUIF-1 19:00
Analysis and Implementation of Quick-Start Pulse Generator by CMOS Flipped on Quartz Substrate

Parit Kanjanavirojkul, Nguyen Ngoc Mai-Khanh, Tetsuya Iizuka, Toru Nakura, Kunihiro Asada; University of Tokyo, Japan

Abstract: This paper presents a pulse generator (PG), aiming at low power applications with low duty cycle. The PG is capable to provide an efficient pulse generation at a frequency near and beyond CMOS's F_{max}. It also features quick starting time and zero stand-by power. The PG is designed by CMOS flipped to a transmission line resonator on a quartz substrate. Efficiency, oscillation frequency and pulse duration can be tuned by adjusting the transmission line parameters. Two prototypes with coupling gap of 1μm and 2μm at 11.5GHz oscillation frequency are fabricated. Measurement shows energy conversion efficiency of 2.37% and 2.05%, respectively, with energy consumption of 5.4pJ/pulse.

RSUIF-2 19:00
An 8–10GHz Upconversion Mixer, with a Low-Frequency Calibration Loop Resulting in Better Than -73dBc In-Band Spurs

Johan C.J.G. Withagen, A.J. Annema, Bram Nauta, F.E. van Vliet; University of Twente, The Netherlands

Abstract: An 8–10 GHz X-band upconversion quadrature mixer stage implemented in 250 nm SiGe BiCMOS is presented. Orthogonality of the spurious responses caused by clock feed through, I/Q mismatch and baseband harmonics after self-mixing was exploited to realize a baseband calibration scheme reducing all in-band spurs down to below -73dBc, for baseband signals up to a bandwidth of 2MHz and with an IF center frequency up to 100MHz. Utilizing a low-frequency output spectrum analysis of an integrated self-mixer at the upconversion mixer output for calibration, eliminates the need for expensive microwave frequency spectrum analyzers.

RSUIF-3 19:00

A Damping Pulse Generator Based on Regenerated Trigger Switch

Nguyen Ngoc Mai-Khanh, Tetsuya Iizuka, Kunihiro Asada; University of Tokyo, Japan

Abstract: This paper presents a new microwave pulse generator based on a positive feedback scheme. The positive feedback is proposed to produce a quick regenerated trigger switch to spark an LC circuit and then generate a shock pulse. The proposed circuit does not need any edge-sharpener circuit or over-sized transistors and hence requires a small chip area. A testing prototype is fabricated in a 0.18-μm CMOS technology ($f_{max} \approx 40$ GHz). A 120-mV peak-to-peak pulse output at a center frequency of 13.4GHz with a wide bandwidth of 7.46 GHz is measured. The pulse center frequency is achieved with 33.5% of the f_{max}. The proposed pulse generator is suitable for transmitter design in low-cost low-power wideband sensing network applications.

RSUIF-4 19:00

A 6GS/s 9.5 Bit Pipelined Folding-Interpolating ADC with 7.3 ENOB and 52.7dBc SFDR in the 2nd Nyquist Band in 0.25μm SiGe-BiCMOS

M. Buck[1], M. Grözing[1], R. Bieg[1], J. Digel[1], X.-Q. Du[1], P. Thomas[1], M. Berroth[1], M. Epp[2], J. Rauscher[2], M. Schlumpp[2]; [1]Universität Stuttgart, Germany, [2]Airbus DS Electronics and Border Security, Germany

Abstract: A pipelined folding-interpolating ADC with a distributed quantizer is presented. The low-mismatch analog frontend provides for excellent SFDR and SNDR without calibration or digital post processing. The algorithm of the digital coder relaxes the requirements on the interface between analog core and digital coder. The single-core ADC achieves 7.3 ENOB and a SFDR of 52.7 dBc in the 2nd Nyquist band at 6 GS/s with an overall power consumption of 10.2 W.

RSUIF-5 19:00

RF Induced Communication Errors in RFFE MIPI Controlled Power Amplifiers

Douglas Teeter, Ming Ji, David Southcombe, Praveen Nadimpalli, David Widay; Qorvo, USA

Abstract: As the number of RF components increases inside mobile devices, the industry has rapidly adopted and utilized MIPI's RFFE serial bus specification to communicate with these devices and reduce the amount of control line routing between components. However, the use of a serial bus within the RF front end increases the risk that RF energy, particularly from the Power Amplifier (PA), can corrupt the RFFE bus communication. RF coupling to areas such as the RFFE serial clock (SCLK) signal seen within the PA's RFFE state machine can result in communication errors with the PA. This coupling can be to the SCLK signal itself, or to the PA's CMOS controller's ground reference. PA designers must pay special attention to the positioning and design of the CMOS controller and the internal routing of signals to the controller to avoid these problems. This paper provides a detailed analysis of how RF energy coupling to the internal CMOS controller can create "glitches" on the SCLK signal that cause communication errors. A simple example is provided to illustrate how choices in PA module layout can significantly impact these issues. A natural extension of these concepts applies to phone or radio board layouts, too.

RSUIF-6 19:00

A Highly-Efficient 138–170GHz SiGe HBT Frequency Doubler for Power-Constrained Applications

Christopher Coen[1], Saeed Zeinolabedinzadeh[1], Mehmet Kaynak[2], Bernd Tillack[2], John D. Cressler[1]; [1]Georgia Institute of Technology, USA, [2]IHP, Germany

Abstract: This paper presents a 138–170 GHz active frequency doubler implemented in a 0.13 μm SiGe BiCMOS technology with a peak output power of 5.6 dBm and peak power-added efficiency of 7.6%. The doubler achieves a peak conversion gain of 4.9 dB and consumes only 36 mW of DC power at peak drive through the use of a push-push frequency doubling stage optimized for low drive power, along with a low-power output buffer. To the best of our knowledge, this doubler achieves the highest output power, efficiency, and fundamental frequency suppression of all D-band and G-band SiGe HBT frequency doublers to date.

RSUIF-7 19:00

A Transformer-Based Inverted Complementary Cross-Coupled VCO with a 193.3dBc/Hz FoM and 13kHz 1/f³ Noise Corner

Song Hu, Fei Wang, Hua Wang; Georgia Institute of Technology, USA

Abstract: This paper presents a transformer-based inverted complementary cross-coupled voltage-controlled oscillator (VCO) topology. Without compromising the start-up condition, it isolates the source nodes for the cross-coupled devices, suppresses the flicker noise up-conversion, and thus results in a superior phase noise performance. A prototype is implemented in a standard 130nm bulk CMOS process with a core area of 0.34mm^2. At 1.86GHz, the measured FoM is 190.3/192.2/193.3dBc/Hz at 10k/100k/ 1MHz offsets with a 1/f³ phase noise corner of only 13kHz. The VCO consumes 1.1mA from a 1.5V supply. High FoM and low 1/f³ phase noise corners are consistently achieved over 20.8% frequency tuning range (1.68–2.07GHz).

RSUIF-8 19:00

A Low Power High Performance PLL with Temperature Compensated VCO in 65nm CMOS

V. Ravinuthula, S. Finocchiaro; Texas Instruments, USA

Abstract: This paper presents a fully integrated, low power, low noise Phase-Locked Loop (PLL) implementing a temperature compensated class-C dual-core Voltage Controlled Oscillator (VCO) achieving state of the art phase noise performance. The PLL exhibits low integrated noise enabling the integration of low jitter clocks for high performance data converters supporting GSM requirements for Wireless Infrastructure applications. Implemented in 65 nm CMOS process, the 8 GHz VCO achieves Phase Noise of -140 dBc/Hz at 1 MHz offset measured at 2 GHz output. The PLL exhibits -60 dBc rms noise integrated from 10 kHz to 20 MHz, while maintaining lock for the ambient temperature range -40°C to 105°C, and dissipating ≈ 140 mW.

RSUIF-9 19:00

An Ultra-Wideband Low-Power ADPLL Chirp Synthesizer with Adaptive Loop Bandwidth in 65nm CMOS

Liheng Lou, Bo Chen, Kai Tang, Supeng Liu, Yuanjin Zheng; Nanyang Technological University, Singapore

Abstract: The paper presents an ultra-wideband, low-power frequency synthesizer for Ku-band FMCW radars. This ADPLL-based frequency synthesizer generates chirps with configurable rate from 0.4 to 3.2GHz/ms, up to 2GHz bandwidth in triangle or sawtooth mode. Adaptive loop bandwidth is adopted to reduce variations of the loop tracking characteristic during ramping under different chirp rate, by which, a low frequency RMS error of ~179kHz is achieved for the chirp rate below 2GHz/ms. Fabricated in a 65nm CMOS, the synthesizer generates a wideband chirp from 13.8GHz to 15.8GHz, and consumes 36.3mW, featuring state of the art performance.

RSUIF-10 19:00

Millimeter-Wave Bandpass Filter Using High-Q Conical Inductors and MOM Capacitors

Venkata Narayana Rao Vanukuru; GLOBALFOUNDRIES, India

Abstract: This paper describes an efficient implementation of a lumped millimeter-wave (mm-wave) narrow bandpass filter at 60 GHz. The mm-wave filter uses layout optimized conical spiral inductors which are shown to have higher quality factor (Q) and self resonant frequency values than standard spiral inductors. The filter also uses interdigital metal-oxide-metal capacitors which are shown to have Q values than nitride metal-insulator-metal (MIM) capacitors at these high frequencies. The filter is fabricated in 0.18 μm high resistivity RF silicon-on-insulator CMOS technology. The filter has a center frequency of 60 GHz and 3 dB bandwidth of 8 GHz, with a fractional bandwidth of 13.3% and a loaded Q of 7.5 occupying an area of $(150\times215)\mu m^2$. Monte-carlo simulations of the filter demonstrate excellent robustness against process variations due to usage of only two top thick metals and exclusion of MIM capacitors.

RSUIF-12 19:00

A 16.2Gbps 60GHz SiGe Transmitter for Outdoor Wireless Links

B. Sheinman[1], E. Bloch[1], N. Mazor[1], R. Levinger[1], R. Ben-Yishay[1], O. Katz[1], R. Carmon[1], A. Golberg[2], J. Vovnoboy[1], A. Bruetbart[2], M. Rachman[2], D. Elad[1]; [1]IBM, Israel, [2]Tadiad, Israel

Abstract: A fully integrated 60 GHz transmitter in 130 nm BiCMOS SiGe technology for outdoor applications is presented. The transmitter covers the entire 57–66 GHz band supporting a record data rate of 16.2 Gbps at 6 dBm output power, 512 QAM with an EVM of -34 dB. The single ended saturated power, OP1dB, and OIP3 are above 18 dBm, 16 dBm and 23 dBm respectively. The transmitter meets the most stringent ETSI emission mask for point-to-point communication at class6LB, 500 MHz bandwidth with an output noise floor below -133 dBm/Hz. The area of the transmitter is 15 mm^2 and it consumes 1.2 W.

Monday, 23 May 2016
08:00–09:40
Marriott Salons 1–3
Session RMO1A: Advanced Passive, Switch and Active Device Modeling
Chair: Francois Rivet, University of Bordeaux
Co-Chair: Vipul Jain, Anokiwave

RMO1A-1 08:00
Experimental Characterization of Packaged Switch Devices for RF and Millimeter-Wave Applications
Thanh Vinh Dinh[1], Philippe Descamps[1], Daniel Pasquet[1], Dominique Lesénéchal[1], Sidina Wane[2]; [1]CRISMAT, France, [2]NXP Semiconductors, France

Abstract: In this paper we present experimental characterization of packaged switch devices in terms of their RF attributes: isolation, insertion loss, power consumption, and linearity. Packaging and Board assembly significantly reduce their RF and mm-Wave performances. A broadband experimental setup is developed for the qualification of packaged switch devices accounting for deembedding effects both with on-board/on-package and on-chip probing. Module-based switch devices have been measured then, plastic molding, Si cap, and bonding wires have been sequentially removed to investigate their influences. Different challenges with packaged switch devices are identified and effective solutions are proposed for their qualification.

RMO1A-2 08:20
Compact Quad-Band Bandpass Filter Based on Stub-Loaded Resonators
Mohamad Farhat[1], Bal S. Virdee[2], Muhammad Riaz[2]; [1]American College of the Middle East, Kuwait, [2]London Metropolitan University, UK

Abstract: This paper presents a planar quad-band bandpass filter with high out-of-band rejection. The filter is based on inter-coupled stub-loaded resonators, where pairs of resonators are electromagnetically coupled to each other and the feedlines. This results in excitation of passbands, where the first and the third passbands are generated by $\lambda/4$ resonators. The second and the fourth passbands are excited by $\lambda/2$ resonators. The proposed technique provides sufficient degree of freedom to control the center frequency and bandwidth of the four passbands. In addition, the five transmission zeros created around the passbands results in a quad-band filter with high selectivity, sharp 3 dB cut-off frequency, high isolation, and low passband insertion-loss. The proposed technique was verified practically. Design methodology and experimental results of the prototype filter are provided.

RMO1A-3 08:40

Toroidal versus Spiral Inductors in Multilayered Technologies

José M. Lopez-Villegas[1], Neus Vidal[1], Jesús A. del Alamo[2]; [1]Universitat de Barcelona, Spain, [2]MIT, USA

Abstract: This work is aimed to compare the performance of toroidal inductors and planar spiral inductors in multilayered technologies. Toroidal inductors are investigated theoretically, and closed formula is derived for the inductance as a function of geometrical parameters. The obtained model is validated by experimental results and EM simulation. From the comparison of the inductance of toroidal inductors and compact spiral inductors, a selection rule is proposed to choose the most suitable topology that leads to the most compact design.

RMO1A-4 09:00

On the Characterization of Thermal Coupling Resistance in a Current Mirror

Tianbing Chen, Bhuvaneshwaran Vijayakumar, Tzung-Yin Lee, Chun-Wen Paul Huang, Mike McPartlin; Skyworks Solutions, USA

Abstract: In this work, the thermal coupling resistance (R12) between the reference transistor and the output transistor in a current mirror is characterized by two different measurement techniques: the constant voltage, and the constant current R12 extractions. The extracted R12 from both methods are very similar. The constant voltage method is deemed to be more physical or accurate than the constant current method. Further TCAD simulation agrees well with R12 measurement data.

Monday, 23 May 2016
08:00–09:40
Marriott Salons 10–12
Session RMO1C: Next Generation Cellular and Wireless Connectivity Transceivers
Chair: Julian Tham, Broadcom
Co-Chair: Yuan-Hung Chung, MediaTek

RMO1C-1 08:00
A Direct-Conversion Transmitter for Small-Cell Cellular Base Stations with Integrated Digital Predistortion in 65nm CMOS

Chris Mayer, David J. McLaurin, Jason Fan, Steve Bal, Christopher Angell, Oliver E. Gysel, Martin McCormick, Manish J. Manglani, Richard P. Schubert, Brian Reggiannini, John Kornblum, Lu Wu, Lex Leonard, Shipra Bhal, Alex Kagan, Tony Montalvo; Analog Devices, USA

Abstract: Network densification and FD MIMO in cellular networks require higher levels of base station integration while still meeting stringent performance requirements. We present a monolithic transmitter with integrated digital predistortion and calibration which allows RF agile, multi-carrier operation and enables efficient small cell and FD MIMO systems to be realized below 24dBm/antenna.

RMO1C-2 08:20
A 65nm CMOS Carrier-Aggregation Transceiver for IEEE 802.11 WLAN Applications

Xiang Yi[1], Kaituo Yang[1], Zhipeng Liang[1], Bei Liu[1], Khanna Devrishi[1], Chirn Chye Boon[1], Chenyang Li[1], Guangyin Feng[1], Dror Regev[2], Shimi Shilo[2], Fanyi Meng[1], Hang Liu[1], Junyi Sun[1], Gengen Hu[3], Yannan Miao[3]; [1]Nanyang Technological University, Singapore, [2]Huawei, Israel, [3]Huawei, China

Abstract: This work presents a parallel direct-conversion and double-conversion transceiver to solve the problems of crosstalk and LO pulling in the carrier aggregation scenario. An EVM of -34.9 dB is obtained when the output power of the PA driver is 0.4 dBm. Three aggregated carriers with 80 MHz 256-QAM modulation are demonstrated. To the authors' best knowledge, this work is the first CMOS integrated transceiver for IEEE 802.11 WLAN carrier aggregation application.

RMO1C-3 08:40
A Direct-Conversion Receiver for Multi-Carrier 3G/4G Small-Cell Base Stations in 65nm CMOS

David J. McLaurin, Kevin G. Gard, Richard P. Schubert, Robert Glenn, David Alldred, Trevor C. Caldwell, Zhao Li, Steve Bal, Christopher Angell, Jianxun Fan, Manish J. Manglani, Brian Reggiannini, John Kornblum, Lu Wu, Chris Mayer, Oliver E. Gysel, Wei An, Shipra Bhal, Bruce E. Wilcox, Tony Montalvo; Analog Devices, USA

Abstract: We present a 65nm direct conversion receiver for small cell 3G/4G basestations. The receiver supports up to 100MHz of RF BW and carrier frequencies from 400MHz to 6GHz, with 80dB image rejection and 76dB in-band SFDR. The direct conversion architecture eliminates IF filtering and the need for RF filtering of images and MxN mixing products, reducing basestation size and cost.

RMO1C-4 09:00

A 19.2mW 1Gb/s Secure Proximity Transceiver with ISI Pre-Correction and Hysteresis Energy Detection

Dang Liu, Xiaofeng Liu, Woogeun Rhee, Zhihua Wang; Tsinghua University, China

Abstract: This paper presents a 1Gb/s 6.5-to-8.5GHz transceiver for secure proximity communication systems. A prototype transceiver implemented in 65nm CMOS achieves the maximum data rate of 1Gb/s with the sensitivity of -53dBm and the communication range of 15cm. Consuming only 19.2mW, the proposed ultra-wideband (UWB) transceiver enables future applications such as smartphone-mirrored high-resolution display systems which require low power mainly for the transmitter in the smartphone, thus making it possible to further improve the transceiver performance with the complex receiver in the display equipment.

RMO1C-5 09:20

An RF Receiver for Multi-Band Inter- and Intra-Band Carrier Aggregation

Youngmin Kim, Pilsung Jang, Junghwan Han, Heeseon Shin, Suseob Ahn, Daehyun Kwon, Jaewon Choi, Sanghoon Kang, Seungchan Heo, Thomas Byunghak Cho; Samsung, Korea

Abstract: An RF receiver for carrier aggregation employing a low noise amplifier with a current reusing technique and a frequency-band switchable transformer is demonstrated in a 28nm LP CMOS technology. The proposed single-ended low-noise amplifier can support multiple-channel RF signals for both inter- and intra-band carrier aggregation with high performance and low DC current consumption. Moreover, a frequency-band switchable transformer is developed to realize a size-efficient receiver for handling three carrier components carrier aggregation. The receiver operates at frequency bands, ranging from 0.7 to 2.7 GHz. The receiver has conversion gain more than 70 dB and noise figure of less than 3.5 dB for all carrier aggregation combinations.

Monday, 23 May 2016
08:00–09:40
Marriott Salons 13–15
Session RMO1D: Advanced Techniques for RF Receivers
Chair: Yanjie Wang, Intel
Co-Chair: Hongtao Xu, Fudan University

RMO1D-1 08:00
A 5-GHz Inductor-Noise Cancelling Receiver with 1.8dB Noise Figure in 65nm LP CMOS

Chuan Qin, Lei Zhang, Zhijian Pan, Li Zhang, Yan Wang, Zhiping Yu; Tsinghua University, China

Abstract: In this paper, a novel receiver architecture with inductor-noise cancellation technique is presented. The proposed receiver employs two separate down-conversion paths driven by I/Q LOs respectively, and the noise of on-chip gate inductor of common-source LNA is cancelled at the baseband output, without additional penalty on power consumption, while the signal is in-phase and strengthened. The noise figure is therefore significantly improved versus prior arts. A demo 5-GHz receiver employing the proposed architecture is designed and implemented in a 65-nm low power CMOS process. Measured result shows a noise figure of 1.8 dB at 5 GHz band, while consuming only 95 mW of power from a 1.2 V supply.

RMO1D-2 08:20
Low-Power Inductorless RF Receiver Front-End with IIP2 Calibration Through Body Bias Control in 28nm UTBB FDSOI

Dajana Danilovic[1], Vladimir Milovanovic[2], Andreia Cathelin[1], Andrei Vladimirescu[3], Borivoje Nikolic[2]; [1]STMicroelectronics, France, [2]University of California, Berkeley, USA, [3]ISEP, France

Abstract: A compact energy-efficient receiver front-end designed and implemented in 28nm UTBB FDSOI CMOS supports in-device coexistence of Bluetooth (BT) with an LTE FDD Band 7 transmitter module. The receiver is based on an inductorless low-IF current-mode LNTA-first architecture and features IIP2 calibration. IIP2 improvement is implemented through the body bias of the passive mixer switching pairs. The fabricated receiver has an active area of 0.12mm^2, power consumption of 4.4mW, achieves IIP2 improvement of over 25dB through body bias tuning, NF of 8.6dB and gain of 26.7dB, all within BT specification.

RMO1D-3 08:40

A 5GHz All-Passive Negative Feedback Network for RF Front-End Self-Steering Beam-Forming with Zero DC Power Consumption

Min-Yu Huang, Taiyun Chi, Hua Wang; Georgia Institute of Technology, USA

Abstract: This paper presents an all-passive negative feedback network to perform autonomous RF front-end beam-forming towards the direction of the incident RF beam. The beam-forming front-end block consists of a passive network for RF signal processing, voltage rectifiers, and voltage-controlled phase shifters, all of which are passive components and consume zero DC power. A proof-of-concept 4-element self-steering beam-forming block at 5GHz is implemented in a standard 130nm CMOS process and occupies an area of 4.1mm^2. The measurements demonstrate that a high-quality 4-element array factor is successfully synthesized for the input progressive phase shift from -120° to +120°. At an input power P_{in} of -17dBm/element, the normalized array factor is -4.3dB/-3.2dB at +90°/-90° input progressive phase shift in the closed-loop operation, out-performing reported active self-steering beam-formers. To the best of our knowledge, this is the first demonstration of an all-passive network for front-end self-steering beam-forming with zero DC power.

RMO1D-4 09:00

A 3-Stage Recursive Weaver Image-Reject Receiver

Rangakrishnan Srinivasan, Wei-Gi Ho, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A low-power Weaver image-reject receiver based on 3rd-order signal recursion is demonstrated. The design employs two downconverters and seeks to enhance the dynamic range and gain-bandwidth product per unit power dissipation metric by adopting recursive gain reuse at multiple frequencies. Utilizing an LO at frequency f_{LO}, the downconverter recursively amplifies an RF signal at f_{RF} at 3 distinct frequencies, namely f_{RF}, $f_{RF} - f_{LO}$ and $f_{RF} - 2f_{LO}$, while using the same DC bias current. Further, the receiver uses the same quadrature mixers to perform the two frequency translations. The design is implemented in a 130 nm CMOS process. Over a current range from 650 μA to 2 mA, employing a supply voltage of 1.2V, the design achieves a corresponding conversion gain in the range from 57.2–82.7 dB, flicker noise corner < 20 kHz, and a SSBNF of 13.6–6.8 dB for f_{RF} = 404/434 MHz, in each downconverter. The architecture is suitable for application in a low-IF MICS/ISM band receiver, and low-power sensor applications.

RMO1D-5 09:20

A 10GHz CMOS RX Frontend with Spatial Cancellation of Co-Channel Interferers for MIMO/Digital Beamforming Arrays

Sanket Jain, Yunqi Wang, Arun Natarajan; Oregon State University, USA

Abstract: An architecture for low-noise spatial cancellation of co-channel interferer (CCI) at RF in a digital beamforming (DBF)/MIMO receiver (RX) array is presented. The proposed RF cancellation can attenuate CCI prior to the ADC in a DBF/MIMO RX array while preserving a field-of-view (FoV) in each array element, enabling subsequent DSP for multi-beamforming. A novel hybrid-coupler/polyphase-filter based input coupling scheme that simplifies spatial selection of CCI and enables low-noise cancellation is described. A 4-element 10GHz prototype is implemented in 65nm CMOS that achieves >20dB spatial cancellation of CCI while adding <1.5dB output noise.

Monday, 23 May 2016
10:10–11:50
Marriott Salons 1–3
Session RMO2A: Advances in Processing and Materials for RF Applications
Chair: Edward Preisler, TowerJazz
Co-Chair: Chang-Ho Lee, Qualcomm

RMO2A-1 10:10
Single Crystal AlGaN Bulk Acoustic Wave Resonators on Silicon Substrates with High Electromechanical Coupling

Jeffrey B. Shealy, Michael D. Hodge, Pinal Patel, Ramakrishna Vetury, Alexander Yu. Feldman, Shawn R. Gibb, Mark D. Boomgarden, Michael P. Lewis, James B. Shealy, James R. Shealy; Akoustis Technologies, USA

Abstract: Bulk acoustic wave (BAW) resonators using single crystal AlGaN piezoelectric films are reported. Metal-organic chemical vapor deposition (MOCVD) growth was used to obtain single crystal AlGaN films on 150-mm diameter <111> silicon substrates with (0002) XRD rocking curve FWHM of 0.37°. Series-configured 12 Ω BAW resonators with resonant frequency of 2.302GHz were fabricated with insertion loss of 0.29dB and an electromechanical coupling of 4.44%. Maximum resonator Q_{max} was 1277, leading to a figure of merit (FOM) of 57. Unloaded acoustic Q_r was 4243, leading to a FOM of 188. These FOM are the highest reported to date for MOCVD-based single crystal resonators.

RMO2A-2 10:30
An Optimized Isolated 5V EDMOS in 55nm LPx Platform for Use in Power Amplifier Applications

Ming Li, ShaoQiang Zhang, Parthasarathy Shyam, Purakh Raj Verma; GLOBALFOUNDRIES, Singapore

Abstract: Power Amplifier (PA) modules are becoming more and more complex in modern wireless systems. In order to meet the efficiency/linearity design schemes such as Envelope elimination and restoration (EER) and Envelope tracking (ET) are increasingly becoming popular in PA applications. This paper describes an optimized isolated 5V EDMOS in 55nm Low Power extended (LPx) platform which is ideal for use in the bias modulator and controller of the PA module. Industry leading Rsp of 0.96 mohm-mm^2 for high voltage NMOS and 2.6 mohm-mm^2 for the high voltage PMOS is reported. Drain to source breakdown voltages of 10.5V was achieved for these devices. Due to special considerations given to optimizing the CGD capacitance while maintaining the Rsp, high Johnson's figure of merit (fT*BVDS) of 536 GHz-V and 168 GHz-V were achieved for the NMOS and PMOS respectively.

RMO2A-3 10:50

A 2.22–2.92GHz LC-VCO Demonstrated with an Integrated Magnetic-Enhanced Inductor in 180nm SOI CMOS

Rui Ma[1], Fei Lu[1], Qi Chen[1], Chenkun Wang[1], Feng Liu[2], Wanghui Zou[3], Albert Wang[1]; [1]University of California, Riverside, USA, [2]Wuhan University, China, [3]Hunan University, China

Abstract: We demonstrate a 2.22–2.92GHz LC voltage-controlled oscillator (LC-VCO) in an 180nm SOI CMOS integrated with a novel compact inductor with vertical magnetic core. The new magnetic-enhanced inductor was fabricated using a new CMOS-compatible process. Measurements show that the single-layer magnetic-cored inductor increases its inductor density by 16.9% within the operation frequency range, leading to a phase noise reduction for the VCO from -106.97dBc/Hz to -113.49dBc/Hz at 10MHz offset frequency. This VCO prototype demonstrates the potential of designing RF system-on-a-chip (SoC) using new vertical magnetic-cored inductors.

RMO2A-4 11:10

CMOS RF Performance Gain by Gate Resistance Optimization

Christoph Schwan[1], Kok Wai Johnny Chew[2], Byounghak Lee[3], Oscar D. Restrepo[3], Murali Kota[3], Wai Heng Chow[2], Shih Ni Ong[2], Michael Cheng[2], Xi Sung Loo[2], Ralf Illgen[1], Andreas Huschka[1], Maciej Wiatr[1], Bhoopendra Singh[1], Uwe Kahler[1], Josef Watts[3]; [1]GLOBALFOUNDRIES, Germany, [2]GLOBALFOUNDRIES, Singapore, [3]GLOBALFOUNDRIES, USA

Abstract: We report experimental improvement of both RF and digital AC performance of a 28nm CMOS technology by predoping the gate poly. The results are explained in terms of the physical structure of the gate and the atomic structure of the gate TiN/Si interface in the gate stack.

Monday, 23 May 2016
10:10–11:50
Marriott Salons 10–12
Session RMO2C: High-Performance Fractional-N Frequency Synthesizers

Chair: Stefano Pellerano, Intel

Co-Chair: Xiang Gao, Marvell Semiconductor

RMO2C-1 10:10

A 28GHz Quadrature Fractional-N Synthesizer for 5G Mobile Communication with Less Than 100fs Jitter in 65nm CMOS

W. El-Halwagy[1], A. Nag[1], P. Hisayasu[2], F. Aryanfar[2], P. Mousavi[1], M. Hossain[1]; [1]University of Alberta, Canada, [2]Samsung, USA

Abstract: A 26–32GHz quadrature cascaded phase locked loop (PLL) is presented. The PLL is implemented in 65nm bulk CMOS, consuming 27mW and has less than 100fsec integrated jitter with -114.4 and -112.6dBc/Hz phase noise at 1MHz offset for integer and fractional modes, respectively.

RMO2C-2 10:30

A 93.4-to-104.8GHz 57mW Fractional-N Cascaded Sub-Sampling PLL with True In-Phase Injection-Coupled QVCO in 65nm CMOS

Xiang Yi, Zhipeng Liang, Guangyin Feng, Chirn Chye Boon, Fanyi Meng; Nanyang Technological University, Singapore

Abstract: A fully integrated 93.4-to-104.8 GHz 57 mW cascaded PLL, with true in-phase injection-coupled QVCO, occupies 0.88 mm^2 in 65 nm CMOS. By cascading the fractional-N PLL and the sub-sampling PLL, good phase noise, high resolution and wide acquisition range are achieved simultaneously. The measured phase noise of QVCO and PLL are -112.67 and -108.75 dBc/Hz at 10 MHz offset, respectively. The FOM and FOM_T of the QVCO at 10 MHz offset are -177.5 and -179.0 dBc/Hz, respectively.

RMO2C-3 10:50

A 2.8–4.3GHz Wideband Fractional-N Sub-Sampling Synthesizer with -112.5dBc/Hz In-Band Phase Noise

Masoud Moslehi Bajestan, Hubert Attah, Kamran Entesari; Texas A&M University, USA

Abstract: A 2.8–4.3GHz low noise fractional-N sub-sampling frequency synthesizer in 40nm CMOS technology is presented in this paper. The reference sampling clock is modulated by a 10-bit edge modulator to achieve fractional phase lock. A novel fast two-step background calibration is used to correct gain errors in the edge modulator, reducing fractional spurs. For a 3.75GHz carrier, the synthesizer achieves 376fs rms jitter with a worst case fractional spur of -48.3dBc. The in-band phase noise at 200kHz offset is -112.5dBc/Hz. The system consumes a total power of 9.18mW from a 1.1V supply and occupies an area of 0.41mm^2.

RMO2C-4 11:10

Fractional-N Open-Loop Digital Frequency Synthesizer with a Post-Modulator for Jitter Reduction

Tapio Rapinoja[1], Yury Antonov[2], Kari Stadius[2], Jussi Ryynänen[2]; [1]TDK Nordic, Finland, [2]Aalto University, Finland

Abstract: This paper presents a 0.4 to 2.1 GHz open-loop fractional-N multiplying delay-locked loop based frequency synthesizer in 65 nm CMOS. The proposed frequency synthesizer architecture is based on Digital Period Synthesis that features wide frequency range, fine frequency resolution, instantaneous frequency switching and is capable to provide several independent outputs. An inherent challenge of fractional-N synthesis is a notable deterministic jitter. In this paper we present a high-speed direct delay modulation circuit (DDM) that provides over ten-fold reduction in deterministic jitter over the entire frequency range. The measured deterministic period jitter, related to the fractional mode operation, is reduced from 51 ps to 4 ps by using the DDM. Furthermore, in this paper we demonstrate, for the first time, how the implemented synthesizer can produce two totally independent outputs at different frequencies.

RMO2C-5 11:30

An 802.11 a/b/g/n Digital Fractional-N PLL with Automatic TDC Linearity Calibration for Spur Cancellation

Dongyi Liao[1], Hechen Wang[1], Fa Foster Dai[1], Yang Xu[2], Roc Berenguer[3]; [1]Auburn University, USA, [2]Illinois Institute of Technology, USA, [3]Innophase, USA

Abstract: This work presents a 1.9~5.6 GHz fractional-N DPLL with digi-phase spur canceller. It utilizes a ramp signal generated from the fractional-N accumulator to automatically calibrate the TDC linearity. The chip also includes an MMD that overcomes the division ration skipping problem associated with the prior art MMDs. The ADPLL achieves a worst fractional spur level of -55 dBc and an in-band phase noise of -109 dBc/Hz (0.63 ps integrated jitter) while consuming 9.9 mW.

Monday, 23 May 2016
10:10–11:50
Marriott Salons 13–15
Session RMO2D: High Performance Integrated RF Components
Chair: Domine Leenaerts, NXP Semiconductors
Co-Chair: Danilo Manstretta, University of Pavia

RMO2D-1 10:10
Passive Coupled-Switched-Capacitor-Resonator-Based Reconfigurable RF Front-End Filters and Duplexers

Run Chen, Hossein Hashemi; University of Southern California, USA

Abstract: High-Q resonators may be used to synthesize selective bandpass filters. Many commercial radio-frequency filters are based on coupled-resonators and realized in surface and bulk acoustic wave technologies due to the high quality factor and compact size of acoustic resonators. In this paper, it is shown that discrete-time equivalent of coupled-resonator bandpass filters may be realized using passive switched-capacitor circuits. The center frequency and the bandwidth are determined by the frequency of the switch driving signals and the capacitor values. The proposed passive filters can be linear, low noise, and compact. To further enhance the in-band linearity, an RF bootstrapping technique is proposed. Design and experimental verification of a fourth-order RF BPF and a duplexer, realized in a 65nm CMOS technology, are reported.

RMO2D-2 10:30
A Wideband Complementary Noise Cancelling CMOS LNA

Benqing Guo[1], Jun Chen[1], Yao Wang[1], Haiyan Jin[1], Guoning Yang[2]; [1]UESTC, China, [2]Qualcomm, China

Abstract: A complementary noise cancelling CMOS Low-noise amplifier (LNA) for mobile DTV application with enhanced linearity is proposed. Intrinsic noise cancellation mechanism maintains acceptable NF with reduced power consumption due to current reuse principle. Complementary multi-gated transistor (MGTR) technique is further employed to null the third-order distortion and compensate second-order nonlinearity of noise cancelling stage. Implemented in a 0.18-μm CMOS process, measurement results show that the proposed LNA provides a NF of 3 dB, and a maximum gain of 17.5 dB from 0.1 to 2 GHz. An input 1-dB compression point (IP_{1dB}) and an IIP3 of -3 dBm and 14.3 dBm, respectively, are obtained. The circuit core only draws 9.7 mA from a 2.2 V supply.

RMO2D-3 10:50

Adaptive Integrated CMOS Circulator

Seyyed Amir Ayati, Debashis Mandal, Bertan Bakkaloglu, Sayfe Kiaei; Arizona State University, USA

Abstract: An adaptive circulator fabricated on a 130 nm CMOS is presented. Circulator has two adaptive blocks for gain and phase mismatch correction and leakage cancellation. The impedance matching circuit corrects mismatches for antenna, divider, and LNTA. The cancellation block cancels the Tx leakage. Measured isolation between transmitter and receiver for single tone at 2.4 GHz is 90 dB, and for a 40 MHz wide-band signal is 50dB. The circulator Rx gain is 10 dB, with NF = 4.7 dB and 5 dB insertion loss.

RMO2D-4 11:10

A 28GHz SiGe BiCMOS Phase Invariant VGA

B. Sadhu, J.F. Bulzacchelli, Alberto Valdes-Garcia; IBM, USA

Abstract: The paper describes a technique to design a phase invariant variable gain amplifier (VGA). Variable gain is achieved by varying the bias current in a BJT, while the phase variation is minimized by designing a local feedback network such that the applied base to emitter voltage has a bias-dependent phase variation which compensates the inherent phase variation of the transconductance. Two differential 28GHz VGA variants based on these principles achieve <5° phase variation over 8dB and 18dB of gain control range, respectively, with phase invariance maintained over PVT. Implemented in GF 8HP BiCMOS technology, the VGAs achieve 18dB nominal gain, 4GHz bandwidth, and IP1dB > -13dBm while consuming 35mW.

RMO2D-5 11:30

A 48–61GHz LNA in 40-nm CMOS with 3.6dB Minimum NF Employing a Metal Slotting Method

Hao Gao, Kuangyuan Ying, Marion K. Matters-Kammerer, Pieter Harpe, Qian Ma, Arthur van Roermund, Peter Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents a low noise amplifier realized in 40-nm CMOS technology for the 60 GHz ISM band. To reduce the noise contribution from the input passive structure, a new metal slotting method is applied to the transmission line for increasing the effective conducting cross-section area. The design incorporates additional noise matching between the common-source stage and the common-gate stage to reduce the noise impact by the latter stage. The measured noise figure is below 4 dB from 51 GHz to 65 GHz, 3.6 dB at 55 GHz and 3.8 dB at 60 GHz. The achieved 3 dB power gain bandwidth is 13 GHz, from 48 GHz to 61 GHz. The peak transducer gain (G_t) is 15 dB at 55 GHz, and 12.5 dB at 60 GHz. The total power consumption is 20.4 mW.

Monday, 23 May 2016
13:30–15:10
Marriott Salons 1–3
Session RMO3A: Mixed-Signal/RF Circuits for Wideband Transceivers
Chair: Fred Lee, Verily Life Sciences
Co-Chair: James Wilson, US Army Research Laboratory

RMO3A-1 13:30
A Wideband Delta-Sigma Based Closed-Loop Fully Digital Phase Modulator in 45nm CMOS SOI

Hamed Gheidi[1], Toshifumi Nakatani[2], Vincent Leung[3], Peter M. Asbeck[1]; [1]University of California, San Diego, USA, [2]MaXentric Technologies, USA, [3]Qualcomm, USA

Abstract: This paper presents a new architecture for an RF phase modulator that significantly improves the phase resolution. The modulator utilizes 32 variable delay elements in a delay lock loop (DLL) configuration to provide wideband 1–3GHz operation with coarse 5-bit resolution. A 5-bit multiplexer selects different taps of the DLL according to the baseband digital phase data to generate desired phase modulated signal at the output. A high speed 5-bit digital delta-sigma modulator is additionally used to compensate for the phase truncation occurring in the 5-bit DLL. The phase modulator IC is implemented in 45nm CMOS SOI and achieves <2% rms EVM while achieving 55dB rejection of close-to-carrier emissions for an 8Mb/s GMSK signal at 2.3GHz, with power consumption below 35mW.

RMO3A-2 13:50
A 7.5mW 35–70MHz 4th-Order Semi-Passive Charge-Sharing Band-Pass Filter with Programmable Bandwidth and 72dB Stop-Band Rejection in 65nm CMOS

Yang Xu, Praveen Kumar Venkatachala, Spencer Leuenberger, Un-Ku Moon; Oregon State University, USA

Abstract: This paper proposes a highly reconfigurable charge-domain switched-g_m-C biquad band-pass filter (BPF) topology that uses a semi-passive charge-sharing technique. It uses only switches, capacitors, digital circuitry for 3-phase non-overlapping clock generation and linearity-enhanced g_m-stages. A 4th-order BPF prototype operating at 1.2GS/s sampling rate is implemented using a cascade of two independent biquads in a 65nm LPE CMOS. A tunable center frequency of 35–70MHz is measured with programmable bandwidth and a maximum stop-band rejection of 72dB. The in-band 1-dB compression point is -2.4dBm, and the in-band IIP3 is +9dBm. The filter prototype consumes 7.5mW from a 1.2V supply, and occupies an active area of 0.17mm^2.

RMO3A-3 14:10
0.84-THz Imaging Pixel with a Lock-In Amplifier in CMOS

Rui Xu[1], Ja-Yol Lee[2], Dae Yeon Kim[1], Shinwoong Park[3], Zeshan Ahmad[1], Kenneth K. O[1]; [1]University of Texas at Dallas, USA, [2]ETRI, Korea, [3]Virginia Tech, USA

Abstract: An 840-GHz Schottky diode detector is integrated with an analog lock-in amplifier in

130-nm bulk CMOS. The integrated lock-in amplifier can support a modulation frequency of up to 10MHz with a gain of 54dB, a dynamic range of 42dB, and an input referred noise of less than 10 nV/√Hz at modulation frequencies higher than 100kHz. The integrated lock-in amplifier occupies an area of 0.17 mm^2 and consumes 4.9mA from a 1.2-V supply. The detector and on-chip lock-in amplifier combination was used to form terahertz images.

RMO3A-4 14:30

A Mode-Configurable Analog Baseband for Wi-Fi 11ac Direct-Conversion Receiver Utilizing a Single Filtering ΔΣ ADC

Chi-Yun Wang, Shu-Wei Chu, Tzu-Hsuin Peng, Jen-Che Tsai, Chih-Hong Lou; MediaTek, Taiwan

Abstract: A mode-configurable filtering ΔΣ ADC is utilized as the analog baseband in a Wi-Fi 11ac direct-conversion receiver (RX). The filtering ΔΣ ADC providing both 2^{nd}-order out-of-band filtering and 3^{rd}-order in-band noise shaping is realized with only two opamps. A SAR-quantizer with built-in discrete-time (DT) excess-loop delay (ELD) compensation technique is also adopted. The filtering ΔΣ ADC is clocked at 480 MHz or 960 MHz and achieves 77-to-58 dB dynamic range (DR) in 10 MHz – 80 MHz bandwidth. With the aid of the filtering ability, the interferer DR at 4x bandwidth is at least 71.3 dB over modes. This work is fabricated in 28-nm low-power (LP) technology with 0.06 mm^2 of active area. It consumes 3.97 mW or 6.39 mW over different clock rates, resulting a highest Schreier's FoM of 171 dB (BW20) and a best 4x-bandwidth Walden's FoM of 13.3 fJ/c (BW160) among all modes.

RMO3A-5 14:50

A 28nm, 475mW, 0.4-to-1.7GHz Embedded Transceiver Front-End Enabling High-Speed Data Streaming Within Home Cable Networks

S. Spiridon[1], D. Koh[1], J. Xiao[1], M. Brandolini[1], B. Shen[1], C.-M. Hsiao[2], H. Huang[2], D. Guermandi[3], S. Bozzola[4], H. Yan[4], M. Introini[4], L. Krishnan[1], K. Raviprakash[5], Y. Shin[1], R. Gomez[1], J. Chang[1]; [1]Broadcom, USA, [2]Broadcom, Taiwan, [3]imec, Belgium, [4]Broadcom, The Netherlands, [5]Apple, USA

Abstract: A 28 nm CMOS Software-Defined Transceiver (SDTRX) enabling High-Speed Data (HSD) streaming, including Ultra HD TV, within home cable networks is presented. By making efficient use of available cable bandwidth, the SDTRX dynamically handles up to 1024QAM OFDM-modulated HSD streams. This paper addresses SDTRX system-level design methodology as the key driver in enabling performance optimization for achieving a wide frequency range of operation at the lowest power and area consumption. By employing an optimized architecture constructed on available state-of-the art 28 nm functional building blocks, the monolithic SDTRX consists of a mixer-based harmonic rejection RX with a DAC-based TX and a smart PLL system. It operates over a 0.4-to-1.7 GHz frequency range while consuming less than 475 mW in half-duplex mode. Moreover, by developing a simple TX-RX loopback circuit, the system is enabled to efficiently calibrate TX output power and to remove the need for a dedicated external pin. This low-cost SDTRX is embedded in various 28 nm CMOS multimedia SoCs and is, to the authors' knowledge, the first reported transceiver front end to enable true high-speed data streaming within home cable networks.

Monday, 23 May 2016
13:30–15:10
Marriott Salons 10–12
Session RMO3C: Millimeter-Wave and THz Signal Sources
Chair: Ehsan Afshari, Cornell University
Co-Chair: Ping Gui, Southern Methodist University

RMO3C-1 13:30
An E-Band, Scalable 2×2 Phased-Array Transceiver Using High Isolation Injection Locked Oscillators in 90nm SiGe BiCMOS

Najme Ebrahimi, Mahdi Bagheri, Po-yi Wu, James F. Buckwalter; University of California, San Diego, USA

Abstract: This paper presents the first E-band phased array transceiver that uses injection locked oscillators (ILOs) for beamforming. We propose a current injection distribution network with wide locking range and high isolation. A 2×2 bidirectional transceiver is demonstrated to operate from 71–86 GHz and measurements verify that each oscillator can be controlled independently with phase shift over ±300 degrees with < 5° phase error and under 0.9 dB amplitude variation. Each channel has a 9.5-dB noise figure in RX mode and a 10-dBm output power in TX mode. The phase noise of the locked oscillator exhibits less than 2.5 dB variation across the phase steering range. The 90-nm SiGe BiCMOS chip consumes 386.4 mW in TX mode and 286 mW in RX mode per channel.

RMO3C-2 13:50
A 0.34-THz Varactor-Less Scalable Standing Wave Radiator Array with 5.9% Tuning Range in 130nm BiCMOS

Hossein Jalili, Omeed Momeni; University of California, Davis, USA

Abstract: A 1×4 scalable mm-wave power generation and radiation array is designed using a standing wave harmonic oscillator architecture. A varactor-less scheme has been used to improve the tuning range above 300 GHz. The circuit with on chip patch antennas is implemented in a 130nm SiGe process with 215 GHz of f_{max} and is measured to provide 5.9% tuning range, -10.5 dBm total radiated power and 1.2 dBm EIRP at 342 GHz while consuming 425 mW DC power from 1.8 V supply voltage.

RMO3C-3 14:10

160–310GHz Frequency Doubler in 65-nm CMOS with 3-dBm Peak Output Power for Rotational Spectroscopy

Navneet Sharma, Wooyeol Choi, Kenneth K. O; University of Texas at Dallas, USA

Abstract: A 160–310 GHz frequency doubler for rotational spectroscopy with a driver amplifier is demonstrated in a 65-nm bulk CMOS process. At 0-dBm input power, the measured output power (P_{out}) varies from 3 to -8 dBm. The wide operating range is attributed to wide bandwidth driver and matching structure based on broadband open and short leading to >40dB difference between fundamental and second harmonic power at the output. The doubler-amplifier combination has the comparable output power and a larger operating frequency range than 200–300 GHz COTS GaAs modules.

RMO3C-4 14:30

A Quad-Core-Coupled Triple-Push 295-to-301GHz Source with 1.25mW Peak Output Power in 65nm CMOS Using Slow-Wave Effect

Amir Hossein Masnadi Shirazi, Amir Nikpaik, Shahriar Mirabbasi, Sudip Shekhar; University of British Columbia, Canada

Abstract: Achieving high output power in (sub-)THz voltage-controlled oscillators (VCOs) has been a severe design challenge in CMOS technology. In this work, an architecture for coupled terahertz (THz) VCOs is presented. The architecture utilizes four coupled triple-push VCOs and combines the generated third harmonic currents using slow-wave coplanar waveguide (S-CPW) at 300 GHz. Coupling four cores increases output power, and use of S-CPW reduces the loss and increases the quality factor of the VCO tank. It is shown that using S-CPW results in ~2.6 dB of lower loss as compared to the conventional CPW or grounded-CPW (GCPW) structures. The VCO is tuned using parasitic tuning technique and achieves 1.7% frequency tuning range (FTR). The proposed structure is designed and fabricated in a 65-nm bulk CMOS process. The measured peak output power of the 295-to-301 GHz VCO is 0.9 dBm (≈1.25 mW) at 300 GHz while consuming 235 mW (with a DC to RF efficiency of 0.52%).

RMO3C-5 14:50

An Efficient 210GHz Compact Harmonic Oscillator with 1.4dBm Peak Output Power and 10.6% Tuning Range in 130nm BiCMOS

Chen Jiang[1], Andreia Cathelin[2], Ehsan Afshari[1]; [1]Cornell University, USA, [2]STMicroelectronics, France

Abstract: A compact 210GHz harmonic oscillator is presented. By utilizing a device-centric bottom-up design methodology as well as the return-path gap coupler and self-feeding structure, the harmonic power generation is optimized. Fabricated with a 130nm SiGe BiCMOS process, the oscillator core occupies only 290×95 μm^2 area. It achieves a 1.4dBm peak output power and 2.4% peak DC-to-RF efficiency. The output frequency can be tuned from 197.5GHz to 219.7GHz. The phase noise is measured to be -87.5dBc/Hz at 1MHz offset.

Monday, 23 May 2016
13:30–15:10
Marriott Salons 13–15
Session RMO3D: Mixed-Signal Power Amplifiers
Chair: Jeffrey Walling, University of Utah
Co-Chair: Patrick Reynaert, KU Leuven

RMO3D-1 13:30
A Digital Polar Transmitter with DC-DC Converter Supporting 256-QAM WLAN and 40MHz LTE-A Carrier Aggregation

Qiuyao Zhu[1], Sheng Yu[1], Sizhou Wang[2], Lun Huang[2], Zhaogang Wang[3], Xuejun Zhang[2], Yang Xu[1]; [1]Illinois Institute of Technology, USA, [2]Innophase, USA, [3]Innophase, China

Abstract: A digital polar transmitter is introduced using 9-b thermometer-coded uniform cells to achieve high linearity for wideband signal. A 960 MHz delay tuner is designed for precise amplitude and phase alignment. An on-chip DC-DC is included for direct battery connection and output power control. Boosted bias improves PA efficiency at low power region. This digital polar transmitter outputs peak power 21.9 dBm with 41% drain efficiency, achieves EVM -30.7dB with 802.11ac compliance of 20 MHz 256-QAM signal, also 4.5%/4.8% with LTE-A 40 MHz carrier aggregation compliance of 64-QAM signal.

RMO3D-2 13:50
A Compact Broadband Mixed-Signal Power Amplifier in Bulk CMOS with Hybrid Class-G and Dynamic Load Trajectory Manipulation Operations

Song Hu[1], Shouhei Kousai[2], Hua Wang[1]; [1]Georgia Institute of Technology, USA, [2]Toshiba, Japan

Abstract: We present a mixed-signal PA with real-time Class-G and dynamic load trajectory manipulation (DLTM) hybrid operations to achieve PA efficiency enhancement up to the deep power back-off (PBO) region. Moreover, the PA load trajectory is dynamically manipulated to achieve PA efficiency peaking during the PBO operation, and the PA load modulation network is realized by only one on-chip transformer balun for an ultra-compact layout. A prototype PA fully integrated in a standard 65nm bulk CMOS process achieves +24.6dBm peak output power (P_{out}) and 45.6% maximum drain efficiency (DE) at 2.4GHz. By combining the real-time Class-G and DLTM hybrid operations with mixed-signal AM and PM linearization, the PA delivers a +18.5dBm 10MSym/s 64-QAM signal with 32.6% DE and -27.8dB EVM. The DLTM operation also extends the PA P_{out} 1dB bandwidth by 40%. The total chip area is only 1.9mm^2.

RMO3D-3 14:10

A 5.9GHz RFDAC-Based Outphasing Power Amplifier in 40-nm CMOS with 49.2% Efficiency and 22.2dBm Power

Zhebin Hu[1], Leo C.N. de Vreede[2], Morteza S. Alavi[2], David A. Calvillo-Cortes[3], Robert Bogdan Staszewski[2], Songbai He[1]; [1]UESTC, China, [2]Technische Universiteit Delft, The Netherlands, [3]Qualcomm, USA

Abstract: In this paper, we present a fully integrated RFDAC-based outphasing power amplifier (ROPA) in 40-nm CMOS that achieves 22.2 dBm peak output power with 49.2% drain efficiency at 5.9 GHz. It employs differential quasi-load-insensitive Class-E branch PAs that can dynamically be segmented using a 3-bit digital amplitude control word to improve efficiency at power back-off. At 8 dB back-off, this segmentation technique improves the ROPA drain and system efficiency by 5% and 7%, respectively, when compared to a non-segmented approach.

RMO3D-4 14:30

A Multiphase Switched Capacitor Power Amplifier in 130nm CMOS

Wen Yuan, Jeffrey S. Walling; University of Utah, USA

Abstract: This paper presents a multiphase switched-capacitor power amplifier (MP-SCPA). Cartesian combining architectures suffer reduced output power and efficiency owing to combination of out-of-phase signals. The multiphase architecture reduces the phase difference between the basis vectors that are combined, increasing the output power and efficiency compared to the Cartesian combiners. 16 equally spaced phases are produced by a phase generator with each phase's relative amplitude weighted on the bottom plate of a capacitor array and combined on a common top plate, resulting in linear amplification. The MP-SCPA delivers a peak output power and PAE of 26 dBm and 24.9%, respectively. When amplifying an LTE signal the average output power and PAE are 20.9 dBm and 15.2%, respectively while achieving <-30 dBc ACLR and 3.5%-rms EVM.

RMO3D-5 14:50

A 40nm CMOS Single-Ended Switch-Capacitor Harmonic-Rejection Power Amplifier for ZigBee Applications

Chenxi Huang, Yongdong Chen, Tong Zhang, Visvesh Sathe, Jacques C. Rudell; University of Washington, USA

Abstract: This paper describes a single-ended switch-capacitor harmonic-rejection power amplifier to operate in the 915 MHz ISM band for ZigBee applications. A multipath feed-forward harmonic-rejection technique is employed to suppress the $2^{nd}/3^{rd}/4^{th}$ harmonics of the switch-capacitor power amplifier (PA) by 48/17/24 dB, respectively. The measured PA peak drain efficiency is 43% at a peak output power of 8.9dBm with the harmonic-rejection enabled. This PA was implemented in a 40nm TSMC CMOS process with an active area of 180μm×700μm.

Monday, 23 May 2016
15:40–17:20
Marriott Salons 1–3
Session RMO4A: Low-Power Transceivers
Chair: Gernot Hueber, NXP Semiconductors
Co-Chair: Yao-Hong Liu, imec

RMO4A-1 15:40
A 420μW, 4GHz Approximate Zero IF FM-UWB Receiver for Short-Range Communications

Vladimir Kopta[1], David Barras[2], Christian C. Enz[1]; [1]EPFL, Switzerland, [2]CSEM, Switzerland

Abstract: A low-power FM-UWB receiver intended for short range communications in wireless sensor networks is presented in this paper. It utilizes an "approximate zero IF" architecture which combines a free-running ring oscillator as the RF LO with a modified delay-line demodulator. The main benefit comes from implementing the gain stages and the demodulator at the IF instead of RF, allowing significant power savings. Integrated in a 65nm CMOS technology, the whole receiver chain consumes 420μW from a 1V supply while achieving -68dBm sensitivity at the data rate of 100 kb/s.

RMO4A-2 16:00
A Fully Integrated 320pJ/b OOK Super-Regenerative Receiver with -87dBm Sensitivity and Self-Calibration

Vahid Dabbagh Rezaei[1], Stephen J. Shellhammer[2], Mohamed Elkholy[1], Kamran Entesari[1]; [1]Texas A&M University, USA, [2]Qualcomm, USA

Abstract: This paper presents an ultra-low power super-regenerative receiver (SRR) suitable for OOK modulation. The receiver is fabricated in 40 nm CMOS technology and operates in the ISM band of 902–928 MHz. It exploits a SAR architecture to calibrate the internally generated quench signal. Employing an on-chip inductor and a single to differential architecture for the input amplifier has made the receiver fully integrable, eliminating the need for external components. A power consumption of 320 μW from a 0.65 V supply results in an excellent energy efficiency of 80 pJ/b at 4 Mb/s data rate, while the best sensitivity is -87 dBm at 1 Mb/s data rate.

RMO4A-3 16:20
An RF-Powered FSK/ASK Receiver for Remotely Controlled Systems

Ranieri Guerra[1], Alessandro Finocchiaro[1], Giuseppe Papotto[1], Benedetta Messina[2], Leandro Grasso[2], Roberto La Rosa[1], Giulio Zoppi[1], Giuseppe Notarangelo[1], Giuseppe Palmisano[2]; [1]STMicroelectronics, Italy, [2]Università di Catania, Italy

Abstract: A fully integrated RF-powered receiver for remotely controlled systems is presented. The receiver adopts ASK and FSK modulations and is capable of operating in the ISM bands of 433 MHz, 869 MHz, and 915 MHz, while achieving a bit rate down to 62 kb/s. The circuit includes an RF harvester and a power management unit for the RF to DC power conversion and control, respectively, and an OTP memory with a digital interface for the operating configuration. Measurements show a harvester sensitivity of -18.8 dBm and accurate ASK demodulation with a modulation index as low as

10%. The current consumption is 87 μA and 720 μA for the ASK and FSK receiving mode, respectively. The circuit was fabricated in a 0.13-μm CMOS technology and occupies a core area of 2.2 mm^2.

RMO4A-4 16:40

A 540μW RF Wireless Receiver Assisted by RF Blocker Energy Harvesting for IoT Applications with +18dBm OB-IIP3

Omar Elsayed, Mohamed Abouzied, Edgar Sánchez-Sinencio; Texas A&M University, USA

Abstract: This paper introduces a wireless receiver system that harvests energy from the out-of-band RF blockers which enables sustainable operation and extends battery life for IoT applications. Operating at 900 MHz band and fabricated in CMOS 180 nm, the proposed RF receiver system architecture can operate at the presence of unavoidable high out-of-band blockers (≈0 dBm) yet consumes 534 μW. Moreover, 46% of this dc power is extracted from existing blockers via RF energy harvesting techniques.

RMO4A-5 17:00

An RF-Powered 58Mbps-TX 2.5Mbps-RX Full-Duplex Transceiver for Neural Microimplants

Yashar Rajavi[1], Mazhareddin Taghivand[2], Kamal Aggarwal[1], Andrew Ma[1], Ada S.Y. Poon[1]; [1]Stanford University, USA, [2]Qualcomm, USA

Abstract: A wirelessly-powered, high-data-rate transceiver for neuro-modulation applications is presented. The transceiver achieves 58Mbps in TX, and 2.5Mbps in RX. It enables bidirectional full-duplex communication using an external duplexer. The TX operates at 1.74GHz and consumes 93μW, while the RX operates at 1.86GHz and consumes 7.2μW. The prototype was fabricated in 40nm LP CMOS and occupies 0.8mm^2. The overall system size including the duplexer is 3.2mm^2.

Monday, 23 May 2016
15:40–17:20
Marriott Salons 4–6
Session RMO4B: Interferer Resilient Receivers
Chair: Oren Eliezer, University of Texas at Dallas
Co-Chair: Tim LaRocca, Northrop Grumman

RMO4B-1 15:40
A Cellular Receiver Front-End with Blocker Sensing
Mohammed Abdulaziz, Waqas Ahmad, Anders Nejdel, Markus Törmänen, Henrik Sjöland; Lund University, Sweden

Abstract: A receiver front-end supporting contiguous and non-contiguous intra-band carrier aggregation scenarios with a fully integrated spectrum sensor that can detect both in-gap and out-of-band blockers has been implemented in 65nm CMOS technology. An NF of 2.5dB is achieved using a noise canceling LNTA, and linearized OTAs are used to achieve an IIP3 improvement of up to 6.5dB in-band and 11dB at the filter band edge. The spectrum sensor can detect blocker levels in 22 steps of 9MHz between -100MHz and 100MHz IF. The system consumes between 36.6mA and 57.6mA from a 1.2V supply.

RMO4B-2 16:00
A 4-Phase Blocker Tolerant Wideband Receiver with MMSE Harmonic Rejection Equalizer
Esmail Babakrpur, Won Namgoong; University of Texas at Dallas, USA

Abstract: This paper presents a blocker tolerant low-noise wideband receiver that employs digital harmonic rejection equalizer to suppress high order harmonic interferers. Unlike the commonly employed 8-phase harmonic rejection mixers (HRMs), the proposed wideband receiver suppresses any of the harmonic interferers including the seventh and ninth. The wideband receiver employs a two-path front-end structure, consisting of a highly linear mixer-first primary path and gm-first secondary path. An adaptive minimum mean-squared error (MMSE) harmonic rejection equalizer is employed that minimizes the desired signal distortion in the mean-squared error sense in the presence of arbitrary harmonic interferers and the correlated noise between the two paths. Using two sets of 4-phase clocks, a 100–1450MHz receiver that achieves HRR >75dB up to the ninth harmonic while being robust to mismatches is implemented.

RMO4B-3 16:20
A Cross-Coupled Switch-RC Mixer-First Technique Achieving +41dBm Out-of-Band IIP3
Hugo Westerveld, Eric Klumperink, Bram Nauta; University of Twente, The Netherlands

Abstract: With the growing amount of wireless devices, interference robustness is a receiver specification of increasing importance. This paper presents a technique that improves both out-of-band compression and weakly non-linear distortion. It mitigates the effect of non-linearity in the baseband amplifier by preceding it by a cross-coupled passive filter. This provides a highly linear

passive shunt path for out-of-band currents, while maintaining wideband input matching. The 65nm CMOS prototype chip achieves 41dBm out-of-band IIP3 at 40MHz offset and an 11dBm out-of-band blocker compression point. The chip has an area of 0.8mm^2 and consumes 46mW from a 1.2V supply.

RMO4B-4 16:40

A Self-Clocked Blocker-Filtering Technique for SAW-Less Wireless Applications

Saeed Pourbagheri[1], Kartikeya Mayaram[1], Terri S. Fiez[2]; [1]Oregon State University, USA, [2]University of Colorado Boulder, USA

Abstract: A blocker filtering technique is presented that extracts the clock from the blocker for SAW-less receivers. The extracted clock is utilized to suppress the blocker without requiring any prior information of the exact location of the blocker. This clock runs at the blocker frequency and drives a notch filter that steers the blocker current away from the signal path. Implemented in a 65 nm CMOS process, the filter is able to track the blocker within 1 to 1.6 GHz and provides about 20 dB of rejection relative to the signal at the notch frequency for blockers from -40 dBm to -10 dBm.

Monday, 23 May 2016
15:40–17:20
Marriott Salons 13–15
Session RMO4D: Wideband Power Amplifiers
Chair: Margaret Szymanowski, NXP Semiconductors
Co-Chair: Donald Lie, Texas Tech University

RMO4D-1 15:40
A 130-nm SOI CMOS Reconfigurable Multimode Multiband Power Amplifier for 2G/3G/4G Handset Applications

Pierre Ferris[1], Gauthier Tant[2], Alexandre Giry[1], J.D. Arnould[3], J.M. Fournier[3]; [1]CEA-LETI, France, [2]NXP Semiconductors, France, [3]IMEP-LAHC, France

Abstract: This paper presents a reconfigurable multimode multiband power amplifier (MMPA) integrated in a 130nm SOI CMOS technology. In 2G mode, a saturated output power of 34.6/35.5dBm with a corresponding power added efficiency (PAE) of 61/53% was measured at 800/900MHz. In 3G/4G mode, a linear output power higher than 28/27dBm with a PAE higher than 34/33% while keeping adjacent channel leakage power ratio (ACLR) less than -36/-33dBc was measured with WCDMA and LTE signals respectively in the 700–900MHz frequency range. At 900MHz, up to 39/37% PAE is achieved with WCDMA/LTE signals. Up to 15% boost in PAE was achieved at 700MHz and 900MHz by using reconfigurable matching network, which validates the usefulness of the proposed reconfigurable architecture. The fabricated circuit occupies an area of 2.9mm^2. To our best knowledge, this 2-stage reconfigurable single-core MMPA is the first reported SOI LDMOS MMPA addressing 2G/3G/4G modes and covering an extended frequency range from 700MHz to 900MHz.

RMO4D-2 16:00
Broadband Digitally-Controlled Power Amplifier Based on CMOS/GaN Combination

Varish Diddi[1], Shuichi Sakata[2], Shintaro Shinjo[2], Voravit Vorapipat[1], Richard Eden[3], Peter M. Asbeck[1]; [1]University of California, San Diego, USA, [2]Mitsubishi Electric, Japan, [3]Technology Applications, USA

Abstract: A multiWatt RF power amplifier operating in the frequency range 0.5 to 1.2 GHz is reported, whose output amplitude is determined by digital input words (“RF Power DAC operation”). The amplifier employs a CMOS IC for digital control, directly connected to a GaN FET operating in common-gate mode. The use of the GaN FET allows power supply voltages in excess of 15 V to be used. A load resistance of 50 ohms can be directly connected to the GaN FET, thereby avoiding bandwidth limitations from output matching networks. Output power in the range 2 to 3 W and drain efficiencies above 50% are obtained over more than an octave of bandwidth.

RMO4D-3 16:20

A PMOS mm-Wave Power Amplifier at 77GHz with 90mW Output Power and 24% Efficiency

Jefy A. Jayamon, James F. Buckwalter, Peter M. Asbeck; University of California, San Diego, USA

Abstract: In deeply scaled CMOS processes with gate lengths below 40 nm the analog performance of NMOS and PMOS FETs are comparable. At the same time PMOS FETs can typically operate under higher operating voltages than NMOS devices. In this paper, we present the first millimeter-wave power amplifier exclusively employing PMOS. The single stage, 3-stack power amplifier operates at 65–92 GHz with more than 35% fractional bandwidth and 12 dB gain. At 78 GHz, the PA achieves a maximum output power of 19.6 dBm and PAE of 18% with class-A bias, and 18.7 dBm and 24% PAE with class-AB bias. The PA has been fabricated in 32 nm CMOS SOI process and occupies 440 μm × 280 μm area (only 0.05 mm^2 excluding pads). To the authors' knowledge this PA achieves the highest efficiency for any silicon PA in the 60–90 GHz frequency band. The output power is also the best reported in silicon for this frequency range, for amplifiers that do not use elaborate power-combining approaches.

RMO4D-4 16:40

A Wideband Voltage Mode Doherty Power Amplifier

Voravit Vorapipat, Cooper Levy, Peter M. Asbeck; University of California, San Diego, USA

Abstract: This paper presents a new wideband Doherty Amplifier technique that can achieve high efficiency while maintaining excellent linearity. By modifying a "forgotten" topology originally proposed by Doherty, a new Doherty Amplifier architecture is realized with two voltage mode PAs and transformers, thus eliminating a narrowband impedance inverter. The voltage mode PA is implemented with a switched capacitor PA known for its excellent linearity. The PA is fabricated in 65 nm low-leakage CMOS and achieves 24 dBm saturated power (at standard supply voltage) with 45%/34% PAE at peak and 5.6dB back-off over 750 MHz to 1050 MHz 1dB bandwidth. With memory-less linearization, this PA can transmit 40 MHz 256-QAM 9dB PAPR 802.11ac modulation centered at 900 MHz meeting the spectral mask with measured EVM of -34.8dB and 22% PAE without backing-off or equalization.

RMO4D-5 17:00

A DC to 22GHz, 2W High Power Distributed Amplifier Using Stacked FET Topology with Gate Periphery Tapering

Kohei Fujii; M/A-COM Technology Solutions, USA

Abstract: This paper describes a high power (2W) distributed amplifier (DA) MMIC. DA MMIC was fabricated using an Lg=0.25μm GaAs PHEMT process. DA MMIC contains an impedance transformer and heavily tapered gate periphery design for constant output power performance over 0.1 to 22GHz operational frequency. To obtain high voltage operation, the DA MMIC employed a three stacked FET topology. A 7-section DA demonstrated 2 W saturated output power and 12 dB small signal gain from 0.1 GHz to 22 GHz with peak output power of 3.5 W with power added efficiency (PAE) of 27%. Those test results exceeded recently reported GaN based power DA performance with large margins.

Tuesday, 24 May 2016
08:00–09:40
Marriott Salons 1–3
Session RTU1A: Spectrum Sensing
Chair: Hossein Hashemi, University of Southern California
Co-Chair: Eric Klumperink, University of Twente

RTU1A-1 08:00
A Phaser-Based Real-Time CMOS Spectrum Sensor for Cognitive Radios
Paria Sepidband, Kamran Entesari; Texas A&M University, USA

Abstract: Real time spectrum sensing can be useful for cognitive radio (CR) devices to detect primary signals without the need for a receiver, reducing complexity and false detection. In this paper, an integrated CMOS real time CR spectrum sensor in 57–354 MHz frequency band with a new integrable phaser is presented, which is the first real time spectrum sensor applicable to radio frequency integrated circuit (RFIC) area. The integrated chip has been fabricated in a standard 0.18 μm CMOS IBM technology and draws 11 mA from a 1.8 V supply voltage.

RTU1A-2 08:20
An 8mW, 1GHz Span, Passive Spectrum Scanner with > +31dBm Out-of-Band IIP3
Neha Sinha[1], Mansour Rachid[2], Sudhakar Pamarti[1]; [1]University of California, Los Angeles, USA, [2]Silvus Technologies, USA

Abstract: A 65nm CMOS, 8mW spectrum scanner using simple but linear periodically time-varying (LPTV) circuits is presented. The scanner spans a 1GHz spectrum by providing sharp filters at programmable centre frequencies. Its passive structure gives it a measured out-of-band IIP3 of > +31dBm and a sensitivity of < -142dBm/Hz across the 1GHz band leading to an SFDR of 75dB in a 1MHz resolution bandwidth.

RTU1A-3 08:40
A Compressed-Sampling Time-Segmented Quadrature Analog-to-Information Converter for Wideband Rapid Detection of up to 6 Interferers with Adaptive Thresholding
Rabia Tugce Yazicigil, Tanbir Haque, Manoj Kumar, Jeffrey Yuan, John Wright, Peter R. Kinget; Columbia University, USA

Abstract: A rapid interferer-detector for cognitive radio systems is presented that uses a compressed-sampling time-segmented quadrature analog-to-information converter (TS-QAIC). The TS-QAIC introduces system scalability through adaptive thresholding and time segmentation, while limiting silicon cost and complexity. The TS-QAIC can detect 6 interferers in 2.7–3.7GHz in 10.4μs with 8 physical I/Q branches. The TS-QAIC chip implemented in 65nm CMOS on 0.517mm^2 (active area) consumes 81.2mW from 1.2V.

RTU1A-4 09:00

A Mixer Frontend for a Four-Channel Modulated Wideband Converter with 62dB Blocker Rejection

Douglas Adams[1], Yonina Eldar[2], Boris Murmann[1]; [1]Stanford University, USA, [2]Technion, Israel

Abstract: The Modulated Wideband Converter promises to improve receiver flexibility for cognitive radios by leveraging compressive sensing techniques. We present a prototype IC that adds signal reception to previously demonstrated signal detection. Refactoring the mixing sequence between detection and reception enables targeted reception and blocker rejection. We algorithmically design a three-level mixing sequence and additionally employ delay-based harmonic cancellation. When applied together in our 65-nm chip, we measure 62 dB of in-band blocker rejection, while receiving up to four channels between 0 and 900 MHz.

Tuesday, 24 May 2016
08:00–09:40
Marriott Salons 10–12
Session RTU1C: Millimeter-Wave Systems and Components for W-Band and Above

Chair: Pierre Busson, STMicroelectronics
Co-Chair: Amin Arbabian, Stanford University

RTU1C-1 08:00

A Low-Power SiGe BiCMOS 190GHz Receiver with 47dB Conversion Gain and 11dB Noise Figure for Ultra-Large-Bandwidth Applications

David Fritsche, Gregor Tretter, Christoph Tzschoppe, Corrado Carta, Frank Ellinger; Technische Universität Dresden, Germany

Abstract: This paper presents a 190-GHz direct-conversion receiver capable of supporting higher-order modulation schemes and implemented in a SiGe BiCMOS technology. The circuit consists of a low-noise amplifier, an active fundamental mixer, a LO driver, a variable-gain baseband amplifier and a totem-pole output stage. To exploit the advantages of sub-THz frequencies in terms of available bandwidth at a low DC power consumption, all circuit blocks are concurrently optimized for large bandwidth and high power-efficiency. While consuming only 122 mW of DC power, the fabricated circuit exhibits a record 3-dB RF bandwidth of 35 GHz, a maximum conversion gain of 47 dB, a maximum baseband voltage swing of more than 800 mV_{pp} and a minimum double-sideband noise figure of 10.7 dB.

RTU1C-2 08:20

A 94GHz 4TX-4RX Phased-Array for FMCW Radar with Integrated LO and Flip-Chip Antenna Package

Andrew Townley[1], Paul Swirhun[1], Diane Titz[2], Aimeric Bisognin[3], Frédéric Gianesello[3], Romain Pilard[3], Cyril Luxey[2], Ali Niknejad[1]; [1]University of California, Berkeley, USA, [2]Université Nice Sophia Antipolis, France, [3]STMicroelectronics, France

Abstract: A prototype phased-array IC with four transmitters, four receivers, and integrated LO generation was designed and fabricated in a 130nm SiGe BiCMOS technology. Including LO phase shifter power consumption, the transmit array consumes 71mW per element with a per-element output power of +6.4dBm at 94GHz. The receiver array consumes 56mW per element, and achieves an RX element noise figure of 12.5dB at 94GHz. Integrated LO generation includes a 47GHz VCO, 2× frequency multiplier, 94GHz LO buffers, and a 32× CML divider chain. The transceiver has been integrated into a flip chip antenna module with four transmit and four receive antennas, and achieves TX and RX beam steering over a scan angle range of ±20°. Including LO and bias overhead power, the array has improved per-element power consumption compared with state-of-the-art 94GHz arrays, consuming only 106mW per TX channel and 91mW per RX channel, while achieving comparable performance and levels of integration.

RTU1C-3 08:40

225–280GHz Receiver for Rotational Spectroscopy

Q. Zhong[1], Wooyeol Choi[1], Navneet Sharma[1], Zeshan Ahmad[1], J.P. McMillan[2], C.F. Neese[2], F.C. De Lucia[2], Kenneth K. O[1]; [1]University of Texas at Dallas, USA, [2]Ohio State University, USA

Abstract: A fully integrated CMOS receiver for mm-wave rotational spectroscopy is demonstrated. The receiver consists of a sub-harmonic mixer based receiving front-end which down-converts 225–280 GHz RF input to 20 GHz intermediate frequency, a 20-GHz AM demodulator followed by a baseband buffer amplifier, and an 122–139 GHz local oscillator chain which is comprised of a frequency quadrupler and a driver amplifier. The receiver exhibits responsivity of 400–1200 kV/W and noise equivalent power of 0.4 to 1.2 pW/√Hz from 225 to 280 GHz. Detection of ethanol, propionitrile (EtCN), acetonitrile (CH3CN) and acetone in a mixture is demonstrated using the receiver in a rotational spectrometer setup. This is the first demonstration that a CMOS receiver can be used for rotational spectroscopy and that a CMOS circuit can support an existing application at frequencies above 200 GHz.

RTU1C-4 09:00

A 165–230GHz SiGe Amplifier-Doubler Chain with 5dBm Peak Output Power

Sriram Muralidharan[1], Kefei Wu[2], Mona Hella[2]; [1]Analog Devices, USA, [2]Rensselaer Polytechnic Institute, USA

Abstract: This paper presents the design and measurements of a 165–230 GHz SiGe BiCMOS power amplifier - frequency doubler chain, which can deliver up to 5 dBm peak output power at 204 GHz with a 3-dB bandwidth of 65 GHz. A compact high efficiency power divider is used to split the power from the input mm-wave source and convert the single ended input to two differential signals. The 3-staged transformer-coupled cascode power amplifier is optimized to deliver 14 dBm saturated output power at 110 GHz, while the frequency doubler uses a second harmonic reflector at its input to reduce the conversion loss. The chip is designed in 0.13μm SiGe BiCMOS technology. To the authors' best knowledge, this is the highest output power above 200 GHz from silicon based amplifier-multiplier chains.

RTU1C-5 09:20

75–105GHz Switching Power Amplifiers Using High-Breakdown, High-f_{max} Multi-Port Stacked Transistor Topologies

Kunal Datta, Hossein Hashemi; University of Southern California, USA

Abstract: High-breakdown, high-f_{max} multi-port transistor topologies are presented in this work for realizing high power, highly efficient mm-wave switching power amplifiers at 75–105 GHz. Implemented in a 90nm SiGe BiCMOS process, the proposed active structures comprising of two and three stacked transistors with integrated layout parasitics achieve (f_{max}, breakdown voltage) of (295 GHz, 8V) and (260 GHz, 11 V) respectively and demonstrate peak (output power, PAE) of (22 dBm, 19%) at 85 GHz and (23.3 dBm, 17%) at 83 GHz respectively. The implemented designs are benchmarked against a 88 GHz 19.5 dBm, 16% PAE W-band Class-E power amplifier using native transistor footprints fabricated in the same 90nm SiGe BiCMOS process. The superior performance of the composite transistor designs highlight the benefit of the proposed approach.

Tuesday, 24 May 2016
08:00–09:40
Marriott Salons 13–15
Session RTU1D: Advanced PA Design Techniques
Chair: Ranjit Gharpurey, University of Texas at Austin
Co-Chair: Leon van den Oever, Radiosemi

RTU1D-1 08:00
A Highly Efficient WLAN CMOS PA with Two-Winding and Single-Winding Combined Transformer
Hyunjin Ahn, Seungjun Baek, Hyunsik Ryu, Ilku Nam, Ockgoo Lee; Pusan National University, Korea
Abstract: In this paper, a fully integrated high-efficiency linear CMOS power amplifier (PA) is developed for 802.11g WLAN applications with the proposed power combining transformer. In comparison with conventional power combining transformers, the proposed power combining transformer can offer high-efficiency performances with a smaller die size. The fabricated two-stage PA using a 65nm CMOS technology achieves a saturated output power of 26.7 dBm with a drain efficiency (DE) of 47.7% at 2.48 GHz. The PA is tested with 54Mbps WLAN 802.11g signal and it meets the stringent error vector magnitude (EVM) and spectral mask requirements at a 20.13-dBm output power with a DE of 21.4%.

RTU1D-2 08:20
A Fully Integrated Flip-Chip SiGe BiCMOS Power Amplifier for 802.11ac Applications
Apostolos Samelis, Edward Whittaker, Michael Ball, Alasdair Bruce, John Nisbet, Lui Lam, Craig Christmas, William Vaillancourt; Skyworks Solutions, UK
Abstract: A fully integrated flip-chip SiGe BiCMOS power amplifier for wireless local area network (WLAN) applications in the 2 GHz band is presented. In a front-end module (FEM) configuration and under 802.11ac signal excitation, the PA delivers 29 dB small-signal gain and -30.4 dB dynamic error vector magnitude (EVM) at 20.6 dBm, at nominal operating conditions (3.3 V, 25 °C). The PA tightly controls detector voltage and corrects the dynamic EVM over supply voltage, temperature, orthogonal frequency division multiplexing (OFDM) burst length and duty cycle variations.

RTU1D-3 08:40
A 20dBm Configurable Linear CMOS RF Power Amplifier for Multi-Standard Transmitters
Eli Schwartz, Sergey Anderson, Alex Mostov, Ilya Sima, Udi Suissa, Ron Pongratz, Amit Ezer, Avi Cohen, Michael Gulko, Nadav Snir, Asaf Elazari, Avi Bauer; DSP Group, Israel
Abstract: A new approach to PA design in CMOS for 802.11ac that achieves -35dB EVM with output power higher than 100mW and EVM floor of -47dB is demonstrated. The PA is designed to be operated as part of a configurable RF front-end module and meets the requirements for various WiFi standards including 802.11ac.

RTU1D-4 09:00

Single Die Broadband CMOS Power Amplifier and Tracker with 37% Overall Efficiency for TDD/FDD LTE Applications

Florinel Balteanu; Skyworks Solutions, USA

Abstract: This paper presents a 2.3GHz–2.7GHz broadband CMOS FDD/TDD LTE Band 7, 38, 40 and 41 power amplifier (PA) fully integrated with a fast envelope tracker (ET) on a single 0.18μm CMOS die. The PA and the tracker achieve a 37% overall efficiency for 26.5dBm and -39dBc ACLR1. The entire design including the input/output match uses an active silicon area around 2.7mm^2.

RTU1D-5 09:20

A 1-Watt Ku-Band Power Amplifier in SiGe with 37.5% PAE

Ying Chen, Mark P. van der Heijden, Domine M.W. Leenaerts; NXP Semiconductors, The Netherlands

Abstract: This paper demonstrates a 1-Watt output power amplifier MMIC operating from 13.5GHz to 14.5GHz (Ku-band). The power amplifier employs an on-chip integrated 16-way in-phase output current combiner to achieve the required output power. Implemented in a 0.25-μm SiGe:C BiCMOS technology, the power amplifier achieves a power-added efficiency of 37.5% at 14.1GHz with greater than 35.5% across the band of interest.

Tuesday, 24 May 2016
10:10–11:50
Marriott Salons 1–3
Session RTU2A: Innovative Reconfigurable Transceiver Architectures
Chair: Ramesh Harjani, University of Minnesota
Co-Chair: Vito Giannini, Texas Instruments

RTU2A-1 10:10
A 30-MHz-to-3-GHz CMOS Array Receiver with Frequency and Spatial Interference Filtering for Adaptive Antenna Systems
Naoki Oshima, Masaki Kitsunezuka, Kenta Tsukamoto, Kazuaki Kunihiro; NEC, Japan
Abstract: A 30-MHz-to-3-GHz wideband CMOS phased array receiver with interference suppression capability in frequency and spatial domains is presented. A frequency filtering function is provided by a 16-phase, two-stage harmonic rejection mixer which also works as a 5-bit phase shifter in multi-chip phased array systems. Equipped with 6-bit amplitude control in addition to the phase, the array receiver enables analog null steering that can reduce a spatial interferer coming from a specific direction. The developed IC achieves more than 55-dB suppression of harmonic interference in the wide range from 30 MHz to 3 GHz. The multiple ICs configure a four-element adaptive array system for the measurement of space propagation. It is confirmed that the null steering function reduces spatial interference by 20 dB and improves an EVM from -12.7 dB to -26.3 dB even when a strong interferer exists.

RTU2A-2 10:30
A Wideband Single-PLL RF Receiver for Simultaneous Multi-Band and Multi-Channel Digital Car Radio Reception
Jan van Sinderen[1], Lucien Breems[1], Hans Brekelmans[1], Frank Leong[1], Nenad Pavlovic[1], Robert Rutten[1], Jan Niehof[1], Raf Roovers[1], Bernard Burdiek[2], Jochen Rudolph[2], Ulrich Moehlmann[2], Peter Blinzer[2], Manfred Biehl[2], Niels Gabriel[2], Andreas Wichern[2], Gerd Schippmann[2], Frank Rethmeier[2], Janusz Klimczak[2], Joerg Wenzel[2], Ralf-Gero Pilaski[2]; [1]NXP Semiconductors, The Netherlands, [2]NXP Semiconductors, Germany
Abstract: This paper describes a single-PLL, fixed-oscillator, wide-band multi-tuner HD Radio & DAB/T-DMB receiver for concurrent multi-band & multi-channel car radio reception, fully integrated in a 65nm CMOS SoC. Besides saving area and power for the LO and clock generation, the presented architecture also prevents oscillator pulling and spurs. Harmonic rejection mixers have been used to suppress down-conversion with LO harmonics up to 60dB, which reduces the required amount of RF filtering. The DAB measurement results show best-in-class blocker performance (FoS up to 70dBc) in combination with state-of-the-art sensitivity down to -102dBm.

RTU2A-3 10:50

A Fully Integrated Software-Defined FDD Transceiver Tunable from 0.3-to-1.6GHz

Dong Yang[1], Hazal Yüksel[2], Christopher Newman[2], Changhyuk Lee[3], Zachariah Boynton[2], Noman Paya[4], Miles Pedrone[5], Alyssa Apsel[2], Alyosha Molnar[2]; [1]Broadcom, USA, [2]Cornell University, USA, [3]Columbia University, USA, [4]Texas Instruments, USA, [5]IBM, USA

Abstract: An ideal Software Defined Radio (SDR) requires a reconfigurable, integrated, widely-frequency-tunable transceiver able to support different RX/TX duplex schemes. Here we present an integrated transceiver capable of supporting both TDD and FDD operation with >25dB integrated RX-TX isolation from 0.3–1.6GHz without any off-chip switches or filters. The transceiver uses an artificial transmission line (TL) and distributed PA to separate TX and RX. TX noise in the RX band is further suppressed by >13dB an RX-tracking PA degeneration circuit.

RTU2A-4 11:10

A 200MSPS Reconfigurable ADC with Adjacent Channel Narrowband Blocker Resiliency

Sushil Subramanian, Hossein Hashemi; University of Southern California, USA

Abstract: A 200 MSPS reconfigurable and blocker resilient analog-to-digital converter (ADC) is presented. The system consists of a discrete-time lossy differentiator frontend and a 6-bit noise shaping, pipeline ADC backend, which enables tolerance of a <3 MHz narrowband blocker up to 40 dB stronger than the desired signal. Filtering in the presence of the blocker improves quantization by an additional 3 bits to accommodate the desired signal. With lower blocker power, the system defaults to Nyquist performance and an additional reconfiguration switch enables a 3–6 MHz, ΔΣ ADC. The system is designed in a 65 nm CMOS technology, has a total chip area of 1040 μm × 920 μm, and consumes 6.37 mW of power. Enabling blocker resilience improves the figure-of-merit (FOM) of the system from 474 fJ/lvl to 158 fJ/lvl.

Tuesday, 24 May 2016
10:10–11:50
Marriott Salons 10–12
Session RTU2C: 5G Millimeter-Wave Components and Integrated Systems

Chair: Ed Balboni, Analog Devices

Co-Chair: Mona Hella, Rensselaer Polytechnic Institute

RTU2C-1 10:10

A 60GHz Packaged Switched Beam 32nm CMOS TRX with Broad Spatial Coverage, 17.1dBm Peak EIRP, 6.1dB NF at <250mW

B. Sadhu, Alberto Valdes-Garcia, J.-O. Plouchart, H. Ainspan, A.K. Gupta, M. Ferriss, M. Yeck, M. Sanduleanu, X. Gu, C. Baks, D. Liu, D . Friedman; IBM, USA

Abstract: A low power, small form-factor, 60-GHz radio with beam switching capability is presented. The 3mm×3mm radio IC in 32nm SOI CMOS includes the TX and RX RF front ends, mixers, basebands, PLL and LO chains. The package comprises 2 TX antennas and 2 RX antennas producing low directivity beams in two orthogonal directions to maximize spatial coverage, with an achieved angular coverage of 254°. In board level measurements of the half duplex packaged radio, 17.1dBm EIRP and 6.1dB noise figure are achieved, with power consumption below 250mW.

RTU2C-2 10:30

20–30GHz Mixer-First Receiver in 45-nm SOI CMOS

Charley Wilson III, Brian A. Floyd; North Carolina State University, USA

Abstract: A 20–30 GHz mixer-first receiver implemented in 45-nm SOI CMOS is presented. The receiver employs four-phase passive mixing with input inductor to realize tunable impedance matching up to 30 GHz. The receiver achieves an 8-dB noise figure with reconfigurable 8.9 to 20.6-dB conversion gain and 2:1 impedance tuning range. Input 1-dB compression point ranges from -13 to -9.3 dBm and power consumption is 41 mW.

RTU2C-3 10:50

A 42mW 26–28GHz Phased-Array Receive Channel with 12dB Gain, 4dB NF and 0dBm IIP3 in 45nm CMOS SOI

Umut Kodak, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a low-power 26–28 GHz phased-array receive channel in 45nm CMOS SOI. The design alternates cascode amplifiers with switched-LC phase-shifter cells to result in 5-bit phase control with gain and rms phase error < 0.6 dB and 4°, respectively, over 32 phase states. The measured gain, noise figure (NF) and IIP3 are 12.2 dB, 4 dB and 0 dBm, respectively, and are achieved at a DC power of 42 mW. A gain control of 6-dB is also available without affecting the system NF. To our knowledge, this represents state-of-the-art in mm-wave phased-arrays with the best published linearity at low NF. Application areas include 5G base-stations and hand-held units.

RTU2C-4 11:10

A 28-GHz 4-Channel Dual-Vector Receiver Phased Array in SiGe BiCMOS Technology

Yi-Shin Yeh[1], Benjamin Walker[2], Ed Balboni[2], Brian A. Floyd[1]; [1]North Carolina State University, USA, [2]Analog Devices, USA

Abstract: This paper presents a 28-GHz four-channel phased-array receiver in 120-nm SiGe BiCMOS technology for 5G cellular application. The phased-array receiver employs scalar-only weighting functions within each front-end and then global quadrature power combining to realize beamforming. Differential LNAs and dual-vector variable-gain amplifiers are used to realize each front-end with compact area. Each front-end achieves 5.1 to 7 dB noise figure, -16.8 to -13.8 dBm input compression point, -10.5 to -8.9 dBm input third-order intercept point across 4-bit phase settings and a 3-dB bandwidth of 26.5 to 33.9GHz, while consuming 136 mW per element. RMS gain and phase errors are < 0.6 dB and $< 5.4°$ at 28–32 GHz respectively, and all four elements reveal well-matched responses.

RTU2C-5 11:30

A Ka-Band Digitally-Controlled Phase Shifter with Sub-Degree Phase Precision

Yahya Tousi, Alberto Valdes-Garcia; IBM, USA

Abstract: We present a passive digital-to-phase converter with sub-degree phase precision for phased array frontends. The phase tuning approach is based on manipulating the electromagnetic properties of an artificially constructed transmission line. By simultaneously controlling dispersion, characteristic impedance, and loss across the structure, the phase shifter minimizes phase imprecisions while ensuring a flat amplitude response across different phase settings.

The chip prototype is fabricated in a 130nm SiGe BiCMOS process, occupies an area of 0.18mm^2, and consumes no power. The insertion loss is -9.3 dB $\pm$ 0.25 dB at 28 GHz. The phase control operates with 4.75 degree steps while maintaining an RMS phase error of 0.6 degrees across multiple chips and temperatures, demonstrating the best phase and amplitude accuracy when compared to state-of-the-art integrated microwave and mm-wave phase shifters.

RFIC 2016 Lunchtime Panel Session

Monday, 23 May 2016
12:00–13:00
San Francisco Marriott Marquis, Nob Hill A–D

Bio-Electronics: Silicon in MY Body?!

Panel Organizers and Moderators:
Francois Rivet, *University of Bordeaux, France*
J.C. Chiao, *University of Texas at Arlington, USA*

Panelists: **Harm Tenhoff**, *CEO, BayLink, USA*
Amin Arbabian, *Assistant Professor, Stanford University, USA*
Perry Li, *Principal Engineer, St. Jude Medical, USA*
Mehdi Kiani, *Assistant Professor, Pennsylvania State University, USA*
Arjang Hassibi, *Founder & CEO, InSilixa, USA*

Abstract: In the upcoming decades we expect to witness a proliferation of bio-electronics, providing everyone with affordable powerful technologies for personalized medicine that can not only monitor, but also enhance, improve or repair critical human body functions. This will have a profound impact on life expectancy and quality, but are we prepared for such revolution? Empowering patients with control over their own conditions and providing tools for caregivers with continuous diagnosis and treatment will lead to precision medicine and lower costs. But what would be in the wish-list for the commercial development of such systems? What would this involve in terms of standards, security, safety, privacy, ethical and legal aspects that electronic industries need to consider? And who will bear the costs of research and development or failures of whatever nature, compared to the experience in other pharmaceutical sectors? What would be the social acceptance and impact for this type of electronics? These and more questions are to be debated with the panelists and the audience. Make sure to order the silicon-free lunch box for this lunchtime session.

IMS/RFIC 2016 Lunchtime Panel Session

Tuesday, 24 May 2016
12:00–13:00
Moscone Center, Room 310

Patents – The Good, the Bad and the Ugly

Panel Organizers and Moderators:
Oren Eliezer, *University of Texas at Dallas, USA*
Alfy Riddle, *Kumu Networks, USA*

Panelists: **Osama Shana'a**, *Senior Director, MediaTek, USA*
Amitava Das, *CEO, Tagore Technology, USA*
Robert Bogdan Staszewski, *Professor, University College Dublin, Ireland*
Howard Zaretsky, *Patent Attorney, Zaretsky Group, USA*
Curtis Ling, *Co-Founder & CTO, MaxLinear, USA*
Greg Kisor, *Chief Technologist, Intellectual Ventures, USA*

Abstract: Patents have become an inseparable part of our engineering careers, and are often used (or abused?…) in evaluating companies or even individuals. While the government's patenting system was intended to allow inventors to capitalize on their intellectual property (IP), the sale or cross-licensing of patents, as well as royalty based revenues, appear to be overshadowed by a multi-billion industry of patent related lawsuits at present. Authors are often forbidden by their companies to publish their work at conferences such as this one, so as not to inadvertently reveal details that may trigger claims by so-called "patent trolls", and university collaboration is sometimes hindered by concerns over ownership of the IP.

Our panelist will debate, with the audience's participation, their views on the advantages and shortcomings in the existing system, including the discussion of specific examples.

WORKSHOPS AND SHORT COURSES

Workshops and Short Courses are offered on Sunday, Monday and Friday at the Moscone center. Please see the daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 22 MAY 2016

WSA (Half Day): Sunday 08:00–12:00
Millimeter-Wave R&D for 5G:
Systems, Phased Arrays, and Handset Transceivers

Sponsors: **RFIC, IMS**

Organizers: **Alberto Valdes-Garcia**, *IBM, USA*
Didier Belot, *CEA-LETI, France*
Huei Wang, *National Taiwan University, Taiwan*
Kamran Entesari, *Texas A&M University, USA*
Pierre Busson, *STMicroelectronics, France*
Telesphor Kamgaing, *Intel, USA*

Abstract: Rapidly growing demand for broadband cellular data traffic is driving fifth generation (5G) standardization towards deployment by 2020. The anticipated key to enabling gigabit-per-second 5G speeds is mm-wave operation. Millimeter-wave bands offer 50 times the bandwidth available in existing RF bands but pose numerous technical challenges to the low-cost deployment of millimeter-wave solutions. U.S. regulators recently issued a notice of inquiry for provision of mobile services above 24 GHz. Additionally, reliable coverage over the typical 200 meter cell radius in non-line-of-sight dense urban conditions, and practical antenna array solutions for user equipment (UE) were both demonstrated at 28 GHz. High-volume implementation of the UE radio is also envisioned as multiple-element phased-array transceiver in silicon technologies. However, a great deal of discussion still surrounds how 5G standards and as a result their corresponding wireless accessories will evolve. This workshop is focused on gathering a combination of academic and industry experts in mm-wave circuits and systems and antennas to discuss integrated circuit, system and antenna solutions to potential mm-wave front-ends for 5G standards. This workshop will present state-of-the-art research results in this area and ultimately help participants identify the enabling radio technologies for 5G cellular communications.

Speakers:

1. "5G — Towards 10s of Radios and 10s of Gb/s", **Aleksandar Tasic**, *Qualcomm, USA*
2. "Efficient and Scalable Millimeter-Wave Beamforming Architecture Using 0.13µm SiGe BiCMOS ICs", **Cagri Ulusoy**, *IHP Microelectronics, Germany*
3. "Millimeter Wave Access Points and Backhauling for 5G Heterogeneous Networks", **Cedric Dehos**, *CEA-LETI, France*

4. "Large-Scale Silicon Phased Arrays for 5G Communication Systems", **Gabriel Rebeiz**, *University of California, San Diego, USA*
5. "Novel mmWave Communication Systems: from Highly-Digital Arrays to MIMO and Full-Duplex", **Harish Krishnaswamy**, *Columbia University, USA*
6. "Introduction and Usage of 5G Wireless Systems", **Jan-Erik Thillberg**, *Ericsson, Sweden*
7. "CMOS mm-Wave Transceivers Towards 5G Cellular", **Kenichi Okada**, *Tokyo Institute of Technology, Japan*
8. "Research Advances in Millimeter Wave Integrated Circuits for 5G Applications", **Wei Hong**, *Southeast University, China*

WSB (Half Day): Sunday 13:00–17:00
Highly Efficient 5G PA Design

Sponsor: **RFIC**

Organizers: **Donald Y.C. Lie**, *Texas Tech University, USA*
Nick Cheng, *Skyworks Solutions, USA*

Abstract: 5G cellular systems are expected to see significant deployment in 2020, promising up to 10 Gbps data rate for stationary users and enabling internet connection capacity for billions of devices for IoT applications (e.g., "connected city"). It is very challenging to meet the targeted 5G system specs such as less than 1 msec latency and greater than x1000 bandwidth per unit area, while still achieving the coveted big reduction in energy. Therefore, 5G wireless communication systems are likely to present a paradigm shift that includes very high carrier frequencies with 10+ Gbps bandwidths, extensive MIMO antennas usage, and very dense base station deployment and high device densities for IoT applications. 5G also needs to provide seamless transition and backward compatibility with LTE and WiFi to render universal high-rate coverage. To support all these unprecedented 5G device/system performance metrics, the power and cost efficiencies for the wireless device design will become even more critical. Therefore, high-efficiency and linear broadband RF power amplifier (PA) design for the microwave and millimeter wave frequencies is obviously becoming more challenging as they evolve from 4G to 5G handset and IoT applications. In this workshop, industry and academic experts will examine various perspectives, such as system, circuits and transistor-level design techniques and considerations in regards to the development of microwave/mmWave, highly-efficient linear PA suitable for massive MIMO, small cells, predistortion, new modulation schemes, etc., to meet the challenges and address the issues related to 5G cellular communication and IoT systems.

Speakers:

1. "5G What will it be?", **Peter Gammel**, *Skyworks Solutions, USA*
2. "CMOS Power Amplifiers for 5G", **Peter Asbeck**, *University of California, San Diego, USA*
3. "RFFE and PA Challenges with Emerging 5G Radios", **Paul Draxler**, *Qualcomm, USA*

4. "Design of Highly Efficient MMIC Power Amplifiers for 5G Communication", **Kris Kong**, *Qorvo, USA*
5. "Linear CMOS PA at mm-Wave Band for 5G Application", **Bumman Kim**, *POSTECH, Korea*

WSC (Full Day): Sunday 08:00–17:00
How mm-Wave Systems Reshape the Future of Telecom and Sensing Applications

Sponsors: **RFIC, IMS**

Organizers: **Harish Krishnaswamy**, *Columbia University, USA*
Vito Giannini, *Texas Instruments, USA*

Abstract: Due to high technology costs and limited integration capabilities, mm-wave systems have been mostly restricted to high-end markets. Today, however, we are witnessing a tipping point where both power consumption and cost can be lowered sufficiently to deploy economically viable solutions on a far larger scale. This workshop aims at showing the latest breakthroughs in millimeter-wave systems for mass-market applications. Thanks to these developments, the full potential of such mm-wave systems will become ever more apparent. The telecom industry will rely on mm-wave backhaul for transitioning to the so called 5G. The automotive industry is developing 77/79 GHz radar systems to boost road safety for all users. But millimeter-wave sensors are also applied in industrial, medical and home automation applications. Even consumer electronics will benefit from millimeter-wave technology to enable high-accuracy motion sensing.

Speakers:

1. "Ubiquitous Sensing with mm-Wave CMOS Radars", **Davide Guermandi**, *imec, Belgium*
2. "Highly Integrated mm-Wave Radar Transceiver Arrays", **Brian Ginsburg**, *Texas Instruments, USA*
3. "Project Soli: mmWave Radar for Ubiquitous Gesture Sensing", **Jaime Lien**, *Google, USA*
4. "Towards Autonomic mmWave Systems", **Alberto Valdes-Garcia**, *IBM, USA*
5. "Cost Effective mm-Wave System Development Leveraging Silicon and Digital Manufacturing Technologies", **Frederic Gianesello**, *STMicroelectronics, France*
6. "Material and Channel Measurements at mmWave Frequencies", **Andrzej Partyka**, *Qualcomm, USA*
7. "Large Phased Arrays for 5G Communication Systems", **Gabriel Rebeiz**, *University of California, San Diego, USA*
8. "Reconfigurable Millimeter-Wave Transmit-Array Antennas for Backhaul/Fronthaul Applications in 5G Mobile Networks", **Laurent Dussopt**, *CEA-LETI, France*

WSD (Half Day): Sunday 13:00–17:00
Circuit Techniques and System Architectures for Carrier Aggregation and Multi-Band Radios

Sponsor: **RFIC**

Organizers: **Eric Klumperink**, *University of Twente, The Netherland*
Osama Shana'a, *MediaTek, USA*

Abstract: During the last decades there have been several spectrum auctions of different parts of the mobile communication spectrum, and as a result mobile network operators now own non-contiguous parts of the spectrum. This non-contiguous spectrum allocation coupled with the increasing need for higher data-rate per user has led to the need for concurrent multi-channel operation, also known as carrier aggregation. Technically, this is extremely challenging, for instance because there may be strong unwanted signals between the carrier aggregation spectrum segments. This leads to new requirements and causes problems, for instance with respect to nonlinearity, crosstalk and LO pulling. This workshop will discuss these requirements and will primarily focus on advancements in RFIC transceiver architectures and circuits that enable carrier aggregation. It will also address some related aspects like broadband front ends, blocker detection, linearization, interference cancellation, etc.

Speakers:

1. "Systems Overview of Multi-Mode Multi-Band Radios Supporting Carrier Aggregation for LTE and LTE-A Standards", **Walid Ali-Ahmad**, *Qualcomm, USA*
2. "Design Challenges of Carrier Aggregation RF Receivers for LTE-Advanced", **Abdelatif Bellaouar**, *Global Foundries, USA*
3. "LO Generation and Reception Circuits for Carrier Aggregation", **Christopher Hull**, *Intel, USA*
4. "Design Challenges of Carrier Aggregation Transceivers", **Shahrzad Tadjpour**, *Marvell Semiconductor, USA*
5. "Design and Compensation of Concurrent, MIMO and Carrier-Aggregated Transmitters for Next-Generation Systems", **Fadhel M. Ghannouchi, Abubaker Abdelhafiz**, *University of Calgary, Canada*
6. "Frequency-Agile, Scalable Carrier Aggregation Using Frequency-Translating Quadrature-Hybrid Receivers", **Peter Kinget**, *Columbia University, USA*

WSE (Half Day): Sunday 08:00–12:00
Calibration and Correction Techniques for CMOS Radios

Sponsor: **RFIC**

Organizers: **Danielle Griffith**, *Texas Instruments, USA*
Mohyee Mikhemar, *Broadcom, USA*

Abstract: The state of the art CMOS radios make use of wide range of calibrations and correction techniques to meet their stringent performance and cost requirements. It is therefore critical for the RF CMOS designer to understand the potential and the limitations of the most common calibration and correction techniques. In most cases, these techniques can be used to compensate for device imperfections and random mismatches, which otherwise would require an over design in the Analog/RF domain. For example, the standard digital I/Q correction in receivers frees the designer from the burden of oversizing the analog/RF devices to reduce the effect of random mismatch. In the workshop, the most-common calibration and correction techniques for receivers, transmitters, PLLs, and power amplifiers will be presented.

Speakers:

1. "Calibration Techniques for Reference Oscillators Used in IoT", **Danielle Griffith**, *Texas Instruments, USA*
2. "Practical Correction and Cancellation Techniques in CMOS Receivers and Transmitters", **Masoud Kahrizi**, *Broadcom, USA*
3. "Calibration of CMOS mm-Wave Circuits Using Self-Healing", **Steven Bowers**, *University of Virginia, USA*
4. "Digitally Assisted Calibration and Correction of CMOS RF PLLs", **Thomas Mayer**, *Intel, Austria*

WSF (Full Day): Sunday 08:00–17:00
Advanced ICs and Systems for Wireless Charging and Energy Harvesting

Sponsors: **RFIC, IMS**

Organizers: **David Wentzloff**, *University of Michigan, USA*
Jenshan Lin, *University of Florida, USA*
Kenjiro Nishikawa, *Kagoshima University, Japan*
Patrick Riehl, *MediaTek, USA*

Abstract: Research into wireless power transfer has intensified in the past decade, with a wide spectrum of applications being addressed. Wireless power research spans many orders of magnitude of power (uW to kW), range (mm to km) and frequency (kHz to GHz). Although the basic principles of amplification, impedance matching and rectification have been well understood since Tesla's time, a variety of new techniques are presently being developed to enhance the performance of

wireless power transfer systems. In this interactive workshop, some of the leading researchers in the field will discuss the latest advancements in the campaign to free us from power cords, focusing on practical IC implementations. For consumers, the most exciting everyday application of wireless power today is mobile phone charging. A wide range of consumer devices such as tablets, laptops and wearables are expected to follow the same trend. We will hear from industry researchers pushing the boundaries of performance in mobile device charging using the Qi, PMA and A4WP specifications. Other speakers will focus in on challenging problems in the area of mobile device charging such as adaptive impedance tuning and EMI suppression. A related line of research deals with the problem of transmitting relatively low levels of power over large distance, or to inaccessible locations such as implantable devices. Energy harvesting circuits capture low levels of RF radiation to power the remote sensor nodes that will make up the Internet of Things. Expert presenters will cover the latest advancements towards efficiently extracting power from RF signals, including innovative rectifier designs and wave-shaping techniques.

Speakers:

1. "Integrated Circuit Design for Wireless Power Transmitters", **Patrick Riehl**, *MediaTek, USA*
2. "Considerations in the Design of a Multi-Protocol Wireless Charging Receiver", **Glenn Crosby**, *NXP Semiconductors, USA*
3. "Efficient and Adaptive Inductive Power Transmission and Management", **Mehdi Kiani**, *Pennsylvania State University, USA*
4. "A Smart Wirelessly Powered Home Cage for Long-Term High Throughput Behavioral Experiments", **Maysam Ghovanloo**, *Georgia Institute of Technology, USA*
5. "Electromagnetic Compatibility Issues on Wireless Charging", **Seungyoung Ahn**, *KAIST, Korea*
6. "High Efficient Rectennas with High Impedance Antennas", **Kenji Itoh**, *Kanazawa Institute of Technology, Japan*
7. "Adaptive Threshold-Voltage Compensated RF Energy Harvester", **Kambiz Moez[1], Zohaib Hameed[2]**, *[1]University of Alberta, Canada, [2]3M, USA*
8. "Theoretical Energy-Conversion Efficiency for Energy- Harvesting Circuits Under Power-Optimized Waveform Excitation", **Christopher Valenta**, *Georgia Institute of Technology, USA*
9. "Millimeter-Wave Power Harvesting: from CMOS Circuits to Diode Platforms", **Ke Wu, Pascal Burasa, Simon Hemour**, *École Polytechnique de Montréal, Canada*
10. "Microwave and mm-Wave Near-Field and Far-Field Wireless Power Transfer", **Ali Niknejad**, *University of California, Berkeley, USA*

WSG (Full Day): Sunday 08:00–17:00
Frequency Synthesizers of Multi-Band, Multi-Standard Radios and Internet of Things (IoT)

Sponsors: **RFIC, IMS**

Organizers: **Danielle Griffith**, *Texas Instruments, USA*
Jaber Khoja, *Consultant, USA*
Stefano Pellerano, *Intel, USA*

Abstract: A frequency synthesizer capable of generating LO with a wide frequency range is essential for multi-band, multi-standard radios. For simultaneously working radios in multi-bands and carrier aggregations radios, multiple LOs and synthesizers are needed for them to co-exist in a single radio. This workshop will discuss topics like wide range VCO design, frequency planning for multiple LO supports, along with wide range and power efficient LO distribution. The workshop will continue by introducing the fundamental concepts of oscillator synchronization, the theoretical models which allow us to predict phase noise and lock range of such circuits, and the applications of these concepts to multi-band and multi-standard SOC radios. The workshop will then move onto the practical issues arising from unwanted coupling between oscillators and, in general, among multiple on-chip frequency synthesizers. It would include discussion on the effect of strong coupling from power amplifiers on frequency pulling and frequency locking of frequency synthesizers in multi-bands and carrier aggregations radios. The most recent methods to counteract the negative effects of coupling will be reviewed. The emerging Internet of Things (IoT) market requires radios that operate with very low average power consumption to enable battery life measured in years, or even battery-free operation. This workshop will introduce seven types of oscillators used in these IoT radios, explaining how the low power requirements influence the oscillator architecture, design, and performance targets. This would include an explanation of concepts such as duty-cycling to reduce power consumption, benefits of efficient sleep timers, and standard IoT applications.

Speakers:

1. "Frequency Synthesizers Based on Realigned Oscillators", **Salvatore Levantino**, *Politecnico di Milano, Italy*
2. "Integrated Harmonic Oscillators",**Pietro Andreani**, *Lund University, Sweden*
3. "A Low-Power Low-Complexity Multi-Standard Digital Receiver for Joint Clock Recovery and Carrier Frequency Offset Calibration", **Stefan Heinen**, *RWTH Aachen University, Germany*
4. "Designing RF Frequency Synthesizers Robust to Interference", **Robert Bogdan Staszewski**, *University College Dublin, Ireland*
5. "Understanding VCO Pulling and its Mitigation in Wireless Transceivers", **Ahmad Mirzaei**, *Broadcom, USA*
6. "Pulling Effect and Operating Range Improvement Techniques for Frequency Synthesizers", **Kang-Chun Peng[1], Tzyy-Sheng Horng[2]**, *[1]NKFUST, Taiwan, [2]National Sun Yat-sen University, Taiwan*

7. "Oscillator Design for IoT Applications", **Danielle Griffith**, *Texas Instruments, USA*
8. "Fast-Locking Techniques for Phase-Locked Loops", **Tsung-Hsien Lin**, *National Taiwan University, Taiwan*

WSH (Half Day): Sunday 13:00–17:00
RF/Analog IC Design Challenges in Advanced CMOS Technology

Sponsor: **RFIC**

Organizers: **Madhukar Reddy**, *MaxLinear, USA*
Eric Fogleman, *MaxLinear, USA*

Abstract: Huge demand for lowering power, area and cost of digital circuits in highly integrated SOCs has led to fast development of deep submicron technologies to 28nm and beyond. With these advances and high levels of integration, several new challenges have emerged for RF, Analog and Mixed circuit designers who now have to design circuits in the same technology node as determined by the digital circuit designers. This workshop is aimed at covering the areas related to process technology, device modeling, RF/Analog/Mixed signal circuit design challenges and CAD tools and methodologies in these new advanced nodes. This first talk in this workshop will go through the details of the new process technology development for achieving high volume, production quality deep submicron processes and also explain the various new challenges introduced in these technology nodes. The second talk will explain the various physical effects of both the active and passive devices in these nodes and describe how the device models are being advanced to capture these effects to help the circuit designers predict the performance in simulations. The third and fourth talks will describe the challenges as seen from circuit designers' point of view and how they are being tackled. Despite the numerous challenges, these advanced nodes also offer some advantages which bring benefits to RF, Analog and Mixed signal circuits and new circuit topologies are being innovated to take advantage of these benefits. The final talk in this workshop will focus on CAD tools and methodologies being developed to ensure first silicon success in these nodes where mask and fabrication costs are prohibitively expensive. The workshop is aimed to provide a comprehensive view of technology to help both new and experienced circuit designers to adapt to the challenges in these advanced CMOS nodes.

Speakers:
1. "Advances in Process Technology Performance in Nanoscale CMOS", **Juan Cordovez**, *Global Foundries, USA*
2. "Device Modeling for RF/Analog Design in Advanced CMOS Technology", **Kimihiko Imura**, *MaxLinear, USA*
3. "Challenges for RF/Analog Circuits in 28nm and Beyond", **Uli Klepser**, *Intel, USA*
4. "Challenges in Mixed Signal Circuit Design in 28nm and Beyond", **Yun-Shiang Shu**, *MediaTek, USA*
5. "Advances in CAD Tools & Methodologies for First-Silicon Success in Advanced CMOS Nodes", **Ravi Subramanian**, *Mentor Graphics, USA*

WSJ (Half Day): Sunday 13:00–17:00
Millimeter-Wave Electronics: From Applications to Manufacturing

Sponsors: **RFIC, IMS**

Organizers: **Didier Belot**, *CEA-LETI, France*
Marco Pirola, *Politecnico di Torino, Italy*
Pierre Busson, *STMicroelectronics, France*
Vittorio Camarchia, *Politecnico di Torino, Italy*

Abstract: This workshop is dedicated to mm-wave applications in communications, both for end-user and infrastructure equipment. New products are emerging to answer the increasing market demand, or are in the last development phase. The workshop introduces these applications and products. The final cost of such products, together with the public acceptance of this growing technology, are key factors for the success of the mm-wave industry. The workshop also addresses these aspects, in particular regarding the efficient test of products and the health related issues of mm-wave.

Speakers:

1. "Introduction: Opportunities for the Millimeter-Wave Industry", **Roberto Quaglia**, *Cardiff University, UK*
2. "Capacity Increase: Millimeter-Wave Systems for Backhauling", **Matteo Oldoni**, *SIAE Microelettronica, Italy*
3. "Monolithic Solutions for Digital Radio Link Transceivers", **Maurizio Pagani**, *Huawei Technologies, Italy*
4. "mm-Wave MMIC Power Amplifier with Integrated Linearizer", **Marcus Gavell**, *Gotmic, Sweden*
5. "Antenna-Module with Integrated Shaped Lens for WiGig Applications in Eyewear Devices", **Cyril Luxey**, *Université Nice Sophia Antipolis, France*
6. "Low Cost Industrial mm-Wave Test, a Wish or a Reality", **Cedric Mayor**, *Presto, USA*
7. "The Human Body and Millimeter Wave Wireless Communication Systems: Interactions and Implications", **Philippe Leveque**, *University of Limoges, France*

WSK (Full Day): Sunday 08:00–17:00
e-Health:
Implantable Systems and Communications in the Human Body

Sponsors: **RFIC, IMS**

Organizers: **Amin Arbabian**, *Stanford University, USA*
Francois Rivet, *University of Bordeaux, France*

Abstract: This workshop aims to provide an overview of various in-body electronic systems, from applications to devices, with an emphasis on new technologies and emerging applications. Experts will discuss topics related to medical applications of implantable systems, device technologies to enable safe and long-term use of these technologies, in-body communication schemes and related tradeoffs, energy harvesting in the body, sensing and stimulation mechanisms for closed-loop operation, and future directions in the field. Various technological and legal questions are raised and the role of electronics and communication capabilities are assessed.

Speakers:

1. "Advanced Implantable Neuromodulation Systems", **Kevin Kilgore**, *Case Western Reserve University, USA*
2. "Capsule Endoscope Ultrasound Imaging", **Pierre Khuri-Yakub**, *Stanford University, USA*
3. "Photovoltaic Restoration of Sight in Animals with Retinal Degeneration", **Daniel Palanker**, *Stanford University, USA*
4. "Brain Stethoscope: A Tool for Listening to the Tone of the Human Brain", **Josef Parvizi**, *Stanford University, USA*
5. "Optimizing Devices and Processing at the Bio-Electronic Interface", **Sylvie Renaud**, *Bordeaux INP, France*
6. "Ultrasonically Powered mm-Sized Implantable Devices with Applications in Closed-Loop Neuromodulation", **Amin Arbabian**, *Stanford University, USA*
7. "Intra-Body Communications — Radio-Frequency versus Ultrasonic", **Yann Deval**, *University of Bordeaux, France*
8. "Applications of Signal Propagation Through the Human Body", **Daniel Lai**, *Victoria University, Australia*
9. "Soft Bio-Integrated Sensors", **Roozbeh Ghaffari**, *MC10, USA*

SUNDAY SHORT COURSE – 22 MAY 2016

SSA (Full Day): Sunday 8:00–17:00
Technologies for 5G

Sponsor: **IMS**

SSB (Full Day): Sunday 8:00–17:000
Introduction to RF Power Amplifier Design

Sponsor: **IMS**

MONDAY WORKSHOPS – 23 MAY 2016

WMA (Full Day): Monday 08:00–17:00
Millimeter-Wave Power Amplifier Technology: Where are We and Where are We Headed?

Sponsor: **IMS**

WMB (Half Day): Monday 08:00–12:00
Advances in High-Power SSPA Technology for KW-Operation at Microwave Frequencies

Sponsor: **IMS**

WMC (Half Day): Monday 13:00–17:00
Power and Signal Integrity Characterization Techniques

Sponsors: **IMS, ARFTG**

WMD (Full Day): Monday 08:00–17:00
Radio Miniaturization, Terahertz Nano-Sized Radios and Potential Applications

Sponsor: **IMS**

WME (Full Day): Monday 08:00–17:00
Large Signal Network Analysis: From Instrumentation Architectures to Software Applications for Your RF Design Flow

Sponsors: **IMS, ARFTG**

WMF (Full Day): Monday 08:00–17:00
Tunable and Reconfigurable Front Ends for Multiband Communication Systems

Sponsor: **IMS**

WMG (Full Day): Monday 08:00–17:00
Heterogeneous Integration of Silicon RFIC with III-V

Sponsor: **IMS**

WMH (Full Day): Monday 08:00–17:00
E-Band Communications: Market, Technology and IC Design

Sponsor: **IMS**

WMI (Half Day): Monday 08:00–12:00
Autonomous Vehicles

Sponsor: **IMS**

WMJ (Half Day): Monday 13:00–17:00
Entrepreneurship 101

Sponsor: **IMS**

MONDAY SHORT COURSES – 23 MAY 2016

SMA (Full Day): Monday 8:00–17:00
High-Speed Optical Transceiver Fundamentals

Sponsor: **IMS**

SMB (Half Day): Monday 13:00–17:00
Multi-Beam Antennas and Beam-Forming Networks

Sponsor: **IMS**

FRIDAY WORKSHOPS – 27 MAY 2016

WFA (Full Day): Friday 08:00–17:00
RF Design and Packaging for Wireless Wearable and Implants

Sponsor: **IMS**

WFB (Half Day): Friday 08:00–12:00
Advanced Millimeter-Wave 3D/Multilayer MCM/SoP and Printing Technologies

Sponsor: **IMS**

WFC (Half Day): Friday 13:00–17:00
Antenna and Packaging Integration Technologies for mmWave and Terahertz-Wave Applications

Sponsor: **IMS**

WFD (Half Day): Friday 13:00–17:00
mm-Waves Measurement Needs for 5G

Sponsor: **IMS**

WFE (Half Day): Friday 13:00–17:00
Phase Change Material Switches for a New Class of Microwave Control Components

Sponsor: **IMS**

WFF (Full Day): Friday 08:00–17:00
Emerging Devices for Microwave Circuits and Systems/Beyond Graphene Electronic Devices and their Potential for High-Frequency Applications

Sponsor: **IMS**

WFG (Full Day): Friday 08:00–17:00
Digital Signal Generation with Focus on Direct Digital Synthesis DDS

Sponsor: **IMS**

WFH (Full Day): Friday 08:00–17:00
Microwave and Photonics Techniques for Terahertz Applications in Science and Technology

Sponsor: **IMS**

WFI (Full Day): Friday 08:00–17:00
Theory and Applications of Wireless Power Transfer

Sponsor: **IMS**

WFJ (Full Day): Friday 08:00–17:00
Power Amplifiers with Variable Loads

Sponsor: **IMS**

FRIDAY SHORT COURSES – 27 MAY 2016

SFA (Half Day): Friday 08:00–12:00
Fundamental Advances on 2D Nano-Materials and Devices

Sponsor: **IMS**

SFB (Full Day): Friday 08:00–17:00
Principles of RF and Microwave Imaging Technology: From Radar to MRI

Sponsor: **IMS**

REGISTRATION

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration. It begins Monday, 1 February and will last through Monday, 25 April. Early Bird registration provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird is the 2nd tier or Advance Registration. It extends from Tuesday, 26 April through Friday, 20 May, just prior to the start of Microwave Week. The 3rd and final tier is the On-site Registration, starting on Saturday, 21 May, the first day of Microwave Week, and ending on Friday, 27 May.

Early Bird Registration: 1 February – 25 April 2016 (through midnight Hawaii Standard Time)

Advance Registration: 26 April – 20 May 2016 (through midnight Hawaii Standard Time)

Onsite Registration: 21 May – 27 May 2016

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit http://www.ieee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Registration Categories

Register online: https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=198

Symposia

Microwave Week includes the IMS technical program and exhibit, as well as the RFIC Symposium (http://rfic-ieee.org/), ARFTG Conference (http://www.arftg.org/).

Select the conference(s) you wish to attend.

- **SUPERPASS** registrants can attend as many technical sessions as they can from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend **One** full-day workshop (or half-day workshops, to equal one full-day), the Proceedings for IMS, RFIC, ARFTG, Workshop Electronic Proceedings for all three days and admission to the exhibits. In addition, the SUPERPASS will allow you to attend the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, the Kick-Off Reception on Monday, and the Awards Banquet on Wednesday.
- **RFIC Technical Sessions** are held on Monday and Tuesday. Registration includes admission to the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, exhibits, and the electronic proceedings.
- **IMS Technical Sessions** are held on Tuesday, Wednesday and Thursday. Registration includes admission to the exhibits, the electronic proceedings, and the Kick-Off Reception on Monday.
- **ARFTG Technical Sessions** are held on Friday. Registration includes breakfast, lunch, electronic proceedings, and admission to the ARFTG exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE members.

Exhibit Only Registration

Microwave Week hosts the largest exhibition of its kind with over 400 companies.

Exhibit only registration is available.

Additional Items to Add to Your Registration

1) Guest Registration

Attendees registered for the technical portion of the conference (SUPERPASS, IMS, RFIC, ARFTG) may add a Guest to their registration for an additional fee. Guest Registration includes access to the Hospitality Suite, Plenary Session, and Exhibit Hall, but does not allow access to Technical Sessions and Workshops. Select the Guest Registration tab below to add this to your registration. The name of the guest is added on the checkout page.

2) Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 25 May from 18:00–22:00 at the San Francisco Marriott Marquis in the Yerba Buena Ballroom. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

3) Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

4) Two Full-Day Workshop Registration

Purchase two full-day workshops by selecting the option titled "***Two Full-Day Workshop Registration***" and receive the electronic proceedings for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop electronic proceedings are not available for individual sale.

5) Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. Printed Workshop Notes for the workshop you are registered for are included when registered by the advance registration deadline of 20 May. After 20 May a nominal fee will be required for the printed workshop notes.

Full-day workshops include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and a morning refreshment break. Afternoon workshops include a lunch and an afternoon refreshment break.

6) Short Courses

The short course fee includes access to the short course selected and any materials that the short course organizers may provide.

Full-day short courses include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning short courses include a continental breakfast, and a morning refreshment break. Afternoon short courses include a lunch and an afternoon refreshment break.

7) Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to "2016 IEEE MTT-S". Written requests for refunds will be honored if received by 25 April 2016. Refer to the Refund Policy for complete details.

8) Refund Policy

Written requests received by 25 April 2016 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email when requesting a refund. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027, USA

nannette@mpassociates.com

ON-SITE REGISTRATION

Onsite registration for all Microwave Week events will be available in the South Hall of the Moscone Center. Registration hours are:

Date	Time
Saturday, 21 May	08:00–19:00
Sunday, 22 May	07:00–19:00
Monday, 23 May	07:00–19:00
Tuesday, 24 May	07:00–18:00
Wednesday, 25 May	07:00–18:00
Thursday, 26 May	07:00–16:00
Friday, 27 May	07:00–09:00

There will also be a satellite registration desk at the San Francisco Marriott Marquis on Level B2 for RFIC attendees. Registration hours are as follows:

Date	Time
Saturday, 21 May	08:00–19:00
Sunday, 22 May	07:00–19:00
Monday, 23 May	07:00–19:00
Tuesday, 24 May	07:00–12:00

Exhibit Only Registration

Exhibit only registration is available.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to IMS technical sessions and exhibits. The Press Lounge will available from Monday through Thursday of Microwave Week.

ARFTG Registration

Late onsite registration will be available in the South Hall of the Moscone Center on Friday from 07:00 to 09:00. If at all possible, please pre-register earlier in the week to reduce the onsite workload.

Registration Rates in USD	Early Bird (1 Feb–25 Apr)		Advance (26 Apr–20 May)		On-site (21–27 May)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Superpass						
Superpass	$1,040	$1,565	$1,210	$1,810	$1,405	$2,090
IEEE Life Member (Retiree)	$620		$725		$880	
Student	$620	$640	$725	$745	$880	$895
RFIC						
RFIC Sessions	$245	$345	$275	$400	$295	$435
IEEE Life Member (Retiree)	$170		$190		$210	
Student	$170	$190	$190	$210	$210	$230
IMS						
IMS Sessions	$450	$665	$520	$775	$600	$890
IEEE Life Member (Retiree)	$80		$90		$110	
Student	$80	$140	$90	$150	$110	$175
Single Day Registration	$230	$334	$265	$385	$305	$460
ARFTG						
ARFTG Sessions	$230	$345	$270	$400	$305	$460
IEEE Life Member (Retiree)	$160		$185		$205	
Student	$160	$185	$185	$210	$205	$230
Exhibit Only						
Exhibition Only Pass	$25	$25	$25	$25	$30	$30
Wednesday Exhibition Only Pass	free	free	free	free	free	free
Guest Badge	$30	$30	$30	$30	$30	$30

REGISTRATION RATES (continued)

Registration Rates in USD	Early Bird (1 Feb–25 Apr)		Advance (26 Apr–20 May)		On-site (21–27 May)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Full Day Short Course						
Full Day Short Course	$300	$445	$350	$525	$410	$615
IEEE Life Member (Retiree)	$210		$245		$280	
Student	$210	$235	$245	$265	$280	$300
Half Day Short Course						
Half Day Short Course	$210	$315	$245	$370	$280	$425
IEEE Life Member (Retiree)	$150		$175		$200	
Student	$150	$165	$175	$190	$200	$215
Full Day Workshop						
Full Day Workshop	$175	$255	$190	$280	$235	$350
IEEE Life Member (Retiree)	$135		$145		$165	
Student	$135	$150	$145	$160	$165	$180
Half Day Workshop						
Half Day Workshop	$90	$135	$105	$150	$125	$180
IEEE Life Member (Retiree)	$70		$75		$85	
Student	$70	$85	$75	$90	$85	$105
2 Full Day Workshops (includes all workshop proceedings: Sun Mon Fri)						
2 Full Day Workshops	$450	$665	$490	$725	$615	$910
IEEE Life Member (Retiree)	$335		$365		$415	
Student	$335	$355	$365	$385	$415	$440
Printed Workshop Notes	included	included	included	included	$30	$45

Registration Rates in USD	Early Bird (1 Feb–25 Apr)		Advance (26 Apr–20 May)		On-site (21–27 May)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Proceedings Electronic Download						
RFIC	$50	$75	$60	$90	$70	$105
IMS	$50	$75	$60	$90	$70	$105
ARFTG	$50	$75	$60	$90	$70	$105
Evening Events						
RFIC Sunday Evening Only (includes: RFIC Plenary Session, Industry Showcase and Reception)	$50	$75	$60	$90	$70	$105
Award Banquet (Wednesday Night)	$55	$55	$65	$65	$75	$75
Lunch						
Monday Boxed Lunch	$30	$30	$30	$30		
Tuesday Boxed Lunch	$30	$30	$30	$30		
Wednesday Boxed Lunch	$30	$30	$30	$30		
Thursday Boxed Lunch	$30	$30	$30	$30		

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning — if required — and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 37 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Currently, 37 countries participate in the Visa Waiver Program, as shown below:

Andorra	Germany	Luxembourg	Slovenia
Australia	Greece	Malta	South Korea
Austria	Hungary	Monaco	Spain
Belgium	Iceland	the Netherlands	Sweden
Brunei	Ireland	New Zealand	Switzerland
Czech Republic	Italy	Norway	Taiwan
Denmark	Japan	Portugal	United Kingdom
Estonia	Latvia	San Marino	
Finland	Liechtenstein	Singapore	
France	Lithuania	Slovakia	

For more information, see http://travel.state.gov/content/visas/en/visit.html.

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, http://www.cbp.gov/, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny.

To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. To allow sufficient time for processing, please submit your requests for letters of support well in advance of your interview dates, to Dr. Zaher Bardai at zb@ieee.org. All requests should include complete name (as in your passport) and current mailing address as this information is to be included in the letter for submission to the US Consulate. Also please contact Dr. Bardai for additional visa assistance queries.

Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (information to be posted shortly).

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative source of information is the U.S. Government website at http://travel.state.gov/content/visas/en.html.

SOCIAL EVENTS/GUEST PROGRAM

MONDAY, 23 MAY 2016

Welcome Celebration: 19:30–21:00

IMS2016 starts with a welcome celebration on Monday for all attendees, which will be hosted at the California Academy of Sciences in Golden Gate Park immediately following the IMS2016 Plenary Session.

TUESDAY, 24 MAY 2016

Women in Microwaves Reception: 18:00–19:30

The Women in Microwaves Reception will be held at the San Francisco Marriott Marquis Hotel, just a five minute walk from the Moscone Convention Center.

Young Professionals Panel Session and Networking Reception: 17:30–19:30

The Young Professionals are planning a panel session and networking event at the San Francisco Marriott Marquis. Please refer to the conference website for detailed information on the panel session.

WEDNESDAY, 25 MAY 2016

Industry-Hosted Cocktail Reception: 17:00–18:00

The Industry-Hosted Reception is scheduled on the exhibition floor on Wednesday, 25 May 2016 right before the MTT-S Awards Banquet.

Awards Banquet: 19:00–21:30

The MTT-S Awards Banquet will be hosted at the San Francisco Marriott Marquis and will feature exciting entertainment.

THURSDAY, 26 MAY 2016

Closing Ceremony: 16:00–17:30

The closing ceremony will immediately follow the Thursday closing session at the San Francisco Marriott Marquis.

MONDAY, 23 MAY – FRIDAY, 27 MAY 2016

Guest Lounge at San Francisco Marriott Marquis Hotel

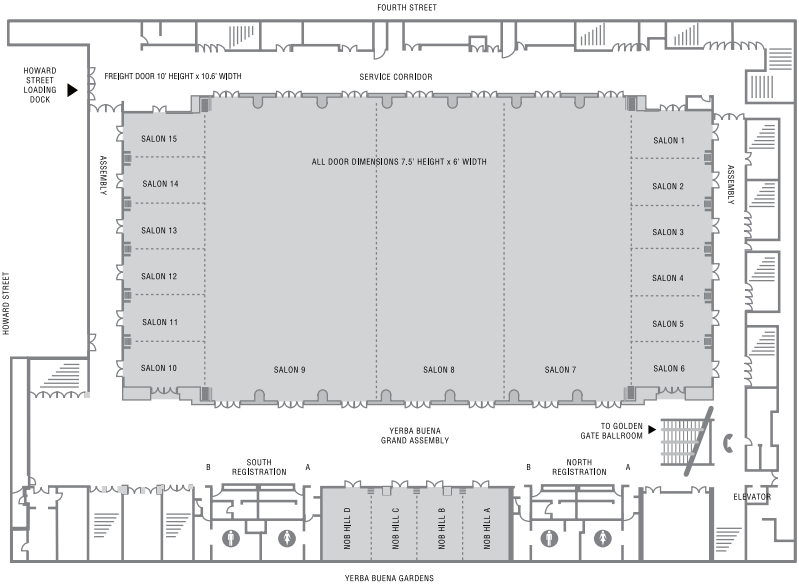
The guest lounge will be located at the San Francisco Marriott Marquis Hotel. Refreshments will be provided for all registered guests. The guest lounge serves as a hub for guests and a starting point for the day.

SAN FRANCISCO MARRIOTT MARQUIS MAPS

RFIC Plenary and Technical Sessions

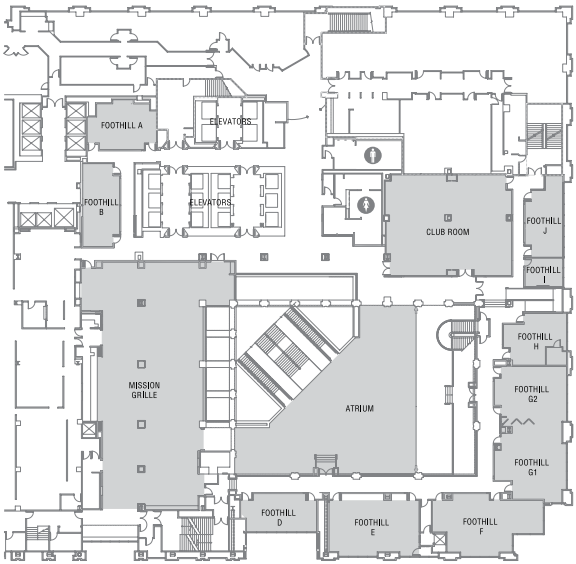
Yerba Buena Ballroom

LOWER B2 LEVEL



Foothill Meeting Rooms

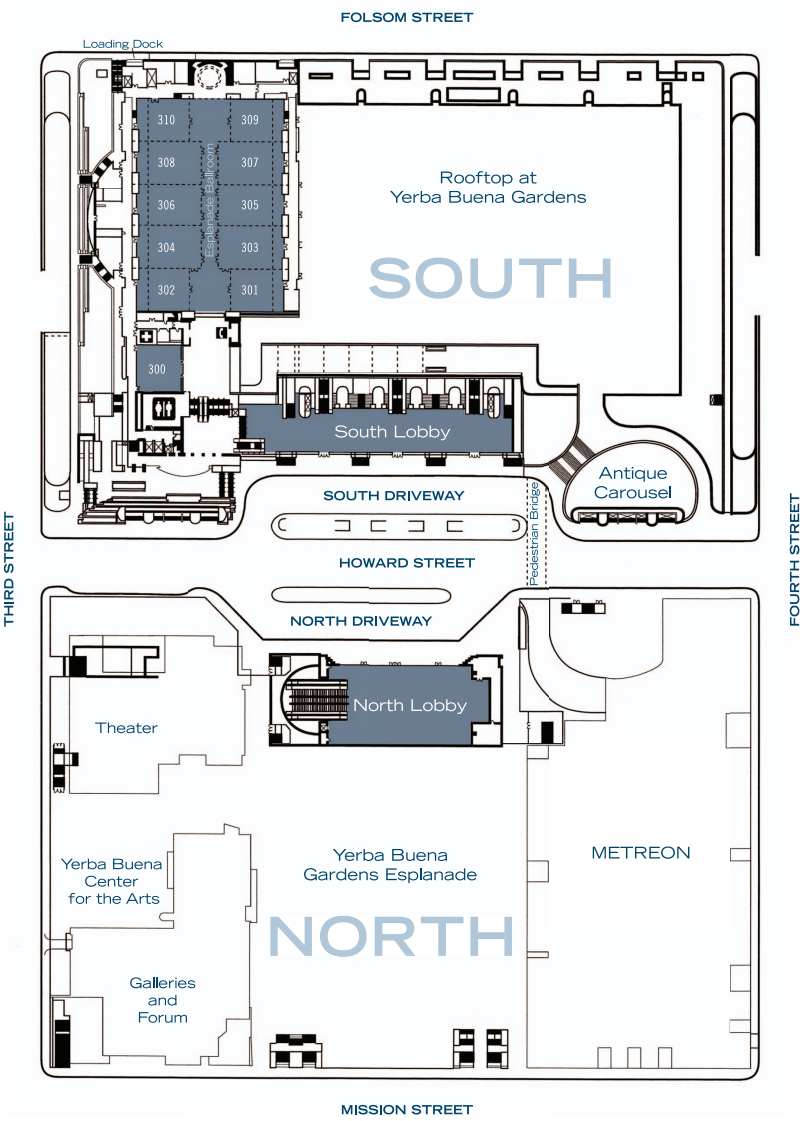
SECOND LEVEL



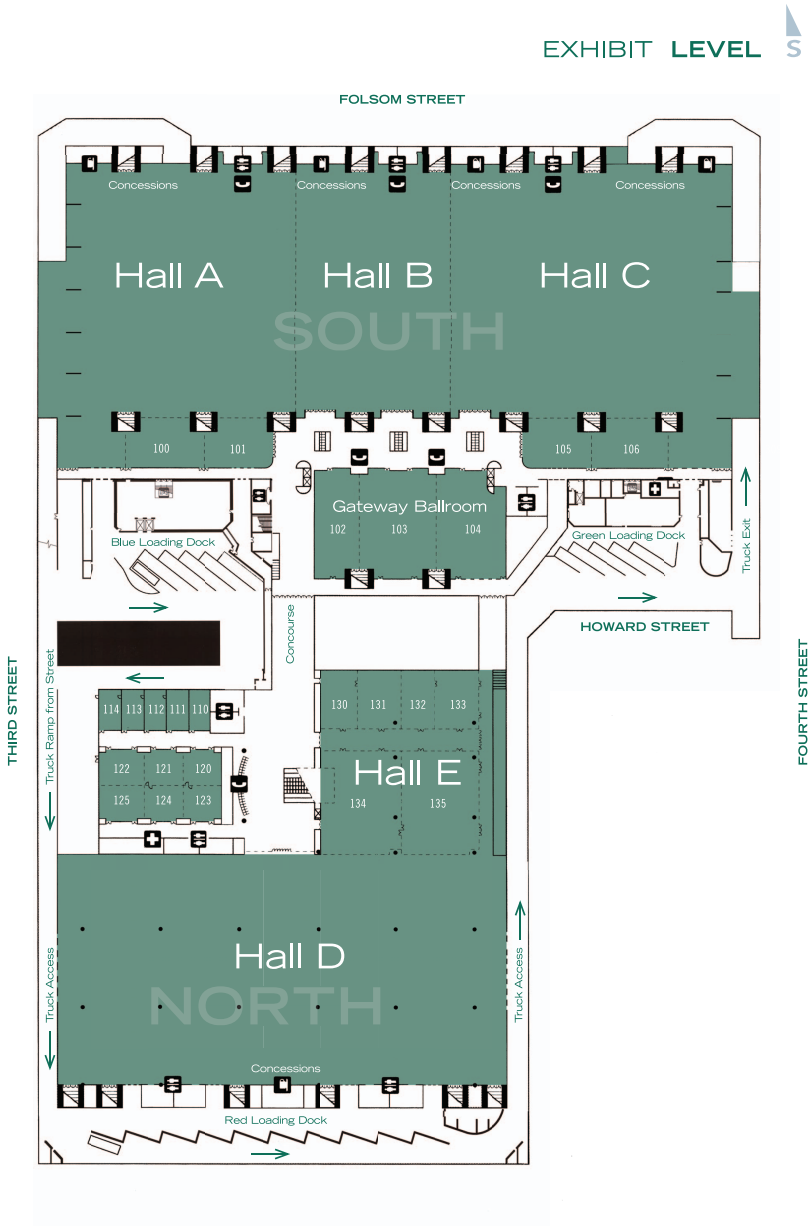
MOSCONE CENTER MAPS

IMS Workshops

ESPLANADE **LEVEL**



IMS Exhibits



NOTES

IEEE
445 Hoes Lane
Piscataway, NJ 08854, USA

2016 RFIC Symposium
San Francisco, California, USA
22–24 May 2016

PROGRAM