2012 IEEE Radio Frequency Integrated Circuits Symposium

Montréal, Canada

17-19 June 2012

IEEE

PROGRAM

Palais des congrès de Montréal
(Montréal Convention Center)

Sponsored by
IEEE Microwave Theory and Techniques Society
IEEE Electron Device Society
and
The IEEE Solid-State Circuits Society

RFIC Plenary and Reception
Sunday Evening (17 June 2012)

After a busy day of excellent RFIC Workshops (see page 63-77) the Plenary Session and RFIC Reception will be held on Sunday evening – 17 June 2012. The Plenary Session starts at 5:40PM in the Palais des congrès de Montréal (PCM), Level 7, Room 710A. The Plenary Session will include two outstanding speakers (see pages 8-10) and the Student Paper Awards ceremony. Immediately following the RFIC Plenary Session is the famous RFIC Reception in Rooms 710B and 715. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the latest news in the wireless industry. Admittance is included with the RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The RFIC Reception is sponsored by the RFIC Steering Committee, our Platinum (MediaTek and Skyworks), Gold (RFMD), and Silver (Anadigics) sponsors.

Platinum

SKYWORKS

MEDIATEK

Gold

RFMD

Silver

ANADIGICS

RFIC Symposium Activities (17-19 June 2012)

Saturday, 16 June 2012

2:00 PM – 6:00 PM	Registration – Palais des congrès de Montréal (PCM)

Sunday, 17 June 2012

7:00 AM – 6:00 PM	Registration - PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – Room 517A
8:00 AM – 5:00 PM	Workshops and Tutorials
11:30 AM – 1:00 PM	Workshops Lunch – Room 517A
5:40 PM – 7:00 PM	RFIC Plenary – Room 710A
7:00 PM – 9:00 PM	RFIC Reception - Rooms 710B and 715

Monday, 18 June 2012

7:00 AM – 5:00 PM	Registration – PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – Room 517A
8:00 AM – 9:40 AM	RMO1B, RMO1C, RMO1E
10:10 AM – 11:50 AM	RMO2A, RMO2C, RMO2D, RMO2E
Noon – 1:20 PM	RFIC Panel and Lunch – Room 516ABC
1:50 PM – 3:30 PM	RMO3B, RMO3C, RMO3D, RMO3E
4:00 PM – 5:20 PM	RMO4A, RMO4B, RMO4E

Tuesday, 19 June 2012

7:00 AM – 5:00 PM	Registration – PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – Room 517A
8:00 AM – 9:40 AM	RTU1A, RTU1B, RTU1C, RTU1D
10:10 AM – 11:50 AM	RTU2A, RTU2B, RTU2C, RTU2D
Noon – 1:20 PM	RFIC Panel and Lunch – Room 516ABC
1:30 PM – 4:00PM	Interactive Forum – Room 517CD

TABLE OF CONTENTS

The RFIC Symposium will be held in Montréal, Canada at the Palais des congrès de Montréal (Montréal Convention Center) on 17-19 June 2012 in conjunction with the International Microwave Symposium. It opens Microwave Week 2012, the largest RF/Microwave meeting of the year. The RFIC Symposium brings focus to the technical accomplishments in RF Systems, circuit device, and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Welcome Message from Chairpersons

Welcome to the 2012 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium (www.RFIC2012.org) which will take place in Montréal, Canada from June 17-19, 2012. Our Symposium, held in conjunction with the IEEE MTT-S International Microwave Symposium, opens Microwave Week 2012, the largest world-wide RF/Microwave meeting of the year.

The 2012 RFIC Symposium continues to build upon its heritage as one of the foremost IEEE technical conferences, increasing each year its impact and reputation of excellence. By bringing focus to the technical accomplishments in RF devices, circuits, and systems, the RFIC Symposium has become essential to both the academic and the industrial communities. This year's exciting technical program will cover a broad spectrum of topics including cellular and wireless-connectivity system ICs, broadband wireless communications, digitally enhanced RF circuits, software-defined radio and reconfigurable front-ends, ultralow-power frontends, silicon millimeter-wave ICs, integrated power amplifier design, frequency synthesis, RF device technology, and modeling and characterization.

The 2012 RFIC Symposium will start on Sunday, June 17 with a full lineup of half-day and full-day workshops. Workshops have been very popular at IEEE RFIC in the past, providing the opportunity for attendees to discuss new technical advances and share their design experiences. Following the success of the RFIC 2011 workshop program, we are pleased to announce a carefully selected, colorful and interesting workshop program for RFIC 2012. The attendees can expect thirteen RFIC workshops and one joint RFIC-IMS workshop for 2012, which cover a broad range of RF topics including: mm-Wave Silicon PAs; Fast-Settling RF Frequency Synthesis; Wireline Transceivers; RF at the Nanoscale; RF Spectrum Sensing and Signal Detection, Mobile and Wireless Front End Modules; RF and mmW PAs including Linearization, ICs for Biomedical Applications; Digital Transmitters; RF Noise Analysis; Short-Range Near-Field Communications; Active and Passive CMOS Mixers, RF Front-End and Transceiver Techniques, Multi-Standard Radio Coexistence, and finally 3D Integrated Circuits. Our committed workshop speakers are design experts from around the world including professors and practicing engineers.

The conference will hold a plenary session on Sunday evening with keynote addresses given by two renowned industry leaders. They will share their views and insights on the direction and challenges the RFIC design community face. The first speaker is Professor Thomas Lee of Stanford University, one of the pioneers of RF CMOS research for wireless communications. He will discuss some of the latest research in "***Terahertz Electronics: The Last Frontier***". The second speaker is Robert Gilmore, VP of Engineering at Qualcomm. He will bring perspective and knowledge from one of the leading wireless suppliers in the industry, with his talk, "***Towards the 5G Smartphone: Greater System Capacity, More Bands, Faster Data Rates, Advanced Applications and Longer Battery Life.***" In addition to the keynote addresses, the conference holds a student paper competition to encourage the publication of innovative research from university students. Awards to the three best student papers will be presented in the plenary session to acknowledge their contributions. The highly anticipated RFIC Reception will follow immediately after the plenary session, providing a relaxing time for all to mingle with old friends and catch up on the latest news.

On Monday and Tuesday, the conference will feature lunch-time panel sessions that traditionally draw strong debate between panel members as well as stimulating interaction between attendees and panelists. The Monday panel session is entitled "***THz Integrated Circuits: Do future markets support highly integrated silicon-based IC development?***", while the Tuesday panel session is

entitled "***RF scaling: Can it keep up with digital CMOS? Should it?***" Be sure to attend these lively and entertaining forums.

Technical papers will be presented all day Monday and Tuesday morning. There will be a total of 124 papers presented in 23 technical sessions. The technical program will conclude with the Interactive Forum session on Tuesday afternoon. This session features poster presentations giving the attendee the chance to speak directly with authors regarding their work.

The RFIC organization is thankful to the IMS 2012 team, whose support and hard work make the success of this conference possible. In addition, we are also grateful to all the technical contributors to the RFIC Symposium. We look forward to your participation in 2012. Please continue to make this conference such a vibrant gathering for the wireless industry!

We look forward to seeing you in Montréal!

Albert Jerng
General Chairman
MediaTek

Chris Rudell
TPC Chairman
Univ. of Washington

Larry Kushner
TPC Co-Chairman
BAE Systems

Steering Committee

Albert Jerng, MediaTek, *General Chair*

Jacques C. Rudell, Univ. of Washington, *TPC Chair*

Larry Kushner, BAE Systems, *TPC Co-Chair*

Yuhua Cheng, SHRIME Peking Univ., *Finance Chai*r

Albert Wang, UC Riverside., *Workshops Chair*

Kevin Kobayashi, RFMD, *Workshops Co-Chair*

Brian Floyd, North Carolina State Univ., *Publications Chair*

Georg Boeck, TU Berlin, *Publicity Chair*

Domine Leenaerts, NXP Semiconductors, *Panel Sessions Chair*

Bertan Bakkaloglu, Arizona State Univ., *Transactions/Guest Editor*

Srenik Mehta, Qualcomm, *Invited Papers Chair*

Freek van Straten, NXP Semiconductors, *Student Papers Chair*

Ian Gresham, NXP Semiconductors, *IMS RFIC Liaison*

Noriharu Suematsu, Tohoku Univ., *Asia Pacific Liaisons*

Takao Inoue, National Instruments, *Website Chair*

Tina Quach, *Conference Coordinator*

Advisory Board

Natalino Camilleri, *RFWDS* • Reynold Kagiwada, *NGAS*
Sayfe Kiae, *Arizona State University*

Joseph Staudinger, *Freescale Semiconductor Inc.*
Stefan Heinen, *RWTH Aachen University* • Luciano Boglione, *NRL*

Executive Committee

Jenshan Lin, *University of Florida*
Yann Deval, *University of Bordeaux, IMS Lab* • David Ngo, *RFMD*
Albert Jerng, *MediaTek*

RFIC 2012 Technical Program Committee

Ali Afsahi, *Broadcom Corp.*
Walid Ali-Ahmad, *MediaTek Inc.*
Bertan Bakkaloglu, *Arizona State University*
Edward Balboni, *Analog Devices*
Jean-Baptiste Begueret, *University of Bordeaux, IMS Lab*
Didier Belot, *ST Microelectronics*
Paul Blount, *Custom MMIC Design*
Georg Boeck, *Berlin Institute of Technology*
Luciano Boglione, *NRL*
Pierre Busson, *ST Microelectronics*
Natalino Camilleri, *RFWDS*
Sudipto Chakraborty, *Texas Instruments*
Richard Chan, *BAE Systems*
Glenn Chang, *MaxLinear*
Jinghong Chen, *Southern Methodist University*
Nick Cheng, *Skyworks Solutions*
Yuhua Cheng, *Shrime Peking University*
Guang-Kaai Dehng, *MediaTek Inc.*
Yann Deval, *University of Bordeaux, IMS Lab*
Oren Eliezer, *XtendWave*
Ayman Fayed, *Iowa State University*
Brian Floyd, *NC State University*
Eric Fogleman, *MaxLinear*
Ranjit Gharpurey, *University of Texas, Austin*
Aditya Gupta, *Northrop Grumman*
David Halchin, *Triquint Semiconductor*
Timothy Hancock, *MIT Lincoln Lab*
Andre Hanke, *Intel Corp.*
Hossein Hashemi, *USC*
Gary Hau, *Anadigics*
Stefan Heinen, *RWTH Aachen University*
Mona Hella, *Rensellaer Polytechnic Institute*
Frank Henkel, *IMST GmbH*
Chun-Ming Hsu, *IBM*
Tian-Wei Huang, *National Taiwan University*
Gernot Hueber, *NXP Semiconductors*
Nobuyuki Itoh, *Okayama Prefectural University*
Waleed Khalil, *Ohio State University*
Jaber Khoja, *Qualcomm*
Sayfe Kiaei, *Arizona State University*
Bumman Kim, *Pohang University of Science and Technology*
Eric Klumperink, *University of Twente*
Kevin Kobayashi, *RFMD*
Youngwoo Kwon, *Seoul National University*
Chang-Ho Lee, *Qualcomm*
Fred Lee, *Fairchild Semiconductor*
Tzung-Yin Lee, *Skyworks Solutions*
Domine Leenaerts, *NXP Semiconductor*
Salvatore Levantino, *Politecnico di Milano*
Donald Y.C. Lie, *Texas Tech. University*
Fujiang Lin, *University of Science and Technology of China*
Jenshan Lin, *University of Florida*
Li Lin, *Marvell Semiconductor*
Danilo Manstretta, *University of Pavia*
Srenik Mehta, *Qualcomm*
Pedram Mohseni, *Case Western*
Jyoti Mondal, *Northrop Grumman*
Arun Natarajan, *IBM*
Kenjiro Nishikawa, *Kagoshima University*
Jeyanandh Paramesh, *Carnegie Mellon University*
Stefano Pellerano, *Intel Corp.*
Sanjay Raman, *Virginia Tech*
Madhukar Reddy, *MaxLinear*
Bill Redman-White, *University of Southampton*
Francis Rotella, *Peregrine Semiconductor*
Derek Shaeffer, *InvenSense, Inc.*
Osama Shana'a, *MediaTek, Inc.*
Eddie Spears, *RFMD*
Bogdan Staszewski, *Delft University of Technology*
Joseph Staudinger, *Freescale Semiconductor Inc.*
Bob Stengel, *Motorola*
Freek van Straten, *NXP Semiconductors*
Noriharu Suematsu, *Tohoku University*
Julian Tham, *Broadcom Corp.*
Mark Tiebout, *Infineon Technologies*
Leon Van den Oever, *Radio Semiconductor Corporation*
Jeffrey Walling, *Rutgers University*
Albert Wang, *University of California, Riverside*
Hua Wang, *Georgia Institute of Technology*
Yanjie Wang, *Intel Corp*
Haolu Xie, *Fujitsu Microelectronic*
Chen Yang, *Shanghai Institute of Microsystem and Information Technology*
Patrick Yue, *The Hong Kong Univ. of Science and Technology*
Gary Zhang, *Skyworks Solutions*

RFIC Schedule 2012

The RFIC Symposium will be held in Montréal, Canada at the Palais des congrès de Montréal (PCM).

Saturday, 16 June 2012

2:00 PM – 6:00 PM	Registration – Palais des congrès de Montréal (PCM)

Sunday, 17 June 2012

7:00 AM – 6:00 PM	Registration - PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – PCM 517A
8:00 AM – 5:00 PM	Workshops and Tutorials – PCM
11:30 AM – 1:00 PM	Workshops Lunch – PCM 517A
5:40 PM – 7:00 PM	RFIC Plenary – PCM Room 710A
7:00 PM – 9:00 PM	RFIC Reception - PCM Rooms 710B and 715

Monday, 18 June 2012

7:00 AM – 5:00 PM	Registration – PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – PCM 517A
8:00 AM – 9:40 AM	RMO1B: Advances in LNA Design
	RMO1C: Spectrum Sensing and Cognitive Radio Receivers
	RMO1E: mm-Wave Power Amplifiers
10:10 AM – 11:50 AM	RMO2A: Millimeter Wave Phase Noise Reduction Techniques
	RMO2C: Advanced SDR Front-End Techniques
	RMO2D: W-band Circuits and Systems
	RMO2E: Advanced Transmitters and Power Amplifiers
Noon – 1:20 PM	RFIC Panel and Lunch – PCM 516ABC
1:00 PM – 2:00 PM	RFIC TPC Lunch Meeting – Westin, 9th floor, Ville Marie A&B
1:50 PM – 3:30 PM	RMO3B: RF Front-End Building Blocks
	RMO3C: Advanced Frequency Synthesis: Phase Locked Loops
	RMO3D: Terahertz Technology
	RMO3E: Multiband and Reconfigurable Power Amplifiers
4:00 PM – 5:20 PM	RMO4A: Low-Power RF Circuits
	RMO4B: Advances in CMOS Receivers
	RMO4E: Power Amplifiers for Wireless
5:30 PM – 7:00 PM	Int. Microwave Symp. Plenary Session, PCM 710

Tuesday, 19 June 2012

7:00 AM – 5:00 PM	Registration – PCM
7:00 AM – 8:00 AM	Speakers' Breakfast – PCM 517A
8:00 AM – 9:40 AM	RTU1A: Frequency Generation Using Injection Locking and Coupling Techniques
	RTU1B: Baseband Circuits and Modulators for Wideband Transceivers
	RTU1C: Advanced Frequency Synthesis: Building Blocks
	RTU1D: Silicon Devices for ICs from RF to Millimeter Waves
10:10 AM – 11:50 AM	RTU2A: Low-Power Solutions for Wireless Sensor Applications
	RTU2B: Advanced Mobile and Wireless Transceivers and SoC´s
	RTU2C: Advanced Modeling and Characterization for RF and mm-Wave Design
	RTU2D: 60 GHz Transceiver Circuits
Noon – 1:20 PM	RFIC Panel and Lunch – PCM 516ABC
1:00 PM – 2:00 PM	RFIC Steering Committee Lunch Meeting – Westin, 9th floor, Ville Marie A&B
1:30 PM – 4:00PM	Interactive Forum – PCM 517CD

Plenary Schedule

Sunday, 17 June 2012
5:40 PM
Montréal Convention Center – Room 710A
Session RSU5A: RFIC Plenary
Chair: Albert Jerng – MediaTek
Co-Chairs: Jacques C. Rudell - Univ. of Washington
Larry Kushner – BAE Systems

5:40 PM	Welcome Message from General and TPC Chairs, Student Paper Awards
6:00 PM	RSU5A-1: "Terahertz Electronics: The Last Frontier," Thomas Lee, Stanford University
6:30 PM	RSU5A-2: "Towards the 5G Smartphone: Greater System Capacity, More Bands, Faster Data Rates, Advanced Applications and Longer Battery Life," Robert Gilmore, Qualcomm

7:00 PM
Montréal Convention Center – Rooms 710B and 715
Session RSU5B: RFIC Reception

Plenary Speaker 1:

Thomas Lee
Professor
Stanford University

Terahertz Electronics: The Last Frontier

Abstract: Semiconductor technology continues to scale along predicted trajectories, delivering transistors with f_{max} values in the THz range. Unfortunately, a high f_{max} is not quite sufficient by itself. An inverse-quartic rolloff in specific output power, coupled with a dramatically increasing atmospheric attenuation as frequencies increase, create degraded link margins that frustrate exploitation of the valuable spectrum from roughly 300GHz to 3THz. This talk will describe compelling uses of this spectrum, including spectroscopy, imaging and XWB (extreme wideband) wireless communications, and will discuss how transistor technology limitations might be overcome by architectural innovations, as well as by new device structures. Exploitation of the terahertz realm represents perhaps the greatest challenge in the history of RF technology, and arguably represents the greatest opportunity.

About Thomas Lee

Thomas H. Lee has been at Stanford since 1994, where his research focus is on silicon RF IC technology. His graduate work at MIT resulted in the world's first RF CMOS IC in 1989. He has received several "Best Paper" awards, at ISSCC and CICC, and is a Packard Foundation Fellowship recipient.

He served for a decade as an IEEE Distinguished Lecturer of the Solid-State Circuits Society, and has been a DL of the Microwave Society as well. He holds 57 U.S. patents and authored "The Design of CMOS Radio-Frequency Integrated Circuits" and "Planar Microwave Engineering", and co-authored four additional books on RF circuit design. He also cofounded memory company Matrix Semiconductor (acquired by Sandisk in 2006) and Ayla Networks. He is currently on leave from Stanford to serve as Director of the Microsystems Technology Office at DARPA.

Plenary Speaker 2:

Robert Gilmore
Vice President, Engineering
QUALCOMM Inc.

Towards the 5G Smartphone: Greater System Capacity, More Bands, Faster Data Rates, Advanced Applications and Longer Battery Life

Abstract: During the last few years, there has been an explosive increase in demand for Smartphones with ever increasing capabilities, features and performance. Entertainment features, and mobile connectivity anywhere, anytime has become an accepted norm. There is a very competitive landscape driven by insatiable consumer demands, Operating System wars and chip level performance enhancements. There are numerous hardware challenges associated with this demand.

Power consumption is perhaps foremost. There are ever increasing processing power requirements and an increasing number of compute cores. Many of the new capabilities require that some circuitry be always on and always aware. Higher data rates demand wider bandwidth baseband circuits and faster DSP engines. Peak-to-average ratios of the transmitted waveforms increase as well, which increases the demand for more linear PA's and efficient Tx architectures. Channel aggregation and MIMO increase the number of simultaneously processed channels and demand power-efficient modem design.

Increased system capacity and global demand require an increasing number of frequency bands. This leads to a proportional increase in the number of front-end filters and overall RF front-end size and cost. Possibilities include a front end where several filters can be replaced by one tunable filter or by a wideband isolator such as hybrid transformer. This front-end will also require new tunable or broadband PA and LNA designs.

Achieving the system capacity required in future years will require a dense deployment of femto cells which will distribute traffic close to the user terminals. There will be an increased use of higher frequencies which will require greater than 5 GHz design, modeling, packaging and test. Finally, we will briefly touch upon semiconductor process, packaging and thermal issues.

About Robert Gilmore

Robert Gilmore serves as Vice President, ASIC Engineering in QUALCOMM's Corporate Research and Development having re-joined QUALCOMM in March, 2008. Mr. Gilmore has more than 30 years experience in engineering, communication systems design and development. Mr. Gilmore joined QUALCOMM as the ninth employee in October, 1985. His experience includes Senior Vice President of Hardware Engineering where he was responsible for the OmniTRACS production system, early testing of the CDMA cellular system, the Globalstar ground segment including gateways, phones and system engineering, and served as Senior Vice President of Engineering for the Consumer Products Division. From 2000-2008 Rob worked at Mobilian Corporation, Via Technology and Nextwave Inc. He worked at Linkabit Corporation from 1978 until 1984. Mr. Gilmore began his career as a co-op student at Bell Laboratories, where he worked both in digital radio and in satellite research. He earned his BSEE and MSEE degrees from the Massachusetts Institute of Technology.

Monday, 18 June 2012
8:00 AM
Room 511BE
Session RMO1B: Advances in LNA Design
Chair: Domine Leenaerts, NXP Semiconductors
Co-Chair: Danilo Manstretta, University of Pavia

RMO1B-1 8:00 AM
A 1GHz 1.3dB NF +13dBm Output P1dB SOI CMOS Low Noise Amplifier for SAW-less Receivers
B. Kim, D. Im, J. Choi, K. Lee, KAIST, Korea

Abstract: A CMOS capacitive loaded LNA is implemented using a 0.18µm SOI CMOS process. In order to achieve simultaneous improvement of NF and linearity of the LNA, the capacitive loading technique to achieve minimum NF and the complementary superposition with body-bias control to improve linearity are adopted. The measurements demonstrate that the LNA has a power gain of 10.7dB, a NF of 1.3dB, an OIP3 of +29.1dBm, and an output P1dB of +13dBm at 1GHz while drawing 20mA from a 2.5V supply voltage.

RMO1B-2 8:20 AM
A Wideband IM3 Cancellation Technique Using Negative Impedance for LNAs with Cascode Topology
W. Cheng, A. Annema, G. J. Wienk, B. Nauta, University of Twente, Netherlands

Abstract: A negative impedance is used to enable distortion cancellation between the transconductor and the cascode transistor for LNAs with a cascode topology. As a proof of concept, a resistive feedback LNA using this IM3 cancellation technique in a standard 0.16µm CMOS process shows that for 0.1GHz to 1GHz, improvements of 6.3dB to 10dB for IIP3 and 0.2dB to 1dB for gain are achieved without noise degradation. The power consumption for the LNA is increased by 2%, and the die area by about 700µm^2.

RMO1B-3 8:40 AM
A 1.2-6.6GHz LNA Using Transformer Feedback for Wideband Input Matching and Noise Cancellation in 0.13µm CMOS
H. Leung, H. C. Luong, The Hong Kong University of Science and Technology, Hong Kong

Abstract: A novel transformer feedback featuring wideband input matching and noise cancellation is proposed and demonstrated in a wideband differential LNA for software-defined-radio (SDR) applications. Implemented in 0.13µm CMOS with an area of 0.32mm^2, the LNA prototype measures a wideband input matching S11 of less than -10dB from 1.2GHz to 6.6GHz and minimum NF of 1.8dB while consuming 11mA at 1.2V supply.

RMO1B-4 9:00 AM
A CMOS Highly Linear Low-Noise Amplifier for Digital TV Applications
J. Bae[1], S. Kim[1], I. Lee[1], J. Cartwright[2], S. Lee[1], [1]Korea Advanced Institute of Science and Technology, Korea, [2]Virginia Polytech Univerisity

Abstract: This paper presents a highly linear low-noise amplifier (LNA) for Digital TV applications. By including a second-order nonlinear cancelling transistor to the noise cancelling circuit, the proposed LNA achieves high IIP3 which is immune to the offset frequency of two tone signals. The proposed LNA is implemented as a differential architecture in 0.13μm CMOS technology, and measurements show +17.8dBm, 12.4dB and 1.6dB of IIP3, gain and NF, respectively, while drawing 18.45mA from 1.2V.

RMO1B-5 9:20 AM
A 30GHz 2dB NF Low Noise Amplifier for Ka-band Applications
Q. Ma[1], D. Leenaerts[2], R. Mahmoudi[1], [1]Eindhoven University of Technology, Netherlands, [2]NXP Semiconductors

Abstract: A 30GHz Ka-band low noise amplifier (LNA) has been realized in a 0.25μm SiGe:C BiCMOS technology. A noise figure (NF) of 1.8-2.2 dB has been measured at 26-32 GHz. The achieved 3dB-power bandwidth is larger than 7GHz, with a peak gain of 12.4dB at 29.2GHz. The input 1dB compression point (ICP1dB) is -11dBm and input IP3 is -1.3dBm at 30GHz for a total power consumption of 98mW. The chip area including bond pads is 1mmx0.7mm.

Monday, 18 June 2012
8:00 AM
Room 511CF
Session RMO1C: Spectrum Sensing and Cognitive Radio Receivers
Chair: Walid Ali-Ahmad, MediaTek
Co-Chair: Glenn Chang, Maxlinear

RMO1C-1 8:00 AM
A 100MHz-2GHz 12.5x sub-Nyquist Rate Receiver in 90nm CMOS
J. Yoo[1], S. R. Becker[2], M. Loh[1], M. Monge[1], E. Candes[3], A. Emami-Neyestanak[1], [1]California Institute of Technology, [2]Paris 6 University [3]Stanford University

Abstract: A fully-integrated, high-speed, wideband receiver called the random modulation pre-integrator is realized in IBM 90nm digital CMOS. It achieves an effective instantaneous bandwidth of 2GHz, with 54dB dynamic range. Most notably, the aggregate digitization rate is f_s =320MSPS, 12.5x below the Nyquist rate. Signal recovery can be accomplished for any signal with a concise representation. The system is validated using radar-pulses and tones as the input and recovering the time-domain waveforms.

RMO1C-2 8:20 AM
A CMOS Spectrum Analyzer Front-end for Cognitive Radio Achieving +25dBm IIP3 and -169dBm/Hz DANL
M. S. Oude Alink, E. A. Klumperink, A. B. Kokkeler, W. Cheng, Z. Ru, A. Ghaffari, G. J. Wienk, B. Nauta, University of Twente, Netherlands

Abstract: A dual RF-receiver preceded by discrete-step attenuators is implemented in 65nm CMOS and operates from 0.3-1.0 GHz. The noise of the receivers is reduced by cross-correlating the two receiver outputs in the digital baseband, allowing the use of attenuation to increase linearity. With this technique, we obtain a displayed average noise level (DANL) below -169dBm/Hz, and +25dBm IIP3, giving a spurious-free dynamic range (SFDR) of 89dB in 1MHz resolution bandwidth (RBW).

RMO1C-3 8:40 AM
CRAFT: A 5GS/s 12.2pJ/conv. Analog Domain FFT for a Software Defined Radio Front-End in 65nm CMOS
B. Sadhu, M. Sturm, R. Harjani, University of Minnesota

Abstract: This work describes the design of CRAFT (Charge Re-use Analog Fourier Transform): an RF front-end channelizer for software defined radios (SDR) based on a 16 point analog domain FFT. The design relies on charge re-use to achieve 47dB average SNDR on a 5GS/s input, and consumes only 12.2pJ/conv. Due to its wide-band and low power channelization capabilities, it is expected to reduce the sample rate and dynamic range requirements for wide-band digitization in SDRs.

RMO1C-4 9:00 AM
A 12mW, 0.7-3.2GHz Receiver with Resonant Multi-phase LO and Current Reuse Harmonic Rejection Baseband

C. Andrews, L. Diamente, B. Johnson, A. Molnar, Cornell University

Abstract: A passive mixer-first receiver with resonant non-overlapping LO drive and noise-power optimized multi-path baseband amplifier is presented. The receiver consumes 10-12mW over a frequency range of 0.7-3.2GHz with a 1.3V supply. A novel LO generation architecture generates a 12.5% duty cycle resonant clock from standard LC-tank VCOs. A capacitor sharing technique on the baseband side of the mixer doubles the RX frequency range of the 8-phase clock, achieving a NF as low as 7dB.

RMO1C-5 9:20 AM
Transformer-Based Current-Gain-Boosted Technique for Dual-Band and Wide-Band Receiver Front-Ends

A. W. Ng, H. C. Luong, Hong Kong University of Science and Technology, Hong Kong

Abstract: Dual-band and wide-band receiver-front-ends (RFEs) using transformer-based current-gain-boost techniques are designed in 0.13μm CMOS. With a single switchable 3-coil transformer, the first dual-band RFE prototype measures NF of 2.5dB and 3.5dB and voltage gain of 20.7dB and 17dB at 1.7GHz and 3.8GHz, respectively. The second wide-band RFE achieves 0dBm IIP3 with 4dB NF and 13dB voltage gain over a frequency range from 2GHz to 5GHz.

Monday, 18 June 2012
8:00 AM
Room 510BD
Session RMO1E: mm-Wave Power Amplifiers
Chair: Jyoti Mondal, Northrup Grumman
Co-Chair: Leon van den Oever, Radio Semiconductor Corp.

RMO1E-1 8:00 AM
Optimized Power Combining Technique to Design a 20dB Gain, 13.5dBm OCP1 60GHz Power Amplifier Using 65nm CMOS Technology
S. Aloui[1], Y. Luque[1], N. Demirel[1], B. Leite[1], R. Plana[2], D. Belot[3], E. Kerherve[1], [1]University of Bordeaux, France, [2]Laas-CNRS, France, [3]STMicroelectronics

Abstract: Millimeter-wave Distributed Active Transformer (DAT), baluns and zero degree 1-4 splitter have been optimized to design a 60 GHz 65nm CMOS parallel Power Amplifier (PA). A lumped model based analysis is presented to compare pure voltage and mixed voltage and current combining techniques. At 61 GHz, the PA achieves a peak power gain of 20dB with a 13.5dBm 1dB-output compression point OCP1.

RMO1E-2 8:20 AM
A 34% PAE, 18.6dBm 42-45GHz Stacked Power Amplifier in 45nm SOI CMOS
A. Agah[1], H. Dabag[1], B. Hanafi[1], P. M. Asbeck[1], L. E. Larson[2], J. F. Buckwalter[1], [1]University of California, San Diego [2]Brown University

Abstract: A two-stack 42-45GHz power amplifier is implemented in 45nm SOI CMOS. Transistor stacking allows increased drain biasing to increase output power. Additionally, shunt inter-stage matching is used and improves PAE by more than 6%. This amplifier exhibits 18.6dBm saturated output power, with peak power gain of 9.5dB. It occupies 0.3mm² including pads while achieving a peak PAE of 34%. The PAE remains above 30% from 42 to 45GHz.

RMO1E-3 8:40 AM
The Multi-mode 60-GHz Power Amplifier with a Novel Power Combination Technique
J. Yeh[1], J. Tsai[2], T. Huang[1], [1]National Taiwan University, Taipei, Taiwan, [2]National Taiwan Normal University, Taiwan

Abstract: This paper discusses two issues including a new power-combined technique and efficiency enhancement technique in mm-wave power amplifier design. To the best of the author's knowledge, this is the first mm-wave power amplifier with efficiency enhancement technique at power back-off operations. The PA has peak power of 18.5dBm and the drain efficiency of the power stage of 24.1% at 60GHz. At 6dB power back-off operation, the drain efficiencies of power stage can be enhanced from 5.9% to 11.9%.

RMO1E-4 9:00 AM
A 60GHz Class-E Power Amplifier with PAE 25% in 32nm SOI CMOS

O. T. Ogunnika[1], A. Valdes-Garcia[2], [1]Massachusetts Institute of Technology, [2]IBM T. J. Watson Research Center

Abstract: A Class-E tuned CMOS power amplifier (PA) operating in the 60 GHz band is presented. Design and layout considerations to attain high-efficiency millimeter-wave PA operation are discussed. Both single-ended and differential versions of the single-stage PA are implemented in a 32nm SOI CMOS process. Peak power added efficiency of 27% (30%), power gain of 8.8dB (10dB), and saturated output power 9dBm (12.5dBm) are measured at 60GHz from the single-ended (differential) PA with 0.9V supply.

RMO1E-5 9:20 AM
A W-band Power Amplifier in 65-nm CMOS with 27GHz Bandwidth and 14.8dBm Saturated Output Power

K. Tsai, J. Kuo, H. Wang, National Taiwan University, Taiwan

Abstract: A W-band power amplifier in 65-nm CMOS technology is presented in this paper. Choosing high-pass topology for the inter-stage matching network and low-pass matching for the input and output to compensate device frequency response, we achieve a wide band and high output power PA. From the measurement results, under 1.2V supply voltage, the small signal gain of this PA is 12dB with 27GHz (79-106GHz) 3dB bandwidth. The saturated output power is 14.8dBm, and P1dB is 12.5dBm.

Monday, 18 June 2012
10:10 AM
Room 511AD
Session RMO2A: Millimeter Wave Phase Noise Reduction Techniques
Chair: Fred Lee, Fairchild Semiconductor
Co-Chair: Timothy Hancock, MIT Lincoln Laboratory

RMO2A-1 10:10 AM
A 21.8-27.5GHz PLL in 32nm SOI Using Gm Linearization to Achieve -130dBc/Hz Phase Noise at 10MHz Offset from a 22GHz Carrier
B. Sadhu[1], M. A. Ferriss[2], J. O. Plouchart[2], A. S. Natarajan[2], A. V. Rylyakov[2], A. Valdes-Garcia[2], B. D. Parker[2], S. Reynolds[2], A. Babakhani[4], S. Yaldiz[3], L. Pileggi[3], R. Harjani[1], J. Tierno[2], D. Friedman[2], [1]Univ. of Minnesota, [2]IBM, [3]Carnegie Mellon Univ. [4]Rice Univ.

Abstract: This paper describes a new approach to low phase noise LC VCO design based on transconductance linearization. A prototype 25GHz VCO, integrated in a dual loop PLL, is implemented in 32nm SOI, and achieves -130dBc/Hz at 10MHz offset from 22GHz. The paper also introduces a new layout approach that enables 23% tuning range. More than 500 measurements across PVT validate its robustness: phase noise variation across 46 dies is 0.6dB, across 0.7-1.5V supply is 2dB and across 80deg.C is 2dB.

RMO2A-2 10:30 AM
A Low-Phase-Noise 61 GHz Push-Push VCO with Divider Chain and Buffer in SiGe BiCMOS for 122 GHz ISM Applications
Y. Sun, C. J. Scheytt, IHP, Frankfurt Oder, Germany

Abstract: This paper presents a 61GHz push-push VCO with an integrated divide-by-eight divider and an output buffer in a 130nm SiGe BiCMOS process. Its tuning range is 60.85-63.65GHz with a measured output power of above 10dBm. The measured phase noise is -106dBc/Hz at 1MHz offset with an overall VCO/buffer power dissipation of 93.6mW. The VCO/buffer has achieved an efficiency of 14%, a figure-of-merit including output power (FOMP) of 193.1dBc/Hz and an ITRS FOM of 185.6dBc/Hz.

RMO2A-3 10:50 AM
An Ultra-Wideband D-Band Signal Source Chip Using a Fundamental VCO with Frequency Doubler in a SiGe Bipolar Technology
C. Bredendiek[1], N. Pohl[1], K. Aufinger[2], A. M. Bilgic[3], [1]Ruhr-Universitaet Bochum, Germany, [2]Infineon Technologies AG, [3]KROHNE Messtechnik

Abstract: This paper presents an ultra-wideband signal source chip for the D-Band in a SiGe:C bipolar technology. The architecture consists of a fundamental VCO with a frequency doubling stage. The goal of this architecture is to achieve a frequency generation with good phase noise, bandwidth, and output power. The architecture facilitates a 3dBm peak power and a 3dB bandwidth of 39GHz. The phase noise at 1MHz offset is -93dBc/Hz at 147GHz. The total power consumption is 410mW from a 5V supply.

RMO2A-4 11:10 AM
125 to 181GHz Fundamental-Wave VCO Chips in SiGe Technology
M. Jahn[1], K. Aufinger[2], T. Meister[2], A. Stelzer[3], [1]Johannes Kepler University, Austria, [2]Infineon Technologies AG, [3]Johannes Kepler University, Austria

Abstract: This paper presents four signal-generation chips that comprise fundamental-wave voltage-controlled oscillator (VCO), output buffer, and divide-by-32 prescaler. The VCOs with contiguous tuning ranges cover almost the full waveguide band from 110 to 170GHz (D band). The fastest VCO operates up to 181GHz in combination with the prescaler. The VCOs run on 1.8V, draw ~35mA, and achieve a phase noise ranging from -92 to -82dBc/Hz. The circuits are based on a SiGe technology with an *fmax* of 340GHz.

RMO2A-5 11:30 AM
High-resolution 60-GHz DCOs with Reconfigurable Distributed Metal Capacitors in Passive Resonators
W. Wu[1], J. R. Long[1], R. B. Staszewski[1], J. J. Pekarik[2], [1]Electronics Research Laboratory/DIMES, Netherlands, [2]IBM Microelectronics

Abstract: Mm-wave digitally-controlled oscillators (DCOs) with reconfigurable passive resonators are proposed, which achieve wide tuning range (10%) and fine frequency resolution (1MHz) simultaneously. Two 60GHz prototypes: an inductor-based L-DCO and a transformer-based T-DCO are demonstrated in 90nm CMOS. Both DCOs obtain 9.7% linear tuning range and phase noise lower than -90.5dBc/Hz at 1MHz offset. The T-DCO and L-DCO achieve fine frequency tuning step of 2.5MHz and 160kHz, respectively.

Monday, 18 June 2012
10:10 AM
Room 511CF
Session RMO2C: Advanced SDR Front-End Techniques
Chair: Oren Eliezer, Xtendwave
Co-Chair: Julian Tham, Broadcom

RMO2C-1 10:10 AM
A 1.8GHz Amplifier with 39dB Frequency-Independent Smart Blocker Suppression
E. Janssen, D. Milosevic, P. Baltus, Eindhoven University of Technology, Netherlands

Abstract: A 1.8GHz RF amplifier implemented in 140nm CMOS with 39dB frequency-independent blocker suppression is presented. While suppressing a 0-11dBm RF blocker, a small-signal voltage gain of 7.6 to 9.4dB and IIP3 4dBm is measured. This functionality is obtained by the adaptation of a nonlinear current transfer according to the blocker amplitude, which must be known. In case of blocker absence the circuit provides 17dB of voltage gain, 8.4dB noise figure and 6.6dBm IIP3 while consuming 3mW.

RMO2C-2 10:30 AM
A Tunable Differential Duplexer in 90nm CMOS
S. H. Abdelhalem[1], P. S. Gudem[2], L. E. Larson[3], [1]University of California at San Diego, [2]Qualcomm Inc., [3]Brown University

Abstract: An integrated duplexer for FDD standards around 2GHz is presented. The duplexer uses a differential version of a hybrid transformer to enable wideband differential and common-mode isolation. It covers WCDMA bands I, II, III, and IX, with worst-case isolation of 60dB and 40dB at the TX and RX frequencies respectively. The duplexer with a cascaded LNA achieves a noise figure of 5.6dB, and 14dB of gain. The TX insertion loss is 3.8dB. It occupies an active area of 0.6mm² in a 90nm CMOS process.

RMO2C-3 10:50 AM
A 0.3-3GHz Reconfigurable Digital Transmitter with Multi-bit Envelope Delta-sigma Modulator Using Phase Modulated Carrier Clock for Cognitive Wireless Sensor Networks
S. Hori, K. Kunihiro, M. Hayakawa, M. Fukaishi, NEC Corporation, Japan

Abstract: A reconfigurable digital transmitter for cognitive wireless sensor using phase-modulated-carrier-clocking multi-bit envelope delta-sigma modulation is presented. The prototype IC designed in 90nm CMOS process covers 0.3GHz ISM and 3GPP frequency bands up to 3GHz in conformity with IEEE 802.11g, W-CDMA and LTE in 5MHz-mode. The IC dissipates 10mW for 0.3GHz WCDMA and occupies 0.26mm².

RMO2C-4 11:10 AM

An RFDAC Based Reconfigurable Multistandard Transmitter in 65nm CMOS

B. Mohr[1], N. Zimmermann[1], B. T. Thiel[1], J. H. Mueller[1], Y. Wang[1], Y. Zhang[1], F. Lemke[3], R. Leys[3], S. Schenk[3], U. Bruening[3], R. Negra[1], S. Heinen[1], [1]RWTH Aachen University, Germany, [2]University of Heidelberg, Germany

Abstract: An RFDAC based transmitter for wireless mobile and connectivity applications is presented. Switchable LO drivers and unit cells with current shutdown are used to reduce the power dissipation when transmitting OFDM modulated signals with high PAPR (eg. WLAN, LTE). The frontend is capable of transmitting an 64QAM-OFDM WLAN signal at a center frequency of 1GHz with an output power of -8dBm and an EVM of 4.66%. Analog power dissipation is 34mW in this case. The frontend occupies ~0.4mm².

Monday, 18 June 2012
10:10 AM
Room 510AC
Session RMO2D: W-band Circuits and Systems
Chair: Paul Blount, Custom MMIC Design Services
Co-Chair: Brian Floyd, North Carolina State Univ.

RMO2D-1 10:10 AM
High-power High-Linearity SiGe Based E-BAND Transceiver Chipset for Broadband Communication

O. Katz[1], R. Ben-Yishay[1], R. Carmon[1], B. Sheinman[1], F. Szenher[2], D. Papae[2], D. Elad[1], [1]IBM - Haifa Research Labs, Israel, [2]IBM, East Fishkill

Abstract: Fully integrated chipset at E-band frequencies in a superhetrodyne architecture covering the lower 71-76GHz and upper 81-86GHz bands were designed and fabricated in 0.13µm SiGe technology. The receiver achieves a maximum gain of 65dB, 6dB noise figure, better than -10 dBm IIP3, with more than 65dB dynamic range, and consumes 600mW. The transmitter achieves output power at P_{1dB} of 17.5 to 18.5dBm, P_{SAT} of 20.5 to 21.5dBm, an analog controlled dynamic range of 30dB and consumes 1.75W.

RMO2D-2 10:30 AM
Three-Channel 77GHz Automotive Radar Transmitter in Plastic Package

H. Knapp[1], M. Treml[2], A. Schinko[2], E. Kolmhofer[2], S. Matzinger[2], G. Strasser[2], R. Lachner[1], L. Maurer[2], J. Minichshofer[2], [1]Infineon Technologies, [2]DICE, Austria

Abstract: We present a three-channel 77GHz radar transmitter in an embedded wafer-level ball grid array (eWLB) package. The circuit is manufactured in a 0.35µm SiGe bipolar process. It contains a 77GHz push-push oscillator and three independent power amplifiers with a maximum output power of 11.7dBm. An additional 18GHz oscillator and down-converter allow the realization of offset PLLs. The 77GHz and 18GHz oscillators achieve a phase noise of -76dBc/Hz and -93dBc/Hz at 100kHz offset, respectively.

RMO2D-3 10:50 AM
A 70-100GHz Direct-Conversion Transmitter and Receiver Phased Array Chipset in 0.18µm SiGe BiCMOS Technology

S. Shahramian, Y. Baeyens, Y. Chen, Alcatel-Lucent

Abstract: A transmitter and receiver phased array chipset is fabricated in 0.18µm SiGe BiCMOS. Each chip comprises four phased array elements with distributed calibration memory and calibrated direct up and down-conversion mixers. Both arrays operate from 1.5V and 2.5V and consume 1W. Each receive channel has a conversion gain of 33dB and noise figure of 7dB. Each transmit channel has a flat P_{SAT} of 5dBm. The transmitter is demonstrated using a 256QAM signal with 3% EVM and 0dBm output power at 90GHz.

RMO2D-4 11:10 AM
A 76-84 GHz 16-Element Phased Array Receiver with a Chip-Level Built-In-Self-Test System

S. Kim, O. Inac, C. Kim, G. M. Rebeiz, University of California, San Diego

Abstract: A 16-element phased array receiver with built-in-self test (BIST) is demonstrated at 76-84GHz. The BIST technique employs a miniature capacitive coupler located at the input port of each phased-array channel, and uses the receiver I/Q down-converter to measure the amplitude and phase of each channel. BIST measurements show that this technique can be used to greatly lower the testing cost and improve the self-calibration of mm-wave phased-array RFICs.

RMO2D-5 11:30 AM
A CMOS-Centric 77GHz Automotive Radar Architecture

C. Kim[1], P. Park[1], D. Kim[1], K. Park[1], M. Park[1], M. Cho[2], S. Lee[2], J. Kim[2], Y. Eo[2], J. Park[3], D. Baek[3], J. Oh[4], S. Hong[4], H. Yu[1], [1]ETRI, Korea, [2]Kwangwoon University, Korea [3]Chung-Ang University, Korea, [4]KAIST, Korea

Abstract: A CMOS- centric radar architecture is proposed, and one channel transceiver in a 65nm CMOS and LTCC array antenna is implemented. Measured 77GHz I/Q receiver showed a 22dB conversion gain. Two kinds of VCO showed 69.6-81GHz and 75.2-79.2GHz tuning range, respectively. A gain of 14.3dB and P_{1dB} of 10dBm is obtained at PA. The measured results showed a good agreement with simulated one. The performance of one channel radar and antenna will be discussed at conference.

Monday, 18 June 2012
10:10 AM
Room 510BD
Session RMO2E: Advanced Transmitters and Power Amplifiers
Chair: Donald Lie, Texas Tech University
Co-Chair: Joe Staudinger, Freescale, Inc.

RMO2E-1 10:10 AM
An 18dBm Transmitter Frontend with 29% PAE for 24GHz FMCW Radar Applications
W. Hung, H. Chen, S. Chou, L. Lu, National Taiwan University, Taiwan

Abstract: A CMOS transmitter frontend integrated circuit suitable for 24GHz FMCW radar applications is presented in this paper. With a transformer-based power-combining technique and pseudo-differential class AB power amplifiers, the proposed circuit exhibits enhanced output power and efficiency at a nominal supply voltage. The transmitter frontend is fabricated in a 65nm CMOS process, demonstrating an output power of 18dBm and a power-added efficiency of 29% at 1.2V supply voltage.

RMO2E-2 10:30 AM
Integrated S-Band Transmitter with On-chip DC-DC Converter and Control Loop
H. Brouzes[1], S. Geurts[1], P. de Hek[2], G. van der Bent[2], F. van Vliet[2], [1]Thales Nederland, Netherlands, [2]TNO, Netherlands

Abstract: A highly integrated high-power transmitter has been designed in a high breakdown GaAs MMIC technology. The transmitter includes, on top of an S-Band 10 W class-F HPA, a DC/DC converter and its associated gate driver, the full voltage regulation control loop, which provides a significant step for phased array transmit chain miniaturization and transmit pulse flexibility. The DC/DC converter operates at a measured switching frequency around 100MHz with an efficiency of 82%.

RMO2E-3 10:50 AM
A Long-Range, Fully-Integrated, Regulator-less CMOS Power Amplifier for Wireless Sensor Communications
W. Wesson, V. Bhagavatula, K. W. Pang, S. Shin, P. Yang, J. C. Rudell, University of Washington

Abstract: A CMOS PA intended for long-distance sensor communication is presented. The regulator-less PA operates directly off of a super-capacitor. A PA impedance scaling approach is implemented to maintain constant output power. The device integrates a 2-to-1 power combiner and a power control loop that monitors the power and digitally modulates the PA load impedance. The PA delivers 24dBm at 1.9GHz. As the PA VDD varies from 2.5V to 1.4V, the loop maintains constant output power with an accuracy of 1.6dB.

RMO2E-4 11:10 AM
A Low-power 20Gb/s Transmitter in 65nm CMOS Technology

M. Honarvar Nazari, A. Emami-Neyestanak, California Institute of Technology

Abstract: A 20Gb/s transmitter employing an analog filtering pre-emphasis equalization technique is presented. The transmitter dissipates 10mW from a 1.2V supply and occupies 0.01mm². This high-frequency boosting equalization technique allows for compensating channel losses up to 20dB at Nyquist-rate. The prototype was fabricated in 65nm CMOS technology and characterized using lossy cables and 5" and 10" FR4 PCB traces.

Monday, 18 June 2012
1:50 PM
Room 511BE
Session RMO3B: RF Front-End Building Blocks
Chair: Osama Shana'a, MediaTek
Co-Chair: Kenjiro Nishikawa, Kagoshima University

RMO3B-1 1:50 PM
A Linear CMOS SOI SP14T Antenna Switch For Cellular Applications
Q. Chaudhry, R. Bayruns, B. Arnold, Anadigics Inc.

Abstract: A high-power low-loss antenna switch is designed and fabricated in a 180nm SOI CMOS process. The RF switch is intended for mobile front ends which cover Quad band GSM and multiple WCDMA and LTE bands. The low loss and high linearity are made possible by the distributed RF architecture along with the multiple domain voltage generation which includes a negative voltage generator. The low loss, high dynamic range and isolation of this switch makes it an ideal candidate for next generation phones.

RMO3B-2 2:10 PM
Monolithically Integrated High Performance Digital Variable Gain Amplifiers
Y. Zhao, B. Hou, S. Zhang, Analog Devices

Abstract: A new monolithically integrated, digitally-controlled variable gain amplifier is presented. This high performance, low cost digital VGA operates from 100MHz to 4000MHz, packaged in LFCSP. Two high performance amplifiers and a digital step attenuator are integrated and fabricated by GaAs BiFET process. The first amplifier showes 41dBm OIP3. The second amplifier is 0.25 watt driver amplifier with 25dBm P1dB and 44dBm OIP3. The pHEMT DSA is 6-bit 0.5dB step and 31.5dB attenuation range.

RMO3B-3 2:30 PM
A Harmonic-Rejection Mixer with Improved Design Algorithm for Broadband TV Tuners
H. Zhang, T. Gao, S. Tan, O. Shana'a, MediaTek

Abstract: A wide-band harmonic rejection mixer for TV tuners with an improved design algorithm is fabricated in 65nm CMOS process. A more realistic mathematical formula is derived to calculate harmonic rejection performance. A systematic design optimization technique pushes the mean of the harmonic rejection performance to a higher value resulting in better yield. The measured 3rd and 5th order harmonic rejection ratio is better than -56dBc for VHFI and II bands without increasing any circuit complexity.

RMO3B-4 2:50 PM

A Transformer-Feedback Based Wideband IF Amplifier and Mixer for a Heterodyne 60GHz Receiver in 40nm CMOS

V. Bhagavatula[1], M. Boers[2], J. C. Rudell[1], [1]University of Washington, [2]Broadcom Corporation

Abstract: A wideband Intermediate Frequency section implemented for a 60GHz receiver is presented. The Transformer-Feedback based amplifier achieves a flat frequency response over 11-13GHz. An on-chip Lange Coupler generates the quadrature (I/Q) oscillator. The mixer employs a three-winding transformer to couple the Gm stage with the switching stages. Measured results show a peak power-gain of 27.6dB with a maximum gain variation of 3.6dB, 4.7dB NF, -22dBm IIP3 while consuming 28.8mW from a 0.9V supply.

Monday, 18 June 2012
1:50 PM
Room 511CF
Session RMO3C: Advanced Frequency Synthesis: Phase Locked Loops
Chair: Stefano Pellerano, Intel Corp.
Co-Chair: Yann Deval, University of Bordeaux

RMO3C-1 1:50 PM
A 90nm CMOS 5GHz Ring Oscillator PLL with Delay-Discriminator Based Active Phase Noise Cancellation
B. Bakkaloglu, S. Kiaei, S. Min, T. Copani, Arizona State University

Abstract: A fully integrated feed-forward, delay-discriminator based noise-cancellation architecture that improves phase noise characteristic of ring-oscillators outside the PLL bandwidth is presented. Proposed technique can improve the phase noise in an arbitrary offset frequency and bandwidth, and it is insensitive to process and temperature variations. The proposed cancellation loop suppresses the phase noise at 1MHz offset by 12.5dB and reference spur by 13dB, with 3.7mA power consumption.

RMO3C-2 2:10 PM
A Wideband Fractional-N PLL with Suppressed Charge-Pump Noise and Automatic Loop Filter Calibration
S. Levantino, D. Tasca, G. Marzin, M. Zanuso, C. Samori, A. L. Lacaita, Politecnico di Milano, Italy

Abstract: This paper discusses the design of a wideband fractional-N frequency synthesizer. The adoption of a bang-bang phase detector and a two-path loop filter reduces the impact of charge-pump noise to negligible levels with no penalty on power dissipation and enables a novel scheme for loop filter calibration. The synthesizer in 65nm CMOS consumes 5mW from a 1.2V voltage supply. Flat in-band noise is -104dBc/Hz over the 5.5MHz bandwidth and reference spur level is -71dBc at 40MHz.

RMO3C-3 2:30 PM
A 2.74-5.37GHz Boosted-Gain Type-I PLL with 15% Loop Filter Area
Y. Sun[1], J. Li[2], Z. Zhang[3], M. Wang[3], N. Xu[3], H. Lv[3], W. Rhee[3], Y. Li[3], Z. Wang[3], [1]Tsinghua University, China, [2]Analog Devices, [3]University of California, San Diego

Abstract: This paper describes a 64% locking-range type-I LC PLL architecture with a small loop filter area. By employing a dual-path LC VCO with a boosted open-loop gain at dc, a reference spur or a static phase error problem with a large frequency offset in the type-I PLL is alleviated. The prototype PLL is implemented in 0.13µm CMOS, achieving 2.74-to-5.37GHz locking range with -50dBc reference spur over active locking range.

RMO3C-4 2:50 PM
A Fully Integrated 1.7-2.5GHz 1mW Fractional-N PLL for WBAN and WSN applications

M. Vidojkovic[1], Y. Liu[1], X. Huang[1], K. Imamura[2], G. Dolmans[1], H. de Groot[1], [1]Holst Centre/Imec, Netherlands, [2]Panasonic

Abstract: This paper presents a wide-range low-power fully integrated fractional-N PLL. The PLL consumes 1.13mW to 1mW at 1.2V supply voltage, in a wide frequency range from 1.7GHz to 2.5GHz. It achieves up to -115 dBc/Hz phase noise at 1MHz offset and up to 2.5 degrees RMS phase error. The settling time is 40µs. The PLL is implemented in 90nm CMOS. The PLL can be used for low power wireless body area network (WBAN) and wireless sensor network (WSN) applications at 900MHz and 2.4 GHz.

RMO3C-5 3:10 PM
An Inductorless Injection-Locked PLL with 1/2- and 1/4-Integral Subharmonic Locking in 90nm CMOS

S. Lee, S. Ikeda, H. Ito, S. Tanoi, N. Ishihara, K. Masu, Tokyo Institute of Technology

Abstract: An inductorless PLL with 1/2- and 1/4-integral as well as integral subharmonic injection locking is realized, which can solve a tradeoff between the selectable frequency step and phase noise of injection-locked PLLs (ILPLLs). The proposed ILPLL was fabricated in 90nm CMOS process (PLL area: 0.083mm²). For a 80MHz reference, it shows that the 1MHz-offset phase noise was -106 dBc/Hz at 1.8GHz with injection. A 15dB reduction was achieved, compared with that in the case without injection.

Monday, 18 June 2012
1:50 PM
Room 510AC
Session RMO3D: Terahertz Technology
Chair: C. Patrick Yue, University of California, Santa Barbara
Co-Chair: Georg Boeck, Berlin University of Technology

RMO3D-1 1:50 PM
A 245GHz Transmitter in SiGe Technology
K. Schmalz, J. Borngräber, B. Heinemann, H. Rücker, J. C. Scheytt, IHP GmbH, Germany

Abstract: A 245GHz transmitter for sensing applications has been realized, which consists of a push-push VCO with optional 1/64 frequency divider, a transformer-coupled one-stage power amplifier, and a frequency doubler. It is fabricated in 0.13µm SiGe:C BiCMOS technology with f/f_{max} of 300GHz/500GHz. The peak output power of the transmitter is 2dBm. The 3dB bandwidth reaches from 229GHz to 251GHz. The transmitter dissipates 0.29 W.

RMO3D-2 2:10 PM
A 108-112GHz 4x4 Wafer-Scale Phased Array Transmitter with High-Efficiency On-Chip Antennas
W. Shin[1], O. Inac[1], Y. Ou[2], B. Ku[1], G. M. Rebeiz[1], [1]University of California, San Diego, [2]Qualcomm Inc.

Abstract: This paper presents 16-element wafer-scale phased array transmitter with scanning in both the E and H-planes. The chip integrates a 108-112 GHz source, together with a 1:16 distribution network, amplifiers, 2-bit phase shifters on each cell, and an on-chip high efficiency differential dipole antenna. Measured patterns show scanning to +/-30° in both planes, and agree well with simulations. The work can be extended to a large number of elements.

RMO3D-3 2:30 PM
A 480GHz Passive Frequency Doubler in 65nm Bulk CMOS with 0.23mW Output Power
R. Han, E. Afshari, Cornell University

Abstract: A passive 480GHz frequency doubler based on thick-gate MOS varactor with a dynamic cutoff frequency of 870GHz is reported. Using a partially-coupled ring structure, the doubler achieves a simultaneous broadband matching for fundamental and 2nd-harmonic signals. At 480GHz output frequency, the doubler has a measured conversion loss of 14.3dB and an unsaturated output power of 0.23mW. The simulated 3dB output bandwidth is 70GHz (14.6%). The doubler is fabricated using 65nm bulk CMOS technology.

RMO3D-4 2:50 PM

A Wideband Gain-Boosting 8mW LNA with 23dB Gain and 4dB NF in 65nm CMOS Process for 60 GHz Applications

E. Cohen[1], O. Degani[1], D. Ritter[2], [1]Intel, Haifa, Israel, [2]Technion, Haifa, Israel

Abstract: A 3 stage single-ended LNA using transformer matching and gain boosting by capacitive feedback for wideband operation in the 57-66GHz band is presented. The LNA fabricated in a 65nm CMOS process achieves 23dB gain and 4dB NF at 6mA and 1.25V supply, with 2dBm P_{SAT} and 0.05mm² in size. Different neutralization topologies were analyzed and compared based on analytical transformer models that were created.

RMO3D-5 3:10 PM

A Three-Stage Cascaded Distributed Amplifier with GBW Exceeding 1.5THz

A. Arbabian, A. M. Niknejad, University of California, Berkeley

Abstract: A three-stage cascaded distributed amplifier is designed in a 0.13µm SiGe BiCMOS process. By optimizing the amplifier both at the architecture and element level, an extremely large measured gain-bandwidth product in excess of 1.5THz is obtained. The core amplifier consumes 75mA from a 3.3V supply and provides an average gain of 24dB from 15GHz to at least 110GHz (limited by equipment BW). A distributed RF-choke design is employed to provide the bias current to the three cascaded stages.

Monday, 18 June 2012
1:50 PM
Room 510BD
Session RMO3E: Multiband and Reconfigurable Power Amplifiers
Chair: Jeffrey S. Walling, Rutgers University
Co-Chair: Nick Cheng, Skyworks Solutions, Inc.

RMO3E-1 1:50 PM
Concurrent L- and S-Band Class-E Power Amplifier in 65nm CMOS
R. Zhang, M. Acar, M. Apostolidou, M. P. van der Heijden, D. M. Leenaerts, NXP Semiconductors, Netherlands

Abstract: A 65nm CMOS dual-band class-E PA using high voltage extended-drain devices is presented. To implement sub-optimum class-E load impedance at L-band (1.0-1.3GHz) and S-band (2.8-3.1GHz), a concurrent transmission-line based dual-band output matching network is designed. The measurements show a η of 61% and a PAE of 50.5% for L-band with a Pout 30.4dBm. For S-band a η=2.6% and a PAE of 30% with a Pout of 28.9dBm are achieved. The output power variations are within 0.8dB and 1.6dB, respectively.

RMO3E-2 2:10 PM
A Fully-Integrated Self-Healing Power Amplifier
S. M. Bowers, K. Sengupta, K. Dasgupta, A. Hajimiri, California Institute of Technology

Abstract: The first fully-integrated self-healing mm-wave power amplifier heals process variation, load mismatch and transistor failure with on-chip sensors, actuators and an integrated digital algorithm ASIC without external calibration. Measurements of 20 chips showed increased RF power up to 3dB, or reduced DC power by 50% in backoff at 28 GHz. Healing 4-1 VSWR load mismatch for RF and DC power improvement was verified, and healing after laser induced transistor failure increased RF power up to 4.8dB.

RMO3E-3 2:30 PM
A Highly Integrated Dual-band SiGe Power Amplifier that Enables 256 QAM 802.11ac WLAN Radio Front-End Designs
C. P. Huang, P. Antognetti, L. Lam, A. Quaglietta, M. Doherty, W. Vaillancourt , Skyworks Solutions

Abstract: A highly integrated SiGe BiCMOS PA enabling the emerging 802.11ac WLAN applications is presented. The dual-band PA design integrates matching circuits, out-of-band rejection filters, power detectors, and bias controls in 1.5x1.6mm. The g-band PA achieves 28dB gain and the A-band PA achieves 32dB gain. Both bands can deliver 18dBm output power with 2% EVM. The design meets not only the regulatory requirements but also the linearity requirement of the emerging 256 QAM 802.11ac standard.

RMO3E-4 2:50 PM

A 3bit, 2Watt, Digital-Analog Gallium Nitride Power Amplifier for 64QAM Bandwidth Efficient Modulation with 25% Power Savings

M. K. Watanabe, T. R. LaRocca, Northrop Grumman Aerospace Systems

Abstract: A 3bit digital-analog power amplifier using 28V 0.2µm AlGaN/GaN HEMT, for high-power, high-rate, linearized transmitters, is presented. Unary-weighted, digitally-controlled auxiliary cells feed a main cell based on signal envelope power. The auxiliary cells compensate gain compression and extend P1dB by 2.5dB. Dynamic simulations with a 64-QAM signal predict 50% EVMRMS improvement and 25% power savings. Static measurements demonstrate 9.6dB linear gain, 2.2W P1dB, and 39.3% PAEP1dB at 7GHz.

RMO3E-5 3:10 PM

A Class-G Dual-Supply Switched-Capacitor Power Amplifier in 65nm CMOS

S. Yoo[1], B. Jann[2], O. Degani[3], J. C. Rudell[1], R. Sadhwani[2], J. S. Walling[4], D. J. Allstot[1], [1]University of Washington, [2]Intel Corp., Hillsboro, [3]Intel Corp., Israel, [4]Rutgers University

Abstract: A switched-capacitor PA (SCPA) that uses dual-supply voltage, class-G architecture is implemented in 65nm CMOS. It implements signal envelope digital-to-analog conversion via switches controlled by digital logic to achieve superior efficiency and linearity. The SCPA delivers peak (avg.) output power of 24.3 (16.8)dBm with peak (avg.) PAE of 44% (33%) for IEEE 802.11a signals with measured EVM of 2.9% in the 2.4GHz band. No digital predistortion is necessary because of the superior linearity.

Monday, 18 June 2012
4:00 PM
Room 511AD
Session RMO4A: Low-Power RF Circuits
Chair: Gernot Hueber, NXP Semiconductors
Co-Chair: Pierre Busson, ST Microelectronics

RMO4A-1 4:00 PM
A 13.56Mbps PSK Receiver for 13.56MHz RFID Applications
R. C. van de Beek[1], M. Ciacci[1], G. Al-Kadi[1], P. Kompan[2], M. Stark[2], [1]NXP Semiconductors, Netherlands, [2]NXP Semiconductors, Austria

Abstract: A phase-shift keying (PSK) receiver for 13.56Mbps communication over a 13.56MHz RFID link is presented, consisting of an analog front-end (AFE) IC and an FPGA digital baseband processor (DSP). The AFE recovers the carrier and performs PSK demodulation using a time-to-digital converter (TDC). The DSP's functions are symbol clock recovery in a closed-loop with the AFE as well as adaptive equalization. Bit error rates of below 2E-4 were achieved for transmitted field strengths above 1.2A/m.

RMO4A-2 4:20 PM
A Low-Cost, Low-Power UHF RFID Reader Transceiver for Mobile Applications
Q. Peng, C. Zhang, Y. Song, Z. Wang, Z. Wang, Tsinghua University

Abstract: A low-cost, low-power UHF RFID reader transceiver in 0.18μm CMOS process for short-distance applications supporting ISO 18000-6C is presented. The reader transceiver is composed of a RF transceiver, a digital baseband, a MCU and host interface. LDO modules are integrated so that the reader works with a lithium battery. Measured results show that the Tx output power is 21dBm; the Rx sensitivity is -55dBm at -1dBm carrier leakage. The chip occupies 14mm² and consumes 471mW from 3.3V power supply.

RMO4A-3 4:40 PM
A 2.45GHz Ultra-Low Power Quadrature Front-End in 65nm CMOS
C. Bryant, H. Sjöland, Lund University

Abstract: This paper presents a 2.45GHz ultra-low power direct conversion receiver front-end, intended for applications such as medical implants and body area networks. It consists of low noise amplifier, passive quadrature mixers, voltage controlled oscillator and frequency divider. Manufactured in 65nm CMOS it achieves 27dB gain and 9dB noise figure while consuming below 400μW from a 0.8V supply. Requiring only two inductors it occupies an area of less than 0.1mm² excluding pads.

RMO4A-4 5:00 PM

An Ultra Low Power, Compact UWB Receiver with Automatic Threshold Recovery in 65nm CMOS

B. Vigraham, P. R. Kinget, Columbia University

Abstract: A compact UWB receiver operating at 4.85GHz is presented in a 65nm CMOS technology. This non-coherent OOK receiver occupies an active area of only 0.4 mm², thanks to the use of few inductors and RF Gm-C filters. It achieves a sensitivity of -88 dBm at a data rate of 1 Mbps (for a BER of 1e-3) while consuming energy at a gradient of 450 pJ/bit from a 1.35 V supply. The receiver incorporates a single bit comparator based demodulator, with automatic threshold recovery for digitization.

Monday, 18 June 2012
4:00 PM
Room 511BE
Session RMO4B: Advances in CMOS Receivers
Chair: Ed Balboni, Analog Devices
Co-Chair: Jeyanandh Paramesh, Carnegie Mellon University

RMO4B-1 4:00 PM
A 2.4GHz MEMS based Sub-Sampling Receiver Front End Employing Low Power Channel Selection Filtering at RF
A. Heragu, D. Ruffieux, C. Enz, Csem SA, Jaquet Droz 7, Switzerland

Abstract: A sub-sampling RF front end which exploits the intrinsically high quality factor of MEMS devices for performing channel filtering at RF is proposed in this work. This narrow band filtering directly at RF also acts as a good anti-aliasing filter to support down-conversion by sub-sampling. The front end is integrated in 0.18µm CMOS process and it exhibits up to 300kHz bandwidth filtering at RF with 44.2dB conversion gain and 62dB rejection at 10MHz offset from the center frequency.

RMO4B-2 4:20 PM
A 42mW Wideband Baseband Receiver Section with Beamforming Functionality for 60GHz Applications in 40nm Low-Power CMOS
V. Szortyka[1], K. Raczkowski[1], M. Kuijk[2], P. Wambacq[1], [1]Imec, Belgium, [2]Vrije Universiteit Brussel, Belgium

Abstract: A 4-antenna path beamforming analog baseband section implemented in 40nm low power CMOS for use in a phased-array 60GHz receiver is presented. The circuit combines fourth-order filtering with a cutoff frequency of 1GHz, beamforming and variable gain between 10.6dB and 30dB. Output IP3 above 10dBm and output noise below 4.2mVrms over the whole gain range yield an SFDR larger than 31.2dB, which is sufficient for QAM16 modulation according to IEEE 802.15.3c. The circuit consumes less than 42mW.

RMO4B-3 4:40 PM
Harmonic Rejection Mixer at ADC Input for Complex IF Dual Carrier Receiver Architecture
L. Sundström[1], M. Anderson[1], M. Andersson[2], P. Andreani[2], [1]Ericsson AB, [2]Lund University

Abstract: This paper presents a receiver architecture for intra-band dual-carrier reception as specified for the upcoming releases of 3GPP HSPA and LTE standards. It is based on a time-discrete harmonic rejection complex-IF mixer to limit the bandwidth requirements on the ADCs to that of a single carrier. The mixer has been designed and fabricated together with a 3rd order continuous-time delta-sigma-ADC for proof-of-concept evaluation. Measurements show at least 68dB rejection at 2nd to 4th LO harmonic.

RMO4B-4 5:00 PM
A 600MHz to 3.4GHz Flexible Spectrum-Sensing Receiver with Spectrum-Adaptive Reconfigurable DT Filtering

D. T. Lin, H. Chae, L. Li, M. P. Flynn, University of Michigan

Abstract: A flexible spectrum-sensing receiver in 65nm CMOS consists of a wideband front-end, spectrum-adaptive (SA) filtering, switched-capacitor amplifiers, and a filtering SAR ADC. The SA filter uses a DT spectrum-analyzer and a reconfigurable DT notch filter to detect and suppress large interferers over a 55MHz range. In IEEE 802.15.4 tests, the receiver exceeds sensitivity and interferer rejection requirements. With SA filtering enabled, it achieves ≥+55dB rejection of +25 to +65MHz FM interferers.

Monday, 18 June 2012
4:00 PM
Room 510BD
Session RMO4E: Power Amplifiers for Wireless
Chair: Gary Zhang, Skyworks Solutions, Inc.
Co-Chair: Gary Hau, Anadigics Inc.

RMO4E-1 4:00 PM
Wideband Envelope Tracking Power Amplifier for LTE Application
D. Kim[1], D. Kang[1], J. Kim[1], Y. Cho[2], B. Kim[1], [1]Pohang University of Science and Technology, [2]WCU, Korea

Abstract: This paper describes an envelope tracking PA for LTE with large channel bandwidth up to 30 MHz. For the wideband operation, a supply modulator with accurate and fast envelope tracking is essential. The bandwidth of the supply modulator is increased about 2 times without stability degradation by inserting a zero in a feedback path of a linear amplifier. An implemented envelope tracking PA delivers efficiencies of 40.0/39.4/38.5% for 10/20/30MHz LTE signals at output power of 27dBm.

RMO4E-2 4:20 PM
A WCDMA 41% Power Efficiency Direct DC Coupled Hybrid CMOS/GaAs Power Amplifier with Pre-distortion Linearization
D. Leipold[1], W. Allen[2], G. Hau[2], P. Sheehy[1], [1]Anadigics, Warren NJ, [2]Anadigics, Tyngsboro MA

Abstract: A 1710-1755MHz hybrid power amplifier module consisting of a CMOS driver and a GaAs HBT output stage is described. Parallel CMOS gain stages are used to generate the gain and bias current expansion needed to maintain the HBT output stage linearity into class C operation. This increased the linear output power range by 0.5dBm and results in an increase of power added efficiency (PAE) with ACLR1 of -40dBc from 39.0% at 28dBm output power to 41.3% at 28.5dBm output power for a WCDMA signal.

RMO4E-3 4:40 PM
0.75 Watt and 5 Watt Drivers in Standard 65nm CMOS Technology for High Power RF Applications
M. Acar, M. P. Heijden, D. M. Leenaerts, NXP Semiconductors, Netherlands

Abstract: We present two high voltage (10V supply voltage), RF drivers in standard 65nm CMOS. The medium power(MP) driver operates from 0.5GHz to 4GHz with up to 9.6Vpeak-to-peak(pp) output voltage swing while driving a 3pF load capacitance. This driver consumes 0.75W dc power at 2GHz and achieves a duty-cycel control of 23% to 82% at 1GHz and 38% to 73% at 2GHz. The high power(HP) driver consumes 5W dc power at 2.14GHz while driving an RF power device (50W) with 30pF input capacitance.

RMO4E-4 5:00 PM
GaAs Bi-FET RF Front-end MMIC for WiMAX Applications

P. Wu[3], J. Li[1], Y. Wang[2], P. Hsu[3], [1]Industrial Technology Research Institute, Hsinchu, Taiwan, [2]WIN Semiconductor Corporation, [3]National Taiwan University

Abstract: A single-chip WiMAX RF front-end MMIC using GaAs Bi-FET process of WIN semiconductor corporation is presented. The MMIC integrates an HBT power amplifier, an E-mode pHEMT low-noise amplifier, and a D-mode pHEMT antenna switch. On-chip thermal and electrical isolation structures mitigate the interference problem from high-power devices. The MMIC delivers 24dBm linear power of 64QAM 802.16e signal with 17% power-added efficiency at antenna switch output. The chip size is 1.85mmx1.1mm.

Tuesday, 19 June 2012
8:00 AM
Room 511AD
Session RTU1A: Frequency Generation Using Injection Locking and Coupling Techniques

Chair: Nobuyuki Itoh, Okayama Prefectural University
Co-Chair: Madhukar Reddy, Maxlinear

RTU1A-1 8:00 AM
Fine Frequency Tuning through Injection-Control in a High-Swing 1.2V 65nm CMOS Quadrature Oscillator

A. Visweswaran, R. B. Staszewski, J. Long, Delft University of Technology

Abstract: Fine-tuning based on injection locking is proposed. The output frequency varies linearly with controllable relative strength of the injected signal. A prototype in 65nm CMOS, exhibits linear fine-tuning of 60MHz at an output swing where digital switches and CMOS varactors encounter fine-tuning limitations. The phase noise at 1 MHz, varies by only 1.15dB, and quadrature error from 0.3-1.6 degrees over the fine tuning. The fine-tuning response deviates from a straight line by less than 4%.

RTU1A-2 8:20 AM
CMOS LC Quadrature Oscillators with Enhanced Tuning Range by Selective Mode Switching

M. Bagheri[1], R. Bagheri[2], L. E. Larson[3], [1]University of California San Diego, [2]BroMarks, [3]Brown University

Abstract: Quadrature oscillators (QOSCs) can operate in two selective modes of quadrature oscillation. By controlling the mode of oscillation, different wide tuning range CMOS LC QOSCs have been designed. The measured tuning range is 60% for 3.7GHz design and to 94% for 1.3GHz design. Phase noise measurement shows that by this modified series coupled QOSC (S-QOSC) a FOMT (figure of merit with tuning range) of 199dB can be achieved.

RTU1A-3 8:40 AM
A 33% Tuning Range High Output Power V-Band Superharmonic Coupled Quadrature VCO in SiGe Technology

I. Nasr, M. Dudek, R. Weigel, D. Kissinger, University of Erlangen-Nuremberg, Germany

Abstract: This paper presents a wide tuning range 70GHz superharmonic coupled quadrature Colpitts VCO with high output power. The quadrature VCO employs a novel area efficient coupling technique that uses second harmonic coupling. The quadrature outputs have a maximum measured phase imbalance of 2 degrees over a 6GHz tuning range. The QVCO has a measured record tuning range of 33%. The maximum measured output power is +10.5 dBm and a minimum phase noise of -97dBc/Hz.

RTU1A-4 9:00 AM
A 0.8V 1.9mW 53.7-to-72.0GHz Self-Frequency-Tracking Injection-Locked Frequency Divider

J. Yin, H. C. Luong, Hong Kong University of Science and Technology, China

Abstract: A self-frequency-tracking (SFT) transformer-based injection-locked frequency divider (ILFD) with enhanced frequency locking range is presented. The SFT technique creates a frequency-dependent phase shift for the total current injected into the tank to relax both the phase and gain conditions. Fabricated in a 65nm CMOS process, the SFT-ILFD achieves an input locking range of 29% from 53.7 to 72.0GHz at 0dBm input power while dissipating 1.9mW from 0.8V, which corresponds to a FOM of 9.53.

RTU1A-5 9:20 AM
A 52-66GHz Subharmonically Injection-Locked Quadrature Oscillator with 10GHz Locking Range in 40nm LP CMOS

G. Mangraviti[1], B. Parvais[1], V. Vidojkovic[1], K. Vaesen[1], V. Szortyka[1], K. Khalaf[1], C. Soens[1], G. Vandersteen[2], P. Wambacq[1], [1]IMEC, Belgium, [2]Vrije Universiteit Brussel, Belgium

Abstract: A mm-wave subharmonically injection-locked quadrature oscillator is demonstrated in a 40nm digital CMOS technology. A large locking range (10GHz), tunable over 52-66GHz, is achieved using coupled resonators. A simple calibration scheme is proposed that only relies on a relative power measurement of the oscillator output signal. The wide locking range, the wide tunability and the simple calibration scheme make this design suitable for frequency synthesis in mm-wave CMOS communication systems.

Tuesday, 19 June 2012
8:00 AM
Room 511BE
Session RTU1B: Baseband Circuits and Modulators for Wideband Transceivers
Chair: Eric Fogleman, MaxLinear
Co-Chair: Ayman Fayed, Iowa State University

RTU1B-1 8:00 AM
A High-Dynamic Range, Broadband, RF Transmit Modulator IC
E. J. Balboni[1], B. Sam[2], D. Carbonari[2], J. Cowles[2], [1]Analog Devices, Wilmington, [2]Analog Devices, Beaverton

Abstract: This paper presents a high-dynamic range broadband transmit modulator IC. The modulator includes a complete high dynamic range baseband to RF signal chain. A high performance LO quadrature generator is also integrated. The modulator input bandwidth exceeds 700MHz and the RF and LO can operate from 400MHz to 6GHz. At 1GHz RF out, the modulator has a +26dBm OIP3 with -160dBm/Hz output noise. The 1.7mmx1.8mm IC consumes 200mA from a 5V supply.

RTU1B-2 8:20 AM
A 45GHz, 2bit Power DAC with 24.3dBm Output Power, 14 Vpp Differential Swing, and 22% Peak PAE in 45nm SOI CMOS
A. Balteanu, I. Sarkas, E. Dacquay, A. Tomkins, S. P. Voinigescu, University of Toronto

Abstract: A novel high efficiency, large output-power, 2-bit tuned mm-wave DAC realized in 45nm SOI CMOS is demonstrated. A record breaking 24.3dBm output power is achieved at 45GHz with 18.3dB saturated gain, 14.5Vpp differential output swing, a drain efficiency of 21.3% and 14.6% PAE. The best PAE is 22% at an output power of 23.5dBm. Operation at 45GHz with up to 2.5Gbps BPSK and up to 1.25Gbps ASK modulation is shown.

RTU1B-3 8:40 AM
An IF Digitizer IC Employing a Continuous-Time Bandpass Delta-Sigma ADC
R. Schreier[1], H. Shibata[1], P. Hendriks[2], M. Aliroteh[1], V. Kozlov[1], H. Tong[1], A. Del Muro[2], P. Shrestha[2], T. Caldwell[1], D. Alldred[1], W. Yang[2], D. Paterson[2], P. W. Lai[2], [1]Analog Devices, Toronto, [2]Analog Devices, Wilmington

Abstract: A 65nm CMOS IC containing a synthesizer, a bandpass delta-sigma ADC and associated digital filter digitizes 200-400MHz inputs with bandwidths up to 100MHz. The gain of the IC is adjustable over a 39dB range using an LNA in parallel with a resistive attenuator. The IC achieves NF = 7.5/26dB and IIP3 = 8/36dBm, at the +/-12dB gain settings. The IC consumes 1W from 1.0V and +/-2.5V supplies.

RTU1B-4 9:00 AM

A 5 Gbps Low Noise Receiver in 130nm CMOS For Wireless Optical Communications

B. Nakhkoob, M. M. Hella, Rensselaer Polytechnic Institute

Abstract: A design methodology for wideband, low noise and high gain wireless optical receivers using imaging architecture is presented. The receiver implemented in IBM 130nm CMOS technology achieves a bit error rate of 10^{-12} at 5Gbps corresponding to 2.8μA current at the input in presence of 1pF input capacitance representing the photodiode. The total power consumption is 68mW from 1.5V DC supply, while the die area including bonding pads and output buffer is 1106x895μm².

Tuesday, 19 June 2012
8:00 AM
Room 511CF
Session RTU1C: Advanced Frequency Synthesis: Building Blocks
Chair: Jaber Khoja, Qualcomm Inc.
Co-Chair: Salvatore Levantino, Politecnico di Milano

RTU1C-1 8:00 AM
Dual Channel Injection-Locked Quadrature LO Generation for a 4GHz Instantaneous Bandwidth Receiver at 21GHz Center Frequency
M. Elbadry[1], B. Sadhu[1], J. Qiu[2], R. Harjani[1], [1]University of Minnesota, [2]Army Research Laboratory

Abstract: This paper presents an LO generation scheme for a 21GHz center-frequency, 4GHz instantaneous bandwidth channelized receiver. A 1.33GHz reference source is used to simultaneously generate 20GHz and 22GHz LOs with quadrature outputs. A harmonic-rich signal, containing both even and odd harmonics of the input reference signal, is generated using a digital pulse slimmer. Two ILO chains are used to lock on to the 10th and 11th harmonics of the reference signal generating the 20GHz and the 22GHz LOs.

RTU1C-2 8:20 AM
A 2.9mW 53.4-79.4GHz Frequency-Tracking Injection-Locked Frequency Divider with 39.2% Locking Range in 65nm CMOS
Y. Chao, H. C. Luong, Hong Kong University of Science and Technology

Abstract: A frequency-tracking technique together with a single-coil distributed differential inductor is proposed to enhance the locking range of mmWave injection-locked frequency dividers (ILFDs). Implemented in a 65nm CMOS process, the proposed ILFD measures a locking range of 39.2% from 53.4GHz to 79.4GHz and consumes 2.9mW from a 0.8V supply corresponding to FOM of 8.97GHz/mW while occupying an area of 0.126mm².

RTU1C-3 8:40 AM
A 14.1GHz Dual-Modulus Prescaler in 130nm CMOS Technology Using Sequential Implication Logic Cells
W. Chen, E. Roa, W. Loke, B. Jung, Purdue University

Abstract: In this work, we demonstrate the use of a nontraditional logic for the implementation of a dual-modulus prescaler. The proposed prescaler consumes less power than TSPC designs and is faster than ETSPC designs. The maximum speed reaches up to 96% of that of a single divide-by-2 D-flip-flop, the theoretical limit. Implemented in 130-nm CMOS technology, the maximum input frequency reaches 14.1GHz with a power consumption of 1.2mW.

RTU1C-4 9:00 AM

A PAE of 17.5% Ka-band Balanced Frequency Doubler with Conversion Gain of 20dB

J. Li[1], Y. Xiong[2], W. Wu[2], [1]Nanjing University of Science and Technology, China, [2]MicroArray Technologies, China

Abstract: A Ka-band frequency doubler from 27 to 41GHz fabricated in 0.13µm SiGe BiCMOS with a maximum Pout of 8dBm and a PAE of 17.5% at Pdc of 35mW is presented. It consists of a balun, a driver amplifier, a common-base (CB) core and a medium PA. The CB topology with balun is designed for broadband and better matching. The measured results showed that a gain of 16.5-19.5dB, an output power of up to 8dBm, and a fundamental rejection of better than 25.7dB from 27 to 41GHz are achieved.

Tuesday, 19 June 2012
8:00 AM
Room 510AC
Session RTU1D: Silicon Devices for ICs from RF to Millimeter Waves
Chair: Aditya Gupta, Northrop Grumman
Co-Chair: Fujiang Lin, University of Science and Technology of China

RTU1D-1 8:00 AM
Millimeter-Wave Characterization of SiGe HBTs Noise Parameters Featuring f_T/f_{MAX} of 310/400 GHz
T. Quemerais, D. Gloria, S. Jan, N. Derrier, P. Chevalier, STMicroelectronics

Abstract: High frequency noise parameters determination of Si/SiGe HBTs are provided in the millimeter-wave range. An integrated tuner is used for the extraction of the noise parameters with the multi-impedance method. The designed tuner is composed of an active part with a low noise amplifier and a passive part with a travelling wave digitally tunable capacitance and both in series with a transmission line design for phase shifting. Measurements exhibit NFmin lower than 2dB at 68GHz for the HBT.

RTU1D-2 8:20 AM
The Impact of Narrow Width Effects on High Frequency Performance and Noise in 35nm Multi-Finger n-MOSFETs
K. Yeh, C. Chang, J. Guo, National Chiao-Tung University, Taiwan

Abstract: The impact of narrow width effects on f_T/f_{MAX}, and RF noise in 35nm multi-finger n-MOSFETs is investigated. Multi-OD devices with extremely narrow width and fixed finger number (NF) reveal higher Rg and Cgg, which lead to the penalty in f_T/f_{MAX}, and NFmin. Narrow-OD devices with larger NF can yield lower Rg and higher f_{MAX}, but still suffer lower f_T and higher NFmin. The mechanisms responsible for narrow width effects on f_T/f_{MAX}, and noise can guide nano-CMOS layout for RF circuits design.

RTU1D-3 8:40 AM
Nano Crystal Quantum Dots Tunable On-Chip ESD Protection
Z. Shi[1], A. Wang[1], Y. Cheng[2], [1]University of California, Riverside, [2]Peking University

Abstract: This paper reports a new nano crystal quantum dots tunable on-chip ESD protection mechanism and structures. Experiments validated the programmable ESD protection concept. Prototype structures achieved an adjustable ESD triggering voltage range of 2.5V, very fast ESD response of ~100pS, ESD protection density of 25mA/μm in HBM and 400mA/μm in CDM, and very low leakage current of Ileak ~15pA. It can be potentially used to design field-programmable ESD protection for mixed-signal IC in nano scales.

RTU1D-4 9:00 AM

A Novel Structure of Millimeter-Wave On-Chip Transmission Line Using Redistributed Copper Wire and Ground Shield

H. Namba, T. Sakamoto, T. Kuramoto, T. Hashimoto, S. Uchida, K. Hayashi, M. Furumiya, H. Ohkubo, Y. Nakashiba, Renesas Electronics Corporation

Abstract: This paper presents novel structures of millimeter-wave (mmW) on-chip transmission lines (TL) using redistributed thick Cu wires with ground shields. Simulations and measurements up to 110GHz prove that global-Cu-wire ground shields produce minimum attenuation: less than 0.5dB/mm at 60GHz. This stands comparison with TL on SOI substrate or Au-wire-bonding TL on GaAs substrate. For the first time, an mmW Si on-chip transmission line on a standard 40nm CMOS process was fabricated successfully.

RTU1D-5 9:20 AM

Stacked-Spiral RF Inductors with Fully-Filled Vertical Nano-Particle Magnetic Core

J. Zhan[1], X. Wang[2], Q. Fang [2], Z. Shi[2], Y. Yang[1], T. Ren[1], A. Wang[2], Y. Cheng[3], X. Li[4], C. Yang[4], [1]Tsinghua University, [2]University of California, Riverside, [3]Peking University, [4]Shanghai Institute of Microsystem and Information Technology

Abstract: A new concept of stacked-spiral inductor fully-filled with VERTICAL closed-circuit nano-particle magnetic core in CMOS is reported. Prototypes, fabricated in a six Al metal layer CMOS backend process using ferrite nano-particles, show a high inductance-density up to 920nH/mm² in multi-GHz, which is promising for making super compact inductors in RF system-on-a-chip (SoC).

Tuesday, 19 June 2012
10:10 AM
Room 511AD
Session RTU2A: Low-Power Solutions for Wireless Sensor Applications

Chair: Pedram Mohseni, Case Western Reserve University
Co-Chair: Hua Wang, Georgia Institute of Technology

RTU2A-1 10:10 AM
A 98nW Wake-Up Radio for Wireless Body Area Networks

N. E. Roberts, D. D. Wentzloff, University of Michigan

Abstract: A 0.13µm CMOS low power wake up radio is presented. The wake up radio operates with -41dBm sensitivity at 915MHz using OOK modulation with a data rate of 100kbps while consuming 98nW active power, 11pW sleep power, and has an energy efficiency of 0.98pJ/bit. The wake-up radio occupies 0.03mm² and uses two external components (an inductor and a capacitor). All biasing and calibration for process variation and mismatch is included on-chip. The entire radio operates from a single 1.2V supply.

RTU2A-2 10:30 AM
Highly Sensitive and Low Power Injection-Locked FSK Receiver for Short-Range Wireless Applications

R. Ye[1], T. Horng[1], J. Wu[2], [1]National Sun Yat-Sen University, Taiwan, [2]National Kaohsiung Normal University, Taiwan

Abstract: A highly sensitive non-coherent frequency-shift keying (FSK) receiver with low power consumption that is based on the injection-locking technique for short-range wireless applications is proposed and fabricated using 90nm CMOS technology. The proposed injection-locked FSK receiver comprises a sub-mW low-noise amplifier (LNA), a transformer splitter with three interlaced wires, and an injection-locked FSK demodulator that is based on a self-oscillating mixer.

RTU2A-3 10:50 AM
Multi-channel 180pJ/b 2.4GHz FBAR-based Receiver

P. M. Nadeau, A. Paidimarri, P. P. Mercier, A. P. Chandrakasan, Massachusetts Institute of Technology

Abstract: A three-channel 2.4GHz OOK receiver is designed in 65nm CMOS and leverages MEMS to enable multiple sub-channels of operation within a band at a very low energy per received bit. The receive chain features an LNA/mixer architecture that multiplexes signal pathways without degrading the quality factor of the resonators. The signal is then efficiently amplified at IF to enable envelope detection. The receiver consumes 180pJ/b from 0.7V with a sensitivity of -67dBm at 1Mb/s.

RTU2A-4 11:10 AM
A 4.9mW 7.5Mbps DAC-less 16QAM Transmitter for WBANs in Medical Applications

Q. Zhang, W. Lou, W. Liu, N. Wu, Institute of Semiconductors, Chinese Academy of Sciences, China

Abstract: A 4.9mW 7.5Mbps DACless 16QAM transmitter for wireless body area networks (WBANs) is presented. The conventional transmitter architecture with power hungry DACs and Mixers is avoided. And the new transmitter architecture with direct phase signal generation, combing and amplitude switching is proposed to achieve the 16QAM in a low power way. Implemented in a 0.18μm CMOS process, the transmitter delivers 0.23dBm output power with 7.5Mbps data rate and dissipates only 4.9mW power.

Tuesday, 19 June 2012
10:10 AM
Room 511BE
Session RTU2B: Advanced Mobile and Wireless Transceivers and SoC´s

Chair: Srenik Mehta, Qualcomm Inc.
Co-Chair: Andre Hanke, Intel Corp.

RTU2B-1 10:10 AM
Invited Paper: The Path towards Gb/s Wireless LANs

M. Zargari, Qualcomm-Atheros

Abstract: Enabling Gb/s throughputs in wireless LAN systems require significant upgrades to the 802.11 standard which in turn brings new challenges for the radio designers. This paper describes some of these challenges and potential solutions.

RTU2B-2 10:30 AM
A WLAN and Bluetooth Combo Transceiver with Integrated WLAN Power Amplifier, Transmit-Receive Switch and WLAN/Bluetooth Shared Low Noise Amplifier

R. Winoto, M. He, Y. Lu, D. Signoff, E. Chan, C. Lin, W. Loeb, J. Park, L. Lin, Marvell Semiconductor

Abstract: Front-end circuit of a System-on-a-Chip (SoC) containing an IEEE 802.11b/g/n wireless LAN (WLAN) and a Bluetooth transceiver is presented. The SoC integrates a WLAN power amplifier (PA), a transmit-receive switch (T/R switch), a power detector and a low-noise amplifier (LNA) that is shared between WLAN and Bluetooth. The class AB power amplifier has a maximum saturated output power of +29dBm, while still meeting -28dB EVM for QAM64 modulation at an output power of +21dBm.

RTU2B-3 10:50 AM
A Multiband LTE SAW-Less CMOS Transmitter with Source-Follower-Drived Passive Mixers, Envelope-Tracked RF-PGAs, and Marchand Baluns

T. Kihara[1], T. Sano[1], M. Mizokami[1], Y. Furuta[1], T. Nakamura[2], M. Hokazono[1], T. Maruyama[1], K. Toyota[3], K. Maeda[4], Y. Akamine[4], T. Yamawaki[4], T. Heima[1], K. Hori[3], H. Sato[1], [1]Renesas Electronics Corp., Itami-shi, [2]Hitachi, Ltd., [3]Renesas Electronics Corp.[4]Renesas Mobile Corp.

Abstract: We present a multiband LTE SAW-less CMOS transmitter. Source followers, which drive passive mixers, contribute to the small-area and low-power transmitter. An envelope-tracking technique improves the linearity of RF programmable gain amplifiers, and Marchand baluns are suitable for multiband operation. The transmitter, which includes digital-to-analog converters and a phase-locked loop, covers 700MHz to 2.6GHz with -42dBc ACLR RX-band noise of -161dBc/Hz is good enough for SAW-less operation.

RTU2B-4 11:10 AM

A 65nm GSM/GPRS/EDGE SoC with Integrated BT/FM

C. Chiu[1], H. Chang[1], T. Wu[1], S. Chen[1], C. Chin[1], W. Hong[1], S. Wong[2], L. Lai[1], C. Wang[1], S. Yang[1], T. Lin[1], J. Chen[1], H. Tsai[1], H. Yang[1], H. Chen[1], A. Marques[3], C. Wang[4], G. Chien[5], [1]MediaTek, Taiwan, [2]MediaTek, Singapore, [3]Consultant, Portugal, [4]MediaTek, Austin, [5]MediaTek, San Jose

Abstract: A highly integrated RF transceiver for GSM/GPRS/EDGE application is implemented in a 65nm SOC with BT and FM systems. Techniques are employed to minimize the coupling and interference effects among three wireless systems and results show the sensitivity and the output spectrum stay unchanged. The EDGE digital low-IF receiver achieves -110dBm sensitivity and -9dBm IIP3; while the EDGE polar transmitter achieves an ORFS of -66dB at 400kHz. This transceiver consumes 61/60mA in RX/TX EDGE modes.

Tuesday, 19 June 2012
10:10 AM
Room 511CF
Session RTU2C: Advanced Modeling and Characterization for RF and mm-Wave Design

Chair: Tzung-Yin Lee, Skyworks Solutions, Inc.
Co-Chair: Francis Rotella, Peregrine Semiconductor

RTU2C-1 10:10 AM
An Improved VBIC Model for InP DHBTs

Y. Shi[1], Z. Jin[2], Y. Su[2], Y. Cao[2], Y. Wang[1], [1]Tsinghua University, [2]Institute of Microelectronics, Chinese Academy of Sciences, China

Abstract: An emprical model is established for InP/InGaAs DHBTs based on the VBIC model. The heterojunction barrier and current blocking effect are considered in the current expressions. And new empirical models for transit time and collector capacitance are proposed by considering the voltage and current dependence. The excellent fitting results show that the improved model has better accuracy than the conventional VBIC model.

RTU2C-2 10:30 AM
Characterization and Modeling of Enhanced Voltage RF MESFETs on 45nm CMOS for RF Applications

S. J. Wilk[2], M. R. Ghajar[1], W. Lepkowski[2], B. Bakkaloglu[1], T. J. Thornton[1], [1]Arizona State University, [2]SJT Micropower Inc.

Abstract: Enhanced voltage silicon MESFETs have been fabricated on a 45nm SOI CMOS technology with no process changes. MESFETs scaled to Lg=184nm showed a peak fT of 35GHz, current drive of 112mA/mm and breakdown voltages exceeding 4.5V whereas the nominal CMOS voltage was less than 1V on the same process. The devices were characterized from DC to 40GHz and an industry standard TOM3 model has been developed. A board level Class AB power amplifier operating at 433MHz was designed, fabricated and measured.

RTU2C-3 10:50 AM
On-Wafer CMOS Transistors De-Embedding Method Using Two Transmission Lines of Different Lengths

H. J. Saavedra-Gómez[1], J. R. Loo-Yau[1], B. E. Figueroa-Resendiz[1], J. A. Reynoso-Hernández[2], [1]Centro de Investigación y de Estudios Avanzados del I. P. N. Unidada Guadalajara, Zapopan, [2]Centro de Investigación Científica y de Educación Superior de Enseanada, Mexico

Abstract: This paper introduces an alternative method to de-embed parasitic structures by using measurements on transmission lines of arbitrary characteristic impedance with different lengths. Experimental S-parameters data of on-wafer CMOS FETs de-embedded with the proposed L-L method and the Pad-Open-Short De-embedded (PSOD) method are compared. High correlation between the S-parameter data de-embedded with the PSOD and with the proposed two-tier L-L validates the method.

RTU2C-4 11:10 AM
An Ultra-Broadband Model for On-Chip Transformers Based on Pole-Residue Formulae

C. Qiu, H. Wang, J. Liu, Z. Yu, L. Sun, Hangzhou Dianzi University, China

Abstract: A novel compact model using pole-residue method for ultra-broadband on-chip transformer is presented. This model possesses several paralleled branches for high-order effects of transformers, and it can be easily extracted using the procedure of vector fitting (VF) written in MATLAB. Meanwhile, the key features of the existing equivalent circuit models have been analyzed. The proposed model reaches high accuracy and fits well with 100GHz measured S-parameters of an on-chip transformer.

RTU2C-5 11:30 AM
A Broadband, Millimeter Wave, Asymmetrical Marchand Balun in 180nm SiGe BiCMOS Technology

D. C. Howard, C. Cho, J. D. Cressler, Georgia Tech.

Abstract: A silicon-compatible, broadband, millimeter wave Marchand balun operating at a center frequency of 65GHz is presented. This balun is asymmetrical and broadside-coupled and exhibits excellent performance over a 30-90GHz frequency range. The gain imbalance is -1.6dB at 30GHz, and +0.6dB at 90GHz, with a phase imbalance of ± 5.2 degrees, respectively. To the author's knowledge, this is the widest bandwidth millimeter wave balun reported to date.

Tuesday, 19 June 2012
10:10 AM
Room 510AC
Session RTU2D: 60 GHz Transceiver Circuits
Chair: Arun Natarajan, IBM T. J. Watson Research Center
Co-Chair: Luciano Boglione, University of Massachusetts

RTU2D-1 10:10 AM
A Four-Path 60 GHz Phased-Array Receiver with Injection-Locked LO, Hybrid Beamforming and Analog Baseband Section in 90nm CMOS

K. Raczkowski[1], G. Mangraviti[2], V. Szortyka[2], A. Spagnolo[3], B. Parvais[1], R. Vandebriel[1], V. Vidojkovic[1], C. Soens[1], S. D'Amico[3], P. Wambacq[2], [1]Imec, Belgium, [2]Vrije Universiteit Brussel, Belgium, [3]University of Salento, Italy

Abstract: We present a 60GHz four-antenna phased-array direct conversion receiver in 90nm RF CMOS with an LO based on injection locking to fifth subharmonic, beamforming that is partially in the LO path and at analog baseband. Signal combination is performed at analog baseband, followed by a VGA and a baseband filter, which together allow for 6-th order filtering with 880MHz bandwidth. The system provides conversion gain of 42dB with a power consumption of 450mW and chip area of 3.15—1.9mm.

RTU2D-2 10:30 AM
A 60GHz Wideband Low Noise Eight-Element Phased Array RX Front-End for Beam Steering Communication Applications in 45nm CMOS

S. Drago, M. C. van Schie, A. J. de Graauw, J. F. Osorio, M. Spella, Y. Yu, C. S. Vaucher, R. M. Pijper, L. F. Tiemeijer, NXP Semiconductors

Abstract: This paper presents an 8-elements phased array RX front-end in 45nm CMOS technology. The receiver uses a 4-bit RF phase shifter and an active eight-to-one power combiner enabling beamforming. Each path shows more than 15.8dB of power gain with 0.5dB of RMS gain variation for all 16 phase settings over the 3dB gain bandwidth from 53.2-64.6GHz. Within the 3dB gain BW, the single-path NF ranges from 4.3dB to 6.3dB. The total power consumption is 613mW and the chip size is 4.8x1.5mm².

RTU2D-3 10:50 AM

A CMOS Bidirectional 32-element Phased-Array Transceiver at 60GHz with LTCC Antenna

E. Cohen[1], M. Ruberto[1], M. Cohen[3], O. Degani[1], S. Ravid[1], D. Ritter[2], [1]Intel, Israel, [2]Technion, Israel, [3]Ben-Gurion University, Israel

Abstract: An integrated CMOS 60GHz phased-array antenna module supporting symmetrical 32 TX/RX elements for wireless docking is described. Bidirectional architecture with shared blocks, mm-wave TR switch design with less than 1dB TX loss, and a full built in self test (BIST) circuits with 5deg and +/-1dB measurement accuracy of phase and power are presented. The RFIC size is 29mm², consuming 1.2W/0.85W at TX and RX with a 29dBm EIRP at-19dB EVM and 10dB NF.

RTU2D-4 11:10 AM

A Flip-Chip-Packaged and Fully Integrated 60GHz CMOS Micro-Radar Sensor for Heartbeat and Mechanical Vibration Detections

T. Kao, A. Chen, T. Shen, Y. Yan, J. Lin, University of Florida

Abstract: A 60GHz CMOS micro-radar for non-contact vital sign and vibration detections was designed and tested. Using low-cost PCB antennas, flip-chip packaging demonstrates high level of system integration. First-run success is achieved as the heartbeat and a small vibration displacement (20μm) can be detected at 0.3m away. With a roughly one-tenth patch antenna size compared to previous works, the CMOS integrated micro-radar can be readily embedded in many portable devices for different applications.

RTU2D-5 11:30 AM

A 5mW CMOS Wideband mm-Wave Front-End Featuring 17dB of Conversion Gain and 6.5dB Minimum NF

A. Ghilioni[1], E. Monaco[2], M. Repossi[2], A. Mazzanti[1], [1]Università di Pavia, Italy, [2]STMicroelectronics

Abstract: The low inductors' Q at mmW leads to poor current to voltage conversion in LNAs, thus several stages are required to achieve significant gain leading to large area and power consumption. Current-domain processing of the mmW signal is pursued in this work: a merged LNA & mixer delays the I-to-V conversion to IF, showing overall front-end gain and NF comparable to state-of-the-art CMOS stand-alone LNAs while crucially saving area and power. This solution is targeted for phased-array applications.

Session RTUIF: Interactive Forum
Chair: Waleed Khalil, Ohio State University
Co-Chair: Ayman Fayed, Iowa State University

RTUIF1
A Process-Scalable RF Transceiver for Short Range Communication in 90nm Si CMOS
A. Shirane, M. Otsuru, S. Lee, S. Yonezawa, S. Tanoi, H. Ito, N. Ishihara, K. Masu, Tokyo Institute of Technology

Abstract: This paper presents an RF transceiver that potentially has process scalability in terms of area and supply voltage. The transceiver has no inductor and employs inverter-based topology. The transceiver is fabricated in 90nm CMOS process and achieved area of 0.2mm² and 500Mb/s communication. The transmitter with the new linearity compensation technique provides EVM of less than -28dB at -5dBm output and 0.5 to 2.5GHz range. The receiver realizes sensitivity of -60dBm and dynamic range of 50dB.

RTUIF2
A 3.1-10.6GHz Ultra Wide-band Impulse Radio Transmitter with Notch Implementation for In-Band Interferers in 90nm CMOS
H. Hedayati, K. Entesari, Texas A&M University

Abstract: One of the serious challenges in Ultra Wide-band (UWB) systems, is the in-band interferers in the middle of the UWB band which affects the system performance severely. In this paper an analog in-band interference avoidance IR-UWB transmitter is presented. The fully integrated transmitter generates a novel UWB pulse with a tunable notch at the frequency of 802.11a interferer. The transmitter has bi-phase modulation and covers the UWB spectrum. The transmitter has been fabricated in IBM 90nm CMOS.

RTUIF3
A Bluetooth Radio in 45nm CMOS process for multi radio SoC
A. Lachhwani[1], G. Rajendran[1], A. Sivadas[1], R. Guntreddi[1], A. Joshi[1], B. Krishnakutty[1], N. Tal[2], G. Bitton[2], Y. Peled[2], S. Manian[1], M. Subramaniam[1], [1]Texas Instruments, India, [2]Texas Instruments, Israel

Abstract: RF section of an integrated Bluetooth (BT) Radio in 45nm CMOS is presented. The radio includes an on-chip matching network and a low loss T/R switch scheme in addition to the regular building block. Sensitivity of -94dBm and an output power of 16dBm were achieved at the basic rate. An area efficient RF architecture with RF/analog area near 0.85mm² facilitates integration of this Bluetooth core with several multi radio SoC.

RTUIF4
An Extremely Low Consumption, 53mW, 65nm CMOS Transmitter for 60GHz UWB Applications

M. Ercoli[1], D. Dragomirescu[1], R. Plana[1], D. Belot[3], [1]Laas - CNRS, Toulouse, France, [2]University of Toulouse, [3]STMicroelectronics

Abstract: An extremely low power transmitter based on fully differential architecture is presented. The design based on the maximum energy efficiency optimization of each block, yields state of the art RF performances with a record low power consumption. The transmitter shows a maximal gain of +5 dB at 60GHz with -3.5dBm of output power at the 1dB compression point. The saturated output power is 0.2dBm. The total power dissipation for the transmitter is reduced to 53mW with a bias voltage of 1.2V.

RTUIF5
5.8GHz Low-Flicker-Noise CMOS Direct-Conversion Receiver Using Deep-N-Well Vertical-NPN BJT

Y. Hsiao[1], C. Meng[1], J. Syu[1], C. Wang[1], S. Wong[2], G. Huang[3], [1]National Chiao Tung University, [2]Richwave Technology Corporation, [3]National Nano Device Laboratories

Abstract: This paper demonstrates a 5.8GHz low-power, low-flicker-noise direct-conversion receiver using deep-n-well vertical-NPN BJT based subharmonic Gilbert mixer. The deep-n-well vertical-NPN BJT is employed as LO switching core of the subharmonic mixer and the input transconductance of IF VGA. The flicker noise is improved and the noise figure is 9.5dB at 100kHz. As a result, the maximum gain reaches 50 dB in the operating frequency. The total power consumption is 10mW at 1.8V voltage supply.

RTUIF6
A PA-Noise Cancellation Technique for Next Generation Highly Integrated RF Front-Ends

M. Omer[1], R. Rimini[2], P. D. Heidmann[2], J. S. Kenney[1], [1]Georgia Institute of Technology, [2]Qualcomm Inc.

Abstract: The efficiency evolution in RF PAs has been slow. Inefficient PAs dissipate heat which increases the noise level. This PA noise is attenuated by using duplexers. High selectivity duplexers have high insertion loss. Modern radio designers want to relax duplexer specifications thus increasing the PA noise falling into the receive band. This work looks at a new technique to mitigate this noise by means of a mixed signal architecture. We demonstrate the cancellation of this noise and show SNR gains.

RTUIF7
A 2-11GHz Reconfigurable Multi-Mode LNA in 0.13µm CMOS

X. Yu, N. M. Neihart, Iowa State University

Abstract: This paper presents a reconfigurable multi-mode LNA capable of single band, concurrent dual-band, and ultra-wideband operation. The multi-mode operation is realized by incorporating a switched multi-tap transformer into the input matching network. The proposed LNA achieves single band matching at 2.8, 3.3, and 4.6GHz; concurrent dual-band matching at 2.05 and 5.65GHz; and ultra-wideband matching from 4.3-10.8GHz. The chip was fabricated in 0.13µm CMOS and dissipates 6.4mW from a 1.2V supply.

RTUIF8
Bias Optimized IP2 & IP3 Linearity and NF of a Decade-Bandwidth GaN MMIC Feedback Amplifier
K. W. Kobayashi, RF Micro Devices

Abstract: Bias-optimized performance of a 0.25-3.5GHz Cascode LNA is presented. At 10V-200mA, a NF of 0.88dB, P1dB 1-Watt and OIP3 of 38.7dBm is obtained at 2GHz. This is believed to be the lowest NF achieved from a multi-octave-BW flat-gain GaN LNA with 1-Watt P1dB. At 40V-500mA, the LNA achieves an IP3 of 50.6 dBm, a high IP2 of 70.5 dBm, and a P1B of 37.5 dBm (5.6Watts) at 2GHz with a corresponding NF of 2.2dB. This is an improvement in NF for state of the art GaN LNAs with IP3 50dBm.

RTUIF9
A -32dBm Sensitivity RF Power Harvester in 130nm CMOS
S. Oh, D. D. Wentzloff, University of Michigan

Abstract: This paper discusses a RF power harvester optimized for sensitivity and therefore wireless range, for applications requiring intermittent communication. The RF power harvester produces a 1V output at -32dBm sensitivity and 915MHz. This is achieved using a CMOS rectifier operating in subthreshold and an off-chip matching network. Equations predicting the rectifier performance are presented and verified through measurements of multiple rectifiers using different transistors in a 130nm CMOS process

RTUIF10
A 5bit 1GS/s 2.7mW 0.05mm² Asynchronous Digital Slope ADC in 90nm CMOS for IR UWB Radio
M. Ding[1], P. Harpe[2], H. Hegt[2], K. Philips[1], H. de Groot[1], A. van Roermund[2], [1]Holst Centre, [2]Eindhoven University of Technology, Netherlands

Abstract: A 5bit 1GS/s 4x time-interleaved asynchronous digital slope ADC is presented. New delay cells are introduced to double the speed over prior art, yielding the 250MS/s single-channel. A self-disabled comparator eliminates static leakage and consumes 0.25pJ/conversion. A single circuit corrects offset errors and delay-cell-mismatch, achieving 4.85bit ENOB and 1.5GHz ERBW. The ADC consumes 2.7mW at 1V, enabling 93fJ/step FoM. Compared to other state-of-the-art, it achieves similar power-efficiency.

RTUIF11
A 30-65GHz Reduced-Size with Low LO Power Modulator Using Sub-Harmonic Pumping in 90nm CMOS Technology
P. Tsai, C. Kuo, J. Kuo, S. Aloui, H. Wang, National Taiwan University

Abstract: In this paper, a reduced-size modulator with low LO power using a novel sub-harmonic mixer is presented. This mixer is pumped by a differential LO signal rather than a quadrature LO signal. Therefore, the number of baluns and couplers used in the design is less than the ones used in a conventional modulator. The LO power is also lowered. This modulator demonstrates a conversion gain of -8 ~ -13.5 dB when RF frequency varies from 30 to 65GHz with dBm LO power. The chip size is 890×560μm² including pads.

RTUIF12
An 84mW 0.36mm² Analog Baseband Circuits for 60GHz Wireless Transceiver in 40nm CMOS

M. Miyahara, H. Sakaguchi, N. Shimasaki, A. Matsuzawa, Tokyo Institute of Technology

Abstract: This paper presents a low-power analog baseband (ABB) circuits for 60GHz wireless transceiver in 40nm CMOS. The ABB circuits consist of 0-to-40dB VGAs and 5b 2304MS/s flash ADCs for the receiver, and 6b 3456MS/s DACs for the transmitter. The receiver demonstrates SNDR of 27.3dB at 2304MS/s with 16dB VGA gain. The DAC demonstrates SFDR of 40dB at 3456MS/s up to 200MHz. The ABB circuit consume 84mW from a 1.1 V supply. The entire ABB circuits occupy an area of 0.36mm².

RTUIF13
A Phase-Shifting Up-Converter for 30GHz Phased Array Applications

Y. Pei[1], Y. Chen[1], D. M. Leenaerts[1], R. Mahmoudi[2], [1]NXP Semiconductors, [2]Eindhoven University of Technology

Abstract: A phase-shifting up-converter is proposed using a phase-oversampling vector modulator in the LO domain to generate variable phases and amplitudes for each array element. A complex gain constellation with 81 points is formed with 10° phase resolution and 2-bit amplitude resolution. The up-converter has a measured maximal +10dB conversion gain and +3dBm OIP3 while consuming 393mW from a 3.3V supply voltage. Implemented in 0.25µm SiGe:C BiCMOS the up-converter has a compact core area of 0.135mm².

RTUIF14
A Low-power K-band CMOS UWB Radar Transceiver IC for Short Range Detection

S. Lee, S. Kong, S. Hong, KAIST, Korea

Abstract: This paper presents a low power UWB radar transceiver IC, which is used to make a radar system with precise range accuracy. The range accuracy is allowed by a variable delay circuit which can control the delay by 5 ps resolution. The detecting range of the transceiver is from 0.15m to 3.5m. The measurement results show that the maximum error is 3.75mm.

RTUIF15
A Broadband Millimeter-Wave Passive CMOS Down-Converter

A. Moroni, D. Manstretta, Universita degli Studi di Pavia

Abstract: A power-matched passive mixer suitable for a quadrature direct-conversion mm-wave receiver has been integrated in a 65nm CMOS technology. The design of a simple broadband matching network is presented. Measured down-conversion gain is between 10 and 13dB in the band from 49 to 67GHz, limited by the off-chip driving LO amplifier. In the same bandwidth S_{11} remains below -12dB. Power dissipation is 14mW from a 1.2V supply.

RTUIF16
A 77GHz Automotive Radar Receiver in a Wafer Level Package
C. Wagner[1], J. Boeck[2], M. Wojnowski[2], H. Jaeger[1], J. Platz[1], M. Treml[1], F. Dober[1], R. Lachner[2], J. Minichshofer[1], L. Maurer[1], [1]DICE, [2]Infineon Technologies

Abstract: In this paper, a 77GHz radar receiver is presented, which comes in a wafer level package and thus eliminates the need for wire bonding resulting in significant cost reduction. The high integration level available in the productive Silicon-Germanium (SiGe) technology used in this paper allows for implementation of in-system monitoring of the receiver conversion parameters. This facilitates the realization of ISO26262 compliant radar sensors for safety applications.

RTUIF17
A Novel mmWave CMOS VCO with an AC-Coupled LC Tank
V. P. Trivedi, K. To, Freescale Semiconductor, Inc.

Abstract: We propose the concept of AC-coupled LC tank for minimizing VCO pushing, and to enable multi-terminal tuning of the varactors, in the widely used cross-coupled CMOS VCOs. The proposed concept is demonstrated with a mmWave VCO in 65nm CMOS. Measured data demonstrates 3x lower pushing while achieving 16% wider tuning range compared to a reference cross-coupled CMOS VCO. Phase noise and output power are comparable to the reference VCO. Finally, the proposed VCO is suitable for ultra-low VDD design.

RTUIF18
A 4.1-6.5GHz Transformer-Coupled CMOS Quadrature Digitally-Controlled Oscillator with Quantization Noise Suppression
S. Zheng, H. C. Luong, Hong Kong University of Science and Technology

Abstract: A wideband transformer-coupled quadrature digitally-controlled oscillator (QDCO) operates in Class-C mode with embedded phase shifters and ΣΔ shaped out-band quantization noise filter. The QDCO fabricated in 65nm CMOS measures tuning range of 45% from 4.1GHz to 6.5GHz with frequency resolution of 5Hz while achieving 1.2° phase error and a phase noise of -145.3dBc/Hz at 10MHz. It consumes 15mA from a 1.2V supply corresponding to a FoM of 186.6dBc/Hz and a FoMT of 199.8dBc/Hz.

RTUIF19
A Reconfigurable 4.7-6.6GHz and 8.5-10.7GHz Concurrent and Dual-Band Oscillator in 65nm CMOS
A. Li, H. C. Luong, Hong Kong University of Science and Technology

Abstract: A triple-mode 65nm CMOS VCO is reconfigurable to operate in two bands, 4.7-6.6GHz and 8.5-10.7GHz, either concurrently or one at a time. Operated concurrently, the VCO consumes 1.6mA at 1.2V and measures tuning ranges of 35%/23%, phase noise of -130/-128dBc/Hz at 10MHz offset, and FOMs of -184/187dB. The lower/higher band single-tone modes consume 0.75mA/1.43mA at 1.2V with tuning ranges of 34%/23% and phase noise of -131/-128dBc/Hz at 10MHz offset, and FOMs of -186dB/-185dB, respectively.

RTUIF20
A CMOS Flash TDC with 0.84-1.3ps Resolution Using Standard Cells

T. J. Yamaguchi[1], S. Komatsu[2], M. Abbas[2], K. Asada[2], M. Khanh[2], J. Tandon[2], [1]Advantest Laboratories, Ltd., [2]University of Tokyo

Abstract: This paper proposes a new flash time-to-digital converter (TDC) design, which incorporates deterministic, variable delay into the decision elements. These are implemented with cross-coupled NAND standard cells of variable transistor widths. Both experiment and simulation are used to validate this new design, which provides variable time-difference ranges by controlling the input slew rate. It is also possible to use the proposed flash TDC as a soft macro.

RTUIF21
A 0.6-7 Gbps, 1/7 Rate, Burst Mode Clock and Data Recovery Circuit and Demultiplexer

Y. Chen, W. Chen, National Chiao-Tung University

Abstract: A 1/7 rate, burst mode clock and data recovery circuit incorporating with demultiplexer is proposed. It covers 622Mbps to 7Gbps operation by selective-gating digitally controlled oscillator for phase synchronization and digital frequency-locked loop for frequency tracking. The latency for data recovery and 1:7 demultiplexing is less than 10 bit periods. Incorporating both CDR and demultiplexer, this chip consumes 1.5mW, 6mW, and 17mW respectively at 622Mbps, 2488Mbps, and 7Gbps.

RTUIF22
A Performance Study of Layout and V_t Options for Low Noise Amplifier Design in 65nm CMOS

Q. Pan[1], T. Yeh[2], C. Jou[2], F. Hsueh[2], H. Luong[1], P. Yue[1], [1]Hong Kong University of Science and Technology, [2]Taiwan Semiconductor Manufacturing Company Ltd.

Abstract: This paper presents the performance trade-offs and design guidelines for different cell-based layout styles and Vt options using a set of 5GHz LNAs. The impact of diffusion area at the cascode node, gate contact styles and different-Vt are investigated. Measurement results show that low-Vt devices with separated diffusion area, double-sided gate contact provide better gain and noise performance. On the other hand, normal-Vt devices with merged diffusion area achieve higher linearity.

RTUIF23
Frequency Response Enhancement of Spiral Inductor's Q-Factor by Adopting Defected Ground Structure in Standard CMOS Process

Y. Ye[1,2], J. Gu[1], R. Qian[1], X. Sun[1], [1]Shanghai Institute of Microsystem and Information Technology, [2]Graduate University of Chinese Academy of Sciences

Abstract: A planar spiral inductor with defected ground structure is proposed and fabricated in 65nm CMOS technology. Equations and explanations of the self-resonate frequency and the frequency with maximum quality factor (f_{max}) are obtained based on single π model. Measured results match well with simulations and models up to 75GHz, improving f_{max} from 16GHz to 34GHz and 27GHz to 55GHz compared with traditional inductors, while achieving good flatness of quality factor within broadband mm-wave range.

RTUIF24
Characterization and Modeling of the Junction Diode for Accurate RF Model in the 36nm MOSFET

Y. Wang, W. Tsao, Z. Zeng, MediaTek Inc.

Abstract: Different CV curves of junction diode were observed in the MOSFET with 36nm MOS for the first time. Traditional characterization results of source/body and drain /body junction diode from longer channel MOSFET and large diode are not the same as those in the shorter channel and small diode. In this paper we discussed the discrepancies of traditional diode characterization and proposed a new way for short change MOS with 36nm gate length by S-parameters.

RFIC2012 Panel Sessions

Monday, 18 June 2012
12:00PM – 01:20PM Rooms 516 ABC

THz Integrated Circuits: Do future markets support highly integrated silicon-based IC development?

Panel Organizers: **Mona Hella** (Rensselaer Polytechnic Institute)
Sanjay Raman (Virginia Tech/DARPA)
Sayfe Kiaei (Arizona State University)

Moderator: **Sanjay Raman** (Virginia Tech)
Mona Hella (Rensselaer Polytechnic Institute)

Panelists: **Bobby Brar** (President, Teledyne Scientific)
Tom Crowe (President, Virginia Diode Inc.)
Baher Haroun (Fellow, Texas Instruments)
Gabriel Rebeiz (Professor, UCSD)
Albert Redo-Sanchez (Dir. of Business Development, Zomega THz Corp.)
Peter Siegel (Senior Research Scientist, JPL)

Abstract: The THz spectral range has many scientific uses for investigating the fundamental excitations in matter with emerging opportunities in the medical, security, and communications fields that could launch terahertz technology into the public domain. Semiconductor technology is a key to many of these developments, with recent reported InP HBTs of $f_T \sim 0.8$THz, InP HEMTs with $f_{max} > 1$THz and SiGe HBTs with f_{max} of 500GHz. At the circuit and sub-system levels, we have seen MMICS for applications up to 0.82THz. While significant issues related with the output power level and tunability of integrated sub-THz sources as well as detector/receiver noise remain to be resolved, low-cost THz integrated systems appear to be realizable. The remaining question is "what are the killer applications that will drive the IC market within the THz range (above 300GHz)?"

Our panel of distinguished experts from industry and academia will cover the various aspects of THz systems, including devices, system integration, applications and standardization, representing the views of different market sectors (commercial, defense and startups), and will deliberate this interesting topic with the audience participation.

RFIC2012 Panel Sessions

Tuesday, 19 June 2012
12:00PM – 01:20PM Rooms 516 ABC

RF scaling: Can it keep up with digital CMOS? Should it?

Panel Organizers and Moderators:
Jeffrey Walling (Rutgers University)
Oren Eliezer (Xtendwave)

Panelists:
David Allstot (Professor, Univ. of Washington, USA)
Dominique Brunel (Fellow, ST-Ericsson, France)
Jonathan Jensen (Principal Engineer RF/Analog Circuits, Intel, USA)
Li Lin (Director RF IC Design, Marvell Semiconductor Inc.)
George Chien (Director RF Circuit Design, MediaTek, Taiwan)
Raf Roovers (Dept. Head RF Int. Sol., NXP Semiconductors)
Robert Staszewski (Associate Professor, TU Delft, Netherlands)
Masoud Zagari (Senior Director of Engineering, Qualcomm, USA)

Abstract: The benefits of continued scaling of CMOS transistors are well appreciated within the digital design community, allowing ever increasing integration. The resultant increase in speed and performance has enabled RF-CMOS to evolve to the point where single-chip RF-SoC integration is possible. However, the drawbacks to the continued scaling for RF functions are plentiful. Device scaling comes at the cost of decreases in gain and in SNR, and in increased power consumption due to leakage. In recent years, RF CMOS designers have been able to compensate for these drawbacks with adept changes in architectures and design topologies as CMOS has roared into the nanotechnology realm. Most recently, various cognitive radio (CR) applications have emerged for which integration is likely the key to their widespread adoption. These applications typically require wide bandwidth, high dynamic-range, and high output power, which cannot be easily accomplished simultaneously. Integration in scaled CMOS also includes challenges associated with the linearity and efficiency of the power amplifier. The panelists will present their ideas and opinions and engage in debate with the audience's participation.

WORKSHOPS AND SHORT COURSES

Workshops and Short courses are offered on Sunday, Monday and Friday of Microwave Week. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS 17 JUNE 2012

WSA: Sunday, 8:00 AM – 5:00 PM

Unconventional Power Amplifier Architecture with High Efficiency

Sponsors: **MTT-5, MTT-17**
Organizers: **Bumman Kim**, *Pohang University of Science and Technology*
Frederick H. Raab, *Green Mountain Radio Research Company*
Allen Katz, *The College of New Jersey/Linearizer Technology, Inc.*

Abstract: As the wireless information transmission has become a part of everyday life, producing highly efficiency power amplifiers (PAs) has become of vital importance. The PA is the key system component, and consequently is experiencing very rapid technological advancement. This workshop will cover recent PA progress with a unique focus on advanced PA architectures. We called the architectures to be presented 'unconventional' because for the most part they are not yet being applied in production power amplifiers, and are emerging, and rapidly changing technologies. It is true that these technologies may have been presented in the past individually, but never all together where their advantages and disadvantages can be compared and discussed as a group. The first talk will be an overview of techniques for achieving both highly efficient and linear power amplification. The basic concepts will be reviewed, and recent achievements as well as practical limitations will be discussed. The optimized unit PA, an essential element for enhanced high efficiency performance, will be introduced. The workshop will then cover important recent advances in PA architectures, including Doherty, Envelope tracking/restoration, Outphasing, Class-S voltage-mode, and Digitally modulated amplifiers. Finally, ultra-broad band linear and efficient PAs will be introduced. The leading speakers from all over the globe have been recruited. After the speaker presentations, there will be one hour panel session. During this session the trades between the various technologies presented and related key technology questions will be discussed by the presenters and the audience. Audience participation will be promoted and encouraged. Attendees will be invited to submit a maximum of two slides for presentation as part of this session.

Speakers:

1. "High-Efficiency Power Amplifiers and Transmitters", **F. H. Raab,** *Green Mountain Radio Research, Colchester, United States*
2. "Characteristics of Various Switching Amplifiers and The Optimized Structure", **B. Kim[1], J. Moon[2], S. Jee[1], J. Kim[1]**, *[1]Postech, Pohang, Republic of Korea, [2]Samsung Electronics Company, Suwon, Republic of Korea*
3. "High-efficiency Doherty Amplifier Architectures", **A. Grebennikov**, *Alcatel-Lucent Ireland, Blanchardstown, Ireland*
4. "Envelope Tracking Power Amplifiers at X-band to W-band", **D. Kimball,** *MaXentric Technologies*, *La Jolla, United States*

5. "Enhanced Outphasing Power Amplifiers", **M. P. van der Heijden[1], M. Acar[1], J. Qureshi[1], L. C. de Vreede[2]**, *[1]NXP Semiconductors, Eindhoven, Netherlands, [2]Delft University of Technology, Delft, Netherlands*
6. "The class-S Voltage-mode Concept: State-Of-The-Art Results and Efficiency Analysis", **W. Heinrich**, *Ferdinand-Braun-Institut (FBH), Berlin, Germany*
7. "Digitally-Controlled Power Amplifiers for Handset Applications", **P. Asbeck**, *UCSD, La Jolla, United States*
8. "Achieving Linear Power Amplifiers with Both Wide Bandwidth (Multiple Octave) and High Efficiency", **A. Katz**, *The College of New Jersey, Ewing, United States*

WSB: Sunday, 8:00 AM – 5:00 PM

Modern Techniques for Tunable and Reconfigurable RF/Microwave Filter Development

Sponsors: **MTT-8**
Organizers: **Roberto Gómez-García**, *University of Alcalá*
Xun Gong, *University of Central Florida*

Abstract: This workshop focuses on the area of tunable and reconfigurable RF/ microwave filters by reporting recent research findings in this exciting field. This includes a large variety of novel planar/hybrid tunable circuit realizations for spectrum management and dynamic broad-band filtering, as well as new high-Q micro-electro-mechanical-system-(MEMS)-based reconfigurable filters for wide tuning ranges and their realization through cutting-edge technologies such as substrate-integrated waveguides (SIWs) and evanescent-mode cavity resonators. Latest results on ferroelectric barium-strontium-titanate (BST) materials for high-speed-switching tunable filter design and GaAs and SiGe processes (CMOS, BiCMOS) for MMIC reconfigurable active filter development in single- and differential mode arrangements are also reported.

Speakers:

1. "New Advances in Tunable Hybrid/Planar Filter Technology for Spectrum Management", **A. C. Guyette, D. R. Jachowski**, *Naval Research Laboratory, Washington, United States*
2. "Electronically Reconfigurable Planar Microwave Filters", **J. Hong**, *Heriot-Watt University, Edinburgh, United Kingdom*
3. "Substrate-Integrated-Waveguide RF MEMS Tunable Filters", **K. Entesari[1], V. Sekar[2]**, *[1]Texas A&M University, College Station, United States, [2]Peregrine Semiconductors, San Diego, United States*
4. "Frequency-Agile Reconfigurable Filter Structures Based on Tunable Cavity Resonators", **W. J. Chappell[1], J. Lee[2]**, *[1]DARPA, Arlington, United States, [2]Korea University, Seoul, Republic of Korea*
5. "Widely-Tunable High-Q RF Front-End Filters", **D. Peroulis**, *Purdue University, West Lafayette, United States*
6. "Tunable Bandpass and Bandstop Filters Based on Dual-Band Combline Structures", **I. Hunter[1], A. Abunjaileh[2]**, *[1]University of Leeds, Leeds, United Kingdom, [2]EADS Astrium, Stevenage, United Kingdom*

7. "Tunable Filters Based on BST Materials", **B. Lacroix, J. Papapolymerou**, *Georgia Institute of Technology, Atlanta, United States*
8. "Reconfigurable RF and Microwave Filtering Devices in MMIC Technologies", **B. Barelaud, B. Jarry, J. Lintignat**, *XLIM, Limoges, France*
9. "Tunable Bandpass and Bandstop Filter Topologies Using MEMS and Schottky Diodes", **G. M. Rebeiz**, *The University of California, San Diego, La Jolla, United States*

WSC: Sunday, 8:00 AM – 5:00 PM

3-D Integrated Circuits

Sponsors: **MTT-12, RFIC**
Organizers: **Robert W. Jackson**, *University of Massachusetts*
Wolfgang Heinrich, *FBH-Berlin*
Li Wu Yang, *TransRF Corp.*

Abstract: Three dimensional integrated circuits have been under study for many years now. There are two areas that are of particular interest lately. The combination of high performance indium phosphide with the high integration level of silicon is a type of heterogenous integration which is of particular interest to the military. The second area is the stacking of substrates to combine RF, photonics, signal processing, and control. Topics in this area include wafer bonding techniques, TSV technology, TSV RF modeling, and 3D assembly techniques. Very complex, compact, high performance subsystems result. The current state of the art will be presented.

Speakers:

1. "3D Heterogeneous Integration and the DARPA Diverse Accessible Heterogeneous Integration (DAHI) Program", **S. Raman[1], C. L. Dohrman[2], T. Chang[2], J. S. Rodgers[1]**, *[1]DARPA, Arlington, United States, [2]Booz Allen Hamilton, Arlington, United States*
2. "Heterogeneous Integration of III-V Devices and Si CMOS on a Silicon Substrate", **T. E. Kazior**, *Raytheon Integrated Defense Systems, Andover, United States*
3. "Heterogeneous Integration of InP HBTs and RF-CMOS Technologies for RFICs", **J. C. Li, Y. Royter, T. Hussain, P. R. Patterson, J. R. Duvall, M. C. Montes, I. Valles, M. F. Boag-O'Brien, D. M. Le, D. M. Zehnder, S. J. Kim, E. F. Wang, D., A. Hitko, M. Sokolich, D. H. Chow, K. R. Elliott, P. D. Brewer**, *HRL Laboratories, LLC, Malibu, United States*
4. "Wafer-Scale Assembly & Heterogeneous Integration Technologies for MMICs", **P. Chang-Chien**, *Northrop Grumman Aerospace Systems, Redondo Beach, United States*
5. "Optimal Technology Integration through 3D Wafer-Scale Bonding", **J. B. Muldavin**, *MIT Lincoln Laboratory, Lexington, United States*
6. "High Frequency Modeling and Measurement of TSV in 3D IC", **J. Kim**, *KAIST, Daejeon, Republic of Korea*
7. "TSVs for 3D RF system integration", **W. De Raedt, X. Sun, E. Beyne**, *IMEC, Leuven, Belgium*
8. "3D Integration for Microwave Application", **M. Wolf,** *Fraunhofer IZM, Berlin, Germany*

WSD: Sunday, 8:00 AM – 5:00 PM

RF & mmW PAs: Linearization and Power Challenges

Sponsors: **RFIC**
Organizers: **Eric Kerhervé,** *IMS*
Didier Belot, *ST Microelectronics*

Abstract: Power amplifiers in RF and mmW have two main challenges to target in the same time, the linearity and the power. The modulations are more and more complex — from 16 to 64 QAM in mmW and from 64 to 128 QAM in RF — with multicarriers OFDM on wider and wider bands. In the same time, mainly in RF the power remains a challenge in Silicon technologies. We will have an overview of state of the art technologies and design techniques to address such challenges for RF Cellular Mobile, Base stations, WLAN and mmW WLAN applications.

Speakers:

1. "Embrace Circuit Nonlinearity to get Transmitter 'Linearity' and Energy Efficiency", **E. McCune**, *RF Communications Consulting, Santa Clara, United States*
2. "RF Power Amplifier Design", **L. E. Larson[1], P. Asbeck[2], D. Kimball[2]**, *[1]Brown University, Providence, United States, [2]UCSD, La Jolla, United States*
3. "PA Design for Base Stations", **D. Leenaerts**, *NXP Semiconductors, Eindhoven, Netherlands*
4. "Silicon Based RF Front End Modules", **F. Balteanu**, *Skyworks Solutions, Ottawa, Canada*
5. "RF Silicon PA, How to Aim the Linearity/Power/Efficiency…Tradeoff", **A. Scuderi**, *STMicroelectronics, Catania, Italy*
6. "Cartesian Feedback with Digital Enhancement applied to Fully Integrated CMOS RF Transmitter", **N. Deltimple[1], N. Delaunay[1], W. Sanaa[1], B. Le Gal[1], C. Rebai[2], D. Dallet[1], D. Belot[3], E. Kerhervé[1]**, *[1]IMS Laboratory, Talence, France, [2]CIRTA'COM Research Laboratory, Carthage, Tunisia, [3]STMicroelectronics, Grenoble, France*
7. "CMOS Millimetre-wave Doherty Power Amplifiers", **F. M. Ghannouchi, M. Akbarpour, M. Helaoui**, *University of Calgary, Calgary, Canada*
8. "Holistic Approaches for Power Generation, Linearization, and Radiation in CMOS", **A. Hajimiri**, *California Institute of Technology, Pasadena, United States*

WSE: Sunday, 8:00 AM – 5:00 PM

Towards Watt-Level mm-Wave Efficient Silicon Power Amplifiers

Sponsors: **RFIC**
Organizers: **Hossein Hashemi**, *University of Southern California*
Sanjay Raman, *Virginia Tech*

Abstract: Over the past several years, there has been a significant drive in both academia and industry to demonstrate silicon integrated solutions at mm-waves for emerging applications such as short-range high data-rate wireless communications, automotive radars, and biomedical imaging. Monolithic mm-wave transceivers and phased arrays in SiGe HBT and CMOS have been demonstrated by several groups and entered the market as commercial products. In fact, advancements in silicon mm-wave integrated systems have led to consideration for their usage in military and space systems where historically compound semiconductor solutions have dominated. Despite recent advancements, Watt-level power amplifiers at mm-waves are still challenging research topics. Moreover, the reported low-power (100mW) power amplifiers are typically inefficient (PAE 20%). At this point, virtually all Watt-level mm-wave power amplifiers are implemented in compound semiconductor technologies, but, without the level of integration and complexity offered by advanced silicon technologies. However, there are several research groups that are working towards realizing efficient high-power mm-wave power amplifiers and transmitters using standard silicon technologies. In addition, DARPA has recently invested in the development of efficient Watt-level mm-wave transmitters under the Efficient Linearized All-Silicon Transmitter ICs (ELASTx) program. The aforementioned trend at mm-wave resembles that at Radio Frequencies where monolithic CMOS transceivers (e.g., for cellular phones) were followed by Watt-level efficient CMOS/Si power amplifiers several years later. This proposed workshop consists of representatives from 10 leading research groups in academia and industry that have been working on mm-wave efficient silicon power amplifiers with higher output power levels. Many of the talks will include new research results (either unpublished at the time of RFIC/IMS or to be published in 2012 for the first time). Novel design methodologies will be discussed that may be able to overcome the significant challenges in achieving high efficiency and robust power levels in silicon at mm-wave frequencies.

Speakers:

1. "Design of CMOS mm-Wave Power Amplifier", **P. Reynaert**, *KU Leuven, Leuven, Belgium*
2. "Efficient, Watt-class, mmWave CMOS PAs: Stack Devices Aggressively, Switch Them Hard and Power-Combine", **H. Krishnaswamy**, *Columbia University, New York, United States*
3. "Mixing Things Up: Analog and Digital Techniques for High Frequency Silicon Power Amplifiers", **A. M. Niknejad, J. Chen, L. Ye**, *UC Berkeley, Berkeley, United States*
4. "The Design of Area- and Power-Efficient mm-Wave PAs in Silicon CMOS and BiCMOS Using On-Chip Magnetics", **J. R. Long, Y. Zhao, M. Spirito, D. Cheung**, *TU Delft, Delft, Netherlands*
5. "Design Paradigm of 30dBm Power Amplifier in SiGe", **R. Mahmoudi[1], J. Essing[1], D. Leenaerts[2]**, *[1]Eindhoven University of Technology, Eindhoven, Netherlands, [2]NXP semiconductors, Eindhoven, Netherlands*

6. "High Efficiency Si-Based Mm-Wave Amplifiers Using Free-Space Power Combining", **P. Asbeck[1], G. Rebeiz[2], J. Buckwalter[3], L. Larson[4], S. Voinigescu[5]**, *[1]UCSD, La Jolla, United States, [2]UCSD, La Jolla, United States, [3]UCSD, La Jolla, United States, [4]Brown University, Providence, United States, [5]University of Toronto, Toronto, Canada*
7. "Digital and RF Correction of Linear and Nonlinear Distortion for Efficient Millimeter-Wave SoC CMOS Transmitter Designs", **T. R. LaRocca**, *Northrop Grumman Aerospace Systems, Redondo Beach, United States*
8. "24-GHz to 150-GHz High-Power CMOS PA Combining Architectures Comparison and Stability Analysis", **T. Huang, K. Lin, H. Wang**, *National Taiwan University, Taipei, Taiwan*
9. "High Power, Efficient and Reliable mm-wave CMOS Power Amplifiers, Squaring the Circle?", **B. Martineau**, *STMicroelectronics, Crolles, France*
10. "Large Power, Phase and Amplitude Modulated, Switching PAs for mm-Wave High-Efficiency Digital Transmitters", **A. Balteanu[1], I. Sarkas[1], S. P. Voinigescu[1], P. Asbeck[2], G. Rebeiz[2], J. Buckwalter[2], L. Larson[3]**, *[1]University of Toronto, Toronto, Canada, [2]University of California, UCSD, La Jolla, United States, [3]Brown University, Providence, United States*

WSF: Sunday, 8:00 AM – 5:00 PM
Wide-band (Multi-Octave), Fast Settling, RF Frequency Synthesis

Sponsors: **RFIC**
Organizers: **Behnam Analui**, *USC*
Hossein Hashemi, *USC*

Abstract: Frequency Synthesizers are at the heart of radio frequency (RF) wireless communication systems. With the emergence of programmable radio systems, e.g. multi-standard, cognitive radio (CR) and software-defined radio (SDR), one new key block that needs to be developed is the RF frequency synthesizer. For example, a modern frequency synthesizer for an integrated SDR must meet a new and challenging set of requirements, e.g., wide frequency coverage, while maintaining or improving on traditional specifications such as low phase noise. This full-day workshop focuses on the state of the art developments on the topic of frequency synthesis for wide-band RF applications. Key aspects which are emphasized and covered include: wide (multi-octave) frequency coverage, fast-settling time for frequency switching and hopping, and low-noise and low-spurious tones. Various architectural choices and circuit topologies for RF frequency synthesizers and their application to wide-band RF systems, e.g. SDR and CR, are discussed. Examples of wide-band RF synthesizers used in SDR radios based on advanced CMOS processes (130nm, 90nm, 40nm, etc.) are also presented. Architectures discussed by multiple presenters include: Direct digital frequency synthesis, fractional-N PLL with multi-phase clock generation, open-loop dynamic phase switching, multi-order harmonic generation, and all digital PLL. In addition, various topologies including cyclic coupled ring oscillators and sub-harmonic injection locking synthesizers for wide-band and/or fast settling time operation are presented.

Speakers:

1. "Multi-Order Harmonic Generation for Wideband Frequency Synthesis", **E. Sánchez-Sinencio, M. M. Abdul-Latif**, *Texas A&M University, College Station, United States*
2. "Injection Locking for Wideband, Fast Settling, RF Synthesizers", **R. Harjani**, *University of Minnesota, Minneapolis, United States*
3. "Open Loop Digital Modulation Techniques for Wide Bandwidth Frequency Synthesis", **S. Pamarti**, *University of California, Los Angeles, Los Angeles, United States*
4. "100MHz-6GHz Analog and Digital Frequency Synthesis for SDRs in Nanoscale CMOS", **J. Borremans**, *IMEC, Leuven, Belgium*
5. "Power Efficient Flexible Clock Generation with Low Phase Error", **E. Klumperink**, *University of Twente, Enschede, Netherlands*
6. "Achieving Fast Locking and Wide Bandwidth Operation through All-digital PLL Techniques", **R. B. Staszewski**, *Technische Universiteit Delft, Delft, Netherlands*
7. "Digital to Time Converter DDS: Spur Analysis and Mitigation", **S. A. Talwalkar**, *Motorola Solutions, Inc, Plantation, United States*
8. "Direct Digital Synthesis Technology in High Performance RF Applications", **J. Baird, J. Cavey**, *Analog Devices, Norwood, United States*

WSG: Sunday, 8:00 AM – 5:00 PM

RF and Modem Techniques for Multi-standard Radios Coexistence

Sponsors: **RFIC**
Organizers: **Walid Y. Ali-Ahmad**, *MediaTek Inc.*
Jacques C. Rudell, *University of Washington*

Abstract: Year by year, there is a drive to have more wireless functionalities available at the tip of our fingers, and hence, more push is being done towards multi-radios integration with the use of CMOS technology. These radios cover a diverse group of connectivity and cellular standards. This workshop will address the challenges for RF co-existence on SoC level or in multi-radio platform; it will focus on the use of digital baseband assisted radio architectures, RF front-end and transceiver techniques, and coordination at the UE modems level to result in the optimum multi-standard coexistence and multi-mode concurrency in a multi-radio environment.

Speakers:

1. "High Integration CMOS Frontends in an Increasingly Coexistent Multi-Standard, Cognitive and SDR Radio Environment", **J. C. Rudell**, *University of Washington, Seattle, United States*
2. "A Cost Effective Approach for Accommodating Multi-Radio Coexistence in Consumer Market Devices", **O. E. Eliezer[1], N. Tal[2]**, *[1]Xtendwave, Dallas, United States, [2]Texas Instruments, Ra'anana, Israel*
3. "Coexistence Issues and Mitigation in Multi-mode Band Cellular Radios", **K. Sahota**, *Qualcomm Inc., San Diego, United States*

4. "Uncovering the Mystery of Multi-radio SoC Integration", **G. Chien[1], C. Wu[2], Y. Chung[2], T. Wu[2]**, *[1]MediaTek, Inc., San Jose, United States, [2]MediaTek, Inc., Hsinchu Science Park, Taiwan*
5. "Multi-Radio Coexistence, Enabling RF Performance by Digital Assistance", **A. Hanke**, *Intel, Neubiberg, Germany*
6. "Design Considerations of Multi-functional Radios in SOC Environment", **L. Lin**, *Marvell Semiconductor Inc., Santa Clara, United States*
7. "Techniques to Improve Coexistence in Multi-Standard SoCs", **M. Kohlmann**, *Qualcomm Inc., Santa Clara, United States*
8. "Integration of Radios into High Performance PC based SoCs", **H. Lakdawala**, *Intel Corporation, Hillsboro, United States*

WSH: Sunday, 8:00 AM – 12:00 PM

RF and Analog ICs for Bio-medical Applications

Sponsors: **RFIC**
Organizers: **Fred S. Lee**, *Fairchild Semiconductor*
Mona Hella, *Rensselaer Polytechnic Institute*

Abstract: Applied RFIC and mixed-signal systems have been great enablers in advancing the bio-medical field, ranging from observing bio-molecular interactions to treating cancer. This workshop is designed to expose RF/mixed-signal designers to the challenges and opportunities of designing bio-medical systems in an interdisciplinary environment where ideas can be exchanged. No prior experience in biological systems will be necessary, as all material covering the bio-medical portion will be tutorial based. Through the half-day workshop, we will be covering: Systems and applications of bio-medical devices, Implantable medical devices, In vivo force sensors, THz imaging, Bio-molecular analysis, Microwaves in cancer detection, and Low power radios for wearable wireless sensors.

Speakers:

1. "RF Communication for Implantable Cardiac Rhythm Management Devices", **E. H. Klaassen**, *St. Jude Medical, Sunnyvale, United States*
2. "Requirements for Implantable RF Medical Diagnostic Systems in Orthopaedic Surgery", **E. H. Ledet**, *Rensselaer Polytechnic Institute, Troy, United States*
3. "Chip Design for On-body Wireless Sensing", **B. Otis**, *University of Washington, Seattle, United States*
4. "Microwave Technologies for Breast Health and Disease Management", **M. J. Burfeindt, N. Behdad, B. D. Van Veen, S. C. Hagness**, *University of Wisconsin-Madison, Madison, United States*
5. "Biomedical THz Studies: From in vivo Skin Imaging to Molecular Spectroscopy", **E. Pickwell-MacPherson**, *Hong Kong University of Science and Technology, Hong Kong, China*
6. "Solid-state and Biological Systems Interface", **D. Ham**, *Harvard University, Cambridge, United States*

WSI: Sunday, 8:00 AM – 12:00 PM
RF at the Nanoscale

Sponsors: **RFIC**
Organizers: **Gernot Hueber**, *NXP Semiconductors*
R. Bogdan Staszewski, *Delft University of Technology*
Stefan Heinen, *RWTH Aachen*

Abstract: Advances in CMOS fabrication technology enabled the use of CMOS technology in today RF transceivers for wireless communications. Multi-band and multi-mode radios covering the diversity of communication standards from 2G GSM, 3G UMTS, to 4G LTE and LTE-advanced impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications. As well, nanoscale CMOS on the one hand features the possibility for implementing a significant computational power and complex functionality directly on a single IC, on the other hand it shows poor performance in RF circuits compared to other technologies. The focus of this workshop will be on the challenges the cellular standards pose on future multi-radio integration in nanoscale CMOS, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in a multi-radio SoC or SiP. Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-end.

Speakers:

1. "Multimode Transmitters and Power Amplifiers in Nanometer CMOS." **P. Reynaert**, *KU Leuven, Leuven, Belgium*
2. "Digital Intensive Transmitters in Nanoscale CMOS", **M. Ingels**, *IMEC, Leuven, Belgium*
3. "System Challenges for Future Integration of Multi-mode Multi-band Radios Based on Evolving 3GPP Cellular Standards, Release 9 and Beyond", **W. Y. Ali-Ahmad**, *MediaTek, Singapore, Singapore*
4. "Receiver Architectures for Software-Defined and Cognitive Radio Applications, **H. Darabi**, *Broadcom, Irvine, United States*
5. "Recent Advancements and Future Directions in Digital RF and Digitally-Assisted RF", **R. B. Staszewski**, *Technische Universiteit Delft, Delft, Netherlands*
6. "CMOS Switched-Capacitor Circuits for RF Applications", **D. J. Allstot**, *Univ. of Washington, Seattle, United States*

WSJ: Sunday, 8:00 AM – 12:00 PM

RF Spectrum Sensing and Signal Feature Detection Circuits

Sponsors: **RFIC**
Organizers: **Eric Klumperink**, *University of Twente*
Ranjit Gharpurey, *University of Texas*

Abstract: Spectrum sensing and feature detection are crucial for cognitive radio to detect locally free spectrum and predict interference. This workshop provides an overview of theoretical concepts and techniques, as well as practical circuits and architectures for such applications.

Speakers:

1. "Fundamental Limits on Spectrum Sensing", **R. Tandra**, *Qualcomm Inc., San Diego, United States*
2. "Spectrum Awareness: Signal Classification", **O. A. Dobre**, *Memorial University, St. John's, Canada*
3. "A Wideband Spectrum Sensing Technique with Integrated Dynamic-Range-Scalable Energy Detector", **M. Kitsunezuka**, *NEC Corporation, Kawasaki, Japan.*
4. "Cross-correlation Spectrum Sensing", **M. S. Oude Alink**, *University of Twente, Enschede, Netherlands*
5. "Versatile Sensing for Mobile Devices: Cost, Performance and Hardware Prototypes", **J. Borremans**, *IMEC, Leuven, Belgium*

WSK: Sunday, 8:00 AM – 5:00 PM

Recent Development in CMOS Mixer Design and Application

Sponsors: **RFIC**
Organizers: **Osama Shana'a**, *MediaTek*
Danilo Manstretta, *University of Pavia*

Abstract: The design of RF mixers has evolved in recent years. Some of the main observations are perhaps the use of none 50% duty-cycle LO and the increasing popularity of current driven passive mixers compared to the classic 50% LO driven voltage mode active mixers. Furthermore, there is an increasing demand for harmonic rejection mixers in broadband applications such as TV tuners, as well as the use of passive mixers to construct high-Q RF filters. In additions, modern 3G/4G FDD transmitters rely now on low-noise mixers to achieve SAW-less architecture. This workshop reviews all different mixer topologies and sheds more light on the design considerations and tradeoffs plus merits of each approach.

Speakers:

1. "Passive and Active CMOS Mixers, An Overview", **O. K. Shana'a**, *MediaTek, San Jose, United States*
2. "Analysis and Optimization of Transceivers with Passive Mixers", **A. Mirzaei**, *Broadcom Corporation, Irvine, United States*

3. "Harmonic Rejection Mixers for Wide-band Receivers", **A. A. Rafi**, *Silicon Laboratories, Austin, United States*
4. "Impedance and Noise Interactions Through CMOS Passive Mixers", **A. C. Molnar**, *Cornell University, Ithaca, United States*
5. "Second-Order Intermodulation in CMOS Down-Converters", **D. Manstretta**, *University of Pavia, Pavia, Italy*
6. "Linearity Improvement of Mixers Using Digitally Assisted Mismatch Calibration and Interferer Cancellation", **P. R. Kinget**, *Columbia University, New York, United States*
7. "Mixers for High Performance Transmitters in Advanced CMOS", **J. V. Sinderen**, *NXP, Eindhoven, Netherlands*
8. "Multi-Path Poly-Phase Passive Mixer Circuits for Flexibly Programmable Harmonic Rejection Mixing and High-Q Filtering", **E. Klumperink**, *University of Twente, Enschede, Netherlands*

WSL: Sunday, 8:00 AM – 12:00 PM

Recent Developments of High-Speed Wireline Transceivers

Sponsors: **RFIC**
Organizers: **Chun-Ming Hsu**, *IBM*
Patrick Yue, *The Hong Kong University of Science and Technology*

Abstract: The demand for higher bandwidth data transmission systems has brought the wireline transceiver design into the region of tens of gigabits per second. New applications ranging from business area to home entertainment area will undoubtedly continue to drive the developments of such transceivers in the next decade. To enable a transceiver in such a high data rate at a reasonable level of power consumption, advanced equalization in the transmitter and receiver as well as clock-and-data recovery techniques are necessary to conquer the channel impairments. In addition, intensive digital adaptation and calibration become inevitable to overcome degraded analog characteristics in the state-of-the-art CMOS processes. Consequently, such an IO is not a pure digital circuit any more but becomes a complicated mixed-signal system requiring optimization from both the system and circuit perspectives. This educational workshop is designed to go through the challenges and opportunities in this field with several recent implementation examples covering a wide design space.

Speakers:

1. "A 1.0625-to-14.025Gb/s Multi-media Transceiver with Full-rate Source-Series-Terminated Transmit Driver and Floating-Tap Decision-Feedback Equalizer in 40nm CMOS", **F. Y. Zhong**, *LSI Corporation, Milpitas, United States*
2. "An Adaptive Equalizer for High-speed Backplane Transceivers", **Y. Hidaka**, *Fujitsu Laboratories of America, Inc., Sunnyvale, United States*
3. "Designing Low-Power Serial Links", **F. O'Mahony**, *Intel, Hillsboro, United States*
4. "Interface Architectures & Circuit Design Suitable for Future Low-Power Memories", **J. Zerbe**, *Rambus Inc., Sunnyvale, United States*

5. "An ADC-based AFE for 10Gbps Serial Links over Backplane/MMF and a 2x23Gbps RX/TX Chipset for DQPSK Optical Transmission", **J. Cao**, *Broadcom Corp, Irvine, United States*

WSM: Sunday, 1:00 PM – 5:00 PM
Advances in Noise Analysis for RF Circuits

Sponsors: **RFIC**
Organizers: **Nebabie Kebebew**, *Cadence Design Systems*
Vuk Borich, *Cadence Design Systems*

Abstract: Noise dramatically impacts system-level performance. This is especially pronounced with advanced node RF-IC circuits that have noise sensitive architectures such as sigma-delta ADCs, fractional-N and Integer-N PLLs and SerDes. Thus noise characterization and minimization is a required objective and task for RF-IC designs. Noise sources are inherent in the circuit elements and cannot be eliminated. Because device noise determines the fundamental limits on circuit performance, it plays a significant role in analog/RF circuit design. In this workshop your will hear and learn from experts in different domains: RF circuit designers, research and academia, and noise analysis tool providers. They will present their practical experiences, discoveries, methodology and solutions used to address the challenges with noise characterization for RF-IC designs. You, the attendee will also have an opportunity to share your experience and challenges.

Speakers:

1. "Practical Noise Analysis for a 14GHz PLL and Silicon Correlation", **N. Bhagwan**, *GHz Circuits, Inc, Sunnyvale, United States*
2. "Low-frequency, High-frequency and Phase Noise of Advanced CMOS", **S. Mohammadi**, *Purdue University, West Lafayette, United States*
3. "Accurate and Fast Simulation of Noise in RF Transceivers", **E. Ngoya[1], G. Estep[2], A. Soury[2]**, *[1]XLIM-CNRS, Université de Limoges, Limoges, France, [2]Agilent Technologies, Santa Clara, United States*
4. "RF Circuit Noise Analysis with Full Spectrum Accuracy", **Y. Zhu, X. Lai, Y. Li, R. Davis**, *Cadence Design System Inc, San Jose, United States*

WSN: Sunday, 1:00 PM – 5:00 PM
Short-Range Near-Field Communications (NFC)

Sponsors: **RFIC**
Organizers: **Magnus Wiklund**, *Qualcomm*
Gernot Hueber, *NXP Austria*

Abstract: Short-Range Near-Field Communications (NFC) has become a technology that is on the way to make an impact on our everyday lives. In mobile phones NFC is used in various applications such as Gaming (Angry birds) and mobile payments (Google Wallet). The technological trend of the RFIC community is to explore boundaries of what our modern integrated circuit processes

has to offer. So what kind of challenges and opportunities do 13.56MHz technologies have to offer when advanced research is moving in the direction towards THz circuits? It turns out that RFIC development of NFC circuits is a highly advanced topic. This workshop covers a wide spectrum of what NFC is all about. Leading industrial and academic players are presenting their views on important topics such as - Integration into SoCs - Architecture challenges and systems requirements - Very high data rate systems and RF memories - NFC circuits at the nanoscale - NFC fundamentals (Electromagnetism and circuits, tools, useful theories) - NFC related technologies - New opportunities (both for research and business).

Speakers:

1. "NFC Fundamentals", **M. O. Wiklund, A. Wong**, *Qualcomm Inc, Santa Clara, United States*
2. "Design Considerations for Low Power, Multi-Standard NFC SoCs", **G. Hueber**, *NXP Semiconductors, Gratkorn, Austria*
3. "Large-Scale Radiating Integrated Circuits", **A. Babakhani**, *Rice University, Houston, United States*
4. "From NFC/RFID to Wirelessly Readable and Writable Memories", **J. Jantunen[1], M. Pelissier[2], B. Gomez[2], J. Arponen[1]**, *[1]Nokia, Helsinki, Finland, [2]CEA-Leti, Grenoble, France*
5. "Ultra-low Power MEMS-based Radio for Short-range Wireless Communication", **C. C. Enz[2], D. Ruffieux[1]**, *[1]CSEM, Neuchatel, Switzerland, [2]EPFL, Lausanne, Switzerland*

WSO: Sunday, 1:00 PM – 5:00 PM

Advancements in Front End Modules for Mobile and Wireless Applications

Sponsors: **RFIC, MTT-5, MTT-23**
Organizers: **Joseph Staudinger**, *Freescale Semiconductor Inc.*
Freek van Straten, *NXP*
Gary Zhang, *Skyworks Solutions Inc.*

Abstract: The dramatic growth in cellular and mobile communication devices is placing extraordinary technical challenges to implement the front end electronics in a high performance low cost miniaturized module. Very high module complexity results due to the integration of many components, including switching elements, power amplification, digital controllers, and impedance matching networks, and adaptive tuner matching and controllers to name but a few. The challenges cross many disciplines including packaging, thermal management, EM modeling, to advancements in semiconductor technologies. This workshop will feature experts and specialists who will provide insight and solutions to these complex issues and share their insight into future research activities.

Speakers:

1. "Cellular Radio Complexity and the RF Transceiver", **D. B. Schwartz**, *Fujitsu Semiconductor Wireless Products, Tempe, United States*
2. "Packaging Technology for FEMs- Thermal Design and Modeling", **B. Vijayakumar**, *Skyworks Solutions, Inc., Irvine, United States*

3. "Antenna tuner for hand-sets", **A. V. Bezooijen**, *TDK, Nijmegen, Netherlands*
4. "Silicon-on-Insulator (SOI) Switches for Cellular and WLAN Front-End Applications", **A. Tombak**, *RFMD Inc., Greensboro, United States*
5. "RFIC Front End Module EM Co-Design and Simulation", **W. Sun**, *Skyworks Solutions, Newbury Park, United States*

WSP: Sunday, 1:00 PM – 5:00 PM

Digital Transmitters and PAs for Wireless Applications

Sponsors: **RFIC**
Organizers: **Ali Afsahi**, *Broadcom Corp.*
Waleed Khalil, *Ohio State University*

Abstract: The demand for lower size and power consumption wireless transceivers has been increased significantly in recent years to lower the cost and increase the battery life of mobile devices. More recently, breakthroughs in silicon-based technologies along with the introduction of newer generations of communication networks and the unprecedented surge in demand for high data rates, started the race towards purely digital solutions for all radio standards. In addition, the coexistence of "software revolution" has called for the programmability of the communication systems through software to implement a software radio (SWR). Unfortunately, RF transceivers have not taken as much advantage as baseband processors from process scalability due to many design constrains. This workshop will discuss the challenges and recent achievements in more digital transmitters/ PAs to reduce the size and power consumption. Topics will range from digital-friendly PAs, RF and mm-wave DACs, power DACs and mixers, advances in device technology for high power high switching speed circuits.

Speakers:

1. "Recent Advances in Digital Polar and I/Q Transmitters", **R. B. Staszewski**, *Technische Universiteit Delft, Delft, Netherlands*
2. "Flexible Digital-centric Wireless Transmitters", **R. Negra[1], N. Zimmermann[2], B. T. Thiel[1], B. Mohr[2], J. Mueller[2], Y. Wang[2], S. Heinen[2]**, *[1]RWTH Aachen University, Aachen, Germany, [2]RWTH Aachen University, Aachen, Germany*
3. "InP and GaN Technologies for High-Speed DAC and Switched-Mode Power Amplifiers", **D. A. Hitko**, *HRL Laboratories, LLC, Malibu, United States*
4. "Wide-Band RF Digital to Analog Converter", **M. Choe**, *Teledyne Scientific and Imaging, Thousand Oaks, United States*
5. "Digitally-Modulated Polar Power Amplifiers for Multi-Mode Transmitters: Theory, Implementation and Linearization", **C. D. Presti**, *Qualcomm Inc., San Diego, United States*
6. "A Digitally Modulated Inverse Class-D Power Amplifier for Modern Wireless Standards", **D. Chowdhury[2], A. M. Niknejad[1]**, *[1]University of California at Berkeley, Berkeley, United States, [2]Broadcom Corporation, San Diego, United States*

SUNDAY SHORT COURSES 17 JUNE 2012

SC-1: Sunday, 8:00 AM – 5:00 PM
Graphene and RF Applications

Sponsors: **MTT-25**
Organizers: **Luca Pierantoni**, *Università Politenica delle Marche*
Max Lemme, *Royal Institute of Technology*

Abstract: In view to the new epochal scenarios that nanotechnologics disclose, nanoelectronics has the potential to introduce a paradigm shift in electronic systems design similar to that of the transition from vacuum tubes to semiconductor devices. Since many nano-scale devices and materials exhibit their most interesting properties at radio-frequencies (RF), nanoelectronics provides an enormous and yet widely undiscovered opportunity for the microwave engineering community. Among these materials, graphene is quickly becoming an extremely interesting solutions for a wide variety of electronic devices and circuits. It offers the possibility of outstanding performances with much lower power draw, using processing technology compatible to that used in advanced silicon device fabrication (CMOS).

Graphene science and technology has undergone an astonishing development since its experimental demonstration in 2004, and its unique properties have caught the interest of physicists, chemists and engineers alike. This general excitement has resulted in an explosion of ideas and suggestions for future Radio-Frequency applications and beyond.

In this short course, we aim to take a step back and critically evaluate the real potential of this new material in the context of established semiconductor technology. Hence, this course addresses specific areas of interest to semiconductor device engineers and microwave/RF engineeers.

The attendants of the course will be able to:

- Understand and differentiate the state of the art and the future potential of large area, scalable graphene synthesis methods
- Understand the pros and cons of graphene-based electronic devices for Radio-Frequency electronics, including applications "outside the box" of standard design rules
- Assess the potential of graphene for broadband, high speed optoelectronics up to the THz regime, including photodetection, light modulation and lasing.

The method of presentation includes oral presentation and an open discussion on the lecture topics. This proposal is supported by MTT-25.

MONDAY WORKSHOPS 18 JUNE 2012

WMA: Monday, 8:00 AM – 5:00 PM
Introduction to Advanced Dielectric Measurement Techniques

Organizers: **Michael Janezic**, *NIST*
Shelly Begley, *Agilent Technologies*
Felipe Peñaranda-Foix, *Polytechnic University of Valencia*

WMB: Monday, 1:00 PM – 5:00 PM
Device Model Extraction Based on Vectorial Large-Signal Measurements

Organizers: **Dominique Schreurs**, *K.U. Leuven*
Iltcho Angelov, *Chalmers University*

WMC: Monday, 8:00 AM – 5:00 PM
Advanced Techniques for Electromagnetic-Based Model Generation

Organizers: **Peter H. Aaen**, *Freescale Semiconductor Inc.*
Michel Nakhla, *Carleton University*

WMD: Monday, 8:00 AM – 5:00 PM
Wireless Positioning and Tracking in Indoor/Urban Environments

Organizers: **Alessandro Cidronali**, *University of Florence*
Abbas Omar, *University of Magdeburg*
Upkar Dhaliwal, *Future Wireless Technologies*

WME: Monday, 8:00 AM – 5:00 PM
THz Devices and Systems Based on Nanotechnology

Organizers: **Fabio Coccetti**, *CNRS-LAAS*
Luca Pierantoni, *Università Politecnica Marche*
Erping Li, *A-STAR -IHPC*
Goutam Chattopadhyay, *California Institute of Technology*

WMF: Monday, 8:00 AM – 5:00 PM
Wireless Energy Transfer and Scavenging Techniques

Organizers: **Prof. Alessandra Costanzo**, *University of Bologna*
Prof. Yoshihiro Kavahara, *Tokyo University*

WMG: Monday, 8:00 AM – 5:00 PM
Broadband PAs for Wireless Communications

Organizers: **John Wood**, *Maxim Integrated Products Inc.*

WMH: Monday, 8:00 AM – 5:00 PM

GaN's Destiny: Reliable CW Operation at Power Densities Approaching 40 W/mm - Can it be Fulfilled and When?

Organizers: **John Pierro**, *Telephonics*
Rüdiger Quay, *Fraunhofer Institute Applied SolidState Physics*
Frank Sullivan, *Raytheon Company*

WMI: Monday, 8:00 AM – 5:00 PM

Towards Development of Smarter Substrate Integrated Waveguide Components and Advanced Fabrication Methodologies

Organizers: **Aly Fathy**, *University of Tennessee*
Ke Wu, *Ecole Polytechnique de Montreal, Canada*

WMJ: Monday, 8:00 AM – 12:00 PM

Emerging Technology and Technological Challenges in Low Phase Noise Oscillator Circuit Designs

Organizers: **Dr. –Ing. Ajay K. Poddar**, *Synergy Microwave Corp.*
Prof. Kenji Itoh, *Kanazawa Institute of Technology*

WMK: Monday, 8:00 AM – 12:00 PM

Analytic Concepts and Design Techniques for Low-Noise and Low-Distortion Mixers

Organizers: **Carlos Saavedra**, *Queen's University*

WML: Monday, 8:00 AM – 12:00 PM

Measurement, Design, and Linearization Techniques for High-Efficiency Amplifiers

Organizers: **Antonio, Raffo**, *University of Ferrara*
Domonique Schreurs, *Katholieke Universiteit Leuven*

SC-3: Monday, 8:00 AM – 5:00 PM

Theory and Design of Frequency Synthesizers

Organizers: **Lama Dayaratna**, *Lockheed Martin commercial Space Systems*
Peter White, *Applied Radio Labs*
Cicero Vaucher, Ph.D. *NXP Semiconductors*
Ron Reedy, *Peregrine Semiconductor Corporation*
Patrick Walsh, *Analog Devices*

SC-4: Monday, 8:00 AM – 5:00 PM

Nonlinear Microwave Circuits-Their Dynamics, Bifurcation, and Practical Stability Analysis /Design

Organizers: **Almudena Suárez**, *University of Cantabria*
Christopher P. Silva, *The Aerospace Corporation*

SC-5: Monday, 8:00 AM – 5:00 PM

Dielectric Resonator Antenna, Theory, Design and Applications with Recent Advancement

Organizers: **Ahmed A Kishk**, *Concordia University*

FRIDAY WORKSHOPS 22 JUNE 2012

WFA: Friday, 8:00 AM – 5:00 PM
Integration and Technologies for mm-Wave Sub-systems

Organizers: **Maurizio Bozzi**, *University of Pavia*
Apostolos Georgiadis, *Centre Tecnologic de Telecomunicacions de Catalunya*
Manos Tentzeris, *Georgia Intstitute of Technology*

WFB: Friday, 8:00 AM – 5:00 PM
White Space Technologies – Future Emerging Technology Needs

Organizers: **Nuno Borges Carvalho**, *Dep. Electronica, Telecomunicacoes e Informatica – Instituto de Telecomunicacoes*
Alessandro Cidronali, *University of Florence*

WFC: Friday, 8:00 AM – 5:00 PM
Emerging Technology of Terahertz Imaging Systems, Devices, and Algorithms

Organizers: **Magda El-Shenawee**, *University of Arkansas*
Aly Fathy, *University of Tennessee*

WFD: Friday, 8:00 AM – 5:00 PM
High-Efficiency Transmitters with Dynamic Supplies

Organizers: **Paul Draxler**, *Qualcomm Inc. & UCSD*
Zoya Popovic, *University of Colorado at Boulder*

WFE: Friday, 8:00 AM – 12:00 PM
Gallium Nitride for Low Noise Amplifier Applications

Organizers: **Phillip M. Smith**, *BAE Systems*
Matthias Rudolph, *Brandenburg University of Technology*

WFF: Friday, 8:00 AM – 5:00 PM
Advances in Reconfigurable RF Systems and Materials

Organizers: **Ingo Wolff**, *IMST GmbH*
Rüdiger Follmann, *IMST GmbH*

WFG: Friday, 8:00 AM – 5:00 PM
RF Coils and Components for MRI Receiving Applications

Organizers: **Robert H. Caverly**, *Villanova University*
William E. Doherty, *Microsemi-Lowell*

WFH: Friday, 8:00 AM – 5:00 PM
RFID-based Low-Cost Smart Sensor Networks for Challenging Environments

Organizers: **Hendrik Rogier**, *Ghent University*

WFI: Friday, 1:00 PM – 5:00 PM
The Development of Precision GPS Solutions in 4G

Organizers: **Joy Laskar**, *InSite Partners*
Anh-Vu Pham, *UC-Davis*
Upkar Dhaliwal, *Future Wireless Technologies*

WFJ: Friday, 8:00 AM – 12:00 PM
A World Survey of the State-Of-The-Art in RF MEMS

Organizers: **Gabriel M. Rebeiz**, *UCSD*
Tomonori Seki, *Omron*

WFK:Friday, 8:00 AM – 12:00 PM
Advanced RF, Microwave and MMW Technology for Nuclear, Chemical and Biological Detection Systems

Organizers: **Frank Sullivan**, *Raytheon Company*
Ruediger Quay, *Fraunhofer Institute of Applied Solid State Physics*

WFL: Friday, 1:00 PM – 5:00 PM
System, MMIC and Package Design for a Low-Cost, Surface-Mountable Millimeter-Wave Radar Sensor

Organizers: **Thomas Zwick**, *Karlsruhe Institute of Technology*
Christoph Scheytt, *University of Paderborn*

SC-6: Friday, 8:00 AM – 5:00 PM
Microwave Filters and Multiplexing Networks for Communication Systems

Organizers: **Chandra Kudsia**, *Matrix Inc.*
Vicente Boria, *UPV*

SC-7: Friday, 8:00 AM – 12:00 PM
A Look at Some of the Principle of Wireless Communications from Maxwellian Viewpoint

Organizers: **Tapan K. Sarkar**, *Syracuse University*
Magdalena Salazar-Palma, *Universidad Politécnica de Madrid*

SC-2: Friday, 8:00 AM – 12:00 PM
EMI/EMC Fundamentals for RF & Microwave Engineers

Organizers: **William H. (Bill) Cantrell**, *Reagan Ballistic Missile Defense Test Site*

ADVANCE REGISTRATION

Registration Categories

The registration process is split into three tiers to better serve membership needs. The 1st tier is the Early Bird Registration period. It begins Tuesday, 1 February and will last through Monday, 21 May. This period provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird period is the 2nd tier or Advance Registration period. It extends from Tuesday, 22 May through Friday, 15 June, just prior to the start of Microwave Week. The 3rd and final tier is the On-Site Registration period that will remain the same as in past Symposia, starting on Saturday, 16 June, the first day of Microwave Week, and ending on Friday, 22 June.

EARLY BIRD PERIOD	**1 FEBRUARY**	**21 MAY (THROUGH MIDNIGHT EDT)**
ADVANCE PERIOD	**22 MAY**	**15 JUNE (THROUGH MIDNIGHT EDT)**
ON-SITE PERIOD	**16 JUNE**	**22 JUNE (THROUGHOUT MICROWAVE WEEK)**

Register online: http://reg.mpassociates.com/reglive/ PromoCode.aspx?confid=138

Symposium SUPERPASS

For one low price, registrants can attend as many technical sessions from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend one full-day workshop (or two half-day workshops, if desired). SUPERPASS registration includes the electronic proceedings for IMS, RFIC, ARFTG, and the All Workshop electronic proceedings. Also included is admission to the exhibits. In addition, the SUPERPASS will allow you to attend the RFIC Reception on Sunday, the IMS Welcome Reception on Monday, the Awards Banquet on Wednesday and the Thursday closing ceremonies, as well as, the ARFTG luncheon on Friday.

Early Bird Registration

Please follow these instructions for completing the Early Bird Registration Form on the following page. Early Bird Registration rates provide significant savings from the on-site fees and are available through midnight (EDT) 21 May. Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the workshops, technical sessions, and exhibit hall. This form is not used for guest tour registration, which is described elsewhere in this program book. Each registrant must submit a separate form with payment.

Methods of Registration

Individuals can register online, by fax or by mail. All registrations must be accompanied with a payment; we accept Visa, MasterCard, American Express, and checks drawn from a U.S. bank. Registration forms received without a form of payment will be discarded. We do NOT accept phone registrations.

Personal Information

If you would like to receive information by email from the IEEE, MTT-S, or microwave companies, simply select the appropriate boxes.

Membership

Check boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit www.ieeee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Students, Retirees, and IEEE Life Members receive a discount on some registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full time student carrying a course load of at least nine credit hours.

Symposia

Microwave Week includes the IMS technical program, and exhibit, as well as the RFIC Symposium (www.rfic2012.org), and ARFTG Conference (www.arftg.org).

Select the conference(s) you wish to attend.

- IMS Technical Sessions are held on Tuesday, Wednesday, and Thursday. Registration includes admission to the exhibition and the electronic proceedings.
- RFIC Technical Sessions are held on Monday and Tuesday. Registration includes admission to the RFIC Reception, the exhibition, and the electronic proceedings.
- ARFTG Technical Sessions are held on Friday. Registration includes breakfast, lunch, electronic proceedings, and admission to the ARFTG Exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE Members.
- Microwave Week hosts the largest exhibition of its kind with over 500 companies. Exhibit only registration is available.

Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 20 June from 1800 to 2000 at the Palais des congrès, Level 7- Room 701. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. For Early bird registration ONLY, the workshop's printed notes are also included for the workshop you are registered for with the workshop's fee. For Advance and On-site registration, the workshop's printed notes are NOT included in the workshop's fee and must be purchased separately.

Full-day workshops include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and a morning refreshment break. Afternoon workshops include a lunch and an afternoon refreshment break.

All-Workshop USBs

Purchase two full-day workshops and receive the USBs for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop USBs are not available for individual sale.

Guest Registration

Attendees registered for the technical portion of the conference may add a Guest to their registration for an additional fee. Guest Registration includes access to the guest lounge, plenary session, and exhibit hall, but does not allow access to technical sessions and workshops.

Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to "2012 IEEE IMS". Written requests for refunds will be honored if received by 21 May 2012. Refer to the Refund Policy for complete details.

Policy

Written requests received by 21 May 2012 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email address for the refund check. If registration was paid for by credit card, the refund will be made through an account credit. An account number must be provided if the initial registration was completed on-line. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721Boxelder St., Ste. 107
Louisville, CO 80027
nannette@mpassociates.com

Badge Cash:

- IMS2012 is continuing the Badge Cash and Print on Demand programs this year as part of a continued effort to improve your experience as an attendee of the symposium.
- Attendees registered for All IMS Sessions will have a value of $45.00 credit put onto their badge that can be used at selected locations in the Palais des congrès for breakfast each morning (approximately $15.00/day). This replaces the continental breakfasts that the conference has provided to the IMS attendees in previous years.
- Attendees registered for the Superpass will have a value of $60.00 on their badge and this includes both IMS and RFIC.
- Attendees registered for IMS Single Day will have a value of $15.00 on their badge.
- Attendees registered for RFIC Sessions will have a value of $30.00 on their badge.

How does Badge Cash work?

Select your items at a participating station and hand the cashier your badge. The cashier will scan your badge and the amount purchased will be deducted from your badge. If there is not enough cash value left on your badge you will be responsible for paying the difference.

If I lose my badge, will I receive a new one with the cash value on it?
No, if you lose your badge you will only receive a new badge that WILL NOT have Badge Cash on it.

If I don't use all the money, do I receive the remaining amount in cash?
No, Badge Cash is NOT redeemable for cash, it is only good for food products sold at specific vendors within the Palais des congrès.

IMS2012 Badge Cash locations at the Palais des congrès:

1. Lower level, under the escalator - Place Riopelle Lobby - for breakfast ONLY
2. West Lobby - breakfast and lunch
3. Viger Hall - breakfast and lunch NOTE: this area will have outdoor seating weather permitting
4. Exhibit Hall - as space is available

Print on Demand Stations:

There are three Print on Demand Stations located throughout the Palais des congrès.

1. Fifth level in the corridor outside of rooms 511/512
2. Viger Lobby
3. West Lobby by the Cyber Café

NOTE: ONLY IMS2012 Technical Papers can be browsed and printed at these terminals. Please use the Cyber Café for internet related activities.

ON SITE REGISTRATION

On-Site Registration

On-Site registration for all Microwave Week events will be available in Palais des congrès, Place Riopelle Lobby. Registration hours are:

Day	Time
Saturday, 16 June	1400 – 1800
Sunday, 17 June	0700 – 1800
Monday, 18 June	0700 – 1800
Tuesday, 19 June	0700 – 1800
Wednesday, 20 June	0700 – 1800
Thursday, 21 June	0700 – 1600
Friday, 22 June	0700 – 0900

Exhibit Only Registration

Exhibit only registration is available.

Guest Tour Registration

Registration for guest tours will be available Palais des congrès, Place Riopelle Lobby. Please refer to the Guest Tour Program section of this program book for further details and tour descriptions.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to IMS technical sessions and exhibits. Digests are not included. The Press Room (523A) will available from Tuesday through Thursday of Microwave Week.

ARFTG Registration

Late on-site registration will be available at the Palais des congrès, Place Riopelle Lobby on Friday from 0700 to 0900. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

ON SITE REGISTRATION (continued)

REGISTRATION FEES	MEMBER	NON-MEMBER
SuperPass		
IMS, RFIC, and ARFTG Sessions and Electronic Proceedings, Awards Banquet, Thursday Evening Event, Full Day (or 2 Half Day) Workshop Attendance and All Workshop USBs	$1345	$2000
Student, Retiree, Life Member SuperPass	$840	N/A
IMS		
All IMS Sessions	$575	$850
IMS Single Day Registration	$290	$435
IMS Sessions - Student, Retiree, Life Member	$100	N/A
RFIC Symposium		
All RFIC Sessions	$280	$415
RFIC Sessions - Student, Retiree, Life Member	$200	N/A
ARFTG Conference		
All ARFTG Sessions	$290	$435
ARFTG Sessions - Student, Retiree, Life Member	$195	N/A
Exhibition Only		
Exhibition Only Pass	$30	$30
Guest Registration		
Guest Badge (requires technical conference registration)	$40	$40
Extra Proceedings and Digests		
IMS Electronic Proceedings	$70	$105
RFIC Digest	$70	$105
RFIC Electronic Proceedings	$70	$105
ARFTG Electronic Proceedings	$70	$105
Evening Events		
RFIC Reception Only (Sun. Night)	$50	$70
Awards Banquet (Wed. Night)	$75	$75
Workshops		
Full Day	$225	$335
Full Day Student/Retiree	$155	N/A
Half Day	$115	$170
Half Day Student/Retiree	$80	N/A
Full Day Short Courses	$390	$585
Full Day Short Courses Student/Retiree	$270	N/A
Half Day Short Course	$270	$405
Half Day Short Course Student/Retiree	$190	N/A
Two Full Day Workshops includes All Workshop USBs	$595	$880
Two Full Day Workshops includes All Workshop USBs Student/Retiree	$405	N/A
Printed Workshop Notes	$30	$45
Printed Workshop Notes Student/Retiree	$30	N/A

VISA INFORMATION

For General information on visiting Canada please refer to the following url http://www.cic.gc.ca/english/visit/index.asp

IMS2012 attendees who require an invitation letter

IMS attendees who need an invitation letter for a visitor visa should complete the application found on the IMS2012 Conference Webpage and send it via e-mail to: jules.gauthier@polymtl.ca

US citizens traveling to Canada: Passport is Needed

A visa is not needed for US citizens traveling to Canada. Please note, however, that a valid passport is required (a driver's license is no longer sufficient for travel to Canada).

Exhibitors:

IEEE along with MP Associates has obtained special privileges from the Canada Border Services Agency in order to facilitate the entry of goods into Canada for exhibition. Mendelssohn Event Logistics has been appointed as the official customs broker, and will look forward to working with you. Our exhibition management team is working with the in-house customs broker/freight forwarder to coordinate the shipping of exhibition material through customs directly to the convention center, eliminating duties on any materials sent to the show. Please feel free to contact our exhibitions management at exhibition@ims2012.org or check the exhibition pages in our website for contact information of Mendelssohn Event Logistics for more information on crossing the Canada/US border.

International Students Studying in US:

For foreign students who are currently studying in the US, traveling to Montréal is straightforward. Detailed information on entry to Canada and reentry to the US can be found in http://www.canadavisa.com/us-international-student-travel.html. Most students do not require a new US visa to return to the US from Canada if the stay in Canada is less than 30 days. Note that a visa to enter Canada may still be required depending on your country of origin.

Recommendations

To avoid frustration and disappointment, please note the following:

- Advance planning by travelers is essential. Review your visa status and find out if you need a visa or a visa renewal to enter Canada.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest Canadian embassy or consulate for a current time estimate and recommendations.
- Visit the embassy or consular section where you plan to apply for your visa. Visit their website to find important information on how to schedule an interview appointment and pay fees.
- An interview is required as a standard part of processing for most visa applicants.

Disclaimer: Please note that this information is provided in good faith, but regulations may change and the only authoritative sources of information are government websites and consular services.

SOCIAL EVENTS/GUEST PROGRAM

SUNDAY, 17 JUNE 2012

RFIC Reception: 1900-2100
Palais des congrès, Level 7 – Room 710a

Immediately following the RFIC Plenary Session is the RFIC Reception to be held in adjacent Room 710a at the Palais des congrès. This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

MONDAY, 18 JUNE 2012

IMS 2012 Welcome Reception: 1900-2030
Palais des congrès, Viger Lobby

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by IMS2012 in the Palais des congrès, Viger Lobby.

Chapter Chairs' Meeting (CCM): 2000 – 2200
Hyatt, Grand Salon

All our Chapter Chairs and their designated Chapter representatives are cordially invited to our Reception/Poster Session followed by Dinner and Meeting. For further information contact your Regional Chapter Coordinator, or Bela Szendrenyi at bela.szendre-nyi@verigy.com.

Sponsor: IEEE MTT-S AdCom and the MGA Committee

TUESDAY, 19 JUNE 2012

Women in Microwaves Reception: 1800-1930
Pointe A Calliere Museum, 350 Pl Royale, Montréal

Meet with old friends as well as make new connections to the growing community of women who make a career in the field of high-technology. Enjoy great food, refreshing beverages and warm conversation at the WIM Social Event.

Ham Radio Social: 1830-2130
Hyatt Hotel, Level 4 – Room: Soprano

While enjoying a buffet and open bar, the attendees will have the opportunity to see the accomplishments of amateur radio operators who have skillfully designed and built transceivers for use from VHF to high millimeter wave bands. Some of these transceivers were made from surplus and commercially available components and some are state-of-the-art new designs including SDR. Several will be on display and their builders will be there to answer questions.

All conference attendees are welcome. You will find that amateur radio operators are utilizing their allocated frequency spectrum for very important uses and you may be interested in obtaining your license so you too can test your new designs and microwave propagation.

MTT-S Graduates of the Last Decade (GOLD) and Student Reception: 1930 to 2130 Pub St-Paul, Old Montréal

The IEEE MTT Graduates of Last Decade (GOLD) and Student Committees invite all MTT GOLD and student members to a complimentary reception at the Pub St-Paul in Old Montréal. This will be an excellent opportunity not only to relax and entertain, but also to interact and network with other GOLD and student members.

Sponsor: IEEE MTT-S GOLD and Student Committees

WEDNESDAY, 20 JUNE 2012

Industry Hosted Cocktail Reception: 1700-1800 Palais des congrès, Level 2 – Exhibition Hall

Symposium Exhibitors will host a cocktail reception.

MTT-S Awards Banquet: 1800-2200 Palais des congrès, Level 7 – Room 701

The MTT-S Awards Banquet includes dinner, major society awards presentation and entertainment. This year the entertainment will feature one of the most renowned attractions of Montréal: contemporary circus. Discover this nouveau cirque, which blends comedy, performances and visual effects in a unique way. Tickets can be purchased at the time of registration.

THURSDAY, 09 JUNE 2012

MTT-S Student Awards Luncheon: 1200-1400 Le Westin Hotel, Level 9 – Fortifications Ballroom

All students are invited to attend the luncheon which recognizes recipients of the MTT-S Undergraduate Scholarships, MTT-S Graduate Fellowships, IMS2012 Student Volunteers, IMS2012 Student Paper Awards and the participants/winners of the IMS2012 Stu-dent Design Competitions.

IMS2012 Closing Reception:1730-1830 Palais des congrès, Viger Lobby

All Microwave Week attendees and exhibitors are invited to attend the Closing Reception hosted by IMS2012 in the Palais de congrès. Viger Lobby

Please stop by the Tourisme Montréal information desk on the 5th level of the Palais des congrès for tourist and restaurant information.

Sunday, 17 June - Thursday, 21 June, 1100-1600

Guest Lounge

The Guest Lounge will be located at the Hyatt Regency Montreal on the 6th Floor in the Inspiration Room. It will be a place to relax and meet. The Guest Lounge will also have suggestions and discount coupons for various activities to enjoy while in Montréal as well as fun games and crafts for the families. Guest registration is required and fees do apply.

Sunday, 17 June - Thursday, 21 June, 0700-1630 and Friday, 22 June, 0700-1200

Special Tours:

To register for the following tours, please refer to the Hotel and Travel tab on the conference website at http://ims2012.mtt.org.

City Tour: Montréal Mixes Trendiness & Tradition

Tuesday, 19 June 2012
9:00am to 12:00pm
$48.00 CAD per person

This rate includes the following:

- Professional English Speaking Guide
- Deluxe motorcoach
- Admission to the Notre-Dame Basilica
- Bottle of water
- All taxes

Discover Montreal with its bi-cultural heritage and cosmopolitan blend of the old and new on this comprehensive overview of our city. Old Montreal's rich architectural and historical legacy, the financial district, Montreal's leading museums, the cultural and performing arts institutions, Montreal's elegant upper class communities and Montreal's universities.

Along the way, the tour includes a stop at the summit of Mt. Royal for a panoramic view of Montreal and a guided visit of Notre-Dame Basilica, an outstanding example of neo-gothic architecture.

We will drive through St-Helen's and Notre-Dame Islands, sites of Expo 67', and the Montreal Casino

Flavors and Aromas of Old Montréal

Wednesday, 20 June 2012
9:00am to 12:00pm
$50.00 CAD per person

This rate includes the following:

- Professional English Speaking Guide
- Tastings in 3 different boutiques
- Bottle of water
- All taxes

This gastronomic walk will make you discover the culinary, cultural and historical charms of the oldest district of Montreal. The group will first transfer from the hotel by walk to Old Montreal accompanied by a professional guide.

Hosted in old warehouses and showrooms of the 19th era, some food boutiques open their doors to make you taste their delicacies. Through small and narrow cobblestone streets, the guide explains the influence of the Natives and the nuns on our food habits, and how the venue of the World Expo in 1967 brought exotic food on our tables. That and much more, accompanied by a professional foodie guide who will feed you with historical and gastronomic comments all along.

The tour will include stops in 3 different boutiques. You will have the chance to taste local products including macaroon, duck paté and foie gras on baguette, and gelato sweeten with maple syrup. Return to the hotel by foot.

Old Montréal Walk and the Museum of Archeology

Wednesday, 20 June 2012
9:00am to 12:30pm
$45.00 CAD per person

This rate includes the following:

- Professional Guide
- Admission Fees
- Bottle of water
- All taxes

You will first transfer to Old Montreal by foot with a professional guide. In this historic quarter, you will stroll through a maze of narrow cobblestone lanes and old buildings, providing a perfect opportunity to discover the history and charm of Old Montréal. En route you will see Place d'Armes, Jacques Cartier Square and Montréal City Hall.

One of the highlights of this tour is the visit of the museum of Archeology also called Pointe - à - Callières. The museum is recognized as a national historical and archaeological site, leading visitors through centuries of history. The Museum opened in 1992, the result of over 10 years of digs. It showcases major archaeological discoveries made on this site starting in the 1980s.

The visit will start with the multimedia show, Yours Truly, Montréal. It presents the history of Montréal in 18 spellbinding minutes. The City speaks to us and tells us its story over time: the birth of Mount Royal, the arrival of the Amerindians, the founding of Montréal, French and British regimes, the modern era and the development of networks.

The Where Montréal Was Born permanent exhibition takes visitors to the heart of an authentic archaeological site: Montréal's birthplace. The unusual underground route covering six centuries of history, from the times when Natives camped here to the present day, is an emotion-packed look at the very essence of a city born over 360 years ago.

Your tour starts in the remains of the Royal Insurance Building (1861-1951), which housed Montréal's Customs office from 1871 to 1917. Along the way, you'll cross through an imposing vaulted stone tunnel, where the Little Saint-Pierre River once flowed, and see how it was converted into a collector sewer from 1832-1838.

You will return to the hotel by foot with your guide or, if you prefer, stay in Old Montreal on your own.

The Richelieu Valley: The Gourmet Region

Thursday, 21 June 2012
10:00am to 3:00pm
$105.00 CAD per person

This rate includes the following:

- Professional Guide
- Bus Transportation
- Cider Wine Tastings
- 3 Course Lunch including beer tasting
- Bottle of water
- Taxes
- Lunch Gratuities

The Richelieu Valley, colonized by the French, was the heart of the seigniorial system and is noteworthy for the panoramic scenery it offers.

The Richelieu Valley, also called the Apple Region offers panoramic scenery coupled with an ideal climate for the gardening of market produce. The Monteregians hills are surrounded by huge orchards and apple industries. You will also discover the tasty regional products like apples and apple by-products, as well as delicious wines. During the tour you will visit a cider mill "La Cidrerie Jodoin" and taste their products derived from apples, as an ice sparkling cider or ice cider.

A delicious meal will follow in the village of Chambly at the restaurant Fourquet Fourchette on the banks of the Richelieu River before heading back to Montreal.

A Day in Quebec City and Montmorency Falls

Friday, 22 June 2012
8:00am to 21:00pm
$ 105.00 CAD per person

The rate includes the following:

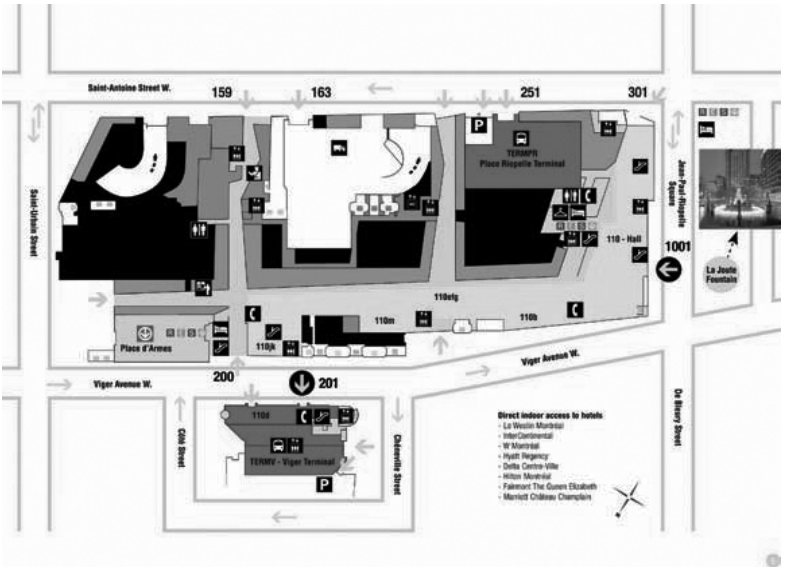
- Transportation
- Specialized tour guide in Quebec City
- Bottle of water
- All taxes

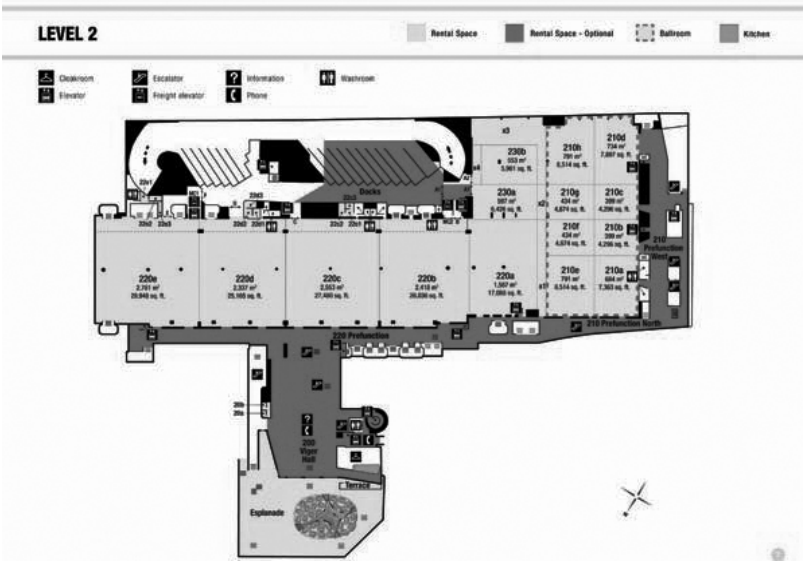
Classified as an international heritage site in 1985 by UNESCO, the city of Québec, capital of the Province of Québec, is the only remaining entirely fortified city in North America. Founded in 1608 by Samuel de Champlain, Québec was the first permanent European settlement in New France. A natural citadel, the site dominates the St. Lawrence. Renowned for its European flavor, the city offers a rich architecture.

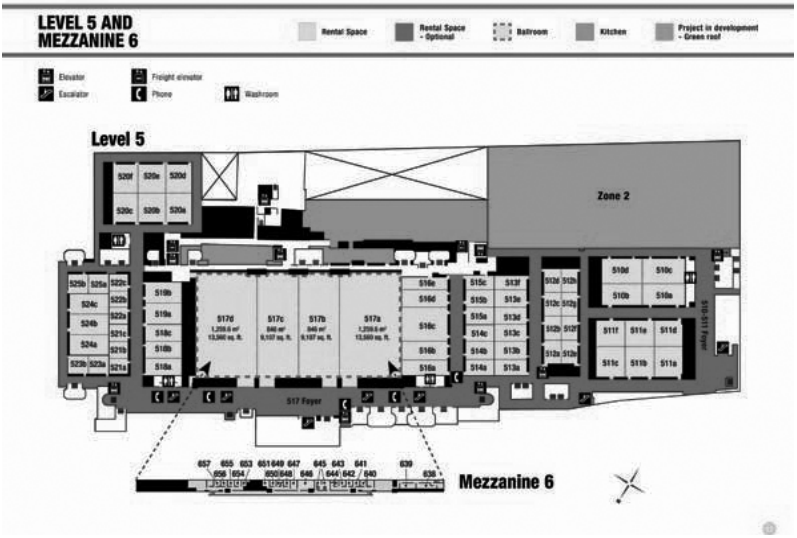
Before entering Quebec City, you will first have a look at the 274ft Montmorency Falls. Then, lunch on your own in Old Québec City. After lunch, tour of the city with a specialized guide where you will see the Plains of Abraham, Notre-Dame Church, Place Royale, the National Assembly, the Citadelle and the famous Château Frontenac. See if you can resist the ambiance of Québec City!

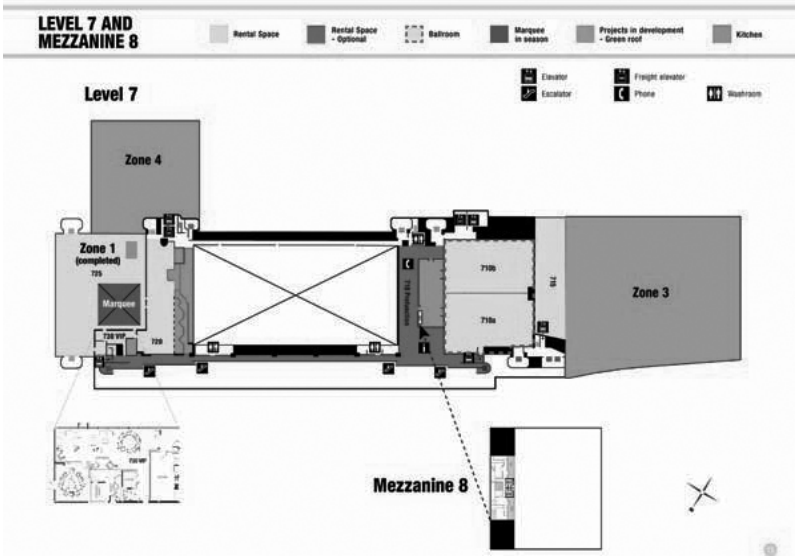
Free time in petit Champlain before heading back to Montreal.

CONVENTION CENTER MAPS






LEVEL 5 AND MEZZANINE 6
Rental Space
Rental Space - Optional
Ballroom
Kitchen
Project in development - Green roof
Elevator
Freight elevator
Escalator
Phone
Washroom
Level 5
Zone 2
S17 Foyer
Mezzanine 6


LEVEL 7 AND MEZZANINE 8
Rental Space
Rental Space - Optional
Ballroom
Marquee in season
Projects in development - Green roof
Kitchen
Elevator
Freight elevator
Escalator
Phone
Washroom
Level 7
Zone 4
Zone 1 (completed)
Marquee
Zone 3
Mezzanine 8

Tina Quach
c/o IEEE
2314 W. Harrison Street
Chandler, AZ 85224

2012 RFIC Symposium
Montréal, Canada
17-19 June 2012

PROGRAM

MICROWAVE WEEK

All reservation requests must be received by 14 May 2012.
Changes to existing reservations may be made through the housing bureau until 8 June 2012. Listed convention rates are available until 14 May 2012 based on availability.

Phone: 514-844-0848
Toll free North America: 1-888-722-2220
Fax: 514-844-6771
Email: reservation@tourisme-Montréal.org
Online: ims2012.mtt.org

Mail: IMS2012 Housing Bureau
Tourisme Montréal
1555 rue Peel, bureau 600
Montréal, Quebéc, Canada H3A 3L8

Instructions and Housing Bureau Policies:

1. Acknowledgements will be sent after each reservation booking, modification and/or cancellation If you do not receive a confirmation via e-mail within 24 hours after any transaction, contact the Housing Bureau by phone or e-mail. You will not receive a confirmation from the hotel.
2. All rates are per room, per night and are subject to 3.5% lodging tax plus a 5% Goods and Services Tax (GST) and 9.5% Provinicial Sales Tax (PST) (subject to change).
3. Request room and bedding and please indicate special requests in the section provided on the form. Specific room types will be assigned at check-in. Please be advised that requests are not guaranteed.
4. A credit card is needed to guarantee a room reservation. Credit cards must be valid through June 2012 to be used for deposits.
5. Changes, modifications and cancellations prior to 14 May 2012 must be made in writing through the Housing Bureau. Reservations guaranteed by a credit card may be cancelled without penalty until 14 May 2012.
6. Any hotel reservation changes or cancellations after 8 June 2012 must be made with the hotel directly.
7. You will receive your hotel confirmation number two weeks before the start of the 2012 IMS Conference.

Housing Reservation Information:

Full Name:_____

E-mail Address: _____

Company:_____

Address: _____

City:_____State:_____ Zip:_____

Country: Daytime Phone: Fax:

Frequent Hotel Stay Number:_____

Credit Card Type (Circle): MasterCard Visa Amex Discover

Cardholder Name (As it appears on card)_____

Cardholder Signature (REQUIRED)_____

Card Number: _____Exp. Date _____

Hotel names, locations and rates are on the facing page. Please list a minimum of three choices.

First Choice: _____ Second Choice:_____ Third Choice: _____

First Choice Rate:_____ Second Choice Rate: _____ Third Choice Rate: _____

Arrival Date_____Departure Date _____

If hotel choice is not available, which is most important: Rate: _____ or Location_____ (Please select one)

Special Requests

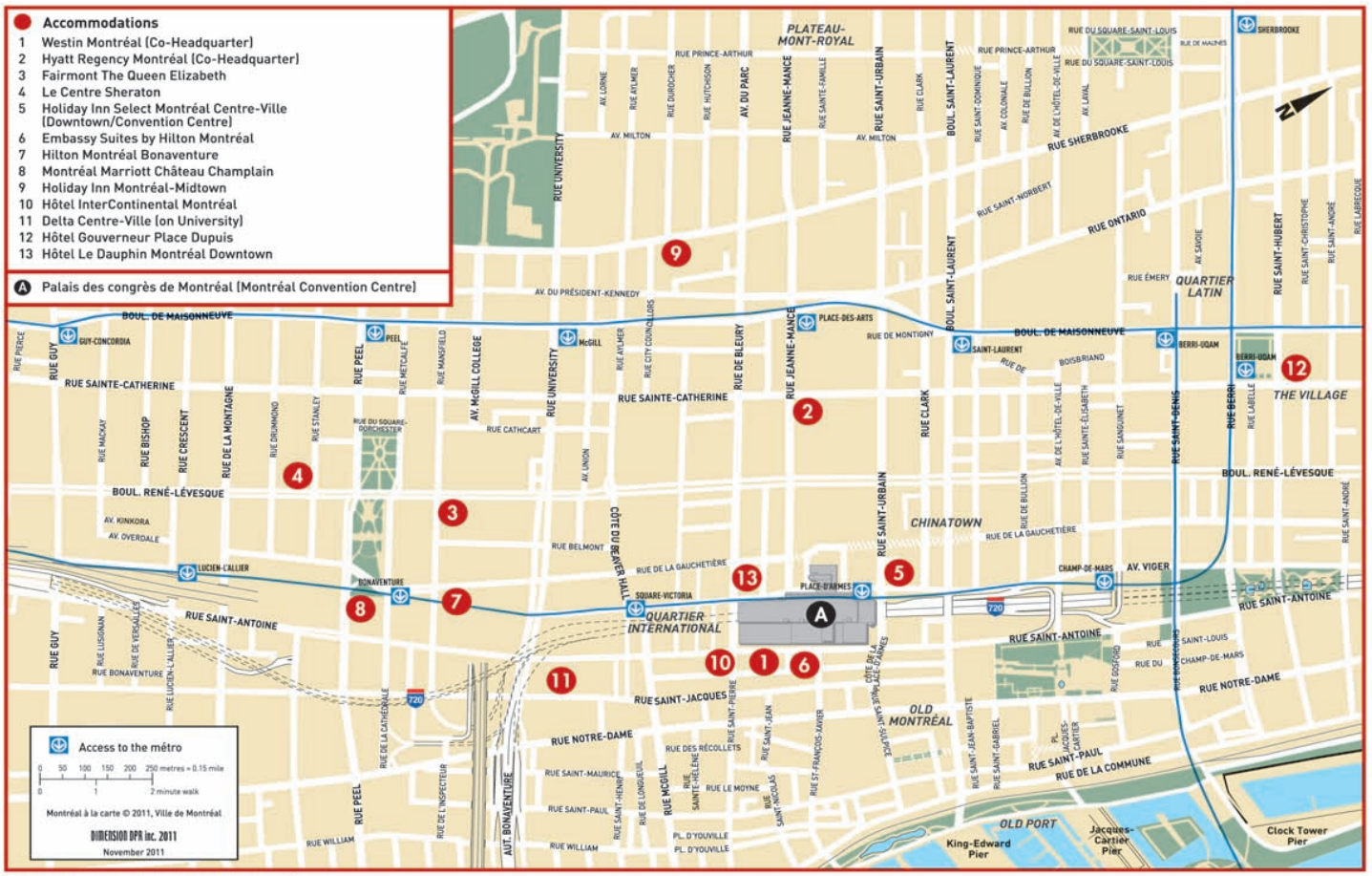
Government Rate King Bed Two Beds Wheelchair Accessible

Other Requests_____

If more than one room is required, attach a list of occupants names and the above information for each additional room.

ACCOMMODATIONS:

The IMS2012 has secured special rates for Attendees at the official IMS2012 hotels in Montréal. The map below shows the location and rates of these hotels. For advanced hotel reservations visit ims2012.mtt.org for online reservations, or submit the Attendee Housing Form by fax or postal mail before 14 May 2012.



DOWNTOWN MONTRÉAL

IEEE International Microwave Symposium 2012 – 17-22 June 2012

Palais des congrès de Montréal (Montréal Convention Centre)

Number on Map	Hotel Name	Rate
1	Le Westin Montréal (Headquarter)	$219 single/double $269 deluxe corner room $169 gov't rate
2	Hyatt Regency Montréal (Co-Headquarter)	$245 single/double $175 gov't rate
3	Fairmont Queen Elizabeth	$219 single/double $114.50 gov't rate
4	Le Centre Sheraton Montréal	$241 single/double $291 club level
5	Holiday Inn Select	$160 single/double $200 executive level $151 gov't rate
6	Embassy Suites Montréal	$221 single/double $199 gov't rate
7	Hilton Montréal Bonaven-ture	$220 single/double $195 gov't rate

Number on Map	Hotel Name	Rate
8	Marriott Chateau Champlain	$240 single/double
9	Holiday Inn Midtown	$154 single/double $145 government rate
10	Intercontinental	$229 single/double $264 triple $299 quad
11	Delta Centre-Ville	$195 single/double
12	Hotel Gouverneur	$139 single/double
13	Hotel Dauphin	$154 single/double

IMS - RFIC - ARFTG Registration Form

Montréal Canada, Palais des Congrès - 17-22 June 2012

1

All Early Bird and Advance registration must be received by 21 May and 15 June, respectively, for appropriate costs to apply.

online: http://ims2012.org/files/IMS2012_reg_form.pdf **by fax:** +1 (303) 530-4334

by mail: IMS2012, MP Associates, Inc.
Attn: Registration Desk
1721 Boxelder St., Ste. 107
Louisville, CO 80027 USA

2 Attendee Information

First Name

Last Name

Company

Mail Stop

Address:

Street

City

State

Postal Code

Country

Email

Telephone

IEEE Membership #

Member of: ❍ MTT-S ❍ ARFTG

Guest Information:

First Name

Last Name

Email

I would like to receive emails from: ❑ IEEE and MTT-S ❑ Industry

3 Attendee Survey

1) What is your principal job function?

- ❑ 101 Executive/Senior Management
- ❑ 102 Engineering Management
- ❑ 103 Design Engineering
- ❑ 104 Engineering Services
- ❑ 105 Manufacturing/Production Engineering
- ❑ 106 Application Engineer
- ❑ 107 Procurement/Purchasing
- ❑ 108 Professor/Research - Academic
- ❑ 109 Research & Development - Government
- ❑ 110 Research & Development - Industry
- ❑ 111 Student
- ❑ 112 Financial or Industry Analyst
- ❑ 113 Editor/Publisher
- ❑ 114 Marketing/Sales
- ❑ 115 Consultant
- ❑ 116 Retiree

2) What primary end product or service do you work on?

- ❑ 201 Communication systems, equipment
- ❑ 202 Wireless (WiFi, WiMAX, UWB)
- ❑ 203 Optoelectronics and Photonics
- ❑ 204 Government - Military
- ❑ 205 Government - Other
- ❑ 206 Defense Electronics
- ❑ 207 Medical Electronics
- ❑ 208 Navigation/telemetry/GPS systems
- ❑ 209 Industrial automation/control systems
- ❑ 210 Transportation (Automotive/Aviation)
- ❑ 211 Consumer Electronics
- ❑ 212 Computers or peripherals
- ❑ 213 Test & Measurement
- ❑ 214 Components/Hardware
- ❑ 215 Data Transmission
- ❑ 216 Semiconductors & Ics
- ❑ 217 Materials
- ❑ 218 Services
- ❑ 219 Software
- ❑ 220 Other_____

3) Which products and/or services in the following areas do you recommend, purchase or influence the purchase of?

(Answer all that apply)

- ❑ 301 Active Components
- ❑ 302 Antennas
- ❑ 303 Control Components
- ❑ 304 Materials
- ❑ 305 Manufacturing Equipment
- ❑ 306 Optoelectronics & Fiber-Optics
- ❑ 307 Passive Components
- ❑ 308 Semiconductors/Integrated Circuits
- ❑ 309 Services
- ❑ 310 Signal Processing Components
- ❑ 311 Software & CAD
- ❑ 312 Subsystems & Systems
- ❑ 313 Test Equipment and Instruments
- ❑ 314 Transmission-Line Components
- ❑ 315 Consultant Services

4) At what frequency is your primary work?

- ❑ 401 RF
- ❑ 402 Microwave
- ❑ 403 Millimeter-wave
- ❑ 404 Terahertz
- ❑ 405 Other_____

5) Number of engineers in your organization

- ❑ 501 10 or fewer
- ❑ 502 11 to 40
- ❑ 503 41 to 100
- ❑ 504 More than 100

6) Is this the first time you have attended International Microwave Week?

- ❑ 601 Yes
- ❑ 602 No

7) Are you an MTT member?

- ❑ 701 Yes
- ❑ 702 No

IMS provides an email list of attendees to exhibitors. If you do NOT want to receive this correspondence, check here: ❑

4 Registration Pricing

	Early Bird (1 Feb - 21 May) IEEE or ARFTG Membership Member	Early Bird (1 Feb - 21 May) IEEE or ARFTG Membership Student, Retiree, Life Member	Early Bird (1 Feb - 21 May) Non-Member	Advance (22 May - 15 June) IEEE or ARFTG Membership Member	Advance (22 May - 15 June) IEEE or ARFTG Membership Student, Retiree, Life Member	Advance (22 May - 15 June) Non-Member	Cost
Superpass							
All IMS, RFIC, & ARFTG Sessions, Awards Banquet, & All Workshop USB (RFIC/IMS) plus Full Day (or 2 Half Day) Workshop Attendance	❍$995	❍$595	❍$1,495	❍$1,155	❍$695	❍$1,730	$
IMS							
All IMS Sessions	❍$425	❍$75	❍$635	❍$495	❍$85	❍$740	$
Single Day Registration	❍$215		❍$320	❍$250		❍$370	$
Select day: ❍ Tuesday ❍ Wednesday ❍ Thursday							
RFIC Symposium							
All RFIC Sessions	❍$230	❍$160	❍$330	❍$260	❍$180	❍$380	$
ARFTG Conference							
All ARFTG Sessions	❍$220	❍$150	❍$330	❍$255	❍$175	❍$385	$
Exhibition							
Exhibition Only Pass	# x $25	# x $25	# x $25	# x $25	# x $25	# x $25	$
Wednesday Exhibition Only Pass	❍FREE	❍FREE	❍FREE	❍FREE	❍FREE	❍FREE	$
Guest Badge	❍$40	❍$40	❍$40	❍$40	❍$40	❍$40	$

5 Extra Proceedings & Digests

IMS Electronic Proceedings (EP) USB	# x $50		# x $75	# x $60		# x $90	$
RFIC Digest	# x $50		# x $75	# x $60		# x $90	$
RFIC EP USB	# x $50		# x $75	# x $60		# x $90	$
ARFTG EP USB	# x $50		# x $75	# x $60		# x $90	$

6 Events

Awards Banquet (Wednesday Night)	# x $55		# x $55	# x $65		# x $65	$
RFIC Reception Only	# x $30		# x $50	# x $40		# x $60	$

7 Lunch

	Mon	Tues	Wed	Thurs					
Boxed Lunches	❍	❍	❍	❍	# x $25		# x $25	# x $25	# x $25	$

8 Workshops and Short Courses Please select from the following:

Full Day Workshops: ❍WSA ❍WSB ❍WSC ❍WSD ❍WSE ❍WSF ❍WSG ❍WSK ❍WMA ❍WMC ❍WMD ❍WME ❍WMF ❍WMG ❍WMH ❍WMI ❍WFA ❍WFB ❍WFC ❍WFD

Half Day Workshops: ❍WSH ❍WSI ❍WSJ ❍WSL ❍WSM ❍WSN ❍WSO ❍WSP ❍WMB ❍WMJ ❍WMK ❍WML ❍WFE ❍WFF ❍WFG ❍WFH ❍WFI ❍WFJ ❍WFK ❍WFL

Full Day Short Course: ❍SC1 ❍SC3 ❍SC4 ❍SC5 ❍SC6

Half Day Short Course: ❍SC2 ❍SC7

Full Day Workshops	# x $165	# x $125	# x $245	# x $180	# x $135	# x $265	$
Half Day Workshops	# x $85	# x $65	# x $125	# x $95	# x $70	# x $140	$
Full Day Short Course	# x $285	# x $200	# x $425	# x $335	# x $235	# x $500	$
Half Day Short Course	# x $200	# x $140	# x $300	# x $235	# x $165	# x $350	$
Printed Notes	# included	# included	# included	# x $20	# x $20	# x $30	$
2 Full day workshops or equivalent - *(includes All 3 Days of Workshop USBs)*	# $435	# x $325	# x $645	# x $475	# x $355	# x $700	$

9

Card Number ☐☐☐☐ ☐☐☐☐ ☐☐☐☐ ☐☐☐☐ Expiration Date ☐☐/☐☐ Total Remittance: $

❍MasterCard ❍Visa ❍American Express Security Code ☐☐☐☐ **Signature:**_____

10 Submit via Fax or Mail to:

Make checks payable to: **IMS2012**

IMS2012, MP Associates, Inc.
Attn: Registration Desk
1721 Boxelder St., Ste. 107
Louisville, CO 80027 USA

Fax registrations accepted with credit card payment only!
Phone Number: (303) 530-4562
Fax Number: (303) 530-4334

Refund Policy: Written requests for cancellations received on or before 21 May 2012 will be honored. Cancellations received after 21 May 2012 will NOT be honored and all registration fees will be forfeited.
After 8 June 2012, faxed registrations will not be accepted in office - You MUST register on-site.
TELEPHONE REGISTRATIONS WILL NOT BE ACCEPTED! ANY REGISTRATION WITOUT PAYMENT WILL BE DISCARDED! If payment is received from a non-US bank, attendees will be charged a collection fee of $45.00.