2011 IEEE Radio Frequency Integrated Circuits Symposium

Baltimore, Maryland

5-7 June 2011

IEEE

PROGRAM

Baltimore Convention Center

Sponsored by

IEEE Microwave Theory and Techniques Society

IEEE Electron Device Society

and

The IEEE Solid-State Circuits Society

RFIC Plenary and Reception
Sunday Evening (5 June 2011)

After a busy day of excellent RFIC Workshops (see page 64- 80) the Plenary Session and RFIC Reception will be held in Sunday evening – 5 June 2011. The Plenary Session starts at 5:40PM in the Baltimore Convention Center (BCC), Level 400, Ballroom III-IV. The Plenary Session will include two outstanding speakers (see pages 8-9), RFIC Service Recognition and Student Paper Awards ceremony. Immediately following the RFIC Plenary Session is the famous RFIC Reception in the adjacent Ballroom I-II. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on latest news in the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The RFIC Reception is sponsored by the RFIC Steering Committee, our Platinum (RFMD) and Gold (Skyworks) sponsors.

Platinum RFMD®

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RFIC Week Activities (5-7 June 2011)

Saturday, 4 June 2011

2:00 PM – 6:00 PM	Registration – BCC

Sunday, 5 June 2011

7:00 AM – 6:00 PM	Registration - BCC
7:00 AM – 8:00 AM	Workshop Breakfast – BCC, Level 300, Foyer
8:00 AM – 5:20 PM	Workshops and Tutorials - BCC
5:40 PM – 7:00 PM	RFIC Plenary – BCC, Level 400, Ballroom III-IV
7:00 PM – 9:00 PM	RFIC Reception - BCC, Level 400, Ballroom I-II

Monday, 6 June 2011

6:30 AM – 8:30 AM	Speakers Breakfast – BCC, Level 400, Ballroom I-IV
7:00 AM – 9:00 AM	Attendee Breakfast – BCC, Level 300, Foyer
7:00 AM – 5:00 PM	Registration – BCC
8:00 AM – 9:40 AM	RMO1A RMO1B RMO1C RMO1D
10:00 AM – 11:40 AM	RMO2A RMO2B RMO2C RMO2D
Noon – 1:20 PM	RFIC Panel and Lunch - BCC, 307-308
2:20 PM – 3:40 PM	RMO3A RMO3B RMO3C RMO3D
4:00 PM – 5:20 PM	RMO4A RMO4B RMO4C RMO4D

Tuesday, 7 June 2011

6:30 AM – 8:30 AM	Speakers Breakfast – BCC, Level 400, Ballroom I-IV
7:00 AM – 9:00 AM	Attendee Breakfast – BCC, Level 300, Foyer
7:00 AM – 5:00 PM	Registration – BCC
8:00 AM – 9:40 AM	RTU1A RTU1B RTU1C
10:00 AM – 11:40 AM	RTU2A RTU2B RTU2C
Noon – 1:20 PM	RFIC Panel and Lunch - BCC, 307-308
Noon – 2:00PM	RTUIF – BCC, Hall A

This Program can be found on the RFIC website http://www.rfic2011.org. IMS sessions and exhibits are held on Tuesday - Thursday. IMS program can be found on the IMS website www.ims2011.org.

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The RFIC Symposium will be held in Baltimore, Maryland at the Baltimore Convention Center (BCC) on 5-7 June 2011 in conjunction with the International Microwave Symposium. It opens Microwave week 2011, the largest RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF Systems, circuit device, and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Welcome Message from Chairpersons

On behalf of the Steering Committee, We would like to welcome you to the 2011 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, which will take place in Baltimore, Maryland 5-7 June, 2011. Our Symposium, held in conjunction with the IEEE MTT-S International Microwave Symposium, opens Microwave Week 2011, the largest world-wide RF/Microwave meeting of the year.

The 2011 RFIC Symposium continues to build upon its heritage as one of the foremost IEEE technical conferences, increasing each year its impact and reputation of excellence. By bringing focus to the technical accomplishments in RF circuits, systems, and devices, the RFIC Symposium has become essential to both the academic and the industrial communities. This year's exciting technical program will showcase the latest innovations in RF integrated circuit design with sessions that cover a broad spectrum of topics from cellular and wireless-connectivity system ICs, broadband wireless communications, digitally enhanced RF circuits, silicon millimeter-wave ICs, and RF device technology, modeling, and characterization. Applications highlighted by the technology include mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Running in conjunction with the International Microwave Symposium and Exhibit, the RFIC Symposium adds to the excitement of the Microwave Week with three days focused exclusively on RFIC technology and innovation.

The 2011 RFIC Symposium will start on Sunday with half-day and full-day workshops covering a wide array of topics. Some of the topics include: New Architectures for Digitized Receivers, RFIC for Bio-Medical Applications, Imaging at mm-wave and beyond, Cognitive Radios and Spectrum Sensing, Advancements in Linear Power Amplifiers, Efficiency Enhancement Techniques for Power Amplifiers and Transmitters, Advancements and Challenges Toward Radio-in-package and Radio-on-chip, Re-configurability Requirements for Multi-standard, Low-Power Operation, and EMI compliant product design practices.

The conference also includes a Plenary Session, which is held on Sunday evening. Keynote addresses will be given by two renowned leaders from in the wireless industry. Both of them will share their views and insights on the direction and challenges that the RF IC design community is facing. The first speaker is the Chief Technical Officer and Co-Founder of Telegent Systems, Dr. Samuel Sheng, who will discuss ***"RF Coexistence - Challenges and Opportunities"***. The second speaker is Mr. Ron Ruebusch, Vice President of R&D of Wireless Semiconductor Division of Avago Technologies. He will discuss ***"3G to 4G Transition – Challenges and Opportunities"***. In addition to the keynote addresses, the conference holds a student paper competition to encourage the publication of innovative research from university students. Consequently, best student paper awards are presented in the Plenary Session to acknowledge these contributions. The highly anticipated RFIC Reception will follow immediately after the Plenary Session, providing a relaxing time for all to mingle with old friends and catch up on the latest news.

On Monday and Tuesday, the conference will feature lunch-time panel sessions that traditionally draw strong debate between panel members as well as stimulating interaction between attendees and panelists. The Monday panel session is entitled ***"Software Defined***

Radios – Facts and Fantasies" while the Tuesday panel session is entitled ***"What is the limit of multi-radio integration… or rather, is it 'disintegration'?"*** Be sure to attend these lively and entertaining forums.

Technical papers will be presented during oral sessions throughout Monday and Tuesday. There will be a total of 129 papers presented in 23 technical focused sessions. On Tuesday's afternoon, our interactive Forum (RTUIF) will feature 31 poster papers and give our attendee a chance to speak directly with authors regarding their work.

The RFIC organization is thankful to the IMS2011 team's strong support for making this conference successful. Most of all, we are particularly thankful to all the technical contributors to the RFIC Symposium. We look forward to your participation. Please continue to make this conference so vibrant within the wireless industry!

We look forward to seeing you in Baltimore!

David Ngo
General Chairman

Albert Jerng
TPC Chairman

Chris Rudell
TPC Co-Chairman

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RFIC Schedule 2011

The RFIC Symposium will be held in Baltimore, MD in the Baltimore Convention Center (BCC). The headquarters hotels are the Hyatt Regency Baltimore and Hilton Baltimore Convention Center Hotel which are adjacent to the BCC. The RFIC Plenary and Reception will be held on Sunday, 5 June 2011 starting at 5:40 PM.

The RFIC Symposium is held as part of Microwave week. It is followed by the IMS Symposium and Exhibition and by ARFTG. Attendees of RFIC are invited to attend the IMS Plenary Session which will be held on Tuesday's Evening, 7 June 2011.

Saturday, 4 June 2011

2:00 PM – 6:00 PM	Registration - ACC

Sunday, 5 June 2011

6:30 AM – 8:30 AM	Speakers Breakfast – BCC, Level 400, Ballroom I-II
7:00 AM – 8:00 AM	Workshop Breakfast – BCC, Level 300, Foyer
7:00 AM – 6:00 PM	Registration - BCC
8:00 AM – 5:20 PM	Workshops and Tutorials - BCC
5:40 PM – 7:00 PM	RFIC Plenary – BCC, Level 400, Ballroom III-IV
7:00 PM – 9:00 PM	RFIC Reception - BCC, Level 400, Ballroom I-II

Monday, 6 June 2011

6:30 AM – 8:30 AM	Speakers Breakfast – BCC, Level 400, Ballroom I-IV
7:00 AM – 9:00 AM	Attendee Breakfast – BCC, Level 300, Foyer
7:00 AM – 5:00 PM	Registration – BCC
8:00 AM – 9:40 AM	RMO1A RMO1B RMO1C RMO1D
10:00 AM – 11:40 AM	RMO2A RMO2B RMO2C RMO2D
Noon – 1:20 PM	RFIC Panel and Lunch - BCC, 307-308
1:00 PM – 2:00 PM	RFIC TPC Lunch Meeting – Hilton Baltimore, Holiday 4
2:20 PM – 3:40 PM	RMO3A RMO3B RMO3C RMO3D
4:00 PM – 5:20 PM	RMO4A RMO4B RMO4C RMO4D

Tuesday, 7 June 2011

6:30 AM – 8:30 AM	Speakers Breakfast – BCC, Level 400, Ballroom I-IV
7:00 AM – 9:00 AM	Attendee Breakfast – BCC, Level 300, Foyer
7:00 AM – 5:00 PM	Registration – BCC
8:00 AM – 9:40 AM	RTU1A RTU1B RTU1C
10:00 AM – 11:40 AM	RTU2A RTU2B RTU2C
Noon – 1:20 PM	RFIC Panel and Lunch - BCC, 307-308
Noon – 2:00PM	Interactive Forum – BCC, Hall A
1:00 PM – 2:00 PM	RFIC Steering Committee Lunch Meeting – Hilton Baltimore, Key 9

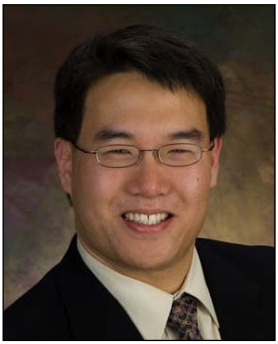
Plenary Schedule

Sunday, 5 June 2011
5:40 PM
Baltimore Convention Center – Level 400, Ballroom III-IV
Session RSU5A: RFIC Plenary

Chair: David Ngo – RFMD, Inc.
Co-Chairs: Albert Jerng – Ralink Technology
Jacques C. Rudell - Univ. of Washington

5:40 PM	Welcome Message from General and TPC Chairs, RFIC Distinguished Service and Student Paper Awards
6:00 PM	RSU5A-1: "RF Coexistence – Challenges and Opportunities", Samuel Sheng, Telegent Systems
6:30 PM	RSU5A-2: "3G to 4G Transition – Challenges and Opportunities", Ron Ruebusch, Avago Technologies

7:00 PM
Baltimore Convention Center – Level 400, Ballroom I-II
Session RSU5B: RFIC Reception



Plenary Speaker 1:

Samuel Sheng
Chief Technical Officer and Co-Founder
Telegent Systems

RF Coexistence – Challenges and Opportunities

Abstract: The explosion in wireless technologies over the past ten years has been nothing short of staggering. WiFi, Bluetooth, ZigBee, ultrawideband, GPS, wireless HDMI, 60 GHz, and 2/3/4G cellular, along with mainstays such as FM radio and broadcast television, have become ubiquitous in consumer devices. The presence of multiple RF transceivers within a single device is now the norm, not the exception. Over the next ten years, the key challenge will shift from simply enabling wireless connectivity to enabling multiple wireless technologies to coexist at the same time in the same device, along with surviving the electromagnetic interference issues caused by the increasing complexity of such devices. While today's devices already feature several transceivers operating simultaneously, over the next ten years the problem will grow exponentially. It is projected that up to 10 RF transceivers may be active at any one time in a cellular handset, covering a frequency range anywhere from 100 MHz up to 3 GHz. This swath of spectrum is also broad enough that these radios will need to reject interference from a plethora of sources, such as microprocessors, switching regulators, LCD backlights, and touch panels. Likewise, the continuing march toward further integration will result in RF coexistence issues not only within devices, but within a single piece of silicon.

To effectively deal with this issue, many techniques will need to be developed and deployed to attack the problem in a disciplined fashion. Active interference mitigation, currently an area of research, will become a mainstay in devices and silicon. Time synchronization between radios of different standards, will become standard practice. Local oscillator and frequency planning between multiple radios will become a necessary design methodology. While currently uncommon, such techniques represent a major aspect in the development of RF technologies over the next decade.

About Samuel Sheng

Dr. Sheng received his BS, MS, and PhD degrees in electrical engineering, and the BA degree in applied mathematics, all from the University of California, Berkeley. Over the past 15 years, he has been involved with architecting and designing leading-edge CMOS RF and DSP chips for silicon tuners, ADSL transceivers, and DVD RF/servo technologies. In 2004, he co-founded Telegent Systems with the vision to develop complex next-generation RF SOC's such as single-chip televisions, and Dr. Sheng currently serves as Telegent's Chief Technical Officer.

Prior to co-founding Telegent Systems, Dr. Sheng was at LSI Logic and responsible for architecting and implementing a series of silicon RF tuners for video-band applications, targeted for cable modems, analog/digital video over cable, and voice over IP as well as highly integrated DVD front-end technologies. Before LSI Logic, Dr. Sheng co-led the ADSL front-end (AFE) development effort at Datapath Systems, Inc. Dr. Sheng was awarded Inventor of the Year at LSI Logic in 2002 and 2003 and was named the 2002 Distinguished Engineer at LSI Logic. He has authored numerous papers and publications on various topics such as low-power CMOS RF wireless systems and low-power CMOS digital design. He has been awarded twelve patents in the areas of RF tuner and DSL modem design.

Plenary Speaker 2:

Ron Ruebusch
Vice President of R&D of the Wireless Semiconductor Division
Avago Technologies

3G to 4G Transition – Challenges and Opportunities

Abstract: The cell phone industry is starting the transition from 3G to 4G networks. In this process, the number of bands that 4G radios have to accommodate is growing rapidly. As the suppliers of radio devices to the cell phone industry, the RFIC world is being challenged to provide a proliferation of new designs in a timely fashion. Without unlimited budgets, managers are being compelled to become more efficient in their product development. At the same time, as the spectrum gets more crowded emerging co-existence issues are becoming apparent which further complicate the RF front end. Lastly, our customers want increased functionality in ever smaller form factors which also raises thermal challenges. How are the successful players in this business going to successfully navigate this transition, what capabilities are required, and where are the opportunities for faster than market growth?

About Ron Ruebusch

Mr Ruebusch is the Vice President of R&D of the Wireless Semiconductor Division of Avago Technologies where he has been working for the last seven years. In that capacity he manages all of the RFIC product development in Avago with a team of several hundred engineers in four major locations around the world. He has over 35 years experience in the communications industry, 30 of which are in semiconductors and the last 20 of which have been in the RF segment. His background includes a broad range of executive responsibilities from division general management, marketing, sales, and R&D.

Monday, 6 June 2011
8:00 AM
Room 337-338
Session RM01A: Wireless Data Transceiver Architectures and Techniques

Chair: Julian Tham, Broadcom
Co-Chair: Li Lin, Marvell

RM01A-1 8:00 AM
A 2.4GHz 2Mb/s Digital PLL-based Transmitter for 802.15.4 in 130nm CMOS

M. Ghahramani[1], M. P. Flynn[1], M. A. Ferriss[2], [1]University of Michigan, Ann Arbor, United States, [2]IBM T. J. Watson Research Center, Yorktown Heights, United States

Abstract: A fully integrated 2.4GHz transmitter for 802.15.4 based on a digital ΣΔ fractional-N PLL is presented. A self-calibrated two-point modulation scheme enables modulation rates much larger than the loop bandwidth. An oversampled 1-bit quantizer is used as a phase detector, avoiding spurs and nonlinearity associated with some TDC-based digital PLLs. The prototype achieves an MSK modulation rate of 2Mb/s, delivers -2dBm of output power, and is free of in-band fractional spurs.

RM01A-2 8:20 AM
Full-Duplex Crystal-less CMOS Transceiver with an On-chip Antenna for Wireless Communication in Engine Controller Board of Hybrid Electric Vehicles

K. Oh[1], S. Sankaran[1], H. Wu[1], J. Lin[1], M. Hwang[1], K. O[2], [1]Silicon Microwave Integrated Circuits Research Group (SIMICS), Gainesville, United States, [2]Texas Analog Center of Excellence, Richardson, United States

Abstract: A full-duplex transceiver for wireless inter-chip data communication in an engine controller board of hybrid electric vehicles that for the first time integrates an on-chip antenna and a duplexer, as well as allowing operation without a crystal frequency reference is demonstrated. The BER degradation of RX due to the TX operation is negligible when the input power is greater than -44dBm necessary to achieve BER of less than 10-12. The transceiver fabricated in 0.13μm CMOS consumes 245mW.

RMO1A-3 8:40 AM
A Fully Integrated 802.11n Radio with 24GHz Harmonic LO Generation for Low-cost, Low Power, Multi-standard Systems

R. Sadhwani[1], O. Degani[2], A. Ben-Bassat[2], R. Banin[2], H. Shang[1], B. Jann[1], [1]Intel Corporation, Hillsboro, United States, [2]Intel Corporation, Haifa, Israel

Abstract: We report a novel harmonic LOG based direct conversion RF transceiver for 802.11n radio. This multi-comm transceiver consists of Bluetooth SoC and WiFi, it includes 19-24GHz VCO, integrated front-end including WiFi T/R and WiFi-BT switches. Fabricated in 90nm digital CMOS technology, this IC consumes 422/560mW (Rx/Tx 802.11n 300/150Mbps), 110mW in BT mode, with an area of approx 19mm². A peak saturated power of 24/9dBm is achieved at antenna in WiFi/BT mode.

RMO1A-4 9:00 AM
Digital RF Receiver Front-end with Wideband Operation Capability for m-WiMAX

H. Seo[1], I. Choi[1], C. Park[2], J. Yoon[2], B. Kim[1], [1]Pohang University of Science and Technology, Pohang, Republic of Korea, [2]Samsung Electronics, Suwon, Republic of Korea

Abstract: A Digital RF receiver front-end with wideband operation capability is presented for m-WiMAX application. By employing sampling mixer and discrete-time filter, the receiver operates in charge domain. In addition to flexibility of the discrete-time (DT) filter, the new Non-Decimation Finite Impulse Response (FIR) filter can be cascaded to a conventional FIR filter. And we can easily increase the order of the sincn-type filtering response to achieve wideband signal process capability.

RMO1A-5 9:20 AM
A QPLL-Timed Direct-RF Sampling Band-Pass ΣΔ ADC with 1.2GHz Tuning Range in 0.13μm CMOS

S. Gupta[1], D. Gangopadhyay[1], H. Lakdawala[2], J. C. Rudell[1], D. J. Allstot[1], [1]University of Washington, Seattle, United States, [2]Intel Corporation, Hillsboro, United States

Abstract: A direct-RF sampled band-pass ΣΔ modulator implemented in 0.13μm CMOS enables reconfigurable RF A/D conversion. It features a programmable narrow-band Q-enhanced low-noise amplifier and a phase-locked loop with quadrature outputs synchronized with the ADC. It consumes 41mW and achieves an SNDR of 40-50dB and IIP3 of -5/-7dBm over the 0.8-2GHz frequency band. Measured PLL phase noise is -113dBc/Hz at a 1MHz offset frequency with a -74.5dBc spur; RMS period jitter is 1.38ps.

Monday, 6 June 2011
8:00 AM
Room 339-340
Session RMO1B: Digital to RF and Sigma-Delta Transmit Modulators
Chair: Noriharu Suematsu, Tohoku University
Co-Chair: Gernot Hueber, NXP Semiconductors

RMO1B-1 8:00 AM
All-Digital Transmitter based on ADPLL and Phase Synchronized Delta Sigma Modulator
J. Chen, L. Rong, F. Jonsson, L. Zheng, Royal Institute of Technology (KTH), Stockholm, Sweden

Abstract: A novel architecture of all-digital polar transmitters is proposed, mainly composed of an ADPLL for phase modulation, a low-pass Sigma Delta modulator for envelope modulation and a class-D PA. The low noise ADPLL and high oversampling rate relief filter design, enabling the use of a on-chip filter. The differential coding scheme enhances the fundamental tone and suppresses the DC and high harmonics. It was fabricated in a 90nm CMOS process, occupying 1.4 mm². Measurements justify the concept.

RMO1B-2 8:20 AM
A 0.7-3GHz Envelope Delta-sigma Modulator Using Phase Modulated Carrier Clock for Multi-mode/band Switching Amplifiers
S. Hori, K. Kunihiro, K. Takahashi, M. Fukaishi, NEC Corporation, Kawasaki, Japan

Abstract: A 1-bit RF modulator using phase-modulated-carrier-clocking envelope delta-sigma modulation for a multi-mode/band transmitter is presented. The prototype IC designed in 90nm CMOS process covers 2.4GHz ISM and 3GPP frequency bands up to 3GHz in conformity with IEEE 802.11g, W-CDMA and LTE in 5MHz-mode. The IC dissipates 8mW for 1.95GHz WCDMA and occupies 0.044mm².

RMO1B-3 8:40 AM
A 12-bit Resolution, 200-MSample/second Phase Modulator for a 2.5GHz Carrier with Discrete Carrier Pre-Rotation in 65nm CMOS
T. W. Barton, S. Chung, P. A. Godoy, J. L. Dawson, Massachusetts Institute of Technology, Cambridge, United States

Abstract: A digital-to-RF phase modulator based on a single current-steering DAC is presented, including a carrier pre-rotation scheme that prevents phase inaccuracy due to carrier feedthrough. The phase modulator has been fabricated in a standard 65nm CMOS process and draws 1.9mW from a 1V supply. The modulator achieves 12bit resolution at a measured 200MSamples/second, state-of-the-art performance in both resolution and sampling speed.

RMO1B-4 9:00 AM
A Direct Sampling Mixer with Complex Coefficient Transfer Function in 65nm CMOS

Y. Morishita[1], T. Morita[1], N. Saito[1], K. Araki[2], [1]Panasonic Corporation, Yokohama, Japan, [2]Tokyo Institute of Technology, Tokyo, Japan

Abstract: The Direct Sampling Mixer (DSM) with complex coefficient transfer function is demonstrated. The operation theory and the detail design methodology are discussed for the 2-pararell architecture, which can achieve large image rejection by introducing the attenuation pole at the image frequency. The proposed architecture was fabricated in a 65nm CMOS process. The measured results agree well with the theory, which proves the validity of the proposed architecture and the design methodology.

RMO1B-5 9:20 AM
Multiband Mixed-Signal Vector Modulator IC

U. Mayer, M. Wickert, R. Eickhoff, F. Ellinger, Technische Universitaet Dresden, Dresden, Germany

Abstract: This paper presents an active BiCMOS vector modulator suitable for WLAN diversity transceivers. It features a LNA, a SPI and 8-bit DACs for vector control and internal references and thus is suitable as a monolithic IC for RF signal weighting. When mounted on a PCB, it delivers a maximum gain of 12dB at 5.6GHz. It draws a current of 17mA from a 3.3V supply. The whole design is free of bulky inductors thus requiring an area of only 1.3 mm².

Monday, 6 June 2011
8:00 AM
Room 341-342
Session RMO1C: mm-Wave Communication Systems
Chair: Luciano Boglione , SSSC/AFRL
Co-Chair: Georg Boeck, Berlin Institute of Technology

RMO1C-1 8:00 AM
Indoor and Outdoor mm-Wave Systems and RF/BB SoCs (Invited Paper)
A. Matsuzawa, K. Okada, Tokyo Institute of Technology, Meguro-ku, Japan

Abstract: This paper gives an overview of the mm-Wave Project to realize the indoor and the outdoor systems over Gbps by developing CMOS RF and Baseband SoCs. A 60GHz direct conversion transceiver was developed using 65nm CMOS and demonstrates 7Gbps using 16QAM. A quadrature VCO attained very low phase noise of -94dBc/Hz @1MHz. For the outdoor system (1km), a baseband mixed signal SoC using 90nm CMOS was developed and demonstrates 600Mbps with 16QAM in 38GHz (BW: 260MHz) band.

RMO1C-2 8:20 AM
A 60-GHz RF IQ DAC Transceiver with on-Die at-Speed Loopback
E. Laskin, A. Tomkins, A. Balteanu, I. Sarkas, S. P. Voinigescu, University of Toronto, Toronto, Canada

Abstract: A transceiver with direct 5.3Gb/s carrier modulation using a 60GHz 2-bit IQ DAC, a zero-IF IQ receiver, a PLL with a single 60GHz VCO and an integrated crystal oscillator, was designed and fabricated in a 130nm SiGe BiCMOS technology. It covers the entire 57-66 GHz band with digitally-programmable 0 to 10 dBm output power and -15 to 60 dB receiver gain, and 5-6dB noise figure. Depending on the receive-path gain, the IP1 varies between -55 and 0dBm. The chip consumes 350/225mW in TX/RX mode.

RMO1C-3 8:40 AM
A 60GHz Digitally Controlled RF Beamforming Array in 65nm CMOS with Off-Chip Antennas
S. Lin[1], K. Ng[2], H. Wong[2], K. Luk[2], S. Wong[1], A. Poon[1], [1]Stanford University, Stanford, United States, [2]City University of Hong Kong, Hong Kong, China

Abstract: An RF path 60GHz band 4element array using proposed phase-oversampling vector modulation is implemented in 65nm CMOS. Digital controlled semi-lookup table method is proposed to compensate for non-idealities in circuits, antenna array, and interfaces. Accurate and high resolution control on the gain and phase is demonstrated. The receiver features an NF of 5.6 dB and 3.5° phase resolution at a backoff of 3dB. It dissipates 178mW from 1V supply and obtains 18.5dB gain for each channel.

RMO1C-4 9:00 AM
A 60dB Gain and 4dB Noise Figure CMOS V-Band Receiver Based on Two-Dimensional Passive Gm-Enhancement

N. Wang[1], H. Wu[1], J. Y. Liu[1], J. Lu[1], H. Hsieh[2], P. Wu[2], C. Jou[2], M. F. Chang[1], [1]University of California Los Angeles, Los Angeles, United States, [2]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan

Abstract: A direct conversion receiver which consists of LNA, mixer and programmable gain amplifier (PGA) for V-band (60GHz) applications is designed and realized in 65nm CMOS. A novel two-dimensional passive gm-enhancement technique is devised to boost the conversion gain and lower the Noise Figure (NF) with insignificant power overhead. An overall minimum SSB NF of 3.9dB and a maximum power conversion gain of 60dB is achieved with an area of 0.2mm² and 34mW of power dissipation.

RMO1C-5 9:20 AM
A 220GHz Subharmonic Receiver Front End in a SiGe HBT Technology

E. Ojefors[1], B. Heinemann[2], U. R. Pfeiffer[1], [1]University of Wuppertal, Wuppertal, Germany, [2]IHP GmbH, Frankfurt (Oder), Germany

Abstract: A monolithic 220GHz receiver front end manufactured in an engineering version of a fT/fmax = 280/435-GHz SiGe technology is presented. The front end consists of a three-stage differential LNA and a subharmonic mixer. A breakout of the 220GHz LNA provides 15dB gain and a bandwidth of 28GHz. The integrated downconverter yields a conversion gain of 15dB, a 15dB DSB NF, and a 30GHz bandwidth when pumped with a 0dBm, 110GHz LO signal.

Monday, 6 June 2011
8:00 AM
Room 343-344
Session RMO1D: Frequency Synthesis: 60GHz and Beyond
Chair: Stefano Pellerano, Intel Corp.
Co-Chair: Jaber Khoja, Zoran

RMO1D-1 8:00 AM
A 60GHz Wideband Injection-Locked Frequency Divider with Adaptive-Phase-Enhancing Technique
H. Wang[1], L. Zhang[1], D. Yang[1], D. Zeng[2], L. Zhang[1], Y. Wang[1], Z. Yu[1], [1]Tsinghua University, Beijing, China, [2]Chinese Academy of Sciences, Suzhou, China

Abstract: A 60GHz injection-locked frequency divider (ILFD) with quadrature outputs is designed in 90nm CMOS technology. An adaptive coupling scheme is proposed to enlarge the phase shift for a wideband locking range. The measured results exhibit an input locking range of 12.1GHz or 20.5% from 52.7 to 64.8GHz at an incident power of 0dBm. The core circuit consumes 8.6mW from a 1.2V power supply and occupies an area of 360x230μm.

RMO1D-2 8:20 AM
A 100GHz Phase-Locked Loop in 0.13μm SiGe BiCMOS process
S. Kang, J. Chien, A. M. Niknejad, University of California at Berkeley, Berkeley, United States

Abstract: A fully integrated 100GHz PLL is demonstrated in 0.13μm SiGe BiCMOS process. The PLL employs a fundamental-frequency differential Colpitts voltage-controlled oscillator with 8.3% tuning range, which achieves a phase noise of -124.5dBc/Hz at 10MHz offset, and a single-ended output power of 3dBm. The total lock range of the PLL is from 92.7 to 100.2GHz, the phase noise is -102dBc/Hz at 1MHz offset, and reference spurs are not observable. The PLL dissipates 570mW and occupies 1.21mm².

RMO1D-3 8:40 AM
W-Band Frequency Synthesis Using a Ka-Band PLL and Two Different Frequency Triplers
Z. Chen, C. Wang, P. Heydari, University of California, Irvine, Irvine, United States

Abstract: Two chips for 96GHz frequency generation employ the same Ka-band PLL and (1) an injection-locked frequency tripler; (2) a harmonic-based frequency tripler in 0.18μm SiGe BiCMOS are presented. The ILFT and HBFT preceded by the same Ka-band PLL achieve measured phase noise of -93dBc/Hz and -92dBc/Hz at 1MHz offset, respectively. Both chips have the same power consumption of 140mW from 1.8V/2.5V supplies.

RMO1D-4 9:00 AM

60GHz CMOS Divide by 5 Injection-Locked Frequency Divider with an Open-Stub-Loaded Floating-Source Injector

M. Li, H. Kuo, T. Huang, H. Chuang, National Cheng Kung University, Tainan, Taiwan

Abstract: A new injector topology is adopted for the design of a 60GHz divide-by-5 injection-locked frequency divider (ILFD). The topology is based on a distributed-element harmonic termination by an open-stub structure connected to the floating source end of the injection pair. With this topology together with an NMOS cross-coupled oscillator core, the supply voltage and power consumption of the ILFD can be greatly reduced, and the locking range of the designed ILFD has been greatly extended by over 70%.

Monday, 6 June 2011
10:00 AM
Room 337-338
Session RMO2A: WiMedia UWB and IR-UWB Receivers and Transmitters

Chair: Domine Leenaerts, NXP Semiconductors
Co-Chair: Yann Deval , IMS Lab

RMO2A-1 10:00 AM
A 65nm CMOS Low-Noise Three Band Group WiMedia UWB Receiver

W. Ko, H. Shin, S. Ko, J. Yim, B. Kang, T. Kim, I. Ryu, S. Yang, J. Bae, H. Park, Samsung Electronics Co., Ltd, Yongin, Republic of Korea

Abstract: A low-noise and high-gain ultra wideband (UWB) receiver was developed using a 65nm CMOS technology. In order to enhance the gain and noise figure, the resistive feedback amplifier and two cascode stages with the inductive load resonating at three different frequencies are employed. The fabricated UWB receiver showed an average high gain of 72.6dB and a noise figure of 4.1-5.8dB in three band groups. The measured sensitivities in three band groups meet all WiMedia PHY specifications.

RMO2A-2 10:20 AM
A WiMedia UWB Transmitter up to 9GHz in 65nm CMOS and Wafer-level Fabricated Package

J. Yim, B. Kang, T. Kim, W. Ko, H. Shin, S. Ko, I. Ryu, S. Yang, J. Bae, H. Park, Samsung Electronics, Yongin, Republic of Korea

Abstract: A 3.1-4.7GHz and 6.3-9GHz RF transmitter fabricated in a 65nm CMOS technology and packaged with a Wafer-level Fabricated Package (WFP) is presented. For high frequency and wideband performances, all the effects of package are considered and loopback paths with a power detector are implemented. A new structure of T/R switch is devised for the low noise performance of Rx and the high linearity of Tx. With these circuits, the transmitter features high linearity, low power consumption.

RMO2A-3 10:40 AM
Low Power, Fully Differential SiGe IR-UWB Transmitter and Correlation Receiver ICs
D. Lin, A. Trasser, H. Schumacher, Ulm University, Ulm, Germany

Abstract: In this paper a 3.1-10.6 GHz impulse-radio ultra-wideband (IR-UWB) transmitter and a correlation receiver are presented. The transmitter comprises a differential impulse generator mounted chip-on-board on a dipole fed circular slot antenna. The receiver front-end, mounted at the feed-point of another dipole antenna, is realized with a differential low noise amplifier, an analog correlator and a template impulse generator. Measurement results show a motion tracking capability in the mm range.

RMO2A-4 11:00 AM
A 520pJ/pulse IR-UWB Radar for Short Range Object Detection
Y. Shim, S. Yuwono, S. Kim, J. Kim, S. Han, S. Lee, KAIST, Daejeon, Republic of Korea

Abstract: This paper presents a low power, low complexity IR-UWB radar transceiver for short range object detection. The transceiver provides robustness against false detections without increasing power consumption, chip size, or complexity. The receiver and the transmitter dissipate only 50 and 470pJ/pulse, respectively. The measured TX pulse spectrum shows -58dBm maximum power and 1GHz bandwidth with 4GHz center frequency. The sensitivity is -45dBm, and the measured RX is fully functional for detecting.

RMO2A-5 11:20 AM
A Self-Synchronized, Crystal-less, 86µW, Dual-Band Impulse Radio for Ad-Hoc Wireless Networks
X. Y. Wang, R. K. Dokania, Y. Zhuang, C. I. Dorta-Quinones , W. Godycki, M. Lyons, A. B. Apsel, Cornell University, Ithaca, United States

Abstract: An 86µW, 150Kbps, self synchronizing 3.5-4.5GHz UWB IR transceiver is presented. Synchronous receiver duty cycling of 0.5% is enabled without a crystal through a pulse coupled oscillator (PCO) network that establishes timing and allows multi-node multi-hop communication. The synchronization scheme is supported by implementation of a low power oscillator and timing circuits to control duty-cycling. Our FCC compliant transceiver uses OOK modulation and has a receiver sensitivity of -86dBm.

Monday, 6 June 2011
10:00 AM
Room 339-340
Session RMO2B: Cellular RF
Chair: Didier Belot, ST-Microelectronics
Co-Chair: Marc Tiebout, Infineon Technologies

RMO2B-1 10:00 AM
Single-Chip Multi-band SAW-less LTE WCDMA and EGPRS CMOS Receiver with Diversity
H. Xie, P. Rakers, R. Fernandez, T. Mccain, J. Xiang, J. Parkes, J. Riches, R. Verellen, M. Rahman, E. Shimoni, V. Bhan, D. B. Schwartz, Fujitsu Semiconductor Wireless Products Inc., Tempe, United States

Abstract: A single-chip multi-mode multi-band saw-less 90nm CMOS receiver is designed and implemented for 4G mobile platform. It supports LTE/WCDMA/EGPRS standards. The receiver achieves a typical 3dB and maximum 4dB noise figure (NF) in all standards and bands. It also automatically calibrates baseband low-pass filter cut-off frequency, mixer image rejection and IIP2 performance.

RMO2B-2 10:20 AM
An L-Band Receiver-Frontend-Architecture using Adaptive Q-Enhancement Techniques in 65nm CMOS as Enabler for Single-SAW GPS Receivers
C. Schultz[1], H. Doppke[1], M. Hammes[1], R. Kreienkamp[1], L. Lemke[1], S. van Waasen[2], [1]Infineon Technologies AG, Duisburg, Germany, [2]Forschungszentrum Jülich, Jülich, Germany

Abstract: A GPS receiver front-end achieves high dynamic input range by using Q-enhancement circuitry. In mobile phone environments the Q of the LNA is automatically increased, improving blocker performance by 11.3dB. The area is 1.9mm² in 65nm CMOS without RF options and requires 25mA from a 1.3V supply with a system NF of 1.5dB.

RMO2B-3 10:40 AM
Reconfigurable Wide-band Receiver with Positive Feed-back Translational Loop
C. Izquierdo[1], A. Kaiser[2], F. Montaudon[1], P. Cathelin[1], [1]ST Ericsson, Crolles, France, [2]IEMN, Lille, France

Abstract: A wide-band receiver for multi-standard cellular applications with a positive feed-back translational loop is presented in this paper. This technique allows tunable RF filtering right on input node of the LNA. The 65nm CMOS prototype circuit achieves, when in WCDMA mode, attenuation of out-of-band interferers of 12dB at 20MHz frequency offset, improving the out-of-band IIP3 by 17dB. The packaged test-chip provides good performance over a very wide frequency range from 1.3GHz to 2.85GHz.

RMO2B-4 11:00 AM
A Digital Calibration Enhanced GSM/GPRS Transmitter
P. Wang, C. Wang, W. Lee, T. Yu, Mediatek, Hsin-Chu, Taiwan

Abstract: This paper presents a digital calibration enhanced transmitter that is capable of self-calibrating loop gain and the non-linearity of the VCO gain of a charge pump PLL in a pre-emphasis transmitter. The results shows that we can achieve 0.5 degree phase error and -68dBc ORFS for GMSK modulation, which prove that the accuracy of the loop gain calibration and VCO gain linearity is within 1%, and two times reduction compared to all digital and analog transmitters.

RMO2B-5 11:20 AM
High Efficiency Envelope Tracking Power Amplifier with Very Low Quiescent Power for 20MHz LTE
M. Hassan[1], M. Kwak[1], V. W. Leung[2], C. Hsia[1], J. J. Yan[1], D. F. Kimball[1], L. E. Larson[1], P. M. Asbeck[1], [1]University of California at San Diego, La Jolla, United States, [2]Qualcomm Inc., San Diego, United States

Abstract: A high efficiency wideband envelope tracking (ET) power amplifier (PA) with low quiescent power is presented. The CMOS envelope amplifier (EA) has a combined linear amplifier (LA) and switching amplifier to achieve high efficiency and wider bandwidth. Quiescent power of the EA is reduced using a source cross-coupled LA with inherently low DC power dissipation. Measurements show a power added efficiency of 45% for the ET PA for 20MHz LTE signal with 6dB PAPR at 2.5GHz at 1W output power.

Monday, 6 June 2011
10:00 AM
Room 341-342
Session RMO2C: Advanced Architecture PAs
Chair: Eddie Spears, RFMD
Co-Chair: Jeffrey Walling, Rutgers University

RMO2C-1 10:00 AM
A W-band Current Combined Power Amplifier with 14.8dBm Psat and 9.4% Maximum PAE in 65nm CMOS

Z. Xu[1], Q. J. Gu[2], M. F. Chang[3], [1]HRL Laboratories, Malibu, United States, [2]University of Florida, Gainesville, United States, [3]University of California, Los Angeles, Los Angeles, United States

Abstract: We present a fully differential 101-117GHz power amplifier(PA) using two way current power combiner in 65nm bulk CMOS. It delivers up to 14.8dBm saturated output power with over 14dB power gain and better than 9.4% power added efficiency (PAE), which also achieves better than 11.6dBm output P1dB. A current power combiner is employed to combine the power from two separate PAs. The entire PA core occupies 0.106 mm2 chip area and dissipates 200mW.

RMO2C-2 10:20 AM
X-to-K band Broadband Watt-level Power Amplifier Using Stacked-FET Unit Cells

Y. Park, Y. Kim, W. Choi, J. Woo, Y. Kwon, Seoul National University, Seoul, Republic of Korea

Abstract: A broadband watt-level stacked-FET power amplifier (PA) has been developed using 0.15μm GaAs pHEMT's. A triple-stacked FET structure is used as a unit cell to combine RF voltage swings to achieve high-output power and broad bandwidth at the same time. The fabricated PA shows a peak power of 33.7dBm with a power added efficiency (PAE) of 29.5% at frequency of 18GHz, and higher than 32dBm output power from 10 to 21GHz. The fractional 3dB output power bandwidth is 84%.

RMO2C-3 10:40 AM
Wideband High Efficiency Envelope Tracking Integrated Circuit for Micro-Base Station Power Amplifiers

M. Kwak[1], D. F. Kimball[1], C. D. Presti[2], A. Scuderi[3], C. A. Santagati[3], J. J. Yan[1], P. M. Asbeck[1], L. E. Larson[1], [1]University of California at San Diego, La Jolla, United States, [2]Qualcomm Inc., San Diego, United States, [3]STMicroelectronics

Abstract: This paper presents a high performance BCD (Bipolar-CMOS-DMOS) monolithic envelope tracking (ET) IC to achieve high efficiency and linearity for micro-base station power amplifier (PA) applications. Measurement of the BCD high voltage envelope amplifier shows an efficiency of 72% using WCDMA input signals (7.7dB PAR). An ET PA has overall drain efficiency above 51%, with an ACLR1 of -49dBc using memory mitigation digital pre-distortion, at an average output power above 2W and a gain of 10dB.

RMO2C-4 11:00 AM
A Power-Combined Switched-Capacitor Power Amplifier in 90nm CMOS

S. Yoo[1], J. S. Walling[2], E. Woo[1], D. J. Allstot[1], [1]University of Washington, Seattle, United States, [2]Rutgers University, New Brunswick, United States

Abstract: A digitally-controlled switched-capacitor RF power amplifier (SCPA) is implemented with a transformer-based power-combiner in 90nm CMOS. The individual SCPA cores can be controlled to provide high average output power and linearity in an all-switching mode or increased dynamic range in a sequential-switching mode. It delivers a peak (average) output power of 27.0 (20.3) dBm with a peak (average) PAE of 31.3% (18.2%) for a 64QAM OFDM modulated signal with measured EVM=3.8% in the 2.4GHz band.

RMO2C-5 11:20 AM
A 1.8GHz Wide-Band Stacked-Cascode CMOS Power Amplifier for WCDMA Applications in 65nm Standard CMOS

S. Leuschner[1], J. Mueller[2], H. Klar[1], [1]Technical University of Berlin, Berlin, Germany, [2]Infineon Technologies AG, Neubiberg, Germany

Abstract: A two-stage power amplifier (PA) for WCDMA operation in standard 65nm CMOS is presented. The power amplifier delivers a saturated output power of 29.4dBm at a PAE of 51% at 1.8GHz. A two-stage interstage matching network was employed to achieve a high bandwidth (300MHz) where the amplifier shows a PAE 45%. With a WCDMA signal a maximum linear output power of 25.4dBm (PAE=37.9%) was measured without digital predistortion (DPD). Using DPD, these figures could be improved to 27.9dBm and 48%.

Monday, 6 June 2011
10:00 AM
Room 343-344
Session RMO2D: Emerging RFIC Device Technologies
Chair: Aditya Gupta, Northrop Grumman
Co-Chair: Eli Reese, Triquint

RMO2D-1 10:00 AM
Non-invasive Monitoring of CMOS Power Amplifiers Operating at RF and mm-Wave Frequencies using an On-chip Thermal Sensor
J. Gonzalez[1], B. Martineau[2], D. Mateo[1], J. Altet[1], [1]Universitat Politècnica de Catalunya, Barcelona, Spain, [2]ST Microelectronics, Grenoble, France

Abstract: In this paper a non-invasive technique for the on-chip observation of PA operation is presented. It uses a differential temperature sensor that transduces the temperature increase due to the power dissipated by active transistors operating at high frequencies into a low frequency signal that is proportional to some relevant PA figures of merit, such as output power or PAE. The technique is demonstrated by using the same thermal sensor in two 65nm CMOS different PAs (a 2GHz PA and a 60GHz PA)

RMO2D-2 10:20 AM
High-Power Digital Controlled Artificial Dielectric GaN Reconfigurable Transmission Lines for Digitally Assisted RFICs
M. K. Watanabe, T. R. LaRocca, Northrop Grumman Aerospace Systems, Redondo Beach, United States

Abstract: The first known GaN implementation of high-power digital controlled artificial dielectric (DiCAD) reconfigurable transmission lines is presented. Standard GaN HEMT processing techniques were used, making DiCAD easily compatible with future circuit designs. The DiCAD transmission line's effective dielectric constant exhibits linear digital control from 15 to 32 with 3-bit resolution up to 50GHz. P1dB is measured to be 27dBm and OIP3 is calculated to be 48dBm for all states.

RMO2D-3 10:40 AM
A New Method to Achieve RF Linearity in SOI Nanowire MOSFETs
A. Razavieh[1], N. Singh [2], A. Paul[1], G. Klimeck[1], D. B. Janes[1], J. Appenzeller[1], [1]Purdue University, West Lafayette, United States, [2]Agency For Science, Technology And Research (A*STAR), Singapore

Abstract: In this paper we show that device level linearity can be achieved if transistors operate in 1-D ballistic transport regime in the quantum capacitance limit. We consider SOI Silicon nanowire MOSFETS and report the IIP3 of about -13dBm for this regime of operation. When normalized the IIP3 values to the power at maximum transconductance 10dB improvement compare to operation in velocity saturation regime is achieved.

RMO2D-4 11:00 AM
Nano Crossbar Electrostatic Discharge Protection for RF ICs

J. Liu[1], L. Zhang[2], X. Wang[1], L. Lin[1], Z. Shi[1], A. Wang[1], R. Huang[2], Y. Cheng[2], [1]University of California, Riverside, Riverside, United States, [2]Peking University, Beijing, China

Abstract: We report design and analysis of new nano crossbar based nano phase switching electrostatic discharge (ESD) protection structures. Measurements confirm ESD protection featuring fast response of 100pS, ultra low leakage Ileak~0.11pA, varying trigger voltage (Vt1) and good ESD protection voltage ratio (ESDV) 230V/μm². This nontraditional nano-crossbar ESD protection can be a potential solution for RF and mixed-signal ICs.

RMO2D-5 11:20 AM
An All-Graphene Radio Frequency Low Noise Amplifier

S. Das[1], J. Appenzeller[2], [1]Purdue University, West Lafayette, United States, [2]Purdue University, West Lafayette, United States

Abstract: In this paper, we propose and quantitatively evaluate an ''All-Graphene nano-ribbon (GNR) circuit'' for high frequency low noise amplifier (LNA) applications, which shows considerable advantage over state-of–the-art technologies. In particular, we discuss how to satisfy the requirements for temperature stability, gain, power dissipation, noise and speed for a high performance LNA circuit by adjusting only the width of the nano ribbons.

Monday, 6 June 2011
2:20 PM
Room 337-338
Session RMO3A: Low Power Wireless Sensor Techniques
Chair: Glenn Chang, MaxLinear
Co-Chair: Ali Afsahi, Broadcom

RMO3A-1 2:20 PM
A 30MHz-2.4GHz CMOS Receiver with Integrated RF Filter and Dynamic-range-scalable Energy Detector for Cognitive Radio

M. Kitsunezuka[1], H. Kodama[1], N. Oshima[1], K. Kunihiro[1], T. Maeda[2], M. Fukaishi[1], [1]NEC Corporation, Kawasaki, Japan, [2]Renesas Electronics Corporation, Kawasaki, Japan

Abstract: A 30MHz-2.4GHz CMOS receiver with a highly linear integrated tunable RF filter, as well as with a dynamic-range-scalable RSSI-based energy detector for both whitespace and interference-level sensing, is reported. The test chip, fabricated in 90nm CMOS process, achieves over 42dB harmonic rejection including seventh-order harmonic without any external device, 67dB gain, 5-8dB NF, +1.7dBm in-band IIP3, and +37dBm IIP2 while drawing only 25-37mA from 1.2V supply.

RMO3A-2 2:40 PM
A 1900MHz-Band GSM-Based Clock-Harvesting Receiver with -87dBm Sensitivity

J. K. Brown, D. D. Wentzloff, University of Michigan, Ann Arbor, United States

Abstract: A 0.13μm CMOS clock-harvesting receiver is presented which extracts a 21Hz clock embedded within the GSM standard for the wake-up of a wireless sensor network. In active mode, the receiver achieves -87dBm sensitivity with 57μs of jitter at the output while consuming 126μW. The receiver is optimized for heavy duty-cycling with a sleep-mode power consumption of only 81pW.

RMO3A-3 3:00 PM
A CMOS Spectrum Sensor Using Injection Locking of Two Voltage-Controlled Oscillators for Cognitive Radio System

F. Wang[1], C. Chen[1], J. Tsai[1], T. Horng[1], K. Peng[2], J. Je-Kuan[3], J. Li[3], C. Chen[3], [1]Department of Electrical Engineering, Kaohsiung, Taiwan, [2]Department of Computer and Communication Engineering, Kaohsiung, Taiwan, [3]Info. and Comm. Re Research Lab., Hsinchu, Taiwan

Abstract: This paper presents a CMOS spectrum sensor to detect spectral usage and spectrum holes for cognitive radio system. The sensor consists of a swept oscillator and a frequency discriminator, both of which use the injection locking of VCO to process the sensed signal without requiring a frequency synthesizer. The sensor can detect the frequency and power for wireless communication signals with high accuracy at a spectrum scanning speed of 100MHz/ms. The sensitivity can be below -100dBm.

RMO3A-4 3:20 PM

A Wirelessly-Powered Passive RF CMOS Transponder with Dynamic Energy Storage and Sensitivity Enhancement

Z. Safarian, H. Hashemi, University of Southern California, Los Angeles, United States

Abstract: A new scheme for a passive sensor is proposed in this work in which the extra received power beyond the sensitivity level is stored and later used to enhance the sensitivity of the sensor. The chip prototype has been designed and fabricated in a 130nm CMOS technology. The measurement results show the sensitivity of the implemented sensor is improved from -19.5dBm to -29dBm at 900MHz, and from -15.4dBm to -26.5dBm at 2.4GHz.

Monday, 6 June 2011
2:20 PM
Room 339-340
Session RMO3B: Low Power LNA Design Techniques
Chair: Danilo Manstretta, University of Pavia
Co-Chair: Jean-Baptiste Begueret, University of Bordeaux

RMO3B-1 2:20 PM
A 60μW LNA for 2.4GHz Wireless Sensors Network Applications
T. Taris, J. Begueret, Y. Deval, University of Bordeaux, Talence, France

Abstract: This work reports on the implementation of a 2.4GHz ultra-low power (ULP) low noise amplifier (LNA) in a standard CMOS 0.13μm process. The proposed design methodology consists of optimizing the tradeoff between RF performance and current consumption of a MOS transistor. The supply of the circuit, controlled by a 3bit DAC, varies from 0.4 to 0.6 V. Experimental results of the circuit indicate a power dissipation of 60μW@0.4V, a noise figure of 5.3dB, and a forward gain of 13.1dB.

RMO3B-2 2:40 PM
A 1.5V, 140μA CMOS Ultra-Low Power Common-Gate LNA
C. Jeong[1], W. Qu[2], Y. Sun[1], D. Yoon[1], S. Han[1], S. Lee[1], [1]Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Republic of Korea, [2]Silicon Works Company Ltd, Daejeon, Republic of Korea

Abstract: This paper presents design guidelines for ultra-low power Low Noise Amplifier design by comparing input matching, gain, and noise figure characteristics of common-source and common-gate (CG) topologies. A current-reused ultra-low power 2.2GHz CG LNA is implemented based on 0.18μm CMOS technology. Measurement results show 13.9dB power gain, 5.14dB NF, and -9.3dBm IIP3, respectively, while dissipating 140μA from a 1.5V supply, which shows best FOM among all published ultra-low power LNAs.

RMO3B-3 3:00 PM
Effects of the Nonlinearity of the Common-Gate Stage on the Linearity of CMOS Cascode Low Noise Amplifier
C. Cui, T. Kim, S. Kim, B. Kim, Sungkyunkwan University, Suwon, Republic of Korea

Abstract: This work presents the effects of the CG stage nonlinearity on the linearity of the cascode LNA. Conventionally, the CG stage is assumed as an ideal current buffer in cascode LNA, but the analysis shows that the CG stage limits the linearity of cascode LNA as the gain increases. Therefore, the simple linearization of the CS stage has difficulties to enhance the gain of LNA as frequency increases. The analysis and measurement show that optimal load impedance that maximizes OIP3 of the LNA exists.

RMO3B-4 3:20 PM

A 1.3mW 20dB Gain Ultra Low Power Inductorless LNA with 4dB Noise Figure for 2.45GHz ISM Band

F. Belmas[2], F. Hameau[2], J. Fournier[1], [1]IMEP, Grenoble, France, [2]CEA, Grenoble, France

Abstract: This paper presents an inductorless low power (LP) low noise amplifier (LNA) based on a Common Gate (CG) topology. The circuit combines gain boosting techniques to enable high gain LP LNA. The circuit is integrated in a 130nm CMOS technology and shows 20dB gain with 4dB Noise Figure and -12dBm IIP3. The power consumption is 1.32mW from a 1.2V supply.

Monday, 6 June 2011
2:20 PM
Room 341-342
Session RMO3C: Devices and circuits for silicon based mm-Wave ICs
Chair: Oren Eliezer, Xtendwave
Co-Chair: Li-Wu Yang, Shanghai Jiao-Tong University

RMO3C-1 2:20 PM
60GHz Antenna Integrated on High Resistivity Silicon Technologies Targeting WHDMI Applications
D. Titz[1], R. Pilard[2], F. Ferrero[1], F. Gianesello[2], D. Gloria[2], C. Luxey[1], P. Brachat[3], G. Jacquemod[1], [1]Université de Nice-Sophia-Antipolis, Valbonne, France, [2]ST Microelectronics, Crolles, France, [3]Orange Labs, La Turbie, France

Abstract: For the 60GHz market to flourish, low cost antennas and packages are required. In order to address these issues, we review in this paper achievable antenna performance using High Resistivity (HR) silicon technologies, discussing possible integration schemes, antenna design and 3D on wafer characterization. Antenna gain of 3.9dBi @ 60GHz has been measured making HR Si technology a promising one to address applications packaged in mm-Wave low cost technology.

RMO3C-2 2:40 PM
A High-Isolation 60GHz CMOS Transmit/Receive Switch
C. Kuo[1], H. Kuo[1], H. Chuang[1], C. Chen[2], T. Huang[1], [1]National Cheng Kung University, Tainan, Taiwan, [2]National University of Tainan, Tainan, Taiwan

Abstract: A 60GHz highly-isolation CMOS single-pole double-throw (SPDT) T/R switch fabricated with TSMC standard 90nm CMOS technology is presented. The leakage cancellation technique is used to increase the isolation between the transmitter and receiver ports. The measured results show the insertion loss is less than 3.5dB, and the isolation is higher than 28dB from 57-64GHz. The port isolation is higher than 34dB and the input 1dB compression point is 6.9dBm at 60GHz.

RMO3C-3 3:00 PM
Integration of Antenna-on-Chip and Signal Detectors for Applications from RF to THz Frequency Range in SiGe Technology
S. Wane[1], R. van Heijster[2], S. Bardy[1], [1]NXP-Semiconductors, Caen, France, [2]TNO Defence, Security and Safety, The Hague , Netherlands

Abstract: This paper presents design solutions for signal detectors and Antenna on-Chip (AoC) using a state-of-the-art SiGe technology. Both CML and CMOS detectors are designed, fabricated and compared in terms of their performances. AoC working at 60GHz, 77GHz, and 94GHz are designed and fabricated. Several AoC structures are proposed to experimentally evaluate bandwidth, near field coupling and radiation efficiency performances.AoC and SiGe Schottky diodes are characterized for THz applications.

RMO3C-4 3:20 PM

On-Chip Vertically Coiled Solenoid Inductors and Transformers for RF SoC Using 90nm CMOS Interconnect Technology

H. Namba, T. Hashimoto, M. Furumiya, Renesas Electronics Corporation, Kawasaki, Japan

Abstract: This paper presents very small on-chip vertically coiled solenoid inductors using 90nm CMOS interconnect technology. A variety of area-saving transformers without any additional processing steps are also presented: a solenoid overlaid with another inside-diameter solenoid, a solenoid coiled around another one, face-to-face solenoids. RF characteristics were evaluated based on S-parameter. Self-resonance frequencies resulted in higher than 40GHz, and coupling coefficients were larger than 0.7.

Monday, 6 June 2011
2:20 PM
Room 343-344
Session RMO3D: mm-Wave VCOs
Chair: Timothy Hancock, MIT Lincoln Laboratory
Co-Chair: Fred Lee, SiTime

RMO3D-1 2:20 PM
A V-band Voltage Controlled Oscillator with Greater than 18GHz of Continuous Tuning range based on Orthogonal E mode and H mode control
A. Jooyaie, F. Chang, University of California at Los Angeles, Los Angeles, United States

Abstract: A technique for wide continuous tuning range of Voltage Controlled Oscillators is presented. Technique relies on separate E and H mode excitation of resonator, avoiding the Q-degrading switches. The standing-wave VCO implemented in CMOS 65nm achieves a continuous tuning range from 58-76.2GHz, with an average phase noise of -89.5dBc/Hz at 1 MHz offset across the entire band, consumes an average of 5.8mW (excluding the output buffers), occupies 177 x177μm and achieves a record FoM.

RMO3D-2 2:40 PM
118GHz fundamental VCO with 7.8% tuning range in 65nm CMOS
W. Volkaerts, M. Steyaert, P. Reynaert, Katholieke Universiteit Leuven, Leuven, Belgium

Abstract: This paper presents a 118GHz fundamental VCO in a 65nm low power CMOS technology. Using accumulation mode varactors, the oscillator covers a frequency range from 113.4GHz to 122.6GHz, which corresponds to a 7.8% tuning range. Combining with a variable supply voltage, the tuning range is extended to 11GHz (9.3%). The VCO draws 5.6mA from a 1V supply and the output is higher than -28.5dBm. The measured phase noise at 118.3GHz is -83.9dBc/Hz at 1MHz offset. The FOMT is -175.7dB.

RMO3D-3 3:00 PM
Fully Monolithic 18.7GHz 16ps GaAs Mode-Locked Oscillators
O. Yildirim, D. Ha, D. Ham, Harvard University, Cambridge, United States

Abstract: We report a mode-locked electrical oscillator fully integrated in GaAs. It self generates a periodic train of pulses with a 16ps pulse width and a 18.7GHz frequency. This is the fastest electrical mode-locked oscillator to date, and the first integration of reflective mode locked electrical oscillator. It works by sending a pulse back and forth on a coplanar waveguide with reflections at both ends. The reflection occurs with level-dependent gain that enables pulse formation and stabilization.

RMO3D-4 3:20 PM
A 77GHz CMOS VCO with 11.3GHz Tuning Range, 6dBm Output Power, and Competitive Phase Noise in 65nm Bulk CMOS

V. P. Trivedi, K. To, W. Huang, Freescale Semiconductor, Inc., Tempe, United States

Abstract: We demonstrate, using a foundry-based 65nm bulk technology, mmWave CMOS VCOs in the range of 38GHz and 77GHz with highest reported continuous tuning range (14%-25%), competitive phase noise (-94dBc/Hz at 1MHz offset at 38GHz), and high Pout (6dBm) needed to readily integrate with CMOS PA and to tolerate PVT variations. Device and design optimizations responsible for the high performance are presented. The impact of temperature and VDD variation is reported for the first time.

Monday, 6 June 2011
4:00 PM
Room 337-338
Session RMO4A: RF characterization and modeling of advanced CMOS

Chair: Bumman Kim, Pohang University of Science and Technology
Co-Chair: Tzung-Yin Lee, Skyworks Solutions

RMO4A-1 4:00 PM
Aging of 40nm MOSFET RF Parameters under RF conditions From Characterization to Compact Modeling for RF Design

L. Negre[1], D. Roy[1], F. Cacho[1], P. Scheer[1], S. Boret[1], A. Zaka[1], D. Gloria[1], G. Ghibaudo[2], [1]STMicroelectronics, Crolles, France, [2]Imep Lahc, Grenoble, France

Abstract: In the framework of MOSFET reliability for mixed-analog application, an investigation of RF parameters degradation is performed. An innovative flow, composed of DC and RF stress with DC and RF aging characterization, is presented. Degradation kinetics of main parameters are physically explained and modeled using PSP compact model to predict the behavior of stressed devices.

RMO4A-2 4:20 PM
Small signal and HF Noise performance of 45nm CMOS technology in mm-Wave range

L. Poulain[2], N. Waldhoff[1], D. Gloria[2], F. Danneville[1], G. Dambrine[1], [1]Institut d'Electronique de Microélectronique et de Nanotechnologie, Villeneuve d'Ascq, France, [2]STMicroelectronics, Crolles, France

Abstract: This paper aims to present DC, small signal and noise performance up mm-Wave range of 45-nm bulk CMOS Technology. S parameters were measured up to 67GHz, a HF noise model was extracted in 6-40GHz frequency range, and its accuracy verified through a comparison with the noise figure measured in W band. The technology offers fT, fMAX respectively of 200 and 300GHz in line with up-to-date published results for a 45nm CMOS Technology. A minimum noise figure of 4.5dB at 94GHz is demonstrated.

RMO4A-3 4:40 PM

Analytical Model for RF Power Performance of Deeply Scaled CMOS Devices

U. Gogineni[1], J. del Alamo[1], A. Valdes-Garcia[2], [1]Massachusetts Institute of Technology, Cambridge, United States, [2]IBM T.J Watson Research Center, Yorktown Heights, United States

Abstract: This paper presents a first order model for RF power of deeply scaled CMOS. The model highlights the role of device on-resistance in determining the maximum RF power. We show excellent agreement between the model and the measured data on 45nm CMOS devices across a wide range of device widths. The model allows circuit designers to quickly and accurately estimate the power and efficiency of a device layout without need for complicated compact models or simulations.

RMO4A-4 5:00 PM

CMOS Digital Tunable Capacitance with tuning ratio up to 13 and 10dBm linearity for RF and mm-Wave Design

R. Debroucke[1], A. Pottrain[1], D. Titz[3], F. Gianesello[1], D. Gloria[1], C. Luxey[3], C. Gaquiere[2], [1]STMicroelectronics, Crolles, France, [2]IEMN, Villeneuve d'ascq, France, [3]LEAT, Vallbone, France

Abstract: Capabilities offered by advanced silicon technologies enable both mm-Wave design and agile circuits development, then the development of high performance tunable capacitance is mandatory. This paper reviews the design, optimization and characterization of Digital Tunable Capacitance using STMicroelectronics BiCMOS 0.13µm technology. DTC with TWC architecture allows synthesized capacitance up to 110GHz, 10dBm P1dB and a tuning ratio equal to 13. Design of a 60GHz RTPS using 4 bits DTC is presented.

Monday, 6 June 2011
4:00 PM
Room 339-340
Session RMO4B: Integrated Front-End RFIC - LNA, Mixers, Filters
Chair: Frank Henkel , IMST GmbH
Co-Chair: Reynold Kagiwada, Northrop Grumman

RMO4B-1 4:00 PM
A 280MHz CMOS Intra-symbol Intermittent RF Front End for Adaptive Power Reduction of Wireless Receivers
M. Nakamura, M. Ugajin, M. Harada, Nippon Telegraph and Telephone Corporation, Atsugi-shi, Japan

Abstract: For adaptive power reduction of wireless receivers, we developed the first intra-symbol intermittent (ISI) CMOS RF front-end. The LNA and mixer operate synchronously and intermittently within a single symbol-length. The experimental results of demodulation and the theoretical analysis of noise figure show the effectiveness of the ISI operation.

RMO4B-2 4:20 PM
A 7dB NF 60GHz-Band mm-Wave Transconductance Mixer
Y. Jin, J. R. Long, M. Spirito, Delft University of Technology, Delft, Netherlands

Abstract: A 60GHz-band doubly-balanced transconductance (Gm) mixer with an on-chip linear L-C combiner for RF and LO signal summation and impedance transformation is described. Class-AB biasing is employed for low quiescent dc power consumption (360μW at 1.2V). At fLO=58GHz and PLO=0dBm, the Gm-mixer prototype realizes 6.9dB DSB(50Ω) NF, 6.2dB power conversion gain, -4.7dBm input-referred P-1dB, and +4.2dBm IIP3.

RMO4B-3 4:40 PM
A 100-3000MHz, Up/Down-Convert, +29dBm IIP3, +13dB NF, Active Mixer with Integrated Fractional-N PLL and VCO
I. Fujimori-Chen[1], B. Walker[2], R. Broughton-Blanchard[2], E. Balboni[2], [1]Analog Devices, Inc., Somerset, United States, [2]Analog Devices, Inc., Wilmington, United States

Abstract: A broadband, high-dynamic range active mixer with integrated PLL and VCO is presented. The synthesizer uses a programmable fractional-N PLL with in-band phase noise FOM of -223dBc/Hz/Hz. The 100-3000MHz active mixer can be configured for up or down conversion. The mixer's linearity can be boosted from +25dBm to +29dBm, and optimized for a range of input frequencies. Designed in Si-Ge 0.25μm BiCMOS, the entire chip occupies 5.84 mm^2 and consumes 250mA from a 5V supply.

RMO4B-4 5:00 PM

A 1 to 5GHz Adjustable Active Polyphase Filter for LO Quadrature Generation

M. Kaltiokallio, J. Ryynänen, Aalto University, Espoo, Finland

Abstract: This paper focuses on the design of a highly tunable active polyphase filter with IRR better than 40dB. The active polyphase filter is implemented as a part of a simple RF receiver to demonstrate its feasibility for wide variety of wireless systems. The design consist of a high frequency adjustable gm-element that is optimized for active PPF. The filter achieves a tuning range of 1 to 5GHz while consuming supply current of 0.7 to 4.4mA. The silicon area of the filter is 64x85μm.

Monday, 6 June 2011
4:00 PM
Room 341-342
Session RMO4C: High performance CMOS Power Amplifiers
Chair: Jyoti P. Mondal, Northrop Grumman
Co-Chair: Leon van den Oever, Radio Semiconductor Corp.

RMO4C-1 4:00 PM
A 550-1050MHz +30dBm Class-E Power Amplifier in 65nm CMOS
R. Zhang[1], M. Acar[2], M. P. van der Heijden[2], M. Apostolidou[2], L. C. de Vreede[1], D. M. Leenaerts[2], [1]Delft University of Technology, Delft, Netherlands, [2]NXP Semiconductors, Eindhoven, Netherlands

Abstract: A 65nm CMOS broadband class-E PA using HV extended-drain devices is presented. To improve reliable operation, sub-optimum class-E operation is applied. The PA is followed by an off-chip two-stage LC ladder. The measurements show a DE 67% and a PAE 52% with a Pout 30dBm within 550-1050MHz. The output power variation is within 1.0dB and efficiency variation is less than 13%. The highest efficiency is observed at 700MHz with peak DE of 77% and peak PAE of 65% at a Pout of 31dBm.

RMO4C-2 4:20 PM
Digital Polar Transmitter Using a Watt-Class Current-Mode Class-D CMOS Power Amplifier
T. Nakatani[2], J. Rode[3], D. F. Kimball[4], L. E. Larson[1], P. M. Asbeck[1], [1]University of California, San Diego, La Jolla, United States, [2]Panasonic Corporation of North America, Cupertino, United States, [3]ZIVA Corporation, San Diego, United States, [4]MaXentric Technologies, LLC, San Diego, United States

Abstract: A digital polar transmitter with a watt-class CMOS power amplifier is demonstrated, implemented with a 0.15μm RF CMOS process. Current-mode class-D configuration and stacked FETs are used to obtain high efficiency and high breakdown voltage. The output stage is fed by a buck converter employing digital pulse width modulation with 47 MHz pulse rate. Overall efficiency of 26.5% efficiency was achieved while maintaining ACLRs within WCDMA specifications at 24dBm average output power.

RMO4C-3 4:40 PM
A Fully-Integrated K-band CMOS Power Amplifier with Psat of 23.8dBm, PAE of 25.1 %
Y. Kawano, T. Suzuki, A. Mineyama, M. Sato, T. Hirose, K. Joshin, Fujitsu Ltd., Atsugi, Japan

Abstract: A fully-integrated K-band power amplifier was designed and fabricated in standard 65nm CMOS process. The fabricated power amplifier shows the broadband characteristics which were the saturation power of more than 20dBm from 16-25GHz with the linear gain of more than 20dB. The peak value of the saturation power was 23.8dBm, and the power added efficiency (PAE) was 25.1% at 19GHz. The chip occupied area including the DC and RF pads is only 1.2x0.8mm.

RMO4C-4 5:00 PM
A Fully-Integrated Efficient CMOS Inverse Class-D Power Amplifier for Digital Polar Transmitters

D. Chowdhury, S. V. Thyagarajan, L. Ye, E. Alon, A. M. Niknejad, University of California at Berkeley, Berkeley, United States

Abstract: We demonstrate a fully-integrated, high-efficiency inverse Class-D power amplifier in 65nm CMOS process. A comprehensive analytical framework has been developed to reveal the design trade-offs and enable efficiency maximization. Operating from a 1V supply, the PA delivers 22dBm output power with a high efficiency of 44% without using any RF process options. The PA efficiency is comparable to that of state-of-the-art CMOS switching PAs, though it uses a much simpler output matching network.

Monday, 6 June 2011
4:00 PM
Room 343-344
Session RMO4D: Frequency Synthesis: Mixed Signal Techniques
Chair: Bertan Bakkaloglu, Arizona State University
Co-Chair: Chun-Ming Hsu, IBM

RMO4D-1 4:00 PM
A Phase-Adjustable Delay-Locked Loop Utilizing Embedded Phase Interpolation
S. W. Callender, A. M. Niknejad, Berkeley Wireless Research Center, University of California at Berkeley, Berkeley, United States

Abstract: This paper presents the design of a 1GHz DLL with embedded phase interpolation. The DLL was designed in a 0.13μm SiGe BiCMOS process and provides a measured single-tap phase range of 50ps (18°) with an average and worst-case phase resolution of 1.36ps (0.49°) and 5ps (1.8°), respectively. This translates to beamsteering resolutions of 3.5mm in free space when integrated into mm-Wave imagers that utilize time-domain beamforming. The DLL has an average output rms-jitter of 860fs.

RMO4D-2 4:20 PM
Dynamic Bandwidth Adjustment of an RF All-Digital PLL
R. B. Staszewski[1], I. Bashir[2], [1]Technische Universiteit Delft, Delft, Netherlands, [2]University of Texas at Dallas, Richardson, United States

Abstract: Recent advances in digitization of RF synthesizers have resulted in all-digital PLL (ADPLL) architectures that enjoy high precision and repeatability of their characteristics. So far, only semi-static selection of these features have been exploited. In this paper, we propose a dynamic manner of the ADPLL transfer function adjustment, which could be used to increase the loop bandwidth due to high instantaneous excursion of a modulating data. Simple experiments confirm its potential.

RMO4D-3 4:40 PM
Process compensated low power LO divider chain with asynchronous odd integer 50% duty cycle CML dividers

E. P. Coleman, S. Chakraborty, W. Budziak, T. R. Blank, P. T. Roine, Texas Instruments Incorporated, Dallas, United States

Abstract: This paper will illustrate the design of low power, high performance LO divide chain using asynchronous CML dividers for a operating at 4Ghz of input RF frequency and provide outputs in 138-960Mhz range by 4,8,12,16,20, and 24 division ratios. All the CML dividers use a dual feedback process compensated analog bias to compensate for load resistor and tail current variations. Frabricated in 180nm CMOS technology, the divider chain consumes 2.2mA from 1.8V regulated supply at the highest band.

RMO4D-4 5:00 PM
A CMOS Auto-Calibrated I/Q Generator for Sub-GHz Ultra Low-Power Transceivers

C. M. Ippolito, A. Italia, G. Palmisano, Università di Catania, Catania, Italy

Abstract: An ultra low-power 0.3-1GHz auto-calibrated in-phase/quadrature generator has been designed and fabricated in a 90nm CMOS technology. The circuit generates quadrature signals by means of master-slave dividers and the calibration is performed by using a delay-locked loop.The process tolerances phase error is lower than 4 degree and can be cancelled.Phase error is lower than 1 degree with frequency, temperature, and supply variations.The circuit current consumption is 0.5mA from a 1.2V supply.

Tuesday, 7 June 2011
8:00 AM
Room 337-338
Session RTU1A: mm-Wave modeling of parasitic and passives
Chair: Kevin McCarthy, University College Pork
Co-Chair: Francis Rotella, Peregrine Semiconductor

RTU1A-1 8:00 AM
A Layout Technique for mm-Wave PA Transistors
C. Liang, B. Razavi, UCLA, Los Angeles, United States

Abstract: The distributed interconnect parasitics within large transistors markedly egrade the output power and efficiency at mm-Wave frequencies. This paper develops a model for such structures and proposes a layout technique to reduce the effect of source terminal parasitics. The technique is applied to a 60GHz prototype in 65-nm CMOS technology, raising the output power from 5 to 10dBm and the drain efficiency from 3.7% to 10.7%.

RTU1A-2 8:20 AM
mm-Wave Modeling of Isolated MOS substrate Network through Gate-Bulk Measurements
B. Dormieu[2], C. Charbuillet[1], F. Danneville[2], N. Kauffmann[1], P. Scheer[1], [1]STMicroelectronics, Crolles, France, [2]IEMN, Villeuneuve d'Ascq, France

Abstract: This paper presents a novel methodology for the extraction of the substrate network components in 45nm nMOS isolated devices, based on original "Gate-Bulk" structures. Since the main model acceptance criteria is the frequency dependency, a large part is devoted to accurately model distributed effects in the p-well and the deep n-well layers up to 80GHz. The main structures are completed with intermediate structures which give a better understanding of the substrate distribution effects.

RTU1A-3 8:40 AM
A Unified Model for On-chip CPWs with Various Types of Ground Shields
H. Wang[1], D. Zeng[2], D. Yang[1], L. Zhang[1], L. Zhang[1], H. Qian[1], Y. Wang[1], Z. Yu[1], [1]Tsinghua University, Beijing, China, [2]Chinese Academy of Sciences, Suzhou, China

Abstract: Coplanar waveguides are promising candidates for passive devices in mm-Wave frequency bands. In this paper, CPW transmission lines with and without ground shields have been fabricated on 65nm CMOS technology. A physical-based model is proposed to describe the frequency-dependent per-unit-length L, C, R, and G parameters. Influences of ground shields have been analyzed and included into the general model. The accuracy of the model is confirmed by experimental results.

RTU1A-4 9:00 AM

Direct, S-Parameter Measurement-Based Modeling of Ultra-Low Resistance Passive Components

M. D. Brunsman[1], R. D. Hayward[2], K. W. Mays[3], [1]TriQuint Semiconductor, Hillsboro, United States, [2]TriQuint Semiconductor, Hillsboro, United States, [3]TriQuint Semiconductor, Hillsboro, United States

Abstract: This paper presents a methodology for modeling the resistance of MIM capacitors, directly from measured S-Parameters using an ultra-low impedance measurement known as the S21-Shunt technique. Model parameters are determined using slope and intercept methods directly from measured data that is acquired on "series-shunt" configured test structures. Errors attributable to probe contact resistance (PCR) and its associated variability are eliminated through application of the presented methodology.

Tuesday, 7 June 2011
8:00 AM
Room 339-340
Session RTU1B: Broadband and Low-Noise Amplifiers
Chair: Madhukar Reddy, MaxLinear
Co-Chair: Eric Klumperink, University of Twente

RTU1B-1 8:00 AM
A CMOS Distributed Amplifier with Active Input Balun Using GBW and Linearity Enhancing Techniques
A. Jahanian, P. Heydari, University of California, Irvine, Irvine, United States

Abstract: A CMOS highly linear 818GHz-GBW distributed amplifier (DA) with distributed active input balun is presented. Each gm cell in the DA employs dual-output 2-stage topology that improves gain and linearity without adversely affecting BW and power. Fabricated in a 65nm LP CMOS process, the 0.9mm² DA achieves 22dB of gain and 10dBm of P1dB while consuming 97mW from a 1.3V supply. A distributed balun using the same gm cell achieves BW 70GHz and 4dB gain with 19.5mW power consumption from 1.3V supply.

RTU1B-2 8:20 AM
60GHz High-Gain Low-Noise Amplifiers with a Common-Gate Inductive Feedback in 65nm CMOS
H. H. Hsieh[1], P. Y. Wu[1], C. P. Jou[1], F. L. Hsueh[1], G. W. Huang[2], [1]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, [2]National Nano Device Laboratories, Hsinchu, Taiwan

Abstract: In this paper, a novel design technique of common-gate inductive feedback is presented for mm-Wave LNAs. Using a 65nm CMOS process, transmission-line-based and spiral-inductor-based LNAs are fabricated for demonstration. The transmission-line-based LNA exhibits a gain of 20.6dB and a NF of 5.4dB at 60GHz while a 3dB bandwidth is 14.1GHz. As for the spiral-inductor-based LNA, the circuit shows a gain of 18.0dB and a NF of 4.5dB at 60GHz while a 3dB bandwidth is 12.2GHz.

RTU1B-3 8:40 AM
1.9-2.6GHz Tuning Range Variable Gain Low-Noise Amplifier with Digital Assisted Automatic Tuning Loop
X. Wang, C. Dong, S. Cao, N. Yan, X. Tan, H. Min, Fudan University, ShangHai, China

Abstract: A wide tuning range LNA with digital assisted tuning loop for multi-mode receiver is proposed in this paper. Tuning mechanism reuses the output load inductor and capacitor tank to configure an auxiliary oscillator while tuning and re-configures it back to narrowband LNA. Measurement show performance of 8~26dB variable voltage gain, 2dB NF, -5.5dBm IIP3 and S11 -10dB. Frequency tuning range covers 1.9-2.6GHz with 1% tuning error. The circuit consumes 8mA with 1.2V supply.

RTU1B-4 9:00 AM

Wideband Common-Gate Low-Noise Amplifier with Dual-Feedback for Simultaneous Input and Noise Matching

R. Ye[1], T. Horng[1], . Wu[2], [1]National Sun Yat-Sen University, Kaohsiung, Taiwan, [2]National Kaohsiung Normal University, Kaohsiung, Taiwan

Abstract: The design is based on a mechanism of dual-feedback, which is composed of a transformer and a gm-boosting feedback, to overcome the trade-off between noise and input matching in common-gate topology without consuming additional dc power. Simultaneously, the noise figure and power gain are improved. The implemented wideband CG LNA achieves an S11 of below -10dB, a NF of 1.9–2.65dB, a power gain of 13.5–16.5dB, and an IIP3 of -2–3dBm, with a 3dB gain bandwidth of 1–8 GHz.

Tuesday, 7 June 2011
8:00 AM
Room 341-342
Session RTU1C: mm-Wave Imagers
Chair: Paul Blount, Custom MMIC Design Services Inc.
Co-Chair: Brian Floyd, North Carolina State University

RTU1C-1 8:00 AM
A Fully Integrated 96GHz 2x2 Focal-Plane Array with On-Chip Antenna
C. Wang, Z. Chen, H. Yao, P. Heydari, University of California, Irvine, Irvine, United States

Abstract: A fully integrated 96GHz 2x2 focal-plane array (FPA) direct conversion imager in 180nm SiGe BiCMOS (fT/fmax=200/180GHz) employing four integrated antennas with Dicke switches and LO generation/distribution is presented. The PLL plus tripler achieves a locking range of 92.67-98.2GHz and phase noise of -93dBc/Hz at 96GHz measured at 1MHz offset. The 3.5×3mm² chip achieves an average responsivity and NEP of 285MV/W and 8.1fW/√Hz, respectively, across 86-106GHz band and an NETD of 0.48K.

RTU1C-2 8:20 AM
A CMOS Fully Differential W-Band Passive Imager with <2K NETD
Q. J. Gu[1], Z. Xu[2], H. Jian[3], M. F. Chang[3], [1]University of Florida, Gainesville, United States, [2]HRL Laboratories, Malibu, United States, [3]University of California, Los Angeles, Los Angeles, United States

Abstract: This paper presents a fully differential W-band passive imager that integrates LNA, Dicke switch, detector and filter, with minimum NEPs of $\mathbf{21}\ fW/\sqrt{Hz}$ / $\mathbf{24}\ fW/\sqrt{Hz}$ for without/with switch cases and a peak responsivity of >1.8 MV/W. To authors' knowledge, this represents the largest responsivity to date from a CMOS radiometer chip. It achieves NETD = 1.94 K with 30ms integration time. The chip occupies 0.49 mm^2 active area with 57 mW power consumption.

RTU1C-3 8:40 AM
Lens-Integrated THz Imaging Arrays in 65nm CMOS Technologies
H. Sherry[2], R. Al Hadi[1], J. Grzyb[1], E. Oejefors[1], A. Cathelin[2], A. Kaiser[3], U. R. Pfeiffer[1], [1]University of Wuppertal, Wuppertal, Germany, [2]STMicroelectronics, Crolles, France, [3]ISEN, Lille, France

Abstract: THz CMOS imagers integrated with hyperhemispherical Si-lenses are presented for the first time. focal-plane arrays are designed and implemented in 65nm CMOS bulk and SOI. Measurements of the lens-integrated detectors at 0.65THz show an increase in the SNR of 15dB and 20dB compared to front-side illumination for SOI and bulk respectively. The detectors responsivities Rv are increased and a record minimum noise-equivalent power NEP of 17pW/√Hz is measured for SOI detectors with the Si-lens.

RTU1C-4 9:00 AM

Low Power Wideband Receiver and Transmitter Chipset for mm-Wave Imaging in SiGe Bipolar Technology

M. Tiebout[1], H. Wohlmuth[2], H. Knapp[2], R. Salerno[1], M. Druml[1], J. Kaeferboeck[1], M. Rest[2], J. Wuertele[2], S. S. Ahmed[3], A. Schiessl[3], R. Juenemann[3], [1]Infineon Technologies Austria, Villach, Austria, [2]Infineon Technologies, Munich, Germany, [3]Rohde & Schwarz, Munich, Germany

Abstract: A chipset for high resolution imaging systems operating at 78GHz is presented, with more than 7GHz of bandwidth for optimal depth of field. The frequency generation for both RX and TX ICs consists of a frequency quaddrupler. Both ICs contain 4 channels. The measured RX conversion gain is 23dB with a SSB NF below 10dB over a frequency range from 70 to 82GHz. The transmitter has an output power above 0 dBm in a frequency range from 77 to 85GHz. The power consumption per channel is below 160mW.

RTU1C-5 9:20 AM

A 90GHz Pulsed-Transmitter with Near-Field/Far-Field Energy Cancellation using a Dual-Loop Antenna

A. Arbabian, S. Kang, S. Callender, B. Afshar, J. Chien, A. M. Niknejad, UC Berkeley, Berkeley, United States

Abstract: A reflective, dual-loop, switching antenna utilizing near-field/far-field energy cancellation is integrated in a 90 GHz pulsed transmitter (TX). The TX features high ON/OFF ratio, antenna efficiency and PRF (up to 3.45GHz). It achieves a TX power of 10dBm with 18dB of power tuning. The pulse width is tunable between 46ps to 310ps and initial bistatic measurements distinguish 4 reflectors across a 6cm region signifying progress towards the development of a diagnostic medical imager in silicon.

Tuesday, 7 June 2011
10:00 AM
Room 337-338
Session RTU2A: Wideband Receivers and Building Blocks
Chair: Eric Fogleman, MaxLinear
Co-Chair: Pierre Busson, STMicroelectronics

RTU2A-1 10:00 AM
A Broadband Self-Healing Phase Synthesis Scheme
H. Wang[1], K. Dasgupta[2], A. Hajimiri[2], [1]Intel Corporation, Hillsboro, United States, [2]California Institute of Technology, Pasadena, United States

Abstract: This paper presents a full-range broadband phase synthesis scheme with autonomous phase correction functionality. The on-chip phase measurement is achieved by a set of on-chip LO self-/inter-mixing testing sequences, which eliminates the need for auxiliary test tones. As a design example, a 2-6GHz quadrature phase synthesis system in a 65nm CMOS is demonstrated. The phase self-healing scheme achieves an RMS phase error of less than 0.6° and a full 360° interpolation within the entire band.

RTU2A-2 10:20 AM
Double Quadrature Harmonic Rejection Architecture Insensitive to Gain and Phase Mismatch for Analog/Digital TV Tuner IC
J. Ryu, S. Cho, J. Lee, J. Kim, Y. Ku, K. Kwon, H. Kang, Samsung Electronics, Suwon, Republic of Korea

Abstract: Image and harmonic rejection are important performance parameters in wideband low-IF TV system. In this paper, double quadrature harmonic rejection architecture insensitive to gain and phase mismatch is proposed to satisfy stringent image rejection ratio(IRR) and harmonic rejection ratio(HRR) for analog/digital TV tuner IC. Fabricated in 0.13μm CMOS process, more than 60dB of the IRR is achieved over 42–864MHz RF frequency and more than 69dB of the 3rd HRR is achieved without any calibration.

RTU2A-3 10:40 AM
A Dual-band Digital TV Tuner for CMMB application SoC
H. Kim, S. Kang, J. Choi, T. Kim, B. Lee, J. Bae, W. Choo, H. Park, B. Park, Samsung Electronics, Yongin, Republic of Korea

Abstract: A dual-band digital TV tuner for CMMB application SoC is presented. The single-chip SoC satisfies all requirements of CMMB application with margin. Moreover, the SoC meets the GSM IOP which means the co-operation GSM transmitter and mobile TV reception. To suppress GSM transmitter signal in UHF band, LC-tuned load and tunable input matching scheme are adopted in UHF LNA. The measured sensitivity at UHF for the QPSK mode is -99.8dBm with ADC clock shift scheme.

RTU2A-4 11:00 AM
A 130nm CMOS 100Hz–6GHz Reconfigurable Vector Signal Analyzer and Software-Defined Receiver

A. Goel[1], B. Analui[2], H. Hashemi[3], [1]MediaTek USA Inc., San Jose, United States, [2]University of Southern California, Los Angeles, United States, [3]University of Southern California, Los Angeles, United States

Abstract: A monolithic 100Hz–6GHz reconfigurable Vector Signal Analyzer (VSA) and Software Defined Receiver (SDR), following a two-step up-down conversion heterodyne scheme with robustness to various wide-band interference scenarios, is presented. The 130nm CMOS chip does not require external filters or baseband processing to reduce the effect of interferences or harmonics. A monolithic VSA/SDR enables various commercial and military wireless solutions.

RTU2A-5 11:20 AM
Sub-THz Beam-forming using Near-field Coupling of Distributed Active Radiator Arrays

K. Sengupta, A. Hajimiri, California Institute of Technology, Pasadena, United States

Abstract: The paper demonstrates Distributed Active Radiator (DAR) arrays as a novel way of beam-forming at sub-THz frequencies in CMOS. Near-field coupling is shown as a scalable method for mutually locking multiple DAR elements to generate sub-THz beam of high power. As proofs of concept, the paper also shows beam-forming at near 200GHz for the 2x2 array with broadside EIRP of -1.9 dBm, total radiated power of 54 μW and beam-scanning range for approximately ± 30° in 2D space in 65nm CMOS.

Tuesday, 7 June 2011
10:00 AM
Room 339-340
Session RTU2B: Wide Tuning Range Oscillators
Chair: Waleed Khalil, Ohio State University
Co-Chair: Nobuyuki Itoh, Okayama Prefectural University

RTU2B-1 10:00 AM
A 5.6GHz to 11.5GHz DCO for digital dual loop CDRs
W. S. Titus, J. G. Kenney, Analog Devices, Somerset, United States

Abstract: A DCO is realized in 0.13μm CMOS using 4 cores for a 6 to 11GHz tuning bandwidth to provide the clock for an all digital D/PLL CDR circuit. Locked to maximum data rms jitter is 299 fs @ 9.953Gb/s (Sonet OC-192) from a DCO phase noise of -116dBc/Hz at 1MHz offset. The kDCO gain is 190 ppm/bit with less than 2:1 variation over the full BW. The DCO is novel in that it can track more than a 130°C temperature variation while the CDR maintains an error free lock to data.

RTU2B-2 10:20 AM
A 3.16–12.8GHz Low Phase Noise N-Push/M-Push Cyclic Coupled Ring Oscillator
M. M. Abdul-Latif, E. Sánchez-Sinencio , Texas A&M University, College Station, United States

Abstract: A topology for realizing wideband ring oscillators is introduced. Five three-stage ring oscillators operating over a frequency range of 1-2.56GHz are coupled using uni-lateral cyclic coupling. This provides phase shifted outputs which are combined twice in an N-Push or M-Push operation resulting in an output signal of 3.16-12.8GHz. The phase noise is -103.4 and -101.6 dBc/Hz at 1MHz offset for 3.16GHz and 12.8GHz, respectively. A prototype fabricated in 90nm CMOS.

RTU2B-3 10:40 AM
A 11.5-22GHz Dual-Resonance Transformer-coupled Quadrature VCO
S. Saberi, J. Paramesh, Carnegie Mellon University, Pittsburgh, United States

Abstract: A wide-tuning CMOS quadrature VCO (QVCO) is presented that uses a transformer-coupled resonator that enables quadrature coupling and facilitates alternative tuning methods including mutual inductance switching, magnetic tuning, and dual resonance mode switching besides the conventional capacitor tuning. The QVCO, fabricated in 130nm CMOS, can generate quadrature signals in the frequency range of 11.56-18.1GHz and 18.9-22GHz. The phase noise was measured -107dBc/Hz at 1MHz offset from 13.3GHz.

RTU2B-4 11:00 AM
A 25MHz-6.44GHz LC-VCO Using a 5-port Inductor for Multi-band Frequency Generation

W. Deng, K. Okada, A. Matsuzawa, Tokyo Institute of Technology, Tokyo, Japan

Abstract: This paper proposes a wide tuning range VCO for multi-band frequency generation. The wide band oscillator consists of a dual-mode LC-VCO using a 5-port inductor, and a divider chain. The proposed 5-port inductor provides two different inductances, which could support two resonances in a compact chip area. Thus, for LC-VCO, two operation modes are obtained to increase the tuning range. The experimental results achieve 25MHz-to-6.44GHz of continuous tuning range with a FoMT of -209dBc/Hz.

RTU2B-5 11:20 AM
A Single-LC-Tank 5-10GHz Quadrature Local Oscillator for Cognitive Radio Applications

J. Lu, N. Wang, M. F. Chang, University of California, Los Angeles, United States

Abstract: Presented is a local oscillator that converts 13.3-20GHz from a single-LC-tank VCO to the intended 5-10GHz. A 4-stage differential injection-locked ring oscillator is used to produce quadrature output phases without requiring 50% duty cycle of input signals, which greatly simplifies frequency extension circuits. Implemented in 65nm CMOS, the prototype LO consumes 22mA at 1V supply and exhibits a worst-case phase noise of -102dBc/Hz at 1MHz offset across the entire cognitive radio band.

Tuesday, 7 June 2011
10:00 AM
Room 341-342
Session RTU2C: mm-Wave Power Amplifiers
Chair: Freek van Straten, NXP Semiconductors
Co-Chair: Joseph Staudinger, Freescale Semiconductor

RTU2C-1 10:00 AM
A V-band Self-Healing Power Amplifier with Adaptive Feedback Bias Control in 65 nm CMOS
J. Liu[1], A. Tang[1], N. Wang[1], Q. J. Gu[2], R. Berenguer[3], H. Hsieh[4], P. Wu[4], C. Jou[4], M. F. Chang[1], [1]University of California, Los Angeles, Los Angeles, United States, [2]University of Florida, Gainesville, Gainesville, United States, [3]

Abstract: A self-healing 60GHz power amplifier with amplitude/phase compensation is realized in 65nm CMOS. An adaptive feedback bias scheme with three control knobs is proposed to extend linear operating region and enhance chip-to-chip performance yield. At a 1V supply, the PA achieves a Psat of 14.85dBm, a P1dB of 13.7dBm with a peak PAE of 16.2%. It has a 7GHz bandwidth. To our best knowledge, this PA provides the highest Psat and P1dB with simultaneous high PAE reported to date for a single PA.

RTU2C-2 10:20 AM
A Fully Integrated 60GHz Distributed Transformer Power Amplifier in Bulky CMOS 45nm
J. Essing, R. Mahmoudi, Eindhoven University of Technology, Eindhoven, Netherlands

Abstract: A 60GHz differential power amplifier (PA) based on a distributed active transformer (DAT) topology and implemented in 45nm CMOS technology is described. To cope with the asymmetric nature of DAT, resulting in common-mode and unequal differential voltage-swings at its input-ports, two universal methods which do not impose any layout restrictions and layout adjustments are presented. The PA achieves Po_1dB=13.2dBm, Po_sat=16.3dBm, PAE max is 8.7% and 18.7dBm OIP3, while consuming 178mA at 1.8V.

RTU2C-3 10:40 AM
A 94GHz Differential Power Amplifier in 45nm LP CMOS
N. Deferm[1], J. F. Osorio[2], A. de Graauw[2], P. Reynaert[1], [1]K.U.Leuven, Leuven, Belgium, [2]NXP Semiconductors, Eindhoven, Netherlands

Abstract: This paper presents a 94GHz 4-stage differential transformer-coupled power amplifier with capacitive neutralization. The use of transformers results in excellent common mode isolation between the different stages while providing a good impedance match. The neutralized differential pairs guarantee differential stability. The PA was designed in a 45nm LP CMOS technology.

RTU2C-4 11:00 AM

A 55-to-67GHz Power Amplifier with 13.6% PAE in 65nm standard CMOS

T. Wang, T. Mitomo, N. Ono, O. Watanabe, Toshiba Corporation, Saiwai-ku, Kawasaki, Japan

Abstract: A power amplifier covering 55-67GHz band is presented. The broadband performance is achieved owing to pi-section interstage matching network. Three-stage-current-reuse topology is proposed to enhance efficiency. The PA has been fabricated in 65nm CMOS. At 58GHz, 18dB power gain and 10dBm saturated power are achieved. The PA consumes current of 52mA and has a peak PAE of 13.6%. This work shows the highest PAE among the reported sub-1.2V PAs covering the worldwide 9GHz mm-Wave band.

RTU2C-5 11:20 AM

A 60GHz-band 20dBm Power Amplifier with 20% Peak PAE

Y. Zhao, J. R. Long, M. Spirito, Delft University of Technology, Delft, Netherlands

Abstract: A 3-stage, 60GHz transformer-coupled differential power amplifier is implemented in 130nm SiGe-BiCMOS. Common-base differential pairs extend BVCEO, while neutralization increases isolation, promoting stability. Self-shielded transformers, a combiner and splitter are designed for low loss and compact dimensions. Measured small-signal gain is 20dB with 10GHz -3dB bandwidth. Reverse isolation is 51dB across 50-65GHz. Maximum output power and peak-PAE are 20.5dBm and 20%, respectively, at 61.5GHz.

Session RTUIF: Interactive Forum
Chair: Jeffrey Walling, Rutgers University
Co-Chair: Haolu Xie, Fujitsu Microelectronics

RTUIF-1
A 144GHz 2.5mW Multi-Stage Regenerative Receiver for mm-Wave Imaging in 65nm CMOS
A. J. Tang[1], Z. Xu[2], Q. Gu[3], Y. Wu[4], M. Chang[1], [1]University of California, Los Angeles, Los Angeles, United States, [2]HRL Laboratories, LLC., Malibu, United States, [3]University of Florida, Gainesville, United States, [4]Northtrop Grumman Co

Abstract: This paper introduces the multi-stage regenerative receiver, an architecture that extends the super-regenerative receiver beyond the classical single-stage configuration to achieve higher gain and sensitivity. This makes the receiver ideal for mm-Wave imaging by relaxing the required illumination power in the link budget. The receiver is implemented in 65nm CMOS and achieves a sensitivity of -74 dBm, a NF of 10.2dB, consumes 2.5mW of power and occupies 0.02mm² of chip area.

RTUIF-2
A 9.5mW Analog Baseband RX Section for 60GHz Communications in 90nm CMOS
S. D'Amico[1], A. Spagnolo[1], A. Donno[1], P. Wambaq[3], A. Baschirotto[4], [1]University of Salento, Lecce, Italy, [2]IMEC, Leuven, Belgium, [3]Vrije Universiteit Brussel, Brussel, Belgium, [4]University of Milano-Bicocca, Milan, Italy

Abstract: The analog baseband section of a receiver for high data-rate 60GHz wireless communications is implemented in 90nm CMOS. Gain can be programmed from 0dB up to 20dB with 1dB step control, drawing 9.5mA (0-9dB gain range) or 10.8mA (10-20dB gain range) from a 1V supply. A 8.2dBm IIP3 and a 30.1dB NF are measured at 0dB gain. The entire baseband section occupies 400 x 390μm^2 die area.

RTUIF-3
A Direct Conversion Quadrature Transmitter with Digital Interface in 45nm CMOS for High-Speed 60GHz Communications
M. Abbasi[1], T. Kjellberg[1], A. J. de Graauw[2], R. Roovers[2], H. Zirath[1], [1]Chalmers University of Technology, Gothenburg, Sweden, [2]NXP Semiconductors, Eindhoven, Netherlands

Abstract: A 60GHz direct conversion quadrature transmitter is designed and fabricated in 45nm standard CMOS. The transmitter features an integrated PA with continuous level control and interfaces 300mVpp binary data signals. The measured modulation BW is limited by the setup to 4GHz but is simulated to be as high as 10GHz. The measured image suppression is 22dB with 36dB of carrier suppression corresponding to 8% EVM. The RF frequency can be 54-66GHz and the output power can be adjusted from -3dBm-10dBm.

RTUIF-4
94GHz Power-Combining Power Amplifier with +13dBm Saturated Output Power in 65nm CMOS

D. Sandström[1], B. Martineau[2], M. Varonen[1], M. Kärkkäinen[1], A. Cathelin[2], K. A. Halonen[1], [1]Aalto University, Espoo, Finland, [2]STMicroelectronics, Crolles, France

Abstract: A power combining power amplifier utilizing cascode topology and transformer-based matching elements is presented in this paper. The amplifier achieves +13dBm saturated output power at 94 GHz with a standard 1.2V supply and occupies an active area of only 0.069mm². The amplifier is implemented in an industrial 65nm CMOS process taking into account reliability issues at high output power level. The amplifier is also ESD-protected at the input and at the output.

RTUIF-5
Temperature-Dependent Scalable Large Signal CMOS Device Model Developed for mm-Wave Power Amplifier Design

N. Mallavarpu[1], D. Dawn[2], J. Laskar[3], [1]Georgia Institute of Technology, Atlanta, United States, [2]Georgia Institute of Technology, Atlanta, United States, [3]Samsung, Atlanta, United States

Abstract: This paper describes the development of an empirical large signal model for sub-100nm CMOS transistors and demonstrates its successful use in a 4-stage 60GHz CMOS power amplifier design. A novel drain-source current formulation is used along with optimized extraction for mm -Wave applications and temperature and size scalability, making this modeling approach highly robust.

RTUIF-6
A Transceiver Chipset for Automotive LRR and SRR Radar System at 76-81GHz in SiGe BiCMOS Technology

S. Trotta, Freescale Semiconductor, Munich, Germany

Abstract: We present a transceiver chipset consisting of a four channels Rx and a single channel Tx designed in a 200GHz fT SiGe BiCMOS technology. Each receiver channel shows a conversion gain of 20dB and noise figure of 10dB at 1MHz offset. The channel to channel isolation is 50dB. The transmitter includes two VCOs on the same die to switch between bands. The phase noise is of -96dBm/Hz at 1MHz offset. The output power is 2×13dBm. At 3.3V supply the Rx chip draws 270mA while the Tx 450mA.

RTUIF-7
A Compact-Size Dual-band (Tri-mode) Receiver Front-end with Switched Harmonic Mixer and Technology Scaling

H. Chen[1], K. Lin[2], T. Wang[3], S. Lu[4], [1]National Taiwan University, Taipei, Taiwan, [2]National Taiwan University, Taipei, Taiwan, [3]Chang-Gung University, Tao-Yuan, Taiwan, [4]National Taiwan University, Taipei, Taiwan

Abstract: A new dual-band receiver front-end for 2.5GHz and 4.9 to 5.9GHz is proposed in 90nm CMOS technology. The proposed receiver front-end embraces a 2.5/5~6GHz dual-band LNA, a switchable harmonic mixer, an octuple-phase generator, and a wideband 10GHz PLL. By scaling technology, the chip size for LO part is reduced readily (41.7-94.9% reduction). A low power dissipation is due to short routing path of the new proposed frequency planning.

RTUIF-8
An 8GHz, 0.45dB NF CMOS LNA Employing Noise Squeezing
W. Lee, E. Afshari, Cornell University, Ithaca, United States

Abstract: A LNA using noise squeezing is designed in a 65nm CMOS. The noise squeezing occurs through phase sensitive gain implemented by the degenerate parametric process. This process is carried out inside a nonlinear resonator where energy transfers from a pump to the signal. When the pump frequency is twice that of the signal, the amplifier suppresses one of two quadrature components of the input noise. This concept is exploited to realize an 8GHz LNA with 0.45dB NF for non-suppressed quadrature.

RTUIF-9
A Large-Signal Blocker Robust Transimpedance Amplifier for Coexisting Radio Receivers in 45nm CMOS
A. Pérez-Carrillo[1], S. S. Taylor[2], J. Silva-Martinez[1], A. I. Karşılayan[1], [1]Texas A&M University, College Station, United States, [2]Intel Corporation, Hillsboro, United States

Abstract: A baseband TIA for coexisting radio receivers is presented. It exploits active feedback to improve out-of-band large-signal attenuation, minimizing in-band distortion due to close-in blockers. Experimental results verify that the proposed design handles tones of ±10 mA linearly, and withstands blocking currents of ±9mA at 50MHz before reaching P1dB in a 10MHz BW. The fully-differential 45nm CMOS prototype draws 17mA from 2.5V and occupies 0.25mm².

RTUIF-10
Ultra-Low Power FSK Wake-up Receiver Front-End for Body Area Networks
M. Lont[1], D. Milosevic[1], G. Dolmans[2], A. H. Roermund[1], [1]Eindhoven University of Technology, Eindhoven, Netherlands, [2]Imec-nl, Eindhoven, Netherlands

Abstract: In this paper, we present an ultra low-power Wake-up Receiver front-end operating in the 868/915MHz ISM band. It targets short distance body area networks. Its power consumption is only 126μW, including a low-power on-chip ring oscillator. Since the receiver targets small transmission distances, up to 10m, sensitivity is traded against power consumption. This is achieved by removing the LNA and making all the gain at the low IF frequencies. The receiver sensitivity is -65dBm at a BER of 0.1%.

RTUIF-11
Low-Voltage Low-Power Combined LNA-Single Gate Mixer for 5GHz Wireless Systems
M. A. Abdelghany[1], R. Pokharel[2], H. Kanaya[1], K. Yoshida[1], [1]Kyushu University, Graduate School of Information Science and Electrical Engineering, Nishi-ku, Japan, [2]E-JUST Center, Nishi-ku, Japan

Abstract: This paper describes design of a low-voltage low-power LNA merged with a fully differential double-balanced single gate mixer for 5GHz wireless systems. The system had been designed to operate in subthreshold region for low-power dissipation. The design has been fabricated using TSMC 0.18μm 1P6M CMOS process. At 1mW power consumption from 1V supply voltage, the proposed LNA-mixer design achieves a conversion gain of 27dB and a SSB-NF of 19dB. Measured IIP3 is –3dBm with LO input power of -5dB

RTUIF-12
A 1.2V 0.1-3GHz Software-Defined Radio Receiver Front-End in 130nm CMOS

M. Cao, B. Chi, C. Zhang, Z. Wang, Institute of Microelectronics, Tsinghua University, Beijing, China

Abstract: A wideband SDR receiver front-end is presented. It utilizes the current-driven passive down-conversion system with 25% duty-cycle LO to cover 0.1 to 3GHz range with 3-65MHz baseband bandwidth and 35-55dB conversion gain independently reconfigurability. 3.5-6dB DSB NF and higher than 10dBm OIP3 are obtained in a wide operating frequency range. Additionally, power consumption scalability(14.5mA to 48.5mA) can be achieved by exploiting power/performance trades-offs, and the die area is 2.0x1.2mm².

RTUIF-13
A low noise amplifier simultaneously achieving input impedance and minimum noise matching

B. Kim, D. Im, J. Choi, K. Lee, KAIST, Daejeon, Republic of Korea

Abstract: A CMOS complementary capacitive loaded LNA with inductively source degeneration is implemented. Owing to the capacitive loading technique, the noise figure (NF) of the proposed LNA can be perfectly close to NFmin while maintain the source impedance matching without increasing the source degeneration inductor. The measurements demonstrate that the LNA has a power gain of 12 dB, a NF of 1dB, an IIP3 of +7.7dBm, and an input P1-dB of -5dBm at 900MHz while drawing 16.2mW supply voltage.

RTUIF-14
Differential Source-Pull on the WCDMA Receiver

C. H. Guan, C. Liu, Broadcom, Irvine, United States

Abstract: A practical approach to source-pull differential input LNA is presented using a single-ended RF tuner adapted by a balun. The adaptation only considers balun's differential mode S-parameters. Error analysis on neglecting common mode S-parameters provides guidelines to choose proper balun. The approach is applied to the NF optimization on a cellular WCDMA receiver. The resultant source pull estimation correlates well with the final optimal matching network. The minimum NF is achieved at 2.3dB

RTUIF-15
A 50% Duty Cycle Wide-Locking Range Divide-By-3 Divider up to 6GHz

C. Y. Zhou, L. Zhang, L. Zhang, Y. Wang, Z. P. Yu, H. Qian, Tsinghua University, Beijing, China

Abstract: A divide-by-3 CML divider based on three coupling delay cells with 120° phase splitting injection signals is demonstrated in 0.18μm CMOS process in this paper. The active inductor tanks are used to extend the working frequency. According to the proposed behavior model, locking range and some useful design guidelines are developed. The measured results proves that this divider has realized a true 50% duty cycle output at a high input frequency of 6.5GHz with only 4mW power consumption.

RTUIF-16
A Multi-GHz 130ppm Accuracy FLL for Duty-Cycled Systems

X. Wang, B. Busze, J. Romme, R. M. Vinella, C. Zhou, K. Philips, H. de Groot, Holst Centre, IMEC-NL , Eindhoven, Netherlands

Abstract: A frequency-locked-loop optimized for output frequency accuracy and locking time is implemented in a 90nm CMOS technology. The output frequency ranges from 7-9.8GHz with a reference frequency at 130MHz. The accuracy of the output frequency is 130ppm by minimizing and dithering the fine tuning bits of the oscillator. The estimated locking-time is below 50 reference clock cycles, thanks to the frequency locking nature. The implementation offers itself a suitable solution for duty cycled system.

RTUIF-17
Closed-Loop Spurious Tone Reduction for Self-Healing Frequency Synthesizers

F. Bohn, K. Dasgupta, A. Hajimiri, California Institute of Technology, Pasadena, United States

Abstract: On-chip spurious tone detection and correction in an 8-12GHz CMOS synthesizer is used to automatically reduce spurious output tones at different offset frequencies by up to 20dB. Using synchronous detection, sensitivity is limited by detection time only. The presented methods are generally applicable to frequency synthesizers and phased-locked loops in various applications.

RTUIF-18
A Triple Band Travelling Wave VCO Using Digitally Controlled Artificial Dielectric Transmission Lines

N. Buadana, E. Socher, Tel Aviv University, Tel Aviv, Israel

Abstract: A compact, triple output travelling wave oscillator with combined analog and digital control is presented. Based on an eight phase rotary oscillator employing shielded digitally controlled transmission lines, X, K and Q band outputs are generated using a buffer, a push-push buffer and a quad-push. Fabricated in standard 0.18μm CMOS it occupies 0.48mm² and consumes 64mW. The circuit exhibits 5.5% tuning range in each band, a phase noise of -108 dBc/Hz at 1MHz offset and -1dBm of output power.

RTUIF-19
A Spur-Frequency-Boosting PLL with a -74dBc Reference-Spur Rejection in 90nm Digital CMOS

M. M. Elsayed, M. Abdul-Latif , E. Sánchez-Sinencio, Texas A&M University, College Station, United States

Abstract: An architectural solution for designing a low-reference-spur PLL is proposed. A spur frequency-booster is inserted between the phase-frequency-detector and the charge pump to boost the charge pump's input frequency. Hence, the reference-spurs theoretically vanish. The proposed technique reduces the spur level without sacrificing neither the loop bandwidth nor the VCO's gain. The prototype achieves -74dBc reference-spur suppression along with (KVCO/fref) ratio of 17 at a (fBW/fref) ratio of 1/20.

RTUIF-20
A Simple, Unified Phase Noise Model for Injection Locked Oscillators
S. Kalia, M. Elbadry, B. Sadhu, S. Patnaik, R. Harjani, University of Minnesota, Minneapolis, United States

Abstract: A unified phase noise model for injection locked oscillators is presented. An ILO has been shown to be identical to a type-I first-order PLL. The model predicts the phase noise of ILOs, injection locked frequency dividers (ILFD), and injection locked frequency multipliers (ILFM) as a function of the injection source phase noise and the oscillator phase noise. Measurement results from a discrete 57MHz Colpitts ILO, an integrated 6.5GHz ILFD, and an integrated 24GHz ILFM are presented.

RTUIF-21
A 22µW, 2.0GHz FBAR Oscillator
A. Nelson[1], J. Hu[1], J. Kaitila[2], R. Ruby[2], B. Otis[1], [1]University of Washington, Seattle, United States, [2]Avago Technologies, San Jose, United States

Abstract: We present a 22µW, 2.0GHz FBAR oscillator - the lowest power reported to date for a GHz-range oscillator of this type. Low power consumption is achieved through co-design with a high Rp FBAR and a weakly-forward biased bulk connection. An oscillator with a standard bulk connection was fabricated for comparison. The chip was fabricated in a 0.18µm CMOS process. The weakly-forward biased bulk led to a 41% reduction in power dissipation. The measured phase noise is -121dBc/Hz at a 100kHz offset.

RTUIF-22
DCO with Built-In Compensation for TBF Mismatch
O. E. Eliezer[1], B. R. Staszewski[2], S. K. Vemulapalli[3], [1]Xtendwave, Dallas, United States, [2]Delft University of Technology, Delft, Netherlands, [3]Texas Instruments, Dallas, United States

Abstract: A novel fully-digital compensation mechanism for mismatches in a frequency-tuning capacitor array is demonstrated in a 65nm CMOS GSM/EDGE Digital RF Processor (DRP) based transceiver. It addresses the inevitable mismatch between the smallest frequency step supported by the integer portion of the frequency-tuning array and the dithering-based fractional portion that array.

RTUIF-23
A 1Mb/s 3.2-4.4GHz Reconfigurable FM-UWB Transmitter in 0.18µm CMOS
B. Zhou[1], H. Lv[1], M. Wang[1], J. Liu[1], W. Rhee[1], Y. Li[1], D. Kim[2], Z. Wang[1], [1]Tsinghua University, Beijing, China, [2]Samsung Advanced Institute of Technology, Suwon, Republic of Korea

Abstract: This paper presents a 1Mb/s FM-UWB transmitter for robust non-invasive short range communications. A 51MHz 8 modulo fractional-N PLL with a relaxation VCO is designed to generate a 2FSK modulated triangular waveform which directly modulates an RF oscillator. A 3.2-4.4GHz reconfigurable FM-UWB transmitter whose center frequency and RF bandwidth can be digitally controlled is implemented in 0.18µm CMOS, achieving the data rate higher than the reported by at least four times.

RTUIF-24
A 23µA RF-Powered Transmitter for Biomedical Applications
F. Zhang, M. A. Stoneback, B. P. Otis, University of Washington, Seattle, United States

Abstract: We propose a new tag architecture that employs an active transmitter to decouple the frequencies used for power and data telemetry. Receiving power at 918MHz and transmitting data at 306MHz reduces the complexity of reader design and extends the data transmission range. Injection-locking avoids LO generation circuitry and eliminates quartz crystals. With an on-off keying data rate of 4Mbps, the 23µA transmitter with an output power of -33dBm achieves an energy efficiency of 10pJ/bit.

RTUIF-25
Highly-Linear FM Transmitter for Mobile Applications in 65nm CMOS
B. P. Ginsburg[1], K. Nagaraj[1], N. Nayak[1], M. Ozgun[3], K. Subburaj[2], S. Murali[2], F. Ledesma[1], [1]Texas Instruments, Dallas, United States, [2]Texas Instruments, Bangalore, India, [3]Icera, Richardson, United States

Abstract: An FM frequency synthesizer and antenna driver with 63dB SNR, 0.1% THD, and -101dBc out-of-band emissions at 124dBµV output swing in 65nm digital CMOS is described. The optimized FLL incorporates a DCO with a highly linear capacitor array and flicker noise reduction techniques. Cascaded filtering and a segmented driver improve efficiency and tuning range with minimal high-order distortion.

RTUIF-26
A Class-C Power Amplifier/Antenna Interface for Wireless Sensor Applications
K. Natarajan[1], J. S. Walling[2], D. J. Allstot[1], [1]University of Washington, Seattle, United States, [2]Rutgers University, Piscataway, United States

Abstract: A class-C PA for operation as an antenna interface in body sensor network (BSN) applications is presented. The PA is fabricated in a 0.13µm RF CMOS process for operation in the 400MHz MedRadio band. It achieves a measured peak output power and drain efficiency of -4dBm and 43%, respectively.

RTUIF-27
A 19 dBm 0.13µm CMOS Parallel Class-E Switching PA with Minimal Efficiency Degradation under 6 dB Back-off.
N. Singhal, N. Nidhi, A. Ghosh, S. Pamarti, University of California Los Angeles, Los Angeles, United States

Abstract: This paper implements a digital Zero Voltage Switching (ZVS) Contour based power amplifier previously proposed by the authors in [1]. The proposed PA implemented in 0.13µm digital CMOS technology, achieves a peak power of 19dBm at a peak drain efficiency of 23% and peak power added efficiency (PAE) of 18% at a center frequency of 800MHz from a 1.2V supply. The PA achieves an average drain efficiency of 20% and an average PAE of 15% while generating OQPSK signal with bandwidths up to 20Mbps.

RTUIF-28
Large-Signal Characterization and Modeling of MOSFET for PA Applications
S. Lee, T. Lee, Skyworks Solutions, Inc., Irvine, United States

Abstract: This paper discusses the large-signal model requirements and generation as well as the 1 and 2 tone large-signal characterization for transistors used in CMOS PA design. It is demonstrated that an accurate modeling of Gm as a function of bias, as well as other important extrinsic transistor parameters, enables proper prediction of the 1 tone distortion behavior for a transistor, which in turn determines the quality of prediction for the 2 tone intermodulation product up to the 5th order.

RTUIF-29
Towards Cognitive Built-in-Self-Test (BIST) for Reconfigurable On-Chip Applications
S. Wane, B. Elkassir, C. Kelma, NXP-Semiconductors, Caen, France

Abstract: This paper introduces the concept of cognitive BIST system for reconfigurability of on-chip function blocks. Feasibility of cognitive BIST for reconfigurability of on-chip functions is demonstrated based on design of scalable LNA gain, programmable automatic oscillation amplitude control of PLL reference VCOs and dynamic EVM estimation of IQ systems.In all aforementioned applications impacts of BIST circuits on system performances are evaluated based on simulation and experimental verifications.

RTUIF-30
An active filter achieving 43.6dBm OIP3
H. H. Kim, M. Green, B. A. Miller, A. Bolstad, D. D. Santiago, MIT Lincoln Laboratory, Lexington, United States

Abstract: An active filter with a 50Ω buffer suitable as an anti-alias filter to drive a highly linear ADC is implemented in 0.13μm SiGe BiCMOS. This 6th-order Chebyshev filter has a 3dB cutoff frequency of 28.3MHz and achieves 36.5dBm OIP3. Nonlinear digital equalization further improves OIP3 to 43.6dBm. Measurements show 92dB of rejection at the stopband and a gain of 49dB. The measured in-band OIP3 of 43.6dBm is 19dB higher than previously published designs.

RTUIF-31
A 3.5-4.5-GHz Ultra compact 0.25mm2 Reflection-type 360° Phase Shifter
W. Li[1], J. Tsai[2], M. Huang[1], T. Huang[1], [1]National Taiwan University, Taipei, Taiwan, [2]National Taiwan Normal University, Taipei, Taiwan

Abstract: An ultra-compact reflection-type phase shifter (RTPS) with full 360° continuous phase shift and low insertion loss using standard 0.18μm CMOS technology is demonstrated in this paper. Dual active reflection load using active inductor is utilized in the proposed reflection-type load to cover 360° phase tuning through only one quadrature hybrid, which has the advantages of compact chip size, low insertion loss, and low loss variation.

RFIC2011 Panel Sessions

Monday, 6 June 2011
12:00 PM – 01:00 PM · Rooms 307-308

Software Defined Radios - Facts and Fantasies

Chairs/ Moderators: **Lawrence Kushner,** Intersil Corp.
Timothy Hancock, MIT Lincoln Laboratory

Panelists: **Geoff Dawe,** BWS Consulting
James Kimery, National Instruments
Larry Larson, UCSD
Kamal Sahota, Qualcomm
Bruce Fette, DARPA
Vanu Bose, Vanu, Inc.

Sponsor: **RFIC**

Abstract: The concept of Software Defined Radios (SDR) originated decades ago in the defense sector, culminating in the development of a number of successful SDR demonstrations and deployments. The flexibility of SDR, being able to serve a wide variety of changing radio protocols offers the military interoperability and maintainability not achievable with conventional radios.

Research in Software Defined Radios has accelerated during the past two decades, with work in universities, industry, and government advancing the concepts. Simultaneously, the relentless march of Moore's Law has made digital processing almost free, shifting more and more of the radio processing into the digital domain. The "Holy Grail" of SDR, an antenna followed by an Analog-to-Digital Converter (ADC) and high-performance Digital Signal Processor (DSP) now seems within reach. Similarly, one can conceive of the transmit path consisting of a DSP followed by a DAC and a power amplifier. Do these architectures make sense? Is SDR the best solution in terms of size, weight, power, cost, and cost-of-ownership or is reconfigurable conventional RF hardware with a standard software interface a better solution?

Our panel of experts will discuss and debate the current state-of-the-art of radio design, and how SDR fits in. We will discuss what is a Software-Defined Radio, what applications are best suited for SDR, and where future SDR research is heading. The audience will be encouraged to participate as well, submitting questions for the panel, engaging in the discussion, and voting, in real-time, "fact" or "fantasy" after each topic of debate using an rf audience response system.

Tuesday, 7 June 2011
12:00 PM – 01:00 PM · Rooms 307-308

What is the limit of multi-radio integration … or rather, is it 'disintegration'?

Panel Organizer: **R. Bogdan Staszewski,** Associate Professor, Delft University of Technology

Moderator: **Oren Eliezer,** CTO, Xtendwave

Panelists: **R. Bogdan Staszewski,** Associate Professor, Delft University of Technology
Andre Hanke, Senior Principal RF System Engineer, Intel
Walid Ali-Ahmad, Technical Director, Mediatek
Keith Carter, WLAN Senior Manager, Broadcom
Fred Schindler, Director, RFMD
Thomas Kazior, Principal Engineering Fellow, Raytheon

Abstract: Only a decade ago, single-chip RF-SoC integration was universally thought to be impossible or at least uneconomical. Nowadays, the pioneering days of single-chip radios are largely over and the innovation efforts are applied to integrating multiple radio cores on the same silicon die. This effort has already resulted in commercial offerings of multi-core wireless connectivity and cellular radios from a few companies, but has revealed some interesting RF co-existence issues: Integrating additional radio cores appears to exponentially increase the overall design and productization complexity, more so than in the case of isolated radios. Why is that and what can be done to address that? What is the ultimate limit of multi-core radio integration?

As new wireless standards continue to emerge, it becomes necessary to support additional frequency bands and wider modulation bandwidths, while maintaining backwards compatibility with the existing standards. This puts enormous pressure on the complexity and quality of RF front-end components (PA's, T/R switches, band-pass filters and duplexers) to the point that they predominate in both cost and occupied space, which might suggest the reversal of the integration trend. Can the ever multiplying antenna-interfacing components still be integrated? Do they follow a different integration path from that of RF-SoCs? Does the optimal system partitioning suggest the RF-SoC 'disintegration'?

The panel of distinguished experts, representing three camps (RF-SoC, RF module and compound semiconductor integration), will deliberate this interesting topic with the audience's participation.

WORKSHOPS AND SHORT COURSES

Workshops are offered on Sunday, Monday and Friday of Microwave Week. The workshops present the state of the art within a specific topic to specialists who are already experienced in the area. Short courses are also offered on Sunday and Monday, providing excellent learning experiences within critical microwave topics. All workshops and short courses will be held at the Baltimore Convention Center. Specific room assignments will be announced at check-in.

RFIC AND IMS SPONSORED SUNDAY WORKSHOPS

8:00 AM – 5:20 PM

WSA: Introduction to GaN MMIC Design

Organizers: **Bernie Geller**, *Vadum, Inc.*
Ed Niehenke, *Niehenke Consulting*
Rüdiger Quay, *Fraunhofer Institute*
Tim Lee, *The Boeing Company*

Abstract: This workshop will cover the important and current topic of RF GaN MMIC Design. Workshops in previous years have addressed GaN technology in general, including basic material characteristics, reliability issues, packaging issues, and system implications. This workshop will be educational in nature, with significant time allotted for audience questions and participation. In addition to the usual Q&A time after each talk, we are planning to have an open panel session at the end of the day in which all of the speakers will participate and answer questions from the audience. We encourage attendees to bring questions, design issues, and design hints that they would like to share.

The first presentation will provide an overview of GaN MMIC design, focusing on similarities and differences in the design process between GaAs and GaN MMICs. This will be followed by papers addressing specific designs for radar and communications systems, mm-Wave applications, and "passive" applications such as high power RF switches. The afternoon session will start with a paper discussing issues related to the design and layout of passives and GaN MMICs at mm-Wave frequencies, followed by a paper discussing GaN MMIC processing options and circuit simulation techniques. The final presentation will provide an overview of current non-linear models for GaN devices, including similarities (and differences) with GaAs models and areas where new models are needed.

Speakers:

1. **Thomas Winslow**, *M/A-COM Technology Solutions*, "An Overview of GaN MMIC Design"
2. **Bill Pribble**, *Cree RF and Microwave Products*, "GaN MMIC Design for Radar and Communications Applications"
3. **James Schellenberg**, *QuinStar Technology, Inc.*, "mm-Wave GaN Power MMICs: Design and Status"
4. **Charles F. Campbell**, *TriQuint Semiconductor*, "High Power Switch MMIC Design with Gallium Nitride Transistors"
5. **Rüdiger Quay**, *Fraunhofer Institute of Applied Solid-State Physics (IAF),* "Design, Layout, and Modeling of mm-Wave GaN Passives and MMICs"

6. **Harris (Chip) Moyer**, *HRL Laboratories*, "GaN MMIC Technology and Circuit Simulation Techniques"
7. **Walter R. Curtice**, *W. R. Curtice Consulting*, "Status of Linear and Nonlinear GaN Modeling for MMICs"

8:00 AM – 5:20 PM

WSB: Advancements and Challenges Toward Radio-in-Package and Radio-on-Chip

Organizers: **Kenjiro Nishikawa**, *Kagoshima University*
Noriharu Suematsu, *Tohoku University*
Pierre Busson, *ST Microelectronics*
Eric Kerherve, *IMS Laboratory*

Abstract: Advanced wireless communication systems require multi-functionality and miniaturization of their modules, irrespective of frequency or system. A recent development trend is how we can integrate complete functions on a chip or in a package to achieve a real "radio-in-package" or "radio-on-chip". A design challenge of integrated antennas is the most interesting issue. This workshop will focus on design innovations of radio-in-package/radio-on-chip and the evaluation methods of highly integrated system-in-package/system-on-chip with antennas. Presentation topics will cover integrated antenna design techniques, measurement and evaluation techniques for fully-integrated mm-Wave system-in-package/system-on-chip, reduction of crosstalk and interference, power management techniques of chip/package for phased-array systems, and thermal management techniques of chip/package for phased array system.

Speakers:

1. **Gabriel Rebeiz**, *UCSD*, "mm-Wave Wafer-Scale Phased Arrays and System-on-Chip"
2. **Sorin Voinigescu**, *University of Toronto*, "D-Band Radio and Imaging Transceivers with On-Die Antennas"
3. **Aydin Babakhani**, *Rice University*, "Large-Scale Radiating ICs"
4. **Byunghoo Jung**, *Purdue University*, "The Role of Wireless Inter- and On-Chip Links in Future SoC"
5. **C. Patrick Yue**, *UCSB*, "Fully Integrated Transmitters with Embedded Antenna for On-Wafer Wireless Testing"
6. **Yongxin Guo and Fujiang Lin**, *National University of Singapore*, "New Developments in On-Chip Antennas and Antenna-in-Package for 60-GHz Applications"
7. **Noriharu Suematsu**, *Tohoku University*, "A 60-GHz Ultra Small RF Module with Antenna using 3-D SiP Technology"
8. **Tomohiro Seki**, *NTT Corporation*, "mm-Wave System-in-Package Technology"
9. **Romain Pilard**, *STMicroelectronics France*, "System-in-Package Integrated Antennas in Industrial and Prospective Packages for mm-Wave Applications"
10. **Yoshimasa Sugimoto**, *Kyocera Corp.*, "Ceramic Package with Antenna for 60-GHz WPAN Application"

11. **Dong G. Kam and Scott Reynolds**, *IBM*, "Low-Cost Antenna-in-Package Solutions for 60-GHz Phased-Array Systems"

8:00 AM – 5:20 PM

WSC: Imaging at mm-Wave and Beyond

Organizers: **Arun Natarajan**, *IBM T. J. Watson Research Center*
Fujiang Lin, *University of Science and Technology of China*
Payam Heydari, *University of California, Irvine*

Abstract: Advances in device technologies are making mm-Wave imagers both technologically viable and commercially attractive. These imagers are now targeting exciting applications that capitalize on the unique characteristics of the mm-Wave spectrum. This workshop will present recent developments in mm-Wave imaging, focusing on imagers for security, spectroscopy and clinical diagnosis. Speakers will address the different specifications, architectures and technology tradeoffs for such applications and present passive and active imagers in III-V as well as CMOS device technologies.

Speakers:

1. **Albert Pergande**, *Lockheed Martin*, "The History and Challenges of Passive Millimeter Wave Imaging"
2. **Jonathan Lynch**, *Hughes Research Lab*, "W-band Sensors for Passive Millimeter Wave Imaging"
3. **Arttu Luukanen**, *VTT Technical Research Centre of Finland*, "Passive and Active sub-mm-Wave Imaging for Stand-Off Security Screening Applications"
4. **Frank De Lucia**, *Ohio State University*, "Electronic Approaches to Sensor Applications in the THz Spectral Region: The Intersection of Physics and Technology"
5. **Bhaskar Banerjee**, *University of Texas, Dallas*, "Millimeter and Sub-Millimeter Wave Imaging and Spectroscopy in CMOS"
6. **Ullrich Pfeiffer**, *University of Wuppertal*, "Silicon Solutions for Sub-Millimeter Wave Imaging"
7. **Adrian Tang and Frank Chang**, *University of California, Los Angeles*, "Advantages of CMOS Receivers for Millimeter and Sub-Millimeter Imaging"
8. **Mikael Persson**, *Chalmers University of Technology*, "Clinical Systems for Microwave Imaging and Diagnostics and Treatment"

8:00 AM – 5:20 PM

WSD: Re-configurability Requirements for Multi-Standard Low-Power Operation

Organizers: **Gernot Hueber**, *NXP Semiconductor, Austria*
R. Bogdan Staszewski, *TU Delft, The Netherlands*
Stefan Heinen, *RWTH Aachen University, Germany*

Abstract: Advances in fabrication technology have enabled the use of scaled CMOS in today's highly-integrated RF transceivers for wireless communications. However, multi-band and multi-mode radios covering the diversity of communication standards from 2G GSM, 3G UMTS, to 4G LTE and LTE-advanced as well as WLAN, BT, and GPS impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications.

For base stations to achieve the first steps towards reconfigurability, the excessive usage of compound technologies needs to be changed into the use of Si-based circuit technologies enabling the integration step.

However, integration on one hand features the possibility for implementing a significant computational power and complex functionality directly on a single IC, on the other hand it shows poor performance in RF circuits compared to other technologies. The focus of this workshop will be on the challenges and requirements the wireless standards pose on future multi-radio operation, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in a low-power multi-radio SoC or SiP for terminals and base-stations. Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-end.

Speakers:

1. **Jan Craninckx**, *IMEC, Leuven, Belgium*, "SAW-less Radio Transceivers in 40nm CMOS"
2. **Earl McCune**, *Highspeed and Wireless, CA*, "Unifying PA Approaches for Multi-Standard Low-Power Operation"
3. **Art Morris**, *WiSpry, Irvine, CA*, "High-Performance Digitally Reconfigurable RF Front Ends"
4. **Larry Larson**, *Universiy of California, San Diego, CA*, "Low-Power Multi-Standard Transmitters in Nanoscale CMOS"
5. **Domine Leenarts**, *NXP, The Netherlands*, "Base Stations: The First Steps Towards Re-configurability"
6. **Michael Youssef**, *Broadcom Corporation, Irvine, CA*, "Open-Loop Polar Transmitters for Cellular Application"
7. **R. Bogdan Staszewski**, *TU Delft, The Netherlands*, "Recent Advancements and Future Directions in Digital RF and Digitally-Assisted RF"
8. **Ranjit Gharpurey**, *University of Texas, TX*, "Linearity Enhancement Techniques for Multi-Standard Radio Systems"
9. **Walid Ali-Ahmad**, *MediaTek,* "Towards Reconfigurable Multi-Standard Multi-band Radios: Key System Issues and Architecture Concepts"

8:00 AM – 5:20 PM

WSE: Advancements in Linear Power Amplifiers for Cellular Infrastructure

Organizers: **Joseph Staudinger**, *Freescale Semiconductor, Inc.*
David Runton, *RFMD, Inc.*
Freek van Straten, *NXP*

Abstract: Cellular infrastructure equipment market forces are demanding improvements in power amplifier performance in terms of power, efficiency and linearity for increasingly wider bandwidth signals. This challenge is being addressed with research and advancements on several fronts, including device technology (Si LDMOS, GaAs HBT, GaN), PA circuit architecture (Doherty circuits and high power ICs), and more effective PA linearization techniques. This workshop will feature experts detailing their solutions to these complex issues and sharing their insight of future research activities.

Speakers:

1. **Bill Vassilakis**, *Empower RF Systems Inc.*, High Performance Amplifier Solutions for LTE and Beyond
2. **John Wood and Peter H. Aaen**, *Freescale Semiconductor, Inc.*, Circuit Models for High-Power RF Transistors
3. **John Gajadharsing**, *NXP*, "Recent Advances in Doherty PAs"
4. **Margaret Szymanowski**, *Freescale Semiconductor, Inc*., "Advances in High Power LDMOS Integrated Circuit Amplifiers"
5. **Craig Steinbeiser and Oleh Krutko**, *TriQuint Semiconductor*, "High Power GaAs HVHBT Power Amplifiers"
6. **Christopher Burns**, *RFMD*, "Advancements in GaN Technology "
7. **Roland Sperlich**, *Texas Instruments*, "Linearization Trends for Wireless Infrastructure PAs"

8:00 AM – 5:20 PM

WSF: EMI-Compliant Product Design Practices: Interference Analysis, Floorplanning, Grounding Strategies, Chip-Package-Board Co-Design

Organizers: **Rick Janssen**, *NXP Semiconductors*
Vivek Bhan, *Fujitsu Microelectronics America Inc.*
Oren Eliezer, *Xtendwave*

Abstract: With the integration of RF, mixed signal and digital building blocks on a single die, combined with the trend to go to higher frequencies to accommodate for higher data rates, it is essential to consider various on-chip coupling effects in the early design phases of the RFIC.

Additionally, provisions should be made at the application level by reducing the impact of peripheral interactions (between chip, package, board, antenna, etc.), as well as the potential for self-

interference, such that these are either eliminated or can be resolved on the fabricated product in order to reduce the number of re-spins.

The focus of this interactive workshop will be on preventing EMI problems by applying a number of measures in the early design phase: interference analysis, coupling-aware RFIC floor planning, grounding strategies, chip-package-board co-design practices, frequency planning, clock generation strategies, and modeling and CAD/EDA capabilities to address coupling effects. Recognized Experts in the semiconductor industry will present actual issues encountered in their designs and the solutions/design practices that can be used to address such issues in the early design phase. Interactive discussions will be facilitated to exchange valuable ideas for the benefit of participants and the semiconductor industry at large.

Speakers:

1. **Vivek Bhan**, *Fujitsu Microelectronics America, Inc*., "Signal Isolation in a 2G/3G/4G Multimode Cellular Transceiver with Digital Interface"
2. **Christian Stockreiter**, *Austriamicrosystems AG*, "Simulation of Electromagnetic Interference from ICs Experienced during System Level EMC Tests"
3. **Jan Niehof**, *NXP Semiconductors*, "Optimal RFIC Floorplanning and Grounding Strategies"
4. **Oren Eliezer**, *Xtendwave*, "Fundamentals of Self-Interference Analysis and Prevention in Complex RF SoCs"
5. **HeeSoo Lee[1], Yi Cao[2], Wenjun Shi[2]**, *[1]Agilent Technologies, [2]RIM,* "The Effect of Digital Noise on RF Receiver Sensitivity in Modern Smart-Phones Applications"
6. **Davide Pandini**, *STMicroelectronics*, "Electromagnetic Interference Reduction on an Automotive Microcontroller"
7. **Ram Sadhwani** , *Intel*, "Radio Co-existence Challenges in Multi-Comm SoCs"

8:00 AM – 5:20 PM

WSG: New Architectures for Digitized Receivers

Organizers: **Didier Belot**, *ST Microelectronics - Crolles*
Julien Ryckaert, *IMEC*

Abstract: The recent growth of circuit techniques that leverage the high speed capabilities of deep submicron CMOS devices is gradually renovating the architectures of RF communication systems. The high speed resources of digital circuits allow a redistribution of wireless transceiver functionality among the analog and digital domains. In a receiver, this trend leads to a complete repositioning of the analog to digital conversion and a reassessment of the classical analog signal conditioning that precedes it. Aiming at highly digitized receiver architectures, several disruptive techniques have recently been proposed to reach this paradigm shift as will be presented in this workshop. Today, most techniques use RF bandpass quantization noise shaping inside the ADC to improve its resolution at RF. They use either LC bandpass filter stages, VCOs or ZIF mixing to achieve this. Some other revisit the analog signal conditioning and optimize the position of the sampling operation in the receive chain. Finally some split the high speed ADC in multiple subconverters and use a DSP intensive back-end to recover the signal. All these techniques have in common the attempt to bring the ADC as close as possible to the antenna as was envisioned by Mittola. Leading to highly

digitized architectures, not only the benefits of scaled technologies are better exploited but also the large reconfiguration capabilities of the DSP are optimally utilized.

Speakers:

1. **SeongHwan Cho**, *KAIST*, "Time-based ADCs using VCOs for Digital Intensive RF Receivers"
2. **Andre Mariano**, *Atlantic Innovation ES, Bordeaux and IMS Lab, Univ. Bordeaux,* "Digital Radio Architectures: Where and How Sampling Can Be Done"
3. **Kimmo Koli**, *Nokia*, "Direct DS receivers for Cellular Communications"
4. **Jose Silva-Martinez**, *Texas A&M University*, "Digitally Assisted RF-to-Digital Bandpass Converters for Broadband Communication Systems"
5. **Theodoros Chalvatzis**, *Broadcom*, "Delta-Sigma Digital Receivers with mm-Wave Sampling Clocks"
6. **Martin Snelgrove**, *Kapik*, "Wideband Sampling by Decimation in Frequency"
7. **Hassan Aboushady** and **Nicolas Beilleau** , *Univ. Pierre and Marie Curie, Paris VI and Federal Univ. Rio Grande do Norte, Natal*, "RF LC Bandpass Sigma-Delta ADCs with Finite Impulse Response Feedback DACs"
8. **Julien Ryckaert**, *IMEC*, "RF Bandpass Full Delta-Sigma converters in Scaled CMOS"

8:00 AM – 5:20 PM

WSH: Design for Manufacturability and Self-Testability of RFICs

Organizers: **Jaber A. Khoja**, *Zoran*
Oren Eliezer, *Xtendwave*
R. Bogdan Staszewski, *Delft University of Technology*

Abstract: With the increased complexity and higher level of integration in today's mixed signal SoCs, it has become crucial for RFIC designers to minimize the production-testing costs, while also guaranteeing high production yields, by applying design-for-manufacturability (DfM) approaches early in the design phase. The reduction in test costs and in productization costs in general is achieved through a combination of strategies that may be considered as design-for-testability (DfT) approaches, and in particular built-in self-testing (BiST). As with the common practice in digital design, DfT in mixed-signal circuitry considers the productization- and testing-related needs during the design phase through provisions allowing for simple and low-cost characterization and testing, while also maximizing yield. The on-chip resources for the realization of the DfT mechanisms may include existing circuitry, such as data converters that are used for various purposes during normal operation, dedicated circuits that are added for the sake of testing or calibration/compensation, and dedicated routines that may run on an on-chip processor and memory. The DfT approach must allow for the various mixed-signal functions to be self-calibrated/compensated in accordance with the expected process variations, such that there won't be a need to screen incompliant devices through expensive and lengthy parametric tests, also resulting in yield loss. The workshop will present recent approaches to design and productization of RF circuitry, developed by industry leaders and academia, including many examples demonstrating the implementation of these principles in high-volume products.

Speakers:

1. **Jaber A. Khoja**, *Zoran*, "The Need for Testing: Reliability, Screening and Yield Enhancement"
2. **Mustapha Slamani**, *IBM*, "Production RFIC Testing"
3. **Mani Soma**, *University of Washington*, "DFT and the IEEE 1149.4 Mixed-Signal Test Bus Standard"
4. **K.-T. Tim Cheng**, *Univ. of California, Santa Barbara*, "Emerging Test Paradigms for Low-cost Production Testing of Analog/RF Circuits"
5. **Jose Silva-Martinez**, *Texas A&M University*, "On-Chip Calibration and Novel Performance Monitoring of RF Circuits"
6. **Oren Eliezer**, *Xtendwave*, "Design-for-Manufacturability in Low-Cost Mass-Volume RF SoCs"
7. **Stephen Sunter**, *Mentor Graphics*, "Production Tests and BIST for ADCs and DACs"
8. **R. Bogdan Staszewski**, *Delft University of Technology*, "RF-BIST in the RF-SoC Environment"

Sunday, 8:00 AM – 5:20 PM

WSI: RF Bio-Medical Electronics and Sensors

Organizers: **Sayfe Kiaei**, *Arizona State University*
Brian Otis, *University of Washington*

Abstract: RFIC & Mixed-Signal Integrated Devices have found significant and multifarious applications in the broad bio-electronics and bio-medical domains over the past 30 years. Today, RFIC and Mixed-Signal systems are indispensable to the development of many imaging applications, sensors, actuators, and related products. RF sensors and analog/digital processing are critical to numerous bio-medical components, which include medical implanted devices, embedded wireless sensors in the human body, and external bio-marker sensors. This workshop will focus on the development of emerging fully integrated sensors, RF medical implanted devices, neural sensors, and relevant biomedical applications. This workshop will be a RFIC workshop with emphasis on the latest innovations in RF and Mixed-Signal processing in Bio-Electronics. The topics covered will focus on:

- Medical Implanted Communication System (MICS)
- Bio, Molecular, and Bio-chemical Sensing
- RF Bio-imaging
- Bio Sensors and Actuators

Speakers:

1. **Ben Calhoun**, *University of Virginia*, "System-Level Issues in Wireless Biomedical Systems"
2. **Patrick Chiang**, *Oregon State University*, "Wearable Sensor Electronics for Monitoring the Effects of Aging"

3. **Pedram Mohseni**, *Case Western University*, "Wireless Integrated Systems for Chemical and Electrical Neural Recording: Challenges in High-Site-Density Brain Monitoring"
4. **Brian Otis**, *University of Washington*, "Ultra-Low Power, Miniaturized RF IC for Bio-Medical Applications"
5. **Julien Penders**, *Holst Centre/IMEC*, "Low-Power (1 mW) Multi-Purpose Sensor Node"
6. **Mohamad Sawan**, *Ecole Polytechnique de Montreal*, "Harvesting Energy and Bidirectional Wireless Data Transmission for Implantable BMI Applications"
7. **Thierry Taris**, *University of Bordeaux*, "Micro-W Transceivers for Bio-Medical Application"
8. **Stephen O'Driscoll**, *University of California, Davis*, "Wireless Power and Data Transfer for Implantable Medical Devices"
9. **Sayfe Kiaei**, *Arizona State University*, "Overview of Wireless Medical Implanted Device"

8:00 AM – 5:20 PM

WSJ: Systems & Circuits for Sensing, Co-Existence, and Interference Mitigation in SDR and Cognitive Radios

Organizers: **Ramesh Harjani**, *University of Minnesota*
Brian Sadler, *Army Research Laboratory*
Hossein Hashemi, *University of Southern California*
Jacques C. Rudell, *University of Washington*

Abstract: Cognitive Radios (CR) provide a new paradigm to improve spectrum efficiency by enabling Dynamic Spectrum Access (DSA). In CR, spectrum holes that are unoccupied by primary users can be assigned to appropriate secondary users as long as the interference introduced by secondary users is not harmful to the primary users. In this workshop, we focus on the spectrum sensing problem in CR, in which sensing and detection of primary users is done in order to realize DSA. Spectrum sensing can be a very challenging task for CR due to many factors. First, the sensing bandwidth for CR can expand from hundreds of MHz to several GHz. Second, the sensing radio should be able to detect very weak primary users, which arise due to fading and the hidden terminal problem. Third, the receiver may need to detect a signal in the presence of a strong coexisting transmitter. Traditional time-domain Nyquist sampling or wideband sensing are quite challenging due to bandwidth, dynamic range, power, and resolution requirements. Alternatively, compressed sensing can be used to reduce the sampling rate, taking advantage of the sparsity of the signals in the frequency domain. Spectrum sensing requires reliable signal detection in negative SNR regime within a constrained sensing time. Signal processing algorithms for very low SNRs in a noise dominated regime are quite different from demodulation and detection processing in conventional digital communications.

This full day workshop consists of 9 talks. The morning sessions will focus on motivation and the many system aspects of cognitive radios and Dynamic Spectrum Analysis. The afternoon presentations in this workshop will focus on potential implementation issues surrounding highly-integrated CMOS transceivers characterized by a high degree of programmability, low noise, high dynamic range receivers and transmitters for CR applications. Whenever possible and appropriate,

measurements from actual designs will be used to supplement the theoretical understanding of workshop participants.

Speakers:

1. **Preston Marshal**, *University of Southern California*, "High Density Wireless Operation: Linearity, Interference Tolerance, and Adaptation"
2. **Brian Sadler**, *Army Research Laboratory*, "Shared Spectrum: An Overview of Sensing and Processing"
3. **Mark McHenry**, *Shared Spectrum* , "Dynamic Spectrum Access Software Design"
4. **Danijela Cabric**, *University of California, Los Angeles*, "Signal Processing Approaches for Spectrum Sensing: Theory and Implementation"
5. **Sebastian Hoyos**, *Texas A&M University*, "Mixed-Signal Parallel Compressive Spectrum Sensing for Cognitive Radios"
6. **Larry Larson**, *University of California, San Diego*, "RF Circuit Implementation Issues of Cognitive and Software Defined Radios"
7. **Bram Nauta**, *University of Twente, The Netherlands*, "Wideband and Interferer Robust Software Defined Radio in CMOS"
8. **Jan Craninckx**, *IMEC, Leuven*, "Transceiver Design for Interference-Robust Software-Defined Radios"
9. **Ranjit Gharpurey**, *University of Texas, Austin*, "Design Challenges in Radios for Emerging Broadband Wireless Systems"

1:20 PM – 5:20 PM

WSK: Efficiency Enhancement Techniques of Power Amplifiers and Transmitters for Mobile Applications

Organizers: **Youngwoo Kwon**, *Seoul National University*
Nick Cheng, *Skyworks Solutions*

Abstract: With the proliferation of data services and smart phones, mobile phone manufacturers are faced with new, unprecedented challenges and demands from both mobile operators and consumers. In particular, "thermal issues" and "battery life" are two major challenges related to the transmitter section of the phone. For example, excessive current consumption of the power amplifiers often results in the overheating of the mobile devices, the solution of which may even affect the industrial design of the phones. The added features in the smart phones and the extensive data usage call for the frequent recharges on the battery, which is extremely inconvenient from the users' point of view. Thermal and battery issues will become increasingly difficult to solve at the phone level as the industrial design gets more complex and the data rates continue to increase. The efficiency improvement of the power amplifiers and transmitters is the only solution to address these concerns.

Presentations in this workshop will focus on the novel design techniques to enhance the efficiencies of the transmitters and power amplifiers. The workshop will start with the discussions on front-end topologies to improve the overall transmitter efficiency, and move on to a hot topic of "envelop tracking", which has the potential of proliferation into the handset applications. Ever-growing interest in the CMOS PA's will also be covered with two presentations with a special focus on

the design techniques to overcome the linearity and efficiency limitations of the CMOS devices. Both wireless LAN and 2G/3G applications will be covered.

Speakers:

1. **James Young**, *Skyworks Solutions*, "Front End Topologies and PAE Enhancement Techniques"
2. **Don Kimball**, *University of California, San Diego*, "Highly Efficient RF Front End Using Envelope Tracking Techniques"
3. **Donald Lie**, *Texas Tech University*, "Design of Si-Based High-Efficiency RF Power Amplifiers and Polar Transmitters for Mobile Broadband Wireless Communications"
4. **Songcheol Hong** , *KAIST, Korea*, "RF CMOS PAs for Mobile Communications"
5. **Ali Afsahi**, *Broadcom*, "High Power, Highly Linear CMOS Power Amplifier for WLAN Applications"

IMS SPONSORED SUNDAY SHORT COURSES

8:00 AM – 5:00 PM

SCSA: Techniques and Realizations of Microwave and RF Filters

Organizers: **Prof. Pierre Jarry**, *Bordeaux University*
Prof. Jacques Beneat, *Norwich University*

Abstract: Drawing from research work sponsored by the European Space Agency, French government agencies, and several international corporations, this course provides modern methods of design, synthesis, and realization for over 25 different types of microwave filters and multiplexers operating over a frequency range from 1 GHz to 35 GHz. Students will learn the fundamentals of filter design, as well as modern techniques for the synthesis and practical realization of an assortment of high performance minimum- and non-minimum-phase filters, dual- and triple-band filters, diplexers, and contiguous-band multiplexers. A variety of planar and non-planar technologies will be discussed, including suspended-substrate stripline, single- and multi-mode cavities, and evanescent-mode waveguide.

8:00 AM – 5:00 PM

SCSB: Nonlinear Dynamics and Stability Analysis/Design of Microwave Circuits

Organizers: **Professor Almudena Suarez**, *University of Cantabria*
Dr. Christopher Silva, *The Aerospace Corp.*

Abstract: This course seeks to help designers reconcile the frequent discrepancies (undesired oscillations and chaos) between simulations and measurements of nonlinear microwave circuits. In addition to improving their awareness of what can go on in their nonlinear circuits, students will learn to distinguish between different types of steady-state solutions, identify instability problems through small- and large-signal stability analysis in both the time and frequency domains, and understand the mechanisms for instabilities. Practical examples of instability will be presented for such nonlinear circuits as power amplifiers, frequency multipliers and dividers, and voltage-controlled oscillators, and, in each case, the stability analysis procedure, the impact of instability on measured performance, and techniques for stabilization will be demonstrated. Informal interactive lectures will be accompanied by a hands-on simulation lab – in which stability analysis and control techniques will be demonstrated on real examples using commercial software – and by a hardware demonstration of stability diagnostics using a spectrum analyzer.

IMS/ARFTG SPONSORED MONDAY WORKSHOPS

8:00 AM – 5:20 PM

WMA: High Efficiency, Linear Power Amplifier Technology: Ka-, Q-band and Beyond

Organizers: **Ed Viveiros**, *Army Research Laboratory*
Joe Qiu, *Army Research Laboratory*
Allen Katz, *Linearizer Technology Inc., College of New Jersey*

8:00 AM – 12:00 PM

WMB: Nanotechnologies for Microwave Interconnects and Packaging

Organizers: **Karl Varian**, *Raytheon Company*
Anh-Vu Pham, *University of California, Davis*

8:00 AM – 5:20 PM

WMC: Practical Compression, IMD, Load Pull and Behavioral Modeling Measurements

Organizers: **Jon Martens**, *Anritsu*
Nuno Borges Carvalho, *IT – Universidade de Aveiro*

8:00 AM – 5:20 PM

WMD: Laboratory Class: Wafer-Level S-Parameter Calibration Techniques

Organizers: **Andrej Rumiantsev**, *Cascade Microtech, Germany*

8:00 AM – 5:20 PM

WME: Simulation- and Surrogate-Driven Microwave Design Technology

Organizers: **John W. Bandler**, *Bandler Corporation*
Slawomir Koziel, *Reykjavik University*

8:00 AM – 5:20 PM

WMF: Challenges and Techniques of Magnetic Resonance Imaging (MRI) Systems

Organizers: **Robert Caverly**, *Villanova University*

Abbas Omar, *University of Magdeburg*
William E. Doherty, *Microsemi-Lowell*
Anand Gopinath, *University of Minnesota*
J. Thomas Vaughan, *University of Minnesota*

8:00 AM – 5:20 PM

WMG: Recent Developments in Microwave Imaging and Detection

Organizers: **Natalia K. Nikolova**, *McMaster University*
Aly Fathy, *University of Tennessee*

8:00 AM – 5:20 PM

WMH: Flexible, Autonomous RFID-Enabled Sensors: Novel Applications, Energy Harvesting and Integration Challenges

Organizers: **Apostolos Georgiadis**, *Centre Tecnologic Tele. de Catalunya, Spain*
Emmanouil Tentzeris, *Georgia Institute of Technology, USA*
Li Yang, *Texas Instruments, USA*
Luca Roselli, *University of Perugia, Italy*
Gerald DeJean, *Microsoft, USA*

8:00 AM – 5:20 PM

WMI: Current state of Hexaferrite Materials and Their Applications

Organizers: **Karen Kocharyan**, *Anaren Microwave, Inc.*
Thomas Lingel, *Anaren Microwave, Inc.*

1:20 PM – 5:20 PM

WMJ: Compact Equivalent Circuits and Table Based FET Models - Is There One Winner for Circuit Designers and Foundries?

Organizers: **Mike Golio**, *Golio Consulting*
Iltcho Angelov, *Microwave Electronics Lab, Chalmers*

8:00 AM – 5:20 PM

WMK: High Power Effects on Passive Microwave Components

Organizers: **Vicente E. Boria**, *Technical University of Valencia, Spain*
Ming Yu, *COM DEV, Canada*

IMS SPONSORED MONDAY SHORT COURSES

8:00 AM – 5:00 PM

SCMA: Low Phase Noise Oscillators: Theory, Design, and Laboratory

Organizers: **Prof. Jeremy Everard**, *University of York*

8:00 AM – 5:00 PM

SCMB: Frequency Synthesizer Design Techniques

Organizers: **Dr. Lama Dayaratna**, *Lockheed Martin*
Dr. Peter White, *Applied Radio Labs*
Dr. Cicero S. Vaucher, *NXP Semiconductors*

8:00 AM – 12:00 PM

SCMC: Noise in Electromagnetic Circuits and Systems

Organizers: **Prof. Dr. Peter Russer**, *Technische Universitaet Muenchen*
Prof. Andreas Cangellaris, *Univ. of Illinois, Urbana-Champaign*

1:00 PM – 5:00 PM

SCMD: National and International Spectrum Processes for Microwave Professionals

Organizers: **Nelson Pollack**, *Spectrum Analytics, LLC*
Dr. Michael Marcus, *Marcus Spectrum Solutions LLC*
Laura Stefani, *Goldberg, Godles, Wiener & Wright*

IMS SPONSORED FRIDAY WORKSHOPS

8:00 AM – 5:20 PM

WFA: Wireless Power Transmission

Organizers: **Zhizhang (David) Chen**, *Dalhousie University, Halifax, Canada*
Naoki Shinohara, *Kyoto University, Japan*
Peter Russer, *Technische Universität München, Germany*

8:00 AM – 12:00 PM

WFB: Piezoelectric RF MEMS for Communication and Defense Applications

Organizers: **Ronald G. Polcawich**, *US Army Research Laboratory*
Tony Ivanov, *US Army Research Laboratory*

8:00 AM – 5:20 PM

WFC: The Design Flow of Microwave Power Amplifiers: Challenges and Future Trends

Organizers: **Dominique Schreurs**, *Katholieke Universiteit Leuwen*
Antonio Raffo, *University of Ferrara*

8:00 AM – 5:20 PM

WFD: Medical and Biological Microwave Sensors and Systems

Organizers: **Ed Niehenke**, *Niehenke Consulting*
Olga Boric-Lubecke, *University Of Hawaii*
Jenshan Lin, *University of Florida*
Arye Rosen, *Drexel University*

8:00 AM – 5:20 PM

WFE: Electronically Steered Arrays for Radar, Communications and Electronic Warfare: Are They Affordable And Are They Ready to Assume Their Place in Advanced 21st Century Systems?

Organizers: **John Pierro**, *Telephonics Corporation*
Frank Sullivan, *Raytheon Corporation*
Ruediger Quay, *Fraunhofer Institute Of Applied Solid State Physics*

8:00 AM – 5:20 PM

WFF: Wireless Sensor Network Technologies for Emerging Applications

Organizers: **Debabani Choudhury**, *Intel Corporation, USA*
Nuno Borges Carvalho, *Univ. de Aveiro, Portugal*

8:00 AM – 5:20 PM

WFG: Innovative and Highly Accurate Local Positioning Systems

Organizers: **Thomas Ussmueller**, *University of Erlangen-Nuremberg*
Martin Vossiek, *Clausthal University of Technology*
Robert Weigel, *University of Erlangen-Nuremberg*

8:00 AM – 12:00 PM

WFH: Recent Advances in Multi-Giga Bit Per Second (Gbps) Data Throughput Techniques for Ka-Band Space-to-Ground Links

Organizers: **Kavita Goverdhanam**, *U.S. Army – CERDEC*
Rainee N. Simons, *NASA Glenn Research Center*

8:00 AM – 12:00 PM

WFI: Advances in RF Imaging Techniques

Organizers: **Allen Katz**, *The College of New Jersey*
Robert Caverly, *Villanova University*

8:00 AM – 5:20 PM

WFJ: Nanotechnology-Enabled RF and Cognitive Devices, Components and Systems

Organizers: **Luca Pierantoni**, *Università Politecnica delle Marche, Italy*
Fabio Coccetti, *LAAS-CNRS, France*
Manos M. Tentzeris, *Georgia Tech, USA*
Luca Roselli, *Università degli Studi di Perugia, Italy*

8:00 AM – 5:20 PM

WFK: Practical Design Approaches and Issues in Software Defined Radios

Organizers: **Richard G. Ranson**, *Radio System Design Ltd*
Jeffrey Pawlan, *Pawlan Communications*

ADVANCE REGISTRATION

Registration Categories

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration period. It begins Tuesday, 1 February and will last through Friday, 20 May. This period provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird period is the 2nd tier or Advance Registration period. It extends from Saturday, 21 May through Friday, 3 June, just prior to the start of Microwave Week. The 3rd and final tier is the On-Site Registration period that will remain the same as in past Symposia, starting on Saturday 4 June, the first day of Microwave Week, and ending on Friday, 10 June.

EARLY BIRD PERIOD	**1 FEBRUARY**	**20 MAY (THRU MIDNIGHT ESDT)**
ADVANCE PERIOD	**21 MAY**	**3 JUNE (THRU MIDNIGHT ESDT)**
ON-SITE PERIOD	**4 JUNE**	**10 JUNE (THROUGHOUT MICROWAVE WEEK)**

Symposium SUPERPASS

For one low price, registrants can attend as many technical sessions from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend one full-day workshop (or two half-day workshops, if desired). SUPERPASS registration includes the electronic proceedings for IMS, RFIC, ARFTG, and the All Workshop electronic proceedings. Also included is admission to the exhibits. In addition, the SUPERPASS will allow you to attend the IMS Welcome Reception on Monday, the Awards Banquet on Wednesday and the Crab Feast on Thursday.

The SUPERPASS is a SUPER DEAL offering a significant discount over the combined a la carte pricing.

Early Bird Registration

Please follow these instructions for completing the Early Bird Registration Form on the facing page. Early Bird Registration rates provide significant savings from the on-site fees and are available through midnight (EST) 20 May. Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and exhibit hall. This form is not used for guest tour registration, which is described elsewhere in this program book. Each registrant must submit a separate form with payment.

Methods of Registration

Individuals can register online, by fax or by mail. All registrations must be accompanied with a payment; we accept Visa, MasterCard, American Express, and checks drawn from a U.S. bank. Registration forms received without a form of payment will be discarded. We do NOT accept phone registrations.

Personal Information

If you would like to receive information by email from the IEEE, MTT-S, or microwave companies, simply select the appropriate boxes.

Membership

Check boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit www.ieee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Students, Retirees, and IEEE Life Members receive a discount on some registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full time student carrying a course load of at least nine credit hours.

Symposia

Microwave Week includes the IMS technical program, and exhibit, as well as the RFIC Symposium (www.rfic2011.org), and ARFTG Conference (www.arftg.org).

Select the conference(s) you wish to attend.

- IMS Technical Sessions are held on Tuesday, Wednesday, and Thursday. Registration
- includes admission to the exhibition and the electronic proceedings.
- RFIC Technical Sessions are held on Monday and Tuesday. Registration includes
- admission to the RFIC Reception, the exhibition, and the electronic proceedings.
- ARFTG Technical Sessions are held on Friday. Registration includes breakfast, lunch,
- electron proceedings, and admission to the ARFTG Exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE Members.
- Microwave Week hosts the largest exhibition of its kind with over 500 companies.
- Exhibit only registration is available.

Extra Electronic Proceedings and Digests

Additional electronic proceedings (IMS, RFIC and ARFTG) and digests (RFIC only) are available for purchase and pick-up at the conference. After the Symposium, these digests and electronic proceedings will be available for purchase from IEEE.

Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 8 June from 1820 – 2200 at the Hilton Baltimore. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented. An additional fee applies.

Crab Feast

The Crab Feast is a tradition when IMS is in Baltimore. The Crab Feast will be held on Thursday, 9 June from 1800 – 2200 at the USS Constellation & Pier 1. This is an informal event in the Chesapeake Bay tradition.

Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

Workshops

The workshop fee includes an electronic proceeding for that workshop. Full-day workshops include a continental breakfast, a morning refreshment break, a boxed lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and morning refreshment break. Afternoon workshops include a boxed lunch and an afternoon refreshment break.

The All-Workshop electronic proceedings include material for all RFIC and IMS workshops. In order to be able to purchase the All-Workshop electronic proceedings you must first be registered for three full-day workshops, or equivalent (i.e. two full-day workshops and two half-day workshops).

Note that speaker's printed notes of the workshop are not included with registration and may be purchased during the Early Bird registration period only.

Guest Registration

Attendees registered for the technical portion of the conference may add a Guest to their registration for an additional fee. Guest Registration includes access to the hospitality suite, plenary session, and exhibit hall, but does not allow access to technical sessions and workshops.

Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express). Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, wire transfers, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to "2011 IEEE IMS". Written requests for refunds will be honored if received by 20 May 2011. Refer to the Refund Policy for complete details.

Hospitality Suite

Families and guests will enjoy the hospitality suite located in the Peale room at the Hilton. It will be a place to relax and meet. The hospitality suite will also have suggestions and discount coupons for various activities to enjoy while in Baltimore as well as fun games & crafts for families. Guest registration is required and fees do apply.

IMS2011 BADGE CASH OUTLETS

- IMS2011 is continuing the "Badge Cash" program this year as part of a continued effort to improve your experience as an attendee in Baltimore, MD!
- Attendees registered for All IMS Sessions will have a $45.00 credit put onto their badge that can be use at selected locations in the Baltimore Convention Center for breakfast each morning
- (approximately $15.00/day). This replaces the continental breakfast that the conference has provided to the IMS attendees in previous years.
- Attendees registered for the Superpass will have a value of $60.00 on their badge as this includes both IMS and RFIC.
- Attendees registered for IMS Single Day will have a value of $15.00 on their badge that can be used for the day that they are attending the IMS technical program.
- IMS Registrant Badge Cash is only valid Tuesday – Thursday, 7 – 9 June.
- Attendees registered for RFIC Sessions will have a value of $30.00 on their badge that is valid only Monday - Tuesday, 6 – 7 June.

How does Badge Cash work?

Go to a participating station, select your items and hand the cashier your badge. The cashier will scan your badge and the amount purchased will be deducted from your badge. If there is not enough cash value left on your badge you will be responsible for paying the difference. Badge Cash can be redeemed at the following locations in the Baltimore Convention Center:

If I lose my badge will I receive a new one with the cash value on it?

No, the Badge Cash is not redeemable for cash it is only good for food products sold at the mentioned vendors below.

ON SITE REGISTRATION

On-Site Registration

On-Site registration for all Microwave Week events will be available in the Baltimore Convention Center, Pratt Street Lobby. Registration hours are:

Day	Time
Saturday, 4 June	1400 – 1800
Sunday, 5 June	0700 – 1800
Monday, 6 June	0700 – 1800
Tuesday, 7 June	0700 – 1800
Wednesday, 8 June	0700 – 1800
Thursday, 9 June	0700 – 1600
Friday, 10 June	0700 – 0900

Exhibit Only Registration

Exhibit only registration is available.

Guest Tour Registration

Registration for guest tours will be available in the Baltimore Convention Center, Pratt Street Lobby. Please refer to the Guest Tour Program section of this program book for further details and tour descriptions.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to technical sessions and exhibits. Digests are not included. The Press Room will available from Sunday thru Thursday of Microwave Week.

ARFTG Registration

Late on-site registration will be available at the Baltimore Convention Center, Pratt Street Lobby on Friday from 0700 to 0900. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

Refund Policy

Written requests received by 20 May 2011 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email address for the refund check. If registration was paid for by credit card, the refund will be made through an account credit. An account number must be provided if the initial registration was completed on-line. Address your requests to:

MTT-S Registration

Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027
nannette@mpassociates.com

ON SITE REGISTRATION (continued)

REGISTRATION FEES	MEMBER	NON-MEMBER
SuperPass		
All IMS, RFIC, and ARFTG Sessions and Electronic Proceedings, Awards Banquet, Thursday Crab Feast, Full Day (or 2 Half Day) Workshop Attendance and All Workshop CD-ROM	$1585	$2295
Student, Retiree, Life Member SuperPass	$945	
IMS		
All IMS Sessions	$565	$835
Single Day Registration	$285	$425
Student, Retiree, Life Member All IMS Sessions	$95	
RFIC Symposium		
All RFIC Sessions	$270	$400
RFIC Reception Only	$30	$50
ARFTG Conference		
All ARFTG Sessions	$265	$400
Student, Retiree, Life Member All ARFTG Sessions	$165	
Exhibition Only		
Exhibition Only Pass	$30	$30
Guest Registration		
Guest Badge (requires technical conference registration)	$80	$120
Extra Proceedings and Digests		
IMS Electronic Proceedings	$85	$160
RFIC Digest	$85	$160
RFIC Electronic Proceedings	$85	$160
ARFTG Electronic Proceedings	$85	$160
ARFTG Conference Compendium CDROM 1982 – 2006	$75	$105
Evening Events		
Awards Banquet (Wed. Night)	$75	$75
Crab Feast (Thurs. Night)	$65	$65
Workshops		
Full Day	$220	$330
Full Day Student/Retiree	$150	
Half Day	$100	$150
Half Day Student/Retiree	$75	
Full Day Short Courses	$390	$585
Full Day Short Courses Student/Retiree	$270	
Full Day Short Course w/Lab	$455	$680
Full Day Short Course w/Lab Student/Retiree	$320	
Half Day Short Course	$270	$405
Half Day Short Course Student/Retiree	$190	
All Workshop Electronic Proceedings (Requires workshop registration)	$75	$115

UNITED STATES VISA ADVISORY

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment and pay fees. An interview is required as
- a standard part of processing for most visa applicants.
- Plan on having finger scans as part of the visa application process. Two index-finger scans are normally collected by the consular officer at the visa interview window.
- However; in some countries, they may be collected prior to the actual visa interview.

Visa Waiver Program (VWP)

Citizens of the following countries can travel to the U.S. without a visa for tourism or business for 90 days or less under the Visa Waiver Program (VWP) if they meet other travel requirements. As of 26 June 2005, all VWP travelers must have a machine-readable passport to enter the United States without a visa.

Andorra	France	Lithuania	Singapore
Australia	Germany	Luxembourg	Slovakia
Austria	Hungary	Malta	Slovenia
Belgium	Iceland	Monaco	South Korea
Brunei	Ireland	the Netherlands	Spain
Czech Republic	Italy	New Zealand	Sweden
Denmark	Japan	Norway	Switzerland
Estonia	Latvia	Portugal	United Kingdom
Finland	Liechtenstein	San Marino	

Some citizens of Canada and Bermuda do not need a visa to visit the United States. Contact your nearest U.S. embassy or consulate for guidance. Travelers should be aware that by requesting admission under the Visa Waiver Program, they are generally waiving their right to review or appeal a CBP (Customs and Border Protection) officer's decision as to their application for admission at the port of entry.

Effective January 20, 2010, the Department of Homeland Security is transitioning to enforced compliance of the Electronic System for Travel Authorization (ESTA) requirement for VWP travelers. Therefore, VWP travelers who have not obtained approval through ESTA should expect to be denied boarding on any air carrier bound for the United States. ESTA applications may be completed FREE online at the official DHS website, which is: https://esta.cbp.dhs.gov.

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, https:/www.cbp.gov, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing. Spouses requiring visa assistance must be registered for an IMS Guest Program Event. Check the IMS2011 website (www.ims2011.mtt.org) for Guest Program details. For additional assistance, please contact Mishoun Mah at international@ims2011.org.

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative sources of information are the U.S. Government websites at www.unitedstatesvisas.gov and http://travel.state.gov/visa/visa_1750.html.

SOCIAL EVENTS

SUNDAY, 5 JUNE 2011

RFIC Reception: 1900 – 2100
Baltimore Convention Center, Level 400 - Ballroom I & II

Immediately following the RFIC Plenary Session is the RFIC Reception to be held in adjacent Ballroom III & IV at the Baltimore Convention Center. This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

MONDAY, 6 JUNE 2011

IMS 2011 Welcome Reception: 1900 – 2030 Baltimore Convention Center, Level 400 - Ballroom I & II

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by IMS 2011 in the Baltimore Convention Center, Ballroom III & IV.

TUESDAY, 7 JUNE 2011

Women in Microwaves Reception: 1730 – 1930 Hilton Hotel, Lobby Bar

Connect with past friends as well as make new connections with the community of women who make a career in the field of microwave engineering technology. Spend a few hours enjoying conversation with your peers Tuesday evening, 1730-1930, 7 June at the 2011 WIM Reception. Light appetizers and refreshments served. Space is limited so kindly RSVP by 3 June to secure your attendance: wim@ims2011.org

Student Reception (Still TBD as it may be combined with Gold Recp)
1900-2100 Omni Hotel, International Ballroom D
Student/GOLD Reception: 1900-2100

This year the student reception will be combined with the GOLD reception. Join us for light appetizers and refreshments while networking with fellow students and graduates of the last decade. Visit http://ims2011.mtt.org for more details on the location as they become available

Ham Radio Social: 1800 to 2100
Hilton Hotel, Room Key 12, Hilton Ballroom

IMS2011 attendees and their guests are invited to attend the annual ham radio social. This event provides an opportunity to discuss issues and activities related to amateur radio in a very informal atmosphere while enjoying a buffet and open bar. Some microwave equipment designed or modified by local amateurs for the ham bands will be on display. The equipment designers will be present to answer questions. This year we are encouraging all ham attendees to bring small microwave items related to amateur radio for display and discussion. Please bring a small sign or poster describing your equipment and we will provide the tables. 120VAC power may/may not be available. Please send Roger K3TM an email (r.kaul@ieee.org) by May 31 if you plan to bring an item for display so we can provide space.

A special event call of N3M will be activated during IMS week.

Ham operators are encouraged to bring and post their QSL cards on the display board.

WEDNESDAY, 8 JUNE 2011

Industry Hosted Cocktail Reception: 1715 – 1800
Baltimore Convention Center, Level 100 – Exhibition Hall

Symposium Exhibitors will host a cocktail reception.

MTT-S Awards Banquet: 1820-2200
Hilton Hotel, Level 2 – Key Ballroom 7-12

The MTT-S Awards Banquet includes dinner, major society awards presentation and entertainment. This years entertainment will be provided by TBD. (Explanation of entertainment type.) Tickets can be purchased at the time of registration.

THURSDAY, 9 JUNE 2011

MTT-S Student Awards Luncheon: 1200 – 1400
Hilton Hotel, Level 2 – Holiday Ballroom 6

All students are invited to attend the luncheon which recognizes recipients of the MTT-S Undergraduate Scholarships, MTT-S Graduate Fellowships, IMS2011 Student Volunteers, IMS2011 Student Paper Awards and the participants/winners of the IMS2011 Student Design Competitions.

Crab Fest: 1800-2200 USS Constellation & Pier 1

The Crab Feast is a tradition when IMS is in Baltimore. Join us for food, fun, and all the other fun that comes along with the Crab Feast. It's the perfect way to cap off you IMS2011 social schedule!

HOSPITALITY SUITE

A warm welcome awaits you in the Hospitality Suite located in the Peale room at the Hilton Hotel. Grab your guest badge and come for breakfast in the morning and refreshments in the afternoon. Whether your meeting up with old friends or making new ones, the Hospitality Suite is just the place to kick back and relax. There will be a special area for children with various toys & games as well as local area information for everyone to venture out and explore. All the Guest Tours will depart from the Hospitality Suite.

Open Sunday, 5 June through Thursday, 9 June 0730 to 1530.

THINGS TO DO IN CHARM CITY

Welcome to "Charm City" - Baltimore, Maryland. With nearly 300 years of city history, Baltimore has developed numerous points of interest or "charms". The Inner Harbor is home to a large and varied number of these charms. The Inner Harbor is a short block away from the Baltimore Convention Center. It is a starting point for using the Water Taxi to explore some of the charms of Baltimore.

Suggested visitor sites are arranged by transportation methods.

WALKING DISTANCE FROM THE CONVENTION CENTER:

US Sloop-of-War Constellation (1854 – 1955) was the second US Navy ship to carry that name. Her tour of service and accomplishments are too numerous to recount here. She is permanently docked at Harbor Place in the Inner Harbor. Learn more about this ship at www.historicships.org

Baseball fans already know that Camden Yards is home to the Baltimore Orioles. The Orioles have home games scheduled 03, 04, and 05 June playing the Toronto Blue Jays. On 06, 07, and 08 June, the Orioles play the Oakland Athletics.

Harbor Place offers a shops and eateries for your pleasure.

Let your senses and your mind wander as you experience the numerous sights and hands-on activities at the Maryland Science Center. Featuring an IMAX theater and a planetarium, it's sure to please everyone.

The National Aquarium in Baltimore houses sharks, dolphins, rays and tropical fish among the more than 16,000 creatures in naturalistic exhibits, including a walk-through rain forest, an exciting live-action dolphin show and a new Australian exhibit.

- Baltimore's Maritime Museum features historic ships:
- USCGC Taney (WHEC-37), a Coast Guard cutter
- USS Torsk (SS-423), a WWII-era submarine
- Chesapeake, a lightship
- Seven Foot Knoll Light, a screw-pile lighthouse

BY WATER TAXI:

Fort McHenry was the site of the Battle of Baltimore during the War of 1812. It was during this battle that a local lawyer, Francis Scott Key, was moved to write the poem "A Star Spangled Banner". The inspiration for the poem was the sight of the battle flag flown over Fort McHenry. That flag was made in Flag House on Pratt Street by Mary Pickersgill, her daughter, and her mother together. Learn more about Flag House at http://www.flaghouse.org/index.php/flag/info/the_experience. The original flag is displayed to the public at the Smithsonian Museum of American History, Washington, DC. Learn more about the flag at http://americanhistory.si.edu. Admission to Fort McHenry is through the new (opens in March 2011) Visitor Center. Admission to the fort is $7 US for the week.

Fells Point was established in 1726. It is home to over 120 pubs and restaurants. Additionally, there are antique shops and curio shops. This is an eclectic neighborhood that defies simple explanation.
The Science Center is an educational romp for adults and children.

The Baltimore Museum of Industry displays the history of Baltimore as the center of invention, industry firsts, and manufacturing innovation.

The Baltimore National Aquarium allows one to walk through the tanks and experience sea creatures up close without getting wet.

Historic Ships in Baltimore represents one of the most impressive collections of military vessels in the world. Located within easy walking distance of each other, the US Sloop-of-War Constellation, the US Submarine Torsk, the US Coast Guard Cutter Taney, and the Lightship Chesapeake exhibit life at sea from the mid-19th century to the mid-1980's. Also included in the collection is the Seven Foot Knoll Lighthouse which marked the entrance to the Patapsco River and Baltimore Harbor for over 130 years.

BY CITY BUS OR RAIL:

Bromo Seltzer Tower was built in 1911 by Captain Isaac Emerson, the inventor of Bromo Seltzer. At the time, it was the tallest building in Baltimore. Its distinctive looks make it hard to miss and an interesting photo opportunity.

The Shot Tower was in operation from 182 to 1892 to make lead shot used in guns.

Westminster Cemetery contains the grave of Edgar Allan Poe.

Johns Hopkins University and Johns Hopkins Hospital need no introduction.

Little Italy is home of dozens of Italian restaurants. Go for a meal, play some bocce ball, or enjoy an afternoon cappuccino and fresh Italian deserts.

AMTRAC and MARC trains can spirit you from downtown Baltimore to Union Station in Washington, DC. The Washington Metro connects at Union Station.

The Guest Program will offer suggestions for 'self guided' tours. The Water Taxi is a unique way to transit to and then explore noted museums and scenic locations. Tickets for the

Water Taxi cost $10 US for unlimited rides for the day. Tickets are purchased at the Water Taxi pier. More information about the Water taxi can be found at www.thewatertaxi.com

Additionally, Baltimore boasts an extensive bus system provided by the Maryland Transit Authority (MTA). See http://mta.maryland.gov for route maps, schedules, and fares.

SPECIAL GUIDED BUS TOURS:

There are three guided tours scheduled.

Baltimore City Guided Tour concentrates on the parts of the city outside easy walking distance or water taxi ride. These are some of the other 'charms' of the city that should not be missed. This tour emphasizes the interesting aspects of Baltimore's history. The bus will transport the guests with a knowledgeable tour guide who will explain the history and relevance of the sites visited. A plated lunch is included in this tour at no additional fee.

Annapolis, MD is the state capital. Founded in 1649, we celebrate 350 years as a city which offers a delightful combination of history and a zest for living. Walk along the old brick sidewalks much as George Washington or Thomas Jefferson did in the days when Annapolis was the Capital of the United States. You will see a city which looks remarkably similar to what our Founding Fathers saw in their day. Architecturally, Annapolis boasts some of the finest 17th and 18th Century buildings in the country - including the residences of all four Maryland signers of the Declaration of Independence.

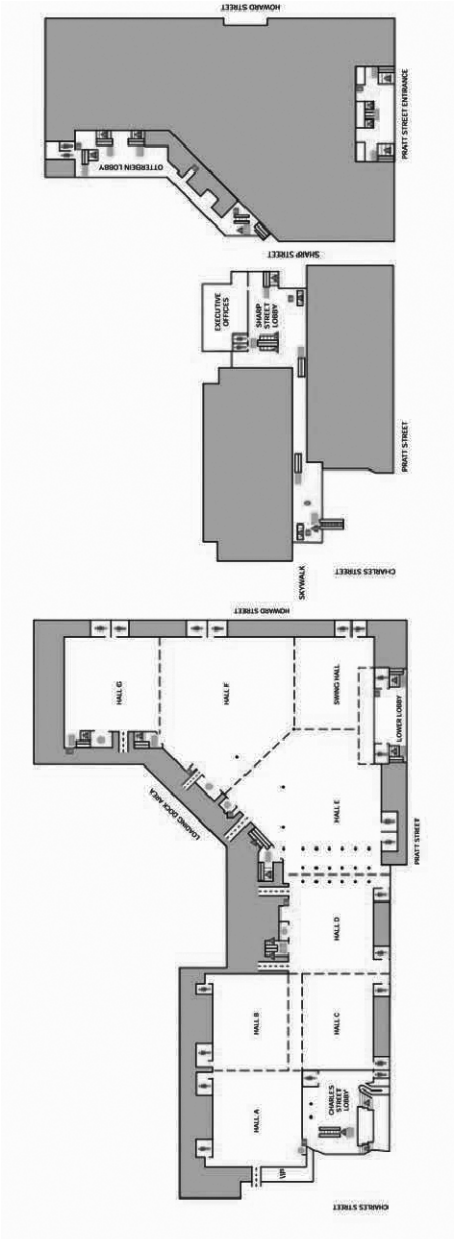
Annapolis is the home of the United States Naval Academy founded in 1845 and also the home of St. John's College, founded in 1696 as King William's School and the third oldest institution of higher learning in the United States.

A bus, with tour guide, will take guests to the city center to start a walking tour of this historical city. Explore the famed waterfront or sit at City Dock and imagine what Annapolis must have been during the 1700's, when the City was a bustling seaport with vessels sailing in to trade from all over the world. Or, watch sailboat races in the harbor and understand why Annapolis is Americas Sailing Capital. Enjoy the many shops, restaurants, activities and scenery Annapolis has to offer. The bus will travel to the US Naval Academy and visit the crypt of John Paul Jones, the 'Father of the United States Navy'. A plated lunch is included in this tour at no additional fee.

Washington, DC offers a plethora of visitor sites that people around the world travel to see. There is too much to be able to see it all in one day, so this tour is designed for maximum impact. This tour is a 'monument hopping' experience. A bus, with tour guide, will travel the National Mall. The Mall, as it is known locally, is the showcase of this planned city. Most monuments and sites in DC are located on or near the Mall. The bus will allow guest to tour famous monuments such as the Lincoln Memorial, Viet Nam Memorial, Franklin Delano Roosevelt (FDR) Memorial, the Jefferson Memorial, the Washington Monument to name a few. The tour will include photo opportunities at the White House and the Capitol Building west lawn. For security reasons, these last two sites are not readily accessible to the public. A plated lunch is included in this tour at no additional fee.

We have only scratched the surface of the entertainment and sightseeing opportunities available in and around Baltimore. For most, the important opportunities will be at the technical sessions or the exhibition during Microwave Week. We hope you have a chance to see some of the rest of Maryland and I hope to see you in Baltimore in June.

BCC FLOOR PLANS



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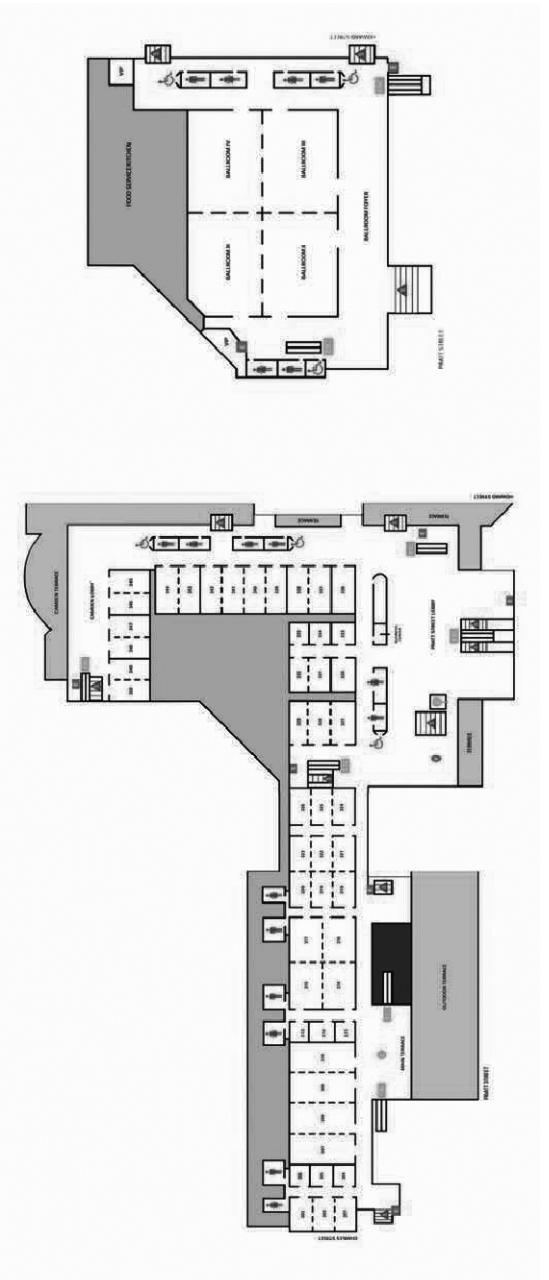
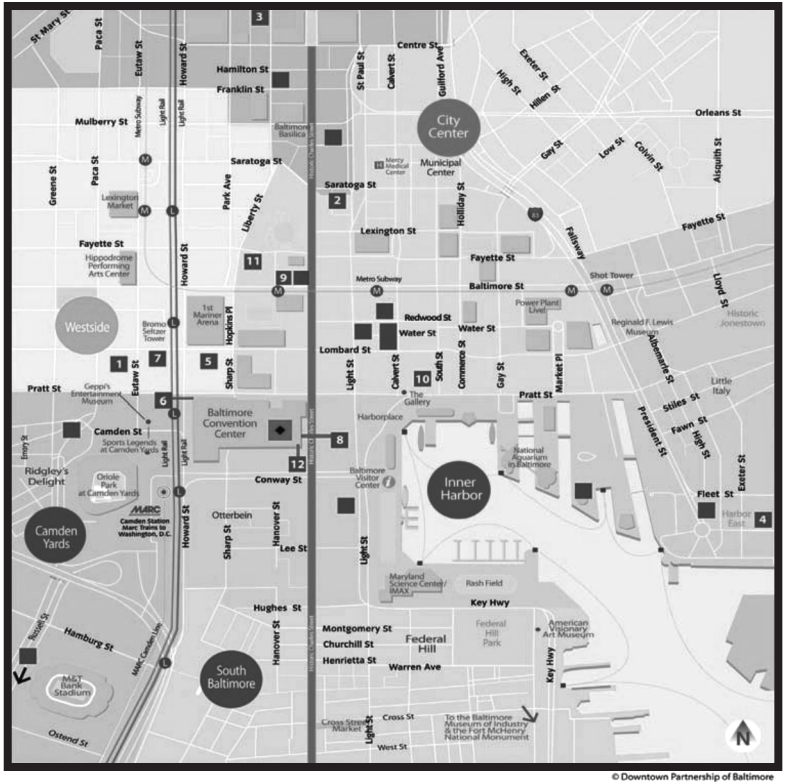


RFIC Attendee Hotels



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PROGRAM