2010 IEEE Radio Frequency Integrated Circuits Symposium

Anaheim, California

May 23-25, 2010

PROGRAM

Anaheim Convention Center

Sponsored by
IEEE Microwave Theory and Techniques Society
IEEE Electron Device Society
and
The IEEE Solid-State Circuits Society

RFIC Plenary and Reception
Sunday Night (May 23, 2010)

After a busy day of outstanding RFIC Workshops (see page 65-82) the Plenary Session and RFIC Reception will be held on Sunday evening – May 23, 2010. The Plenary Session is at 5:30pm in the Anaheim Convention Center (ACC), Room 210ABCD. The Plenary Session will include two outstanding speakers (see pages 8-9), and the Student Paper Award ceremony. Immediately following the RFIC Plenary Session at 07:00pm is the RFIC Reception in the ACC, Room 213BCD. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The Reception is sponsored by the RFIC Steering Committee and Platinum Sponsor Skyworks, Inc.

RFIC Week Activities (May 23-25)

Saturday May 22, 2010

02:00pm - 06:00pm Registration – ACC

Sunday May 23, 2010

07:00am - 06:00pm Registration – ACC
07:00am - 08:00am Attendee Breakfast – ACC, Meeting Foyers
08:00am - 05:00pm Workshops and Tutorials – ACC
05:30pm - 06:40pm RFIC Plenary – ACC, Room 210ABCD
07:00pm - 09:00pm RFIC Reception – ACC, Room 213BCD

Monday May 24, 2010

07:00am - 05:00pm Registration – ACC
07:00am - 08:00am Attendee Breakfast – ACC, Meeting Foyers
08:00am - 05:10pm RFIC Technical Sessions (see pages 10-41)
08:00am - 09:40am RMO1A RMO1B RMO1C RMO1D
10:10am - 11:50am RMO2A RMO2B RMO2C RMO2D
11:50am - 01:20pm RFIC Panel and Lunch – ACC, Room 210CD
01:20pm - 03:00pm RMO3A RMO3B RMO3C RMO3D
03:30pm - 05:10pm RMO4A RMO4B RMO4C RMO4D

Tuesday May 25, 2010

07:00am - 05:00pm Registration – ACC
07:00am - 08:00am Attendee Breakfast – ACC, Meeting Foyers
08:00am - 04:00pm RFIC Oral and IF Technical Sessions (see pages 42-61)
08:00am - 09:40am RTU1B RTU1C RTU1D
11:50am - 01:20pm RFIC Panel and Lunch – ACC, Room 210CD
01:20pm - 03:00pm RTU2A RTU2C RTU2D
02:00pm - 04:00pm RTUIF – ACC, Rooms 208AB and 209AB

This Program can be found on the RFIC website http://www.rfic2010.org. IMS sessions and exhibits are held on Tuesday - Thursday. IMS program can be found on the IMS website www.ims2010.org.

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The RFIC Symposium will be held in Anaheim, California at the Anaheim Convention Center on May 23-25, 2010 in conjunction with the International Microwave Symposium. It opens Microwave week 2010, the largest RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF Systems, circuit device, and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Message from the General Chair

Yann Deval

On behalf of the Steering Committee, I would like to welcome you to the RFIC Symposium!

The 2010 RFIC Symposium maintains its reputation as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development for wireless and wireline communication IC's. Running in conjunction with the International Microwave Symposium and Exhibition, the RFIC Symposium adds to the excitement of Microwave Week with three days focused exclusively on RFIC technology and innovation. The RFIC symposium will be held at the Anaheim Convention Center, May 23-25, 2010.

The RFIC Symposium will start on Sunday with half-day and full-day workshops, covering a large breadth of topics. Some of the topics include: SiGe HBTs towards THz operation, power management for integrated RF circuits, challenges and techniques for 3G/4G multi-mode front end designs and silicon-based design techniques for millimeter-wave applications. Don't miss out on this great opportunity to expand your horizons!

Sunday evening activities continue at 5:30pm with RFIC Plenary Session. Two renowned speakers will share their views on the direction and challenges that the RF IC industry will be facing. The first speaker is Professor David Allstot from the University of Washington, and the second speaker is Gregory Waters, Executive Vice President of Skyworks Inc. In addition to the keynote addresses, the best student paper awards are presented in the Plenary Session. The highly anticipated RFIC Reception will follow immediately after the Plenary Session, providing a relaxing time for all to mingle with old friends and catch up on the latest news.

The technical program includes oral sessions, an Interactive Forum (poster session), and two exciting lunch panel sessions. The oral presentation sessions start on Monday, May 24th with four parallel sessions throughout the morning and the afternoon. The oral sessions continue on Tuesday, May 25th synchronized with the IMS technical Program. The Interactive Forum will be held on Tuesday afternoon. This forum is the perfect place to have an opportunity to have more detailed technical discussions with the authors. Panel Sessions are also planned at lunch time on Monday and Tuesday, the topic being respectively "The Challenges, Competitions and Future Prospect of 60 GHz" and "Future of High-Speed I/O: Electrical, Optical, or Wireless?".

The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall.

The RFIC organization is thankful to the IMS2010 team, without whom we could not make this conference successful. Most of all, we are particularly thankful to all the technical contributors to the RFIC Symposium. We look forward to your participation. Please continue to make this conference so vibrant within the wireless industry!

I look forward to seeing you in Anaheim!

Yann Deval
General Chair
2010 RFIC Symposium

Message from the Technical Program Committee Chairs

David Ngo

Chris Rudell

On behalf of the Technical Program Committee, welcome to the 2010 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. This is a leading-edge IEEE technical conference dedicated to the advancement of integrated circuits and sub-systems for RF, wireless, broadband communications, and many other emerging applications. The RFIC Technical Program Committee has worked diligently to select the best papers and assemble an excellent technical program this year. The symposium's main features include several tutorial workshops, a Plenary Session, an Interactive Forum and numerous technical paper sessions. This year the RFIC Symposium begins on Sunday, May 23rd with workshops at the advanced and tutorial level addressing topics which challenge present day RF IC designers with respect to design techniques in advanced silicon technologies, design and integration of ICs for new emerging wireless application and the latest advances in circuit and system simulation. The Plenary Session will be held on Sunday evening, following the workshops, at which time the General Chair will present best paper awards to the top three student manuscripts of this year's conference.

Two leading experts from the RFIC community will share their views during the plenary session. The first speaker is Professor David James Allstot from the University of Washington, who will present his vision of one of the last great challenges of RF CMOS integration in his talk, ''Power Amplification: Can CMOS Deliver?'' The second speaker, Gregory L. Waters, Executive Vice President and General Manger, Skyworks Solutions, Inc., will discuss ''The Universal Connector: RF Application Trends Over The Next Decade''

The RFIC Reception will follow immediately after the plenary session, providing a relaxing time for all to mingle with old friends and catch up on the latest news. In addition to the technical sessions on Monday and Tuesday, the RFIC Symposium also features panel sessions and many workshops. Monday's lunch panel session entitled "The Challenges, Competitions and Future Prospect of 60GHz" has panelists from both industry and academia debating the future of high data rate wireless networks. Tuesday's lunch panel session, "Future of High-Speed I/O: Electrical, Optical or Wireless?", is posed to stimulate interactive discussions with the audience.

The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to make the RFIC Symposium the technical forum of choice for both industry and academia, to meet, discuss results and exchange ideas. The 2010 RFIC Technical Program Committee will continue to work tirelessly toward the goal of strengthening the technical quality and scope of the program, while maintaining and improving the legacy left by previous Symposia. Of course the success of our conference would simply not be possible without the many contributions of all the authors who put enormous effort each year, to contribute both outstanding presentations and excellent manuscripts. On behalf of the entire Steering and Technical Program Committees, we thank everyone for attending the conference.

We hope you enjoy the 2010 RFIC Symposium!

David Ngo and Chris Rudell
Technical Program Chairs
2010 IEEE RFIC Symposium

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RFIC Schedule 2010

The RFIC Symposium will be held in Anaheim, CA in the Anaheim Convention Center (ACC). The headquarters hotel is the Anaheim Hilton Hotel which is adjacent to the ACC. The RFIC Plenary and Reception will be held on Sunday May 23, starting at 5:30pm.

The RFIC Symposium is held as part of Microwave week. It is followed by the IMS Symposium and Exhibition and by ARFTG. Attendees of RFIC are invited to attend the IMS Plenary Session which will be held on Tuesday Morning, May 25, 2010.

Saturday May 22, 2010

02:00pm - 06:00pm	Registration – ACC

Sunday May 23, 2010

07:00am - 06:00pm	Registration – ACC
06:30am - 08:30am	Speakers Breakfast – ACC, Room 304D
07:00am - 08:00am	Workshop Breakfast – ACC, Meeting Foyers
08:00am - 05:00pm	Workshops and Tutorials – ACC
12:00pm - 01:00pm	Workshop Lunch – ACC, Meeting Foyers
05:30pm - 06:40pm	RFIC Plenary – ACC, Room 210ABCD
07:00pm - 09:00pm	RFIC Reception – ACC, Room 213BCD

Monday May 24, 2010

07:00am - 05:00pm	Registration – ACC
06:30am - 08:30am	Speakers Breakfast – ACC, Room 304D
07:00am - 08:00am	Attendee Breakfast – ACC, Meeting Foyers
07:00am - 05:00pm	Speaker's Prep Room – ACC, Room 203A
08:00am - 05:10pm	RFIC Technical Sessions (see pages 10 to 41)
08:00am - 09:40am	RMO1A, RMO1B, RMO1C, RMO1D
09:40am - 10:10am	Break
10:10am - 11:50am	RMO2A, RMO2B, RMO2C, RMO2D
11:50am - 01:20pm	RFIC Panel and Lunch – ACC, Room 210CD
11:50am - 01:20pm	RFIC-TPC Lunch – ACC, Room TBD
01:20pm - 03:00pm	RMO3A, RMO3B, RMO3C, RMO3D
03:00pm - 03:30pm	Break
03:30pm - 05:10pm	RMO4A, RMO4B, RMO4C, RMO4D

Tuesday May 25, 2010

07:00am - 05:00pm	Registration – ACC
07:00am - 08:00am	Speaker's Breakfast – ACC, Room 304D
07:00am - 08:00am	Attendee Breakfast – ACC, Meeting Foyers

07:00am - 05:00pm	Speaker's Prep Room – ACC, Room 203A
08:00am - 04:00pm	RFIC Oral and IF Sessions (see pages 42 to 61)
08:00am - 09:40am	RTU1B, RTU1C, RTU1D
11:50am - 01:20pm	RFIC Panel and Lunch – ACC, Room 210CD
12:00pm - 01:00pm	RFIC Steering Committee Meeting – ACC, Huntington ABC
01:20pm - 03:00pm	RTU2A, RTU2C, RTU2D
02:00pm - 04:00pm	RTUIF – ACC, Rooms 208AB, 209AB

Plenary Schedule

Sunday, May 23, 2010
05:30 PM
Anaheim Convention Center, ACC, Room 210ABCD
Session RSU5A: RFIC Plenary

Chair: Yann Deval, University of Bordeaux, IMS Lab
Session Co-Chairs: David Ngo, RFMD,
Jacques C. Rudell, University of Washington

05:30pm Welcome message from General and TPC Chairs, Announcement of Student Paper Awards

05:45pm **RSU5A-1:** RF Power Amplification: Can CMOS Deliver?
David J. A. Allstot, Dept. of Electrical Engineering, University of Washington

06:15pm **RSU5A-2:** The Universal Connector: RF Applications Trends Over the Next Decade, **Gregory L. Waters,** Skyworks Solutions, Inc.

Plenary Speaker 1:

David J. Allstot –
Boeing-Egtvedt Chair Professor
Department of Electrical Engineering
University of Washington

RF Power Amplification: Can CMOS Deliver?

Abstract: The total energy consumed by cellular telephones in the United States is currently estimated at about 750,000 times the energy used by an average home in one year. Moreover, about 7,500 tons of CO2 are emitted into the atmosphere.

The RF power amplifier dissipates a large fraction of the total power because of its low efficiency. Despite more than two decades of intensive research, the challenge of on-chip RF PAs with high efficiency in digital-friendly CMOS technologies has not been met.

Switching PA topologies with relatively high efficiency have gained momentum for use in CMOS RF transceivers, and relatively high output power is being delivered using power combining techniques with several PA cells. Supply regulation techniques have enabled higher efficiency when amplifying non-constant envelope modulated signals.

This talk will cite leading-edge designs and on-going research to assess the remaining challenges for CMOS RF power amplifiers.

About David J. Allstot:

David J. Allstot received the B.S. from the Univ. of Portland in 1969, the M.S. from Oregon State Univ. in 1974 and the Ph.D. from the Univ. of California, Berkeley in 1979.

He has held several industrial and academic positions and has been the Boeing-Egtvedt Chair Professor of Engineering at the Univ. of Washington since 1999. He was Chair of the Dept. of Electrical Engineering from 2004 to 2007.

Dr. Allstot has advised approximately 100 M.S. and Ph.D. graduates, published about 275 papers, and received several awards for outstanding teaching and graduate advising. Awards include the 1980 IEEE W.R.G. Baker Award, 1995 IEEE Circuits and Systems Society (CASS) Darlington Award, 1998 IEEE International Solid-State Circuits Conference (ISSCC) Beatrice Winner Award, 1999 IEEE CASS Golden Jubilee Medal, 2004 IEEE CASS Technical Achievement Award, 2005 Semiconductor Research Corp. Aristotle Award, and 2008 Semiconductor Industries Assoc. University Research Award. His service includes: 1990-93 Assoc. Editor and 1993-95 Editor of IEEE TCAS II, 1990-93 Member of Technical Program Committee of the IEEE CICC Conference, 1992-95 Member, Board of Governors of IEEE CASS, 1994-2004, Member, Technical Program Committee, IEEE ISSCC, 1995-97, 2001, 2003-04, Member, Executive Committee of IEEE ISSCC, 1996-2000 Short Course Chair of IEEE ISSCC, 2000-2001 Distinguished Lecturer, IEEE CASS, 2001 and 2008 Co-General Chair of IEEE ISCAS, 2006-2007 Distinguished Lecturer, IEEE Solid-State Circuits Society and 2009 President of IEEE CASS.

Plenary Speaker 2:

Gregory L. Waters –
Executive Vice President and General Manager,
Skyworks Solutions, Inc.

The Universal Connector: RF Application Trends Over the Next Decade

Abstract: RF technology has enjoyed a significant expansion in consumer electronics and everyday appliances over the past two decades. This presentation will outline key new opportunities and requirements for the RF industry to assume a much greater application reach. This talk will outline why RF growth will accelerate in non-traditional markets, and the key technical and commercial problems that must be solved to enable this. We will conclude with examples of how this growth will affect industry R&D practices, and result in a different business model for leading RF firms.

About Gregory L. Waters:

Gregory L. Waters, 49, is executive vice president and general manager, front-end solutions for Skyworks Solutions, Inc. He joined the company in April 2003. Prior to joining Skyworks, he served as senior vice president of Strategy and Business development at Agere Systems, and previously held positions there as Vice president of the Wireless Communications business, and Vice president of the Broadband Communications business. Prior to this, he held a variety of senior management positions within Texas Instruments, including director of Network Access Products and Director of North American sales.

Waters received a bachelor's of science in engineering from the University of Vermont, and a master's in computer science from Northeastern University.

Monday May 24, 2010
08:00 AM
ACC - Room 208AB
Session: RM01A: Cellular Transceivers
Chair: Fazal Ali, Qualcomm
Co-Chair: Didier Belot, ST Microelectronics

RM01A-1 08:00 AM
A 28mW WCDMA/GSM/GPRS/EDGE Transformer-Based Receiver in 45nm CMOS

D. L. Griffith, V. Srinivasan, S. Pennisi, V. Rentala, Y. Su, S. Sankaran, I. Elahi, S. Samala, H. Kiper, B. Patel, S. Akhtar, D. Edmondson, Texas Instruments

Abstract: A transformer-based receiver in 45nm CMOS that meets WCDMA, GSM, GPRS, and EDGE system requirements is presented. The receiver requires no SAW filters and consumes 20mA from 1.4V. The LNA has a transformer at the output to achieve high linearity performance by lowering the voltage swing while simultaneously providing current gain. The analog back end is implemented with two cascaded gain stages and a 2nd order $\Sigma\Delta$ADC. The receiver 60dB gain, NF of 3dB, and IP2>+50dBm. The die area is 1.35mm^2.

RM01A-2 08:20 AM
An EDGE Transmitter with Mitigation of Oscillator Pulling

I. Bashir, R. B. Staszewski, O. Eliezer, K. Waheed, V. Zocias, N. Tal, J. Mehta, P. T. Balsara, B. Banerjee, University of Texas at Dallas, Texas Instruments Inc., USA, Delft University of Technology, Netherlands

Abstract: We propose a polar transmitter architecture that is robust to modulation-induced injection pulling of its RF oscillator by means of a built-in self compensation. A mathematical model is presented which incorporates a digitally-controlled delay that minimizes pulling by adjusting the phase between the final amplitude modulation stage and the RF oscillator. The technique is verified in a 65-nm CMOS GSM/GPRS/EDGE SoC demonstrating compliant error vector magnitude (EVM) and modulation spectral-mask.

RM01A-3 08:40 AM
An All-Digital Offset PLL Architecture

R. B. Staszewski, S. Vemulapalli*. Texas Instruments, *Delft University of Technology

Abstract: We propose an all-digital offset PLL architecture in which the RF oscillator output is frequency translated through quad phase rotation in a simple digital multiplexer before being fed back for the phase comparison with the frequency reference clock. This eliminates spurious tones caused by the finite resolution of the phase detection process when the synthesized frequency is very close to the integer-N multiple of the reference frequency. The technique is validated in a 65-nm CMOS transceiver.

RM01A-4 09:00 AM
An Interstage Filter-Free Mobile Radio Receiver with Integrated TX Leakage Filtering

R. Vazny, W. Schelmbauer, H. Pretl, S. Herzinger*, R. Weigel**, Danube Integrated Circuit Engineering GmbH, Austria, *Infineon Technologies AG, Germany, **Institute for Electronics Engineering Friedrich-Alexander-University Erlangen-Nuremberg, Germany

Abstract: A multi-standard, multi-band fully-integrated interstage filter-free receiver with integrated auto-centered TX leakage filtering is fabricated in a 65 nm CMOS technology. The measured TX selectivity in UMTS band II is 9.1 dB, the receiver gain at 1.96GHz is 54.1 dB, and NF is 3.68 dB. The 0.5 dB reference sensitivity degradation caused by TX leakage is reached at a TX power level of - 20 dBm/3.84MHz.

RM01A-5 09:20 AM
A SAW-less CMOS TX for EGPRS and WCDMA

K. Hausmann, J. Ganger, M. Kirschenmann, G. B. Norris, W. Shepherd, V. Bhan, and D. B. Schwartz, Fujitsu Microelectronics of America

Abstract: A 90 nm CMOS TX path architected for operation without inter-stage SAW filters is shown. The SAW elimination strategy is purely low noise design but the architecture still achieves DG.09 weighted TX current drain of 50 mA from the battery. The combination of a passive interleaved switching mixer plus digital gain control allows 2% EVM at 2 dbm and 4.2% at -78 dbm.

Monday May 24, 2010
08:00 AM
ACC - Room 209AB
Session: RMO1B: RF CMOS Modulators & Receivers
Chair: Sayfe Kiaei, Arizona State University
Co-Chair: Noriharu Suematsu, Tohoku University

RMO1B-1 08:00 AM
A Quadrature Charge-Domain Filter with an Extra In-Band Filtering for RF Receivers

Ming-Feng Huang, SoC Technology Center, Industrial Technology Research Institute, Taiwan

Abstract: A quadrature charge-domain filter (QCDF) for RF receivers is proposed. This QCDF, based on the input phases, could provide a stop-band filtering and support an in-band filtering. Through the use of FIR coefficient, the alias-band rejection (ABR) and in-band suppression (IBS) could be controlled. The measurement shows 27.1dB ABR and 31.3dB IBS from out-of-phase signals and in-phase signals, respectively. The QCDF occupied 0.98mm^2 area is fabricated on the TSMC 90nm CMOS process.

RMO1B-2 08:20 AM
A Low-Power Receiver Down-Converter with High Dynamic Range Performance

D. Ghosh, R. Gharpurey, University of Texas, Austin, USA

Abstract: A low-power down-converter that uses a passive current-commutating mixer for frequency translation, while sharing the bias between the RF and baseband stages is presented. An active noise shaping network is implemented to reduce low-frequency noise at the output. Linearity is enhanced through the use of non-linear feedback. The design, implemented in a 0.18 μm CMOS technology, achieves conversion gain of 35 dB, NF of 9.8 dB, in-channel OIP3 of 15.8 dBV while consuming 2.1 mA from a 1.8 V supply.

RM01B-3 08:40 AM

A Multiphase PWM RF Modulator Using a VCO-Based Opamp in 45nm CMOS

M. Park, M. H. Perrott*, Massachusetts Institute of Technology (now at Maxim Integrated Products), *SiTime Corporation

Abstract: A VCO-based RF modulator employing multiphase PWM is presented. The proposed RF modulator encodes the baseband signal into a set of multiphase PWM signals which are generated by a VCO-based opamp. The use of PWM avoids broadband quantization noise which is produced by **ΣΔ** modulation used in other RFDAC-based modulators. The prototype IC is fabricated in a 45nm CMOS process, consumes 54.3 mW. The measured results satisfy the 802.11g WLAN spectral mask, and EVM for 10-MHz OFDM at 2.4GHz is -30 dB.

RM01B-4 09:00 AM

Spurious Noise Reduction by Modulating Switching Frequency in DC-to-DC Converter for RF Power Amplifier

E. J. KIM, C. Cho*, W. Kim*, C.-H. Lee*, J. Laskar, Georgia Institute of Technology at Atlanta, *Samsung Design Center at Atlanta

Abstract: The presence of a spectrum spreading effect in a DC-DC converter with a modulated switching frequency is analyzed. A DC-to-DC converter with a digital Pulse-Width Modulation ramp signal modulator is implemented in a standard CMOS 0.18-μm process. A low-power digital modulator is used to vary the switching frequency as means of decreasing spurious noise peaks at the output of the switch converter. The measurement shows that the spurious noise peak is reduce 12dB by a monotonic frequency stepping.

RM01B-5 09:20 AM

A Rail-To-Rail Input Receiver Employing Successive Regeneration and Adaptive Cancellation of Intermodulation Products

Edward A. Keehr, Ali Hajimiri, California Institute of Technology

Abstract: A direct conversion receiver is demonstrated which operates in the presence of a rail-to-rail (+12.6dBm) out-of-band blocker and a -16.6dBm blocker, where the ICP1 is +12.5dBm and the effective uncorrected IIP3 is +34.2dBm. IM distortion is adaptively cancelled via feedforward loops that are digitally expanded to reproduce higher order nonlinear reference terms to be used in cancellation. Cancellation improves input-referred even order distortion by over 18dB and overall distortion by over 17dB.

Monday May 24, 2010
08:00 AM
ACC - Room 211AB
Session: RMO1C: Frequency Generation and Synthesis
Chair: Lawrence Kushner, Intersil Co.
Co-Chair: Bertan Bakkaloglu, Arizona State University

RMO1C-1 08:00 AM
A D-Band PLL Covering the 81-82GHz, 86-92GHz and 162-164GHz Bands

S. Shahramian*, A. Hart*, A.C. Carusone*, P. Garcia**, P. Chevalier**, S.P. Voinigescu*,
*University of Toronto, Canada, **STMicroelectronics, France

Abstract: The highest frequency PLL reported to date is presented. It also achieves the widest locking range (81-82GHz, 86-92GHz, 162-164GHz), and the lowest phase noise (-93.8dBc/Hz at 90GHz and -78.9dBc/Hz at 163GHz), both measured at a 100kHz offset. It is fabricated in a 0.13µm SiGe BiCMOS process and integrates two VCOs, a programmable prescaler, charge-pump, and all loop filter components. The PLL output power is -3dBm at 90GHz and -25dBm at 164GHz and consumes 1.25W. The chip area is 1.1mm x 1.7mm.

RMO1C-2 08:20 AM
An Integrated Frequency Synthesizer for 81-86GHz Satellite Communications in 65nm CMOS

Zhiwei Xu, Qun Jane Gu, Yi-Cheng Wu, Heng-Yu Jian, Frank Wang, Mau-Chung Frank Chang,
University of California, Los Angeles, CA 90095, USA

Abstract: We present a frequency synthesizer integrated in transceiver to support 81-86GHz satellite communications in 65nm CMOS. It also features coarse phase rotation to endow the system beam forming capability. The synthesizer core occupies 0.16mm^2 chip area and covers the desired frequency bands. The phase noise is -83dBc/Hz at 1MHz offset deriving from the tested phase noise at one eighth of the VCO frequency (~9.4GHz). Measured reference spur is -49dBc. Total power consumption is 65mW at 1V supply.

RMO1C-3 08:40 AM

Low-Noise Fractional-N PLL Design with Mixed-Mode Triple-Input LC VCO in 65nm CMOS

Yuanfeng Sun*, Xueyi Yu*, Woogeun Rhee*, Sangsoo Ko**, Wooseung Choo**, Byeong-Ha Park**, and Zhihua Wang*, *Tsinghua University, Beijing, China, **MSC Development Team, Samsung Electronics, Yongin-City, Gyeonggi-Do, Korea

Abstract: This paper presents a low-noise ΣΔ fractional-N PLL utilizing a mixed-mode triple-input LC VCO. An analog dual-path VCO control relaxes the nonlinearity problem of the ΣΔ PLL, while a combination of discrete and continuous tuning methods for the coarse-tuning control significantly alleviates noise and coupling problem. A 3.6GHz ΣΔ fractional-N PLL implemented in 65nm CMOS exhibits nearly -100dBc/Hz in-band noise and -53dBc in-band fractional spur performances from a 1.8GHz carrier.

RMO1C-4 09:00 AM

A Wideband Millimeter-Wave Frequency Doubler-Tripler in 0.13-μm CMOS

S. Saberi Ghouchani, J. Paramesh, Carnegie Mellon University

Abstract: A combined frequency doubler and tripler is proposed for wideband millimeter wave frequency generation in CMOS. The circuit consists of a push-push FET frequency doubler along with a single balanced mixer based frequency tripler. The frequency doubler-tripler can generate frequencies in the range of 23-48GHz with more than -20dBm output power into 50Ω. The conversion gains of the doubler and tripler are measured to be -2.6dB and -12.3 dB, respectively, with a 0dBm input at 14.4GHz.

RMO1C-5 09:20 AM

200GHz CMOS Prescalers with Extended Dividing Range via Time-Interleaved Dual Injection Locking

Qun Jane Gu*, Heng-Yu Jian*, Zhiwei Xu*, Yi-Cheng Wu*, Mau-Chung Frank Chang*, Yves Baeyens** and Young-Kai Chen**, *University of California, Los Angeles, CA, USA, **Alcatel-Lucent/Bell-Labs, Murray Hills, NJ, USA

Abstract: A unique time-interleaved dual injection locking scheme has been devised to enable ultra high-speed, low-power frequency division with extended locking range. To prove the concept, two prescalers are realized in 65nm CMOS: one divides continuously from 158GHz to 195GHz, the other divides from 181GHz to 208GHz. These test results set the highest F.O.M. for prescalers implemented in any semiconductor technology up to this date, which in both cases is almost 10 times higher than that of prior arts.

Monday May 24, 2010
08:00 AM
ACC - Room 212AB
Session: RMO1D: W-band and Above
Chair: Jenshan Lin, University of Florida
Co-Chair: Georg Boeck, Berlin Institute of Technology

RMO1D-1 08:00 AM
Transmitter Chipset for 24/77GHz Automotive Radar Sensors

V. Giammello, E. Ragonese, G. Palmisano, Università di Catania, Facoltà di Ingegneria, DIEES, Catania, Italy

Abstract: This paper presents a BiCMOS transmitter chipset for 24/77GHz automotive radar sensors. The chipset adopts a dual-band architecture consisting of a 24GHz section for ultra-wideband short-range radar operation, which is able to drive the 77GHz long-range radar transmitter front-end. The proposed solution allows using a single 24GHz frequency synthesizer to implement both operation modes. The 77GHz transmitter demonstrates an output power of 12 dBm, a gain of 20 dB and an OP1dB of 11dBm.

RMO1D-2 8:20 AM
A 94GHz Passive Imaging Receiver using a Balanced LNA with Embedded Dicke Switch

L. Gilreath, V. Jain*, H.C. Yao, L. Zheng, and P. Heydari, University of California, Irvine, *SaberTek, Irvine CA

Abstract: A fully-integrated silicon-based 94GHz direct-detection imaging receiver with on-chip Dicke switch and baseband circuitry is demonstrated. Fabricated in a 0.18-µm SiGe BiCMOS technology (fT/fMAX = 200GHz), the receiver chip achieves a peak imager responsivity of 43 MV/W with a 3-dB bandwidth of 26GHz. A balanced LNA topology embedded with a Dicke switch provides 30-dB gain and enables a temperature resolution of 0.3-0.4 K. The imager chip consumes 200 mW from a 1.8-V supply.

RM01D-3 08:40 AM

94GHz Silicon Co-integrated LNA and Antenna in a mm-wave Dedicated BiCMOS Technology

R. Pilard (1,2), D. Gloria (1), F. Gianesello (1), F. Le Pennec (2), C. Person (2),
(1) STMicroelectronics, (2) Lab-STICC/MOM, FRANCE

Abstract: A co-integrated LNA with a dipole antenna is designed considering a millimeter-wave dedicated BiCMOS technology. The LNA is based on a high-speed SiGe:C 130 nm HBT. The interest of the co-integration on a common silicon substrate is demonstrated through the decrease of insertion loss between the antenna and the amplifier. The capability of the BiCMOS9MW is demonstrated. A 1-stage configuration achieves a total gain of 3dB (G-LNA+G-Antenna). A 2-stage configuration reaches a total gain of 8.5dB.

RM01D-4 09:00 AM

A 3 G-Bit/s W-Band SiGe ASK Receiver with a High-Efficiency On-Chip Electromagnetically-Coupled Antenna

Jason W. May, Ramadan A. Alhalabi, Gabriel M. Rebeiz, University of California at San Diego

Abstract: A novel high-efficiency on-chip W-Band microstrip antenna is designed in a commercial SiGe process (IBM 8HP). The antenna has a measured gain of 2-4 dB and an efficiency of 50-57% at 92-98GHz. An ASK receiver including a W-Band SPDT, LNA, and power detector is integrated with the antenna and is used to demonstrate a low-power 94GHz 3-Gb/s on-chip wireless data link.

RM01D-5 09:20 AM

A 325GHz Frequency Multiplier Chain in a SiGe HBT Technology

E. Öjefors, B. Heinemann*, U. R. Pfeiffer, University of Wuppertal, *IHP GmbH, Germany

Abstract: A single-chip 325GHz x18 frequency multiplier chain based on two cascaded active differential triplers and a balanced output doubler is presented. The multiplier operates over a 317 to 328GHz bandwidth with a 0-dBm 18GHz input signal. A peak output power of -8 dBm is obtained at 325GHz. The multiplier chain is realized in an evaluation SiGe HBT technology with cut-off frequencies fT/fmax} of 250GHz / 380GHz.

Monday May 24, 2010
10:10 AM
ACC - Room 208AB
Session: RMO2A: RFID Circuits
Chair: Glenn Chang, MaxLinear
Co-Chair: Natalino Camilleri, Alien Technology

RMO2A-1 10:10 AM
Semi-Active High-Efficient CMOS Rectifier for Wireless Power Transmission

S. T. Kim, T. Song, J. Choi, F. Bien*, K. Lim, J. Laskar, Georgia Institute of Technology, *Ulsan National Institute of Science and Technology

Abstract: A semi-active high-efficient (SA-HE) CMOS rectifier with a reverse leakage control has been developed. It employs a cross-coupled NMOS pairs and two leakage control comparators to reduce reverse charge leakage current. In addition, the adaptive body bias control technique is utilized to improve the reliability of the rectifier. The SA-HE rectifier has been fabricated in a 0.18μm CMOS technology and it shows 15% improvement over the conventional ones.

RMO2A-2 10:30 AM
A Single-Chip CMOS UHF RFID Reader Transceiver

Runxi Zhang, Chunqi Shi, Yihao Chen, Wei He, Ping Xu, Shuai Xu and Zongshen Lai, Dept. of Electronic Engineering, Suzhou Vocational University, IMCS, East China Normal University, Shanghai, China

Abstract: A novel single-chip 860-960MHz band UHF RFID reader transceiver IC is fabricated in 0.18μm CMOS process. The transceiver consists of a compact high-linearity low-noise-figure RF front-end, a programmable analog baseband for Rx path; and an image reject filter, a PGA, a switchable up-conversion modulator and a driver amplifier for Tx path. The 3-bit 3rd-order DSM fractional-N frequency synthesizer with optimized all-band phase noise performance implements Rx/Tx frequency translation.

RMO2A-3 10:50 AM

Near Zero Turn-on Voltage High-Efficiency UHF RFID Rectifier in Silicon-on-Sapphire CMOS

P. T. Theilmann, C. D. Presti, *D. Kelly, P. M. Asbeck, University of California at San Diego, *Peregrine Semiconductor Corp., USA

Abstract: A UHF RFID rectifier which turns on at near zero input voltage is demonstrated in 0.25-μm silicon-on-sapphire (SOS) CMOS using near zero threshold devices. A novel improved cross-coupled bridge topology is used. The fabricated rectifier demonstrates a peak efficiency (PCE) of 71.5% at 915MHz with a RF input of -4 dBm and a 30kΩ load. More importantly, a PCE>30% was measured for all input powers between -28 and -4 dBm demonstrating state-of-the-art efficiency across a wide range of input powers.

RMO2A-4 11:10 AM

A Low Power Low Cost Fully Integrated UHF RFID Reader with 17.6dBm Output P1dB in 0.18 μm CMOS Process

J.C. Wang, C. Zhang, Z.H. Wang, Institute of Microelectronics, Tsinghua University

Abstract: A low power low cost fully integrated single-chip UHF radio frequency identification (RFID) reader for short distance handheld applications is presented in this paper. The IC integrates all building blocks-including an RF transceiver, a PLL frequency synthesizer, a digital baseband and a MCU-in a 0.18 μm CMOS process. The measured output P1dB power of the transmitter is 17.6dBm and the measured receiver sensitivity is -60dBm while the total power consumed is 285.4mW.

RMO2A-5 11:30 AM

Far-field RF Powering System for RFID and Implantable Devices with Monolithically Integrated On-Chip Antenna

Soheil Radiom, Majid Baghaei-Nejad*, Guy Vandenbosch, Li-Rong Zheng*, Georges Gielen, MICAS-ESAT, Katholieke Universiteit Leuven Belgium, *Royal Institute of Technology Stockholm Sweden

Abstract: A fully integrated far-field powering system for RFID and implantable devices with monolithically fully integrated on-chip antenna in 0.18μm CMOS is presented. The chip receives power, clock and data wirelessly through RF signal at all the three ISM bands of 915 MHz, 2.45GHz and 5.8GHz. Measurements show with the on-chip antenna at 5.8GHz, the chip can be powered-up at 7.5 cm distance. At 900MHz the minimum input power of -19.41 dBm is needed corresponding to 15.7 meter distance.

Monday May 24, 2010
10:10 AM
ACC - Room 209AB
Session: RMO2B: Wideband LNAs
Chair: Jean-Baptiste Begueret, IMS Lab, University of Bordeaux
Co-Chair: Danilo Manstretta, University of Pavia

RMO2B-1 10:10 AM
A 2-1100 MHz Wideband Low Noise Amplifier with 1.43 dB Minimum Noise Figure

M. El-Nozahi, A. A. Helmy, E. Sanchez-Sinencio, K. Entesari, Department of Electrical and Computer Engineering, Texas A&M University, College station, TX, 77843

Abstract: A new wideband LNA is proposed. The LNA utilizes a composite NMOS/PMOS cross-coupled transistor pair to increase the amplification while reducing the NF. The proposed approach provides partial cancellation of noise generated by the input transistors, hence, lowering the overall NF. An implemented prototype using 90nm CMOS technology shows a measured conversion gain of 20dB across 2-1100MHz, an IIP3 of -1.5dBm at 100MHz, and minimum NF of 1.43dB. The LNA consumes 18mW and occupies 0.06mm^2.

RMO2B-2 10:30 AM
An 0.045mm^2 0.1-6GHz Reconfigurable Multi-band, Multi-gain LNA for SDR

A. Geis*, **, Y. Rolain*, G. Vandersteen*, J. Craninckx**, * Vrije Universiteit Brussel, Belgium, ** IMEC, Belgium

Abstract: A low area fully reconfigurable multi-band LNA based on active feedback amplifiers with mixed resistive and switched inductor loads is presented. The 90nm CMOS implementation covers the entire frequency range of interest for SDR from 0.1 to 6GHz with a dynamic gain range from 0dB to 22dB.A NF as low as 2.7dB and an IIP3 of -4dBm at 16dB gain is achieved. An IIP3 of +9dBm is reached in low gain mode. The LNA draws between 10 and 26mA from a 1.2V supply. The active area of the LNAs is only 0.045mm^2.

RMO2B-3 10:50 AM
A Linearity-Enhanced Wideband Low-Noise Amplifier
K. Choi, T. Mukherjee*, J. Paramesh*, Samsung Electronics, *Carnegie Mellon University

Abstract: Two techniques, namely Wideband Derivative Superposition and Self-biased Current Re-use, are proposed to enhance linearity over wide bandwidths in a low-voltage wideband LNA. Two LNAs are designed in 0.13 μm CMOS to demonstrate these techniques: the (Chebyshev, transformer) LNAs achieved (+10.6, +12.0) dBm IIP3 over (2.3-6.0, 2.0-5.3)GHz, (12.7, 12.4) dB gain, (4.8, 4.9) dB noise figure, while consuming 6.9mA from 1.2V.

RMO2B-4 11:10 AM
Power Efficient Distributed Low-Noise Amplifier in 90 nm CMOS
B. Machiels, P. Reynaert, M. Steyaert, K.U.Leuven, ESAT-MICAS

Abstract: A low-power wideband distributed low noise amplifier (DLNA) in 90 nm CMOS is presented. Various techniques have been combined in the design to increase the distributed amplifier's power efficiency. These techniques range from moderate inversion biasing to transmission line tapering. The measured gain of the 12.5 mW DLNA is larger than 15 dB from DC to 21GHz. The average noise figure in the pass-band is 5.4 dB, the IIP3 at 5GHz is -6.6 dBm and the total die area is 0.41 square mm.

RMO2B-5 11:30 AM
A Wide-Band RF Front-End with Linear Active Notch Filter for Mobile TV Applications
Seung Hwan Jung, Kang Hyuk Lee, Young Jae Lee*, Hyun Kyu Yu* Yun Seong Eo, University of Kwangwoon in Seoul Korea, *Eelctronic and Telecommunications Research Institute in Daejon Korea

Abstract: This paper presents a wide-band RF front-end with linear active notch filter covering both T-DMB and DVB-H. A single to differential converter with the low amplitude/phase error and 6dB step RF VGA using the capacitor are implemented. Also, highly linear and Q-enhanced tunable active inductor is proposed. The linear active notch filter rejects GSM band up to 23dB and achieves 20dB linearity improvement. The RF front-end is fabricated on 90nm CMOS technology and consumes 29.7mW.

Monday May 24, 2010
10:10 AM
ACC - Room 211AB
Session: RMO2C: Millimeter-Wave VCOs
Chair: Jing-Hong Chen, Analog Devices
Co-Chair: Tian-Wei Huang, National Taiwan University

RMO2C-1 10:10 AM
A mm-Wave Arbitrary 2**N Band Oscillator Based on Even-Odd Mode Technique

A. H.T. Yu, S.-W. Tam, D. Murphy, T. Itoh, F. Chang, University of California at Los Angeles

Abstract: A technique to build mm-wave arbitrary 2^N band oscillators is presented based on even-odd mode. It breaks the fundamental tradeoff between frequency switching range and tank Q. As a result, it achieves FOMs comparable to single band oscillators. A quadruple band oscillator with 4 arbitrary chosen frequencies, 43, 49, 58 and 75GHz, is implemented in 65nm CMOS to verify the theory. The phase noises at 1 MHz offset are -100.3, -95.3, -93.8 and -86.2 dBc/Hz. The oscillator core consumes 12 mW.

RMO2C-2 10:30 AM
A 24GHz and 60GHz Dual-Band Standing-Wave VCO in 0.13μm CMOS

L. Wu*, A. W. L. Ng*, L. L. K. Leung** and H. C. Luong*, *Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong, **Qualcomm, San Diego, USA

Abstract: By exploiting the intrinsic multiple oscillation modes of a standing-wave oscillator, a dual-band millimeter-wave VCO is designed. Implemented in 0.13μm CMOS with an area of 0.05mm^2, the VCO prototype measures a dual-band operation at 24GHz and 60GHz with tuning range of 10.8% and 7.2%, phase noise of -120dBc/Hz and -114dBc/Hz at 10MHz offset, power consumption of 11mW and 24mW, corresponding to FoM of -178dB and -176dB, respectively.

RMO2C-3 10:50 AM

Multi-band Local Oscillator Generation for Direct up/down Conversion Transceiver Architectures Supporting WiFi and WiMax Standards

Ram Sadhwani, Assaf Ben Bassat, Adil A. Kidwai, Shahar Rivel*, Jonathan C. Jensen, Intel Corporation, Hillsboro, OR; *Intel Corporation, Petah Tikva, Israel

Abstract: A highly linear LO generation architecture for direct up/down conversion transceiver is designed in standard 45nm 1.15V digital CMOS process. The spectral purity is better than 50dBc for WiFi and 45dBc for WiMax. The frequency plan is targeted to overcome the VCO pulling due to on-chip transmit power amplifiers. This architecture generates LO frequencies for WiFi 802.11b/g and WiMax 802.16e bands covering 2.3-2.7GHz, 3.3-3.8GHz and 4.8-5.8GHz from narrow input VCO range of 8-9.6GHz.

RMO2C-4 11:10 AM

A 0.13-μm CMOS Local Oscillator for 60GHz Applications Based on Push-Push Characteristic of Capacitive Degeneration

Tino Copani, Hyungseok Kim, Bertan Bakkaloglu, Sayfe Kiaei, Electrical, Energy and Computer Engineering, Arizona State University, Tempe, AZ, 85287, USA

Abstract: A 60GHz 10mW CMOS VCO is implemented together with a high-speed prescaler in a 130nm CMOS process. Compared to other push-push topologies, capacitive degeneration technique does not impact the resonator and switching transistors are re-used as buffers minimizing noise due to following amplifiers. The measured phase noise at 1MHz offset is 89dBc/Hz and FoM is 174dBc/Hz.

RMO2C-5 11:30 AM

A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS

M. Nariman, F. De Flaviis, University of California at Irvine, Broadcom Corporation, USA

Abstract: A 34-40GHz VCO fabricated in 65 nm digital CMOS is demonstrated in this paper. The VCO uses a combination of switched capacitors and varactors for tuning and has a maximum Kvco of 240 MHz/V. The VCO achieves a phase noise of better than -98 dBc/Hz at 1 MHz offset across the band while consuming 12 mA from a 1.2 V supply. The results correspond to an FOMT of -182 dBc/Hz. A cascode buffer following the VCO consumes 11 mA and delivers +3 dBm to a 100 Ω differential load.

Monday May 24, 2010
10:10 AM
ACC - Room 212AB
Session: RMO2D: Reconfigurable PA Concepts
Chair: Joseph Staudinger, Freescale
Co-Chair: Jyoti P. Mondal, Northrop Grumman

RMO2D-1 10:10 AM
Multi-Mode WCDMA Power Amplifier Module with Improved Low-Power Efficiency using Stage-Bypass

G. Hau, M. Singh, ANADIGICS, Inc., USA.

Abstract: A multi-mode WCDMA PAM with very low DC bias current and current consumption under large power backoff is presented. A dual-path PA is designed for high/medium power-mode operations, while a stage-bypass is applied to the final stage of the medium-power PA for low-power-mode operation. The PAM achieves a bias current of 3.5mA. At 17dBm and 8dBm backoff Pout, the PAM achieves 22% and 15% PAE, respectively. The current consumption at 8dBm Pout is reduced by 59% with the stage-bypass configuration.

RMO2D-2 10:30 AM
A 3.4GHz to 4.3GHz Frequency-Reconfigurable Class E Power Amplifier with an Integrated CMOS-MEMS LC Balun

L. Wang, T. Mukherjee, Department of ECE, Carnegie Mellon University, Pittsburgh, PA, 15213

Abstract: A monolithically integrated differential class E power amplifier capable of dynamically switching between 3.4GHz and 4.3GHz operation has been designed and fabricated in a 0.35 μm BiCMOS process; this power amplifier also includes an integrated CMOS-MEMS variable capacitor enabled LC balun for differential to single-ended conversion. The power amplifier achieves a maximum output power of 19.1 dBm and a maximum power added efficiency of 15.1% with a supply voltage of 3.3 V.

RMO2D-3 10:50 AM
A Q-band 6W MMIC Power Amplifier with 3-way Power Combination Circuit

Hiroshi Otsuka, Kazuhisa Yamauchi, Koji Yamanaka, Shin Chaki, Kazuhiko Nakahara, Kunihiro Endo, Akira Inoue and Yoshihito Hirano, Mitsubishi Electric Corp., Japan

Abstract: A Q-band 6W MMIC power amplifier was developed, which employed 3-way power combination circuit to combine 12 FET cells for high output power. In addition, the pi type bias and matching circuit was applied to the inter-stage matching circuit to suppress loop oscillation. -37.9dBm-6.2W- saturated output power was successfully achieved, which is the highest output power for Q-band power amplifiers reported to date.

RMO2D-4 11:10 AM
A Multi-Band Reconfigurable Power Amplifier for UMTS Handset Applications

U. Kim, K. Kim, J. Kim*, and Y. Kwon, Seoul National University, *Hanyang University, Korea

Abstract: A new practical reconfigurable structure for a multi-band power amplifier (PA) is proposed for UMTS handset applications. The proposed reconfigurable output matching network can reconfigure the output power as well as the frequency. To demonstrate the performance of the proposed structure, a 5 mm x 5 mm prototype reconfigurable PA module is developed for UMTS high-frequency band application. The fabricated PA module can cover any two bands out of three popular high-frequency UMTS bands.

RMO2D-5 11:30 AM
High-efficiency Reconfigurable RF Transmitter for Wireless Sensor Network Applications

F. Carrara and G. Palmisano, University of Catania - DIEES, Italy

Abstract: In this paper, a 90-nm CMOS 1.2-V RF transmitter for WSNs is presented. A wideband topology guarantees continuous frequency coverage from 300 to 960MHz. At 300MHz (960MHz), the TX delivers a 10.2-dBm (10.3-dBm) output power with 63% (46%) efficiency. Dynamic current biasing is exploited for improved efficiency in back-off, thus achieving > 80% power saving. Linear operation is also demonstrated since the TX exhibits a 8.5-dBm output power, 37% efficiency, and -30-dBc ACPR with a $\pi/4$-DQPSK input.

Monday May 24, 2010
01:20 PM
ACC - Room 208AB
Session: RM03A: CMOS Wideband Transceiver ICs
Chair: Domine Leenaerts, NXP Semiconductor
Co-Chair: Haolu Xie, Fujitsu Microelectronics

RM03A-1 01:20 PM
A Tri-band 65nm CMOS Tuner for ATSC Mobile DTV SoC

Sanghoon Kang, Huijung Kim, Jeong-Hyun Choi, Jae-Hong Chang, Jong-Dae Bae, Wooseung Choo, Byeong-ha Park, Samsung Electronics System LSI MSC team, Korea

Abstract: ATSC mobile receiver SoC is developed for mobile and handheld devices. It supports VHF-I, VHF-III, and UHF bands. The tuner achieves a 2.5/3.0/4.0dB NF at VHF-I, VHF-III and UHF band respectively, while consuming less than 100mW. By using narrowband LNA architecture with input and load tuning ability, it can meet linearity requirement for ATSC mobile with small power consumption. It also automatically calibrates baseband low-pass filter cut-off frequency and LNA LC load resonant frequency.

RM03A-2 01:40 PM
A Multi-standard Multi-band Tuner for Mobile TV SoC with GSM Interoperability

H. Kim, S. Kang, J. Chang, J. Choi, H. Chung, J. Heo, J. Bae, W. Choo, and B. Park, Samsung Electronics Co. LTD.

Abstract: A multi-standard multi-band tuner for mobile TV SoC satisfying the GSM850 & GSM900 Interoperability (IOP) is presented. The single-chip SoC satisfies all requirements of DVB-H/T, ISDB-T, and DAB application with margin. Moreover, this SoC meets not only the GSM900 IOP which is described in MBRAI 2.0, but also GSM850 IOP, in DVB-T/H mode.

RM03A-3 02:00 PM
A 2.2 mW Regenerative FM-UWB Receiver in 65 nm CMOS

N. Saputra, J. R. Long, and J. J. Pekarik, Delft University of Technology, the Netherlands, *IBM Microelectronics, USA

Abstract: A 4-4.5GHz receiver front-end consisting of a 35 dB voltage gain regenerative amplifier, ultra-narrowband RF filter and an envelope detector demodulator for FM-UWB communication is described in this paper. Implemented in 65 nm CMOS, the measured receiver sensitivity is 83 dBm at 100 kbps data rate with 15 dB output SNR (10-6 BER). The 0.3 mm^2 test chip includes a 50 Ohm buffer amplifier to facilitate testing and consumes 2.2 mW (excluding buffer) from a 1 V supply.

RM03A-4 02:20 PM
A 75 pJ/bit All-Digital Quadrature Coherent IR-UWB Transceiver in 0.18μm CMOS

D. Gómez, D. Mateo, J. L. González, Universitat Politècnica Catalunya, SPAIN

Abstract: In this paper a 75 pJ/b all-digital quadrature coherent impulse radio ultra-wideband transceiver in 0.18μm CMOS is presented. It consumes 42 mW operating at a 560 Mbps datarate. The receiver and transmitter share most of the components reducing the area. This design is optimal for low-power low-cost short-range high-speed communications.

RM03A-5 02:40 PM
A 90nm-CMOS, 500Mbps, Fully-Integrated IR-UWB Transceiver Using Pulse Injection-Locking for Receiver Phase Synchronization

C. H. Hu, P. Y. Chiang, K. M.Hu, R. Khanna*, J. Nejedlo*, Oregon State University, *Intel

Abstract: A fully-integrated, 3.1-5GHz Impulse-Radio UWB transceiver with on-chip flash ADC is designed in 90nm-CMOS. A new scheme for receiver phase acquisition is proposed that uses pulse injection-locking to synchronize the receive clock with the transmitted data, eliminating the need for clock/data recovery (CDR). Occupying 2mm^2 die area, the transceiver achieves a maximum data rate of 500 Mbps, energy efficiency of 0.18nJ/b at 500Mbps, and a RX-BER of 10-3 across a distance of 10cm at 125Mbps.

Monday May 24, 2010
01:20 PM
ACC - Room 209AB
Session: RMO3B: Advanced Characterization of mm-Wave Components
Chair: Kevin McCarthy, University College Cork
Co-Chair: Herbert Zirath, Chalmers University of Technology

RMO3B-1 01:20 PM
The "Load-Thru" (LT) De-embedding Technique for the Measurements of mm-Wave Balanced 4-Port Devices

Z. Deng, A. M. Niknejad, Berkeley Wireless Research Center

Abstract: The differential behavior of a balanced 4-port device can be characterized by simple 2-port measurements if baluns are placed at the input and the output. But the traditional insertion loss technique is not able to fully de-embed the baluns. Therefore, we propose the ''load-thru'' de-embedding technique which uses the differential-mode characteristics of a balun to fully extract the complete differential behavior of the DUT. Theoretical analysis and mm-wave measurement verifications are provided.

RMO3B-2 01:40 PM
RF-pad, Transmission Lines and Balun Optimization for 60GHz 65nm CMOS Power Amplifier

S. Aloui, E. Kerherve, R. Plana*, D. Belot**, Universite de Bordeaux 1, IMS Laboratory, 351 Cours de la Liberation, Talence, France., *LAAS-CNRS, 7 avenue du fonel Roche, Toulouse, France., **STMicroelectronics, Central R&D -Crolles, France.

Abstract: Design and optimization of 65nm CMOS passive devices which are used in the implementation of a 60GHz Power Amplifier (PA) are presented. A new optimized Radio Frequency (RF)-pad is used to minimize the losses of the PA access. The PA is matched via balun and Transmission Lines. S-parameters and large signal measurement results demonstrate a maximum output power of 7.3dBm with a gain of 8.5dB while consuming 96mA. The active die area of the chip is 0.065mm^2.

RMO3B-3 02:00 PM

200GHz f_t SiGe HBT Load Pull Characterization at mm-Wave Frequencies

Luciano Boglione, Richard T. Webster*, University of Massachusetts, Lowell, *Air Force Research Laboratories, Hanscom AFB, MA

Abstract: The load pull measurement of a commercially available SiGe HBT device has been performed at Q band over frequency and bias. Measured results for the SiGe process under test at mm-wave frequency have never been made available to the general public before and no comparable information on similar SiGe devices is available in the public domain. The goal of this paper is to fill this gap: load pull results along with a discussion of the characterization setup and procedure are presented.

RMO3B-4 02:20 PM

A Miniature 26-/77GHz Dual-band Branch-line Coupler Using Standard 0.18-μm CMOS Technology

Y. S. Lin*, C. Y. Hsu*, H. R. Chuang*, C. Y. Chen**, *National Cheng Kung University, Tainan, Taiwan, R.O.C, **National University of Tainan, Tainan, Taiwan, R.O.C.

Abstract: A 26-/77GHz dual-band branch-line coupler fabricated using standard 0.18-μm CMOS technology is presented. The dual-band coupler is with a compact size of 1.0 x 1.0 mm^2. The simulated frequency response is to 110GHz. The measured frequency response shows a good performance with amplitude and phase imbalance of ± 0.5 dB and ± 5°, respectively, in the low band. The S21 in the high band is about 7.5 dB The measured isolation and the return loss are better than 15 dB within the two passbands.

RMO3B-5 02:40 PM

Compact Transformer Power Combiners for Millimeter-wave Wireless Applications

Y. Zhao, J. R. Long, M. Spirito, ERL/DIMES, Delft University of Technology, The Netherlands

Abstract: Two current-summing transformer combiners for 60GHz-band power amplification in millimeter-wave wireless applications are characterized. The parasitic-compensated balun and fully-differential combiners mitigate imbalances caused by interwinding capacitance, while self-shielded output windings inhibit substrate coupling. Power loss for both prototypes is <1.0dB at 60GHz with <0.015mm^2 chip area. Reflected impedance uniformity between ports is better than 4.5% in the 60GHz band.

Monday May 24, 2010
01:20 PM
ACC - Room 211AB
Session: RM03C: Advanced Device Technologies & Design Techniques
Chair: Aditya Gupta, Northrup Grumman
Co-Chair: Eli Reese, TriQuint Semiconductor

RM03C-1 01:20 PM
Integration of Multi-standard Front End Modules SOCs on High Resistivity SOI RF CMOS Technology

F. Gianesello*, S. Boret*, B. Martineau*, C. Durand*, R. Pilard*, D. Gloria*, B. Rauber* and C. Raynaud**, *STMicroelectronics, TR&D, STD, Crolles, France, ** CEA Leti, Grenoble, France

Abstract: RF front end modules (FEMs) are currently realized using a variety of technologies. However, since integration drives wireless business in order to achieve the appropriate cost and form factor, we see significant research concerning FEM integration on silicon. In this quest, SOI technology has emerged as a promising one. In this paper, we will focus our investigation on high performance passive functions in order to demonstrate the capability of SOI CMOS technology to integrate the whole FEM.

RM03C-2 01:40 PM
Low-Parasitic Ultra-Low-Triggering ULTdSCR ESD Protection for RF ICs in CMOS

Jian Liu, Lin Lin, Xin Wang, Hui Zhao, He Tang, Qiang Fang, Albert Wang, Hongyi Chen, Haolu Xie, Siqiang Fan and Gary Zhang, Dept. of Electrical Engineering, University of California, Riverside, CA

Abstract: This paper reports design of a novel low-parasitic ultra-low-triggering voltage dual-directional ULTdSCR ESD protection structure in foundry CMOS. It features programmable low triggering voltage of 4.7~6V, low discharging resistance of ~0.77Ω, low leakage of ~0.1nA, extremely low parasitic capacitance of ~10fF and ultra fast response of ~100ps. it achieves ESD protection of >7.8kV HBM and ~500 CDM for a 90μm device. Measurement matches simulation very well. This low-parasitic lowtriggering ESD protection structure is suitable for high data rate and low-voltage RF ICs in CMOS.

RM03C-3 02:00 PM
A Cost-Competitive High Performance Junction-FET (JFET) in CMOS Process for RF Front-End-Module Applications

Y. Shi, R. M. Rassel, R. A. Phelps, P. Candra, D. B. Hershberger, X. Tian, S. L. Sweeney, J. Rascoe, B. Rainey, J. Dunn, and D. Harame, IBM Microelectronics, Essex Junction, Vermont, USA

Abstract: In this paper, we present a cost-effective JFET integrated in 0.18μm RFCMOS process. The design is highly compatible with standard CMOS process, therefore can be easily scaled and implemented in advanced technology nodes. The design impact on Ron and Voff is further discussed, providing the insights and guidelines for JFET optimization. Besides the superior flicker noise (1/f noise) characteristics, this JFET device also demonstrates promising RF characteristics such as maximum frequency, linearity, power handling capability, power-added efficiency, indicating a good candidate for RF front-end module designs.

RMO3C-4 02:20 PM

Reconfiguration of Bulk Acoustic Wave Filters Using CMOS Transistors: Concept, Design and Implementation

M. El Hassan, E. Kerherve*, Y. Deval*, J.B. David**, D. Belot***, University of Balamand - Al koura Lebanon,*IMS Laboratory - UMR 5218 CNRS - ENSEIRB - University of Bordeaux, **CEA-Leti - Minatec - Grenoble, ***STMicroelectronics Crolles.

Abstract: This paper presents the feasibility of a new method to reconfigure the BAW filters by adding capacitors to the shunt resonators and by controlling these capacitors using CMOS transistors. The filter is realized in a ladder topology. It is used for the 802.11b/g standard. The filter presents a measured -3.3 dB of insertion loss, -12.7 dB of return loss and selectivity higher than 33 dB @ 30 MHz of the bandwidth. Moreover, a measured shift of +0.5% of the center frequency is obtained.

RMO3C-5 02:40 PM

A Layout Efficient, Vertically Stacked, Resonator-Coupled Bandpass Filter in LTCC for 60GHz SOP Transceivers

R. E. Amaya, Communications Research Centre

Abstract: This paper describes the design and implementation of a layout efficient bandpass filter implemented in Low-Temperature Co-fired Ceramic (LTCC) substrates. Applications for this filter include band select filters for 60GHz System-On-Package transceivers. Two bandpass filters based on a quasi-elliptic configuration were implemented here using four half-wavelength resonators. The first filter uses all planar resonators to achieved a measured insertion loss of 3.7 dB and a return loss > 10 dB.

RMO3C-6 03:00 PM

Co-Design Considerations for Frequency Drift Compensation in BAW-based Time Reference Application

S. Razafimandimby, D. Petit, P. Bar, S. Joblot, J.-F. Carpentier, J. Morelle, C. Arnaud, G. Parat*, P. Garcia, C. Garnier, STMicroelectronics, Crolles, France, *CEA-LETI/MINATEC, Grenoble, France.

Abstract: New BAW/Integrated Circuits co-integration considerations are presented. For the demonstration, a 2.5GHz reference frequency oscillator has been implemented in a 130nm BiCMOS technology. A 5 bit switched capacitor bank permits to correct process deviation s with a 12.5kHz accuracy while a varactor allows compensating a BAW resonator with a -4.2ppm/°C TCF in a [-40°C,85°C] temperature range. The oscillator achieves a phase noise of -93dBc/Hz at a 2kHz carrier offset for a 7.3mW power consumption.

Monday May 24, 2010
01:20 PM
ACC - Room 212AB
Session: RMO3D: Switch & Switch-mode Technologies
Chair: Nick Cheng, Skyworks Solutions
Co-Chair: Youngwoo Kwon, Seoul National University

RMO3D-1 01:20 PM
High Efficiency and Wideband Envelope Tracking Power Amplifier with Sweet Spot Tracking

D. Kim, J. Choi, D. Kang, B. Kim, Pohang University of Science and Technology, Korea

Abstract: This paper describes the implementation of a high efficiency and wideband envelope tracking power amplifier with sweet spot tracking. By modulating supply voltage of PA, efficiency can be increased significantly. And linearity is improved by envelope shaping and sweet spot tracking. The hybrid switching supply modulator is used to achieve high efficiency as well as wide bandwidth. The measurement results show efficiencies of 36.4/34.1 % for 10/20 MHz LTE signals with PAPR of 7.5/7.42 dB.

RMO3D-2 01:40 PM
A 150MHz, 84\% efficiency, Two Phase Interleaved DC-DC Converter in AlGaAs/GaAs P-HEMT Technology for Integrated Power Amplifier

M. H. Peng, V. Pala, T. P. Chow, and M. Hella, Rensselaer Polytechnic Institute, ECSE Department

Abstract: This paper presents a high efficiency, high switching speed interleaved DC-DC buck converter with negative coupled inductor in AlGaAs/GaAs technology, targeting integrated power amplifier modules. The flip chip DC-DC converter is implemented in 0.5μm GaAs pHEMT process and occupies 4.22mm^2 without the output network. The interleaved DC-DC converter achieves 84% efficiency when operating at 150MHz switching frequency with 4.5V/3.3V and 1A load current.

RM03D-3 02:00 PM
A 0dBm 10Mbps 2.4GHz Ultra-Low Power ASK/OOK Transmitter with Digital Pulse-Shaping

Xiongchuan Huang, Pieter Harpe, Xiaoyan Wang, Guido Dolmans, Harmke de Groot, Holst Centre - IMEC, Eindhoven, The Netherlands

Abstract: The proposed 2.4GHz direct modulation transmitter radiates 1mW with 3.88mW power consumption, and it supports OOK and ASK modulation up to 10Mbps. The novel power amplifier structure enables digital pulse-shaping to improve spectrum efficiency of OOK transmission. When applied with OOK modulation with equal probability of 1's and 0's, it consumes 2.3mW with an energy efficiency of 0.23nJ/bit/mW. The transmitter is implemented in a 90nm CMOS technology and packaged in a QFN56 package.

RM03D-4 02:20 PM
A Linear-in-dB SiGe HBT Wideband High Dynamic Range RF Envelope Detector

Hsuan-yu Marcus Pan and Lawrence E. Larson, University of California, San Diego, 9500 Gilman Drive, La Jolla, CA, 92093, USA

Abstract: A linear-in-dB wideband, SiGe HBT high dynamic range RF envelope detector is presented. The detector operates from 200MHz to 2.5GHz with 50dB maximum dynamic range.

RM03D-5 02:40 PM
Cellular Antenna Switches for Multimode Applications Based on a Silicon-on-Insulator Technology

A. Tombak, C. Iversen*, J.-B. Pierres**, D. Kerr, M. Carroll, P. Mason, E. Spears and T. Gillenwater, RFMD Inc., USA, * RFMD Denmark Design Center, DENMARK, ** RFMD Toulouse Design Center, FRANCE

Abstract: A Silicon-on-Insulator (SOI) CMOS technology on high resistivity silicon substrates is presented for the design of cellular antenna switches. The design and measurement results for an SP9T cellular antenna switch based on this technology are presented. The measured insertion/return loss, isolation, and harmonic distortion performance were better than most cellular antenna switch specifications.

Monday May 24, 2010
03:30 PM
ACC - Room 208AB
Session: RMO4A: Ultra Low Power Receivers and Transmitters
Chair: Julian Tham, Arda Technologies
Co-Chair: Bill Redman-White, NXP

RMO4A-1 03:30 PM
A 120μW Fully-Integrated BPSK Receiver in 90nm CMOS

H. Yan, J. G. Macias-Montero, A. Akhnoukh, L. C. N. de Vreede, J. R. Long, J. J. Pekarik*, J. N. Burghartz, ERL/DIMES, Delft University of Technology, Netherlands, *IBM Microelectronics, Essex Junction, VT, USA

Abstract: In this work a highly integrated, ultra-low-power BPSK receiver for short-range wireless communications is presented. Its demodulation principle is based on the dynamic phase response of the two BPSK signal injected oscillators. As proof of concept a 300MHz receiver was implemented in a 90nm CMOS technology. The whole receiver has an active die area of 0.04mm^2, a sensitivity of -34dBm at 10Mbps and consumes only -120μW from 1V supply, which relates to an energy per bit of only 0.12nJ.

RMO4A-2 03:50 PM
A Fully Integrated 2.4GHz CMOS Diversity Receiver with a Novel Antenna Selection

Yong-IL Kwon*, Sang-Ku Park*, T.J.Park*, and Hai-Young Lee**, *UC solution team, SAMSUNG Electro-Mechanics, Suwon, 443-743, Korea, **Department of Electronics Engineering, Ajou University, Suwon, 443-749, Korea

Abstract: A new, low-complexity antenna diversity architecture, using a 2.4GHz single low-IF receiver chain with a novel antenna selection scheme, is exploited by using 0.18-μm CMOS technology. The receiver has been developed for the IEEE standard 802.15.4 radio system and two RF input channels are selected through an efficient analog-type antenna selection scheme, for achieving diversity. Compared to conventional receivers,a 10~15 dB improvement of the RSS and total power consumption is less than 8.5mW.

RM04A-3 04:10 PM
A 90μW MICS/ISM Band Transmitter with 22% Global Efficiency

J. Pandey, B. Otis, University of Washington, Seattle, WA, USA

Abstract: We propose a highly integrated 90μW 400MHz MICS band transmitter with an output power of 20μW leading to a 22% global efficiency - the highest reported to date for such systems. We introduce a new transmitter architecture based on cascaded multi-phase injection locking and frequency multiplication to enable low power operation. The proposed transmitter has a settling time <250ns. At a data-rate of 200 kbps, the Tx achieves an energy efficiency of 450pJ/bit. Our 400MHz LO has a FoM of 204dB.

RM04A-4 04:30 PM
A 2mW CMOS MICS-Band BFSK Transceiver with Reconfigurable Antenna Interface

S. Min, S. Shashidharan, M. Stevens, T. Copani, S. Kiaei, B. Bakkaloglu, S. Chakraborty*, Arizona State University,*Texas Instruments, USA

Abstract: A 0.18μm CMOS MICS-band transceiver with a reconfigurable RF front-end is presented, reusing the same circuit core for super-regenerative wake-up receiver, receive-mode LNA, and transmit power amplifier. The system uses an All Digital Frequency Locked-Loop (ADFLL) for LO signal generation. The OOK wake-up receiver sensitivity is -80dBm @ 50kbps, while the BFSK receiver's sensitivity is -97dBm for a 75kbps signal and 2mW power consumption. The nominal output power of the transmitter is -5dBm.

RM04A-5 04:50 PM
A 1.8 to 2.4GHz 20mW Digital-Intensive RF Sampling Receiver with a Noise-Canceling Bandpass Low-Noise Amplifier in 90nm CMOS

Joonhee Lee, Jaewook Kim and Seong Hwan Cho, Department of Electrical Engineering, KAIST, Daejeon, Republic of Korea

Abstract: This paper presents a digital-intensive RF sampling receiver which consists of an LNA and an RF ADC for multi-band wireless communication. The proposed LNA employs a transformer to reduce the noise figure and enhance the linearity. In the ADC, a time-based architecture enables 1st order noise shaping without a feedback loop. A prototype chip implemented in 90 nm CMOS has an area of 0.3 mm^2 and achieves SNR of 50 dB for 1-MHz signal bandwidth at 2.4 carrier frequency, while consuming 20 mW.

Monday May 24, 2010
03:30 PM
ACC - Room 209AB
Session: RM04B: Optimized Design Techniques for RF Front-end Building Blocks
Chair: Osama Shana'a, Mediatek Corp.
Co-Chair: Ali Afsahi, Broadcom

RM04B-1 03:30 PM
A Differential 4-Path Highly Linear Widely Tunable On-Chip Band-Pass Filter

A. Ghaffari, E. A. M. Klumperink, B. Nauta, University of Twente, CTIT Institute, IC Design group, Enschede, The Netherlands

Abstract: A passive switched capacitor RF bandpass filter with clock controlled center frequency is realized in 65nm CMOS. An off-chip transformer which acts as a balun, improves filter-Q and realizes impedance matching. The differential architecture reduces clock-leakage and suppresses selectivity around even harmonics of the clock. The filter has a constant -3dB bandwidth of 35MHz and can be tuned from 100MHz up to 1GHz. IIP3 is better than 19dBm, P1dB=2dBm and NF<5.5dB at Pdiss=2mW to 16mW.

RM04B-2 03:50 PM
A CMOS Wide-Bandwidth High-Power Linear-in-dB Variable Attenuator Using Body Voltage Distribution Method

Yan-Yu Huang, Wangmyong Woo, Chang-Ho Lee, Joy Laskar, Georgia Electronic Design Center, Georgia Institute of Technology, Samsung Design Center, USA

Abstract: A wide bandwidth, highly linear variable attenuator designed in 0.18μm triple-well CMOS process is presented. This attenuator is based on three cascade π-networks with body voltage distribution scheme to minimize the effects of the input power levels. Measurements show it achieves minimum 1-dB gain compression of 7.5 dBm. The mid-band insertion loss is 1.6 dB and the max attenuation is 34.8 dB. It has a linear-in-dB controllability from 400 MHz to 3.7GHz with input return loss better than 9dB.

RM04B-3 04:10 PM

A 17GHz Transformer-neutralized Current Re-use LNA and Its Application to a Low-power RF Front-end

S. Kundu, J. Paramesh, Carnegie Mellon University, USA

Abstract: A 17GHz current re-use low noise amplifier (LNA) is designed in 0.13 μm CMOS for low power applications such as wireless sensor networks. The LNA also employs transformer based feedback to neutralize the gate-drain capacitance of a MOSFET. The LNA achieves 15.4 dB gain into a 50 Ω load along with 1.9GHz bandwidth. It features 4.5dB NF and -12 dBm IIP3 while consuming 7.8 mW of power. A 17GHz receiver frontend using a similar two-stage LNA and a mixer is also demonstrated.

RM04B-4 04:30 PM

A Self-Healing 2.4GHz LNA with On-Chip S11/S21 Measurement/ Calibration for In-Situ PVT Compensation

Karthik Jayaraman, Qadeer Khan, *Baoyong Chi, William Beattie, *Zhihua Wang, and Patrick Chiang, School Of Electrical Engineering and Computer Science, Oregon State University, Corvallis,OR,USA, *Institute of Microelectronics, Tsinghua University, China

Abstract: This paper presents a 2.4GHz, reconfigurable RF LNA using on-chip peak detection and calibration to measure and optimize its input impedance (S11) and gain (S21) in-situ, compensating for the unpredictable effects of process, voltage and temperature (PVT) variations. Measurement results show that the calibration of the LNA across PVT corners improves the S11 by 5.1dB, S21 by 3dB, while not significantly degrading the Noise Figure (0.22dB degradation) and linearity (1.7dBm degradation).

RM04B-5 04:50 PM

A Low Power LNA using Miniature 3D Inductor without Area Penalty of Passive Components

Akira Tanabe, Ken'ichiro Hijioka, Hirokazu Nagase, Yoshihiro Hayashi, NEC Electronics Corporation

Abstract: A low power 5GHz LNA without area penalty of inductors has been fabricated. The chip area of this LNA is as small as LNAs without passive components because of miniature 3D vertical solenoid inductors. A noise and a power are smaller than those LNAs. Because of a small parasitic capacitance of the 3D inductor and a controlled series resistance considering skin effect, a 15.7dB power gain and a 2.0dB noise factor at 5GHz has been achieved with only 3.6mW power consumption.

Monday May 24, 2010
03:30 PM
ACC - Room 211AB
Session: RM04C: Temperature Compensated Oscillators
Chair: Timothy Hancock, MIT Lincoln Laboratory
Co-Chair: Donald Y. C. Lie, Texas Tech. University

RM04C-1 03:30 PM
A 65nm CMOS DCXO System for Generating 38.4MHz and a Real Time Clock from a Single Crystal in 0.09mm^2

D. L. Griffith, F. Dulger, G. S. Feygin, A. N. Mohieldin, P. Vallur, Texas Instruments

Abstract: An integrated digitally-controlled crystal oscillator (DCXO) is presented that generates both 38.4MHz and a 32.768kHz real time clock (RTC) from a single 38.4MHz crystal. The DCXO can startup independently and transition seamlessly in and out of software control. The tuning range is 280ppm with 2ppb/step and guaranteed monotonicity. The phase noise is -135dBc/Hz at 1kHz offset. The DCXO is implemented in standard 65nm digital CMOS with a die area of 0.09mm^2.

RM04C-2 03:50 PM
A 50ppm 600MHz Frequency Reference Utilizing the Series Resonance of an FBAR

Julie Hu, Lori Callaghan*, Richard Ruby*, Brian Otis, University of Washington, *Avago Technologies, Inc.

Abstract: A 600MHz FBAR-based differential oscillator in a 0.13μm CMOS process is presented. It employs a cross-coupled pair with an FBAR providing high Q source degeneration to realize oscillation at the series resonance. The measured phase noise is -126 and -150dBc/Hz at 10kHz and 1MHz frequency offsets; the RMS jitter from 10kHz to 20MHz is 50fs. The oscillator achieves a frequency stability of 50ppm over temperature change from 25 to 110 oC. The figure-of-merit (FOM) of the oscillator is 214dB.

RM04C-3 04:10 PM

An Electronically Temperature-Compensated 427MHz Low Phase-Noise AlN-on-Si Micromechanical Reference Oscillator

H. M. Lavasani, W. Pan, F. Ayazi, Georiga Institute of Technology

Abstract: This paper reports on the first demonstration of series tuning for lateral micromechanical oscillators and its application in a temperature-compensated 427MHz AlN-on-Si reference oscillator. The sustaining amplifier is a 0.18μm tunable TIA that uses shunt-parasitic cancellation to increase the tuning by 12x to 810ppm. A 2mW on-chip temperature compensation circuit lowers the drift to 70ppm in -10ºC to 70ºC. The oscillator phase-noise reaches -82dBc/Hz at 1kHz offset with floor below -147dBc/Hz.

RM04C-4 04:30 PM

A Wide Tuning 1.3GHz LC VCO with Fast Settling Noise Filtering Voltage Regulator in 0.18 μm CMOS Process

Hiroshi Akima, Aleksander Dec, and Ken Suyama, Epoch Microelectronics, Inc., Tarrytown, NY, USA

Abstract: A wide tuning LC voltage controlled oscillator (VCO) with integrated voltage regulator is presented. The integrated voltage regulator utilizes on-chip low-corner frequency noise filters to minimize the impact of regulator noise on VCO phase noise. One shot circuit is used with low-corner frequency noise filter to ensure fast settling. With the noise filter, 9dB improvement in phase noise is demonstrated in measurement.

RM04C-5 04:50 PM

A Wide-Range VCO with Optimum Temperature Adaptive Tuning

Behzad Saeidi*, Joshua Cho**, *Marvell Semiconductor, Aliso Viejo, CA 92656; **Skyworks Solutions, Inc., Irvine, CA 92617

Abstract: This paper presents an integrated wide-range VCO with a modified tuning scheme to deal with VCO temperature frequency drift. Here, during the coarse-tune operation, VCO tune voltage is a function of temperature which resembles the inverse function of VCO fine-tune characteristic. It optimizes the maximum tolerable VCO temperature frequency drift over which PLL remains locked. It also facilitates the design of a wide-range VCO with a small gain, making it less sensitive to PLL tune voltage noise.

Monday May 24, 2010
03:30 PM
ACC - Room 212AB
Session: RMO4D: Silicon Millimeter-Wave Amplifiers
Chair: Kevin Kobayashi, RF Micro Devices
Co-Chair: Paul Blount, Custom MMIC Design

RMO4D-1 03:30 PM
A 60GHz Transformer Coupled Amplifier in 65 nm Digital CMOS

Michael Boers, Broadcom Corp., Irvine, CA, 92617, USA

Abstract: A three stage transformer coupled amplifier for operation in the 57-64GHz band is presented. The amplifier uses differential capacitive neutralization and low loss transformers to achieve a gain of 30dB at 61GHz. The amplifier has an output compression point of 7.5dBm at 57GHz and a power added efficiency at 1dB compression of 9% at 57GHz. The amplifier has been fabricated in pure digital CMOS and the occupies an area of 0.055mm^2.

RMO4D-2 03:50 PM
A Stage-Scaled Distributed Power Amplifier Achieving 110GHz Bandwidth and 17.5dBm Peak Output Power

J. Chen, A. M. Niknejad, University of California at Berkeley

Abstract: This paper presents the design of a pseudo-differential distributed power amplifier in a 0.13μm SiGe BiCMOS process. Based on the newly proposed efficiency enhancing stage-scaling technique, the distributed power amplifier achieves a small-signal bandwidth of 110GHz, a peak saturated output power of 17.5dBm and a peak PAE of 13.2%. The measured 3dB output power bandwidth is greater than 77GHz. The amplifier consumes 119mA from a 3V supply.

RM04D-3 04:10 PM
DC Hot Carrier Stress Effect on CMOS 65nm 60GHz Power Amplifiers

T. Quémerais*, L. Moquillon**, V. Huard**, J.-M. Fournier*, P. Benech*, N. Corrao*,
*IMEP-LHAC, UMR INPG/UJF/US/CNRS, 3 parvis Louis Néel, BP 257, 38016 Grenoble Cedex, France, **STMicroelectronics, 850 rue Jean Monnet 38920 Crolles, France

Abstract: The effects of direct current (dc) hot carrier stress on the characteristics of a millimeter wave (mmw) power amplifiers (PA) in a 65nm CMOS technology are investigated. In this way, the power gain, the input and output matching, the output 1 dB compression point (OCP1dB) and the saturated power (Psat) have been measured after hot carrier stress. A decreasing of 5% of the power gain and 7% of the OCP1dB and the Psat are measured on a 4 stages PA at 58GHz after a stress of 50 hours with 1.7V.

RM04D-4 04:30 PM
A Layout-Based Optimal Neutralization Technique for mm-Wave Differential Amplifiers

Z. Deng, A. M. Niknejad, Berkeley Wireless Research Center

Abstract: A layout-based optimal neutralization technique is proposed for the designs of mm-wave differential amplifiers. Based on a new layout style which exploits routing signal capacitive coupling, the need for physical neutralization capacitors are obviated which results in compact and robust layout. Experimental prototype designs at 60GHz and 110GHz amplifiers demonstrate the utility of the idea by direct comparison with unneutralized designs.

RM04D-5 04:50 PM
A 100GHz Transformer-Coupled Fully Differential Amplifier in 90 nm CMOS

N. Deferm, P. Reynaert, K. U. Leuven, ESAT/MICAS, Heverlee, Belgium

Abstract: This paper proposes differential design techniques for W-band CMOS applications. Transformers are used as passive matching circuits, which provide numerous advantages compared to traditional matching circuits. Stabilization and gain improvement of the differential pair is achieved by a wideband neutralization technique. These techniques are combined in a fully differential amplifier which is successfully measured. To our knowledge, this is the first fully differential 100GHz CMOS amplifier.

Tuesday May 25, 2010
08:00 AM
ACC - Room 207AB
Session: RTU1B: CMOS Millimeter-Wave 60/24GHz Radio
Chair: Frank Henkel, IMST GmbH, Kamp-Lintfort
Co-Chair: Mark Ruberto, Intel Corp.

RTU1B-1 8:00 AM
A 68-82GHz integrated wideband linear receiver using 0.18 µm SiGe BiCMOS Technology

A. Y.-K. Chen*,**, Y. Baeyens* , Y.-K. Chen*, and J. Lin**, *Alcatel-Lucent/Bell Laboratories, 600 Mountain Ave. Murray Hill, NJ, 07974, USA, **Department of ECE, University of Florida, Gainesville, FL, 32611, USA

Abstract: This paper presents a highly integrated wideband linear receiver with a 3dB RF bandwidth from 68 to 82GHz. The receiver, fabricated in a low-cost 200/180GHz fT/fmax SiGe BiCMOS process, achieved a maximum gain of 28.1 dB, NF of 8 dB, and IP1dB of -23.6 dBm at 77GHz, dissipates 413 mW, and occupies 1.34 mm². To the best of authors' knowledge, this receiver reports the highest 3 dB RF bandwidth with excellent linearity performance among all the prior arts in SiGe HBT/BiCMOS technologies to date.

RTU1B-2 8:20 AM
A 24GHz Low-Power Fully Integrated Receiver with Image-Rejection using Rich-Transformer Direct-Stacked/Coupled Technique

N. Shiramizu, T. Nakamura, T. Masuda, K. Washio, Hitachi, Ltd.

Abstract: We have developed and fabricated a low-power, fully integrated receiver for 24GHz ISM band wireless communication using a Rich-Transformer Direct-Stacked/Coupled (RT-DSC) technique. This technique makes it possible to reduce supply voltage and current without any performance degradation. Receiver gain of 30 dB and noise figure (NF) of 5.6 dB are obtained at low power consumption of 21.5 mW. This resulted in our achieving power consumption only 30% of that reported previously.

RTU1B-3 8:40 AM
A 60GHz CMOS Receiver Front-End with Integrated 180-degree Out-of-Phase Wilkinson Power Divider

C. C. Chen, J. H. Lee, Y. S. Lin, National Chi Nan University, Taiwan

Abstract: A 60GHz receiver front-end (RFE) with an integrated 180-degree out-of-phase Wilkinson power divider using standard 0.13 um CMOS technology is reported. The RFE comprises a wideband LNA with 12.4-dB gain, a current-reused bleeding mixer, a baseband amplifier, and a 180-degree out-of-phase Wilkinson power divider. The RFE achieved maximum conversion gain of 18.7 dB at RF of 56GHz. The corresponding 3-dB bandwidth of RF is 9.8GHz. The measured minimum NF was 9 dB at 58GHz.

RTU1B-4 9:00 AM
Coherent Parametric RF Downconversion in CMOS
Z Zhao, JF Boudquet*, S. Magierowski**, University of Calgary, Canada

Abstract: Parametric circuits built in CMOS are promising for (sub)mm-wave applications given their potentially high gain and low power consumption.. This paper presents basic parametric downconverter structures, their theory of operation, and the benefits to be gained from CMOS implementation. A low-power, sub-1-V, fully integrated mixer in 130-nm CMOS is introduced.It implements two parametric modes and operates on RF signals between 22 and 24GHz with possible conversion gains in excess of 20 dB.

RTU1B-5 9:20 AM
60GHz Broadband Image Rejection Receiver using Varactor Tuning
J. Kim, W. Choi, Y. Park, and Y. Kwon, Seoul National University, Korea

Abstract: A pHEMT broadband image rejection receiver with an image rejection ratio (IRR) more than 20 dB from 54GHz to 66GHz is presented using varactor tuning topology. Tunable varactors connected in shunt between an RF coupler and mixers are used to control the phase and amplitude of two RF signals. It offers the IRR improvement of 3.1 ~ 21.4 dB in the cost of gain degradation below 1.1 dB from 54GHz to 66GHz except for 65GHz.

Tuesday May 25, 2010
08:00 AM
Room 211AB
Session: RTU1C: CMOS PAs
Chair: Eddie Spears, RFMD
Co-Chair: Freek van Straten, NXP Semiconductors

RTU1C-1 08:00 AM
A Discrete Resizing and Concurrent Power Combining Structure for Linear CMOS Power Amplifier

J. Kim*, H. Kim*, Y. Yoon*, K. H. An*, W. Kim*, C.-H. Lee**, K. T. Kornegay*, and J. Laskar*, Georgia Electronic Design Center, Georgia Institute of Technology, Atlanta, GA 30308, USA*, Samsung Design Center, Atlanta, GA 30308, USA**

Abstract: A new method of power combining for a parallel-combining-transformer (PCT)-based CMOS linear power amplifier (PA) is proposed. The power cell in parallel paths is divided into three sub-cells to implement device resizing for discrete power control. Concurrent power combining of sub-power-cells utilizes the maximum available transformer efficiency even at the low-power mode, boosting overall PA efficiency. The PA demonstrates 30.7/25/19-dBm Pout and 35.8/19.8/10.5-% PAE for HP/MP/LP modes.

RTU1C-2 08:20 AM
A Single-Chip 2.4GHz Double Cascode Power Amplifier under Multiple Supply Voltages in 65nm CMOS for WLAN Application

Mingyuan Li, Ali Afsahi, Arya Behzad, Broadcom Corporation, San Diego

Abstract: A 2.4GHz fully integrated power amplifier with an on-chip balun for embedded WLAN applications with direct battery connection (2.3-5.5V) is presented. With a switched programmable feedback bias network, the PA can deliver 23.5dBm to 28.4dBm CW saturated power and 18.2dBm to 23.2dBm OFDM linear power (-25dB EVM) with PAPD when the supply varies from 2.3V to 5.5V. The PA occupies 1.2mm^2 in 65nm CMOS.

RTU1C-3 08:40 AM

A 31-dBm, High Ruggedness Power Amplifier in 65-nm Standard CMOS with High-Efficiency Stacked-Cascode Stages

S. Leuschner*, S. Pinarello**,***, U. Hodel***, J.-E. Mueller***, H. Klar*, *Technical University of Berlin, **Friedrich-Alexander-Universitaet Erlangen-Nuernberg,
***Infineon Technologies AG

Abstract: A novel, high ruggedness power amplifier topology in a 65-nm CMOS technology is proposed. The proposed stacked cascode topology uses only standard devices available in a modern triple-well CMOS process to achieve breakdown voltages of Vbd>18V. The power amplifier stage delivers 28 dBm output power at a power-added efficiency (PAE) of 69.9% from a 3.6V supply. The saturation gain is 18 dB. A watt-level power amplifier for GSM lowband operation with 31-dBm output power and 61% PAE is presented.

RTU1C-4 09:00 AM

Analysis and Design of a Wideband High Efficiency CMOS Outphasing Amplifier

M. C. A. van Schie, M. P. van der Heijden*, M. Acar*, A. J. M. de Graauw*, L. C. N. de Vreede, Delft University of Technology, *NXP Semiconductors, The Netherlands

Abstract: The design of a novel transformer-based power combiner for an efficient outphasing PA is shown. The power combiner was implemented on PCB with two 65nm CMOS class-E PA's. Measured peak output power is larger than 30dBm over a 29% BW around 700MHz. The 10dB back-off efficiency is larger than 27.3% over the same BW. The drain efficiency at 650MHz is larger than 50% over 10dB back-off, which is, to our best knowledge, the highest back-off efficiency reported in a CMOS outphasing PA to date.

RTU1C-5 09:20 AM

A Highly Efficient 5.8GHz CMOS Transmitter IC with Robustness over PVT Variations

Eun-Hee Kim, Jeong-Ki Choi*, Seok-Oh Yun*, Jinho Ko*, Kwyro Lee, Korea Advanced Institute of Science and Technology, *PHYCHIPS Inc.

Abstract: A highly efficient polar transmitter, fabricated in 0.13 um CMOS process, is proposed for Korean DSRC/ETC applications. It adopts the new PA topology of current-mode PA, which uses current mirroring operation to deliver accurate output power over extreme PVT variations. A speed enhancement technique is added to PA. Moreover, for extending linear range of the PA, an adaptive LO technique is used. The measurement results clearly indicate the potential for high yield transmitter architecture.

Tuesday May 25, 2010
08:00 AM
Room 212AB
Session: RTU1D: Emerging Architectures in Digital Frequency Synthesis
Chair: Stefano Pellerano, Intel Corporation
Co-Chair: Sanjay Raman, Virgina Tech

RTU1D-1 08:00 AM
A 700uA, 405MHz Fractional-N All Digital Frequency-Locked Loop for MICS Band Applications

S. Shashidharan, W. Khalil*, S. Chakraborty**, S. Kiaei, T. Copani and B. Bakkaloglu, Arizona State University, Tempe, AZ, *Ohio State University, Columbus, OH, **Texas Instruments Inc., Dallas, TX, USA

Abstract: An all-digital frequency-locked loop (ADFLL) based frequency synthesizer with a built-in FSK modulator for medical implants communication systems (MICS) band applications is presented. The ADFLL uses a high resolution single-bit digital $\Sigma\Delta$ frequency discriminator in the feedback path and a $\Sigma\Delta$ phase accumulator in the reference path, achieving fractional resolution. The ADFLL uses a digital IIR-based loop filter followed by a digital-intensive $\Sigma\Delta$ current-steering DAC and a first-order-hold filter. The ADFLL achieves 9.5Hz frequency resolution, spanning the ISM 400MHz-410MHz band. The worst-case near-integer spur of -55dBc and a phase noise of -83dBc/Hz at 300kHz offset is measured. The ADFLL is fabricated on a 0.18um CMOS process, occupying 0.14mm2 die area, with a quiescent current consumption of 700uA.

RTU1D-2 08:20 AM
A 2-MHz Bandwidth Δ-Σ Fractional-N Synthesizer Based On a Fractional Frequency Divider with Digital Spur Suppression

P.-E. Su and S. Pamarti, Department of Electrical Engineering, University of California at Los Angeles, U.S.A.

Abstract: A 2-MHz Δ-Σ fractional-N synthesizer based on staggered switching fractional frequency divider is presented. The phase generator based fractional divider provides lower instantaneous phase error at PFD input and hence lowers the Δ-Σ quantization noise, so the PLL bandwidth is enlarged to 2-MHz, enabling 4-Mb/s GFSK modulation. To suppress fractional spurs due to phase errors in the phase generator, a digital spur suppression technique is adopted which effectively reduce the maximum spur by 6-dB.

RTU1D-3 08:40 AM
A 6fJ/step, 5.5ps Time-to-Digital Converter for a Digital PLL in 40nm Digital LP CMOS

J. Borremans, K. Vengattarmane*, J. Craninckx, IMEC, Leuven, Belgium, *KUL, Leuven, Belgium

Abstract: A compact (0.01mm^2) coarse-fine time-to-digital converter (TDC) in 40nm LP CMOS achieves 5.5ps resolution using parallel delay lines. A 6fJ/conversion step efficiency is achieved thanks to efficient residue calculation. A 0.8LSB single-shot precision and low DNL are reached thanks to simple calibration which is possible in fractional-N PLLs. Further, metastability avoidance and digital error correction is implemented. This 14-bit architecture operates at a 40MS/s reference clock.

RTU1D-4 09:00 AM
A 6GHz Direct Digital Synthesizer MMIC with Nonlinear DAC and Wave Correction ROM

D. Y. Wu, G. P. Chen, J. W. Chen, X. Y. Liu, L. X. Zhao, Z. Jin, Institute of Microelectronics of Chinese Academy of Sciences, China

Abstract: Proposes a new DDS architecture combined with Nonlinear DAC and Wave-Correction-ROM(WCR) which shows both high operating speed and accuracy. Based on it, a 6GHz 8-bit DDS MMIC is designed and fabricated in 60GHz GaAs HBT Technology. The measured SFDR is 33.96dBc with 2.367GHz output under a 6GHz clock. It has an average SFDR of 37.5dBc and the worst case SFDR of 31.4dBc within the whole Nyquist band under a 5GHz clock frequency. The whole chip occupies 2.4x2mm^2 of area consuming 3.27W of power.

RTU1D-5 09:20 AM
A 10GHz 8-bit Direct Digital Synthesizer Implemented in GaAs HBT Technology

G. P. Chen, D. Y. Wu, Z. Jin, X. Y. Liu, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China

Abstract: This paper presents a 10GHz 8-bit DDS MMIC implemented in 1um GaAs HBT technology. The DDS takes a Double-Edge-Trigger 8-stage pipeline accumulator with sine-weighted DAC based ROM-less architecture, that can maximize the utilization ratio of GaAs HBT's high-speed potential. With an output frequency up to 5GHz, the DDS can give an average SFDR of 23.24dBc through the first Nyquist range, and consumes 2.4W of DC power from a single -4.6V supply. The total area of the chip is 2.4x2.0mm^2.

Tuesday May 25, 2010
01:20 PM
Room 207AB
Session: RTU2A: WLAN Transceivers and Components
Chair: Albert Jerng, Ralink Technology
Co-Chair: Srenik Mehta, Atheros Communications

RTU2A-1 01:20 PM
Dual-Band CMOS Transceiver with Highly Integrated Front-End for 450Mb/s 802.11n systems

S. Gross, T. Maimon, F. Cossoy, M. Ruberto, G. Normatov, A. Rivkind, N. Telzhensky, R. Banin, O. Ashckenazi, A. Ben-Bassat, S. Zaguri, G. Hara, M. Zajac, N. Shahar, S. Shahaf, A. Fridman, O. Degani, Intel Corporation, Mobile Wireless Group, Haifa, Israel

Abstract: A 3-stream, 802.11n WLAN MIMO transceiver, with fully integrated PAs and LNAs in both 2.4GHz and 5GHz bands, and a T/R switch in the 2.4GHz band, was implemented in a standard 90nm CMOS technology. The transmitter achieves an EVM of -28dB at output power of 19dBm and 17dBm in the 2.4GHz and 5GHz bands, respectively. The transmitter power consumption per Mb of data, in 3-stream mode, is 3.7mW/Mb and 4.5mW/Mb in the 2.4GHz and 5GHz, respectively. Four times lower compared to SISO mode.

RTU2A-2 01:40 PM
A CMOS Transceiver with internal PA and Digital Pre-distortion For WLAN 802.11a/b/g/n Applications

Chia-Jun Chang, Po-Chih Wang, Chih-Yu Tsai, Chin-Lung Li, Chiao-Ling Chang, Han-Jung Shih, Meng-Hsun Tsai, Wen-Shan Wang, Ka-Un Chan, and Ying-Hsi Lin, Realtek Semiconductor Corp., Hsinchu, 300, Taiwan

Abstract: A 2.4/5GHz Fully-Integrated Transceiver is implemented in 65nm CMOS technology. To alleviate the cost of external front-end components, the G-mode RF transmit/receive (T/R) switch and a power-efficient linear CMOS PA are fully integrated on-chip. On the other hand, for better performance, only the A-mode PA is integrated on-chip while the external T/R switch is used. It shows 5dB and 5.5dB NF in the G-mode and A-mode receivers respectively. Also, the transmitter delivers an average power of 18dB

RTU2A-3 02:00 PM

Highly Linear SOI Single-Pole 4-Throw Switch with an Integrated Dual-band LNA and Bypass Attenuators

Chun-Wen Paul Huang, Lui (Ray) Lam, Mark Doherty, and William Vaillancourt, SiGe Semiconductor, Andover, MA 01810, USA

Abstract: A novel SOI SP4T T/R switch is presented, which consists of 2 Rx paths with an integrated dual-band LNA and bypass attenuators and 2 high linearity Tx paths. Tx paths feature 0.1 dB compression to 34 dBm input power and 0.5-0.8 dB loss at 1-6GHz with >25 dB isolation. Rx paths feature 16 dB gain with 2.3 dB NF for 2.4-2.5GHz and 14 dB gain with 2.4-2.6 dB NF for 4.9-5.9GHz. With a dual-band PA, a complex dual-band MIMO front-end module can be easily constructed in a 4 x 5 mm QFN package.

RTU2A-4 02:20 PM

A 6.1GS/s 52.8mW 43dB DR 80MHz Bandwidth 2.4GHz RF Bandpass ΣΔ ADC in 40nm CMOS

J. Ryckaert, A. Geis*, L. Bos*, G. Van der Plas, J. Craninckx, IMEC, *also at VUB

Abstract: A 2.4GHz 4th order BP ΣΔ ADC is presented. The feedforward topology uses Gm-LC resonators that can be calibrated in frequency. The quantizer is split in 6 interleaved comparators to relax speed. Clocked at 6.1GHz, it achieves a DR of 43dB in 80MHz consuming 52.8mW. Implemented in 40nm CMOS, it achieves a FoM of 3.6pJ/conv. step, which is to date the lowest published value for RF BP ADCs.

RTU2A-5 02:40 PM

Single-chip WiFi bgn 1x2 SoC with Fully integrated Front end & PMU in 90nm digital CMOS technology

J.C. Jensen, R. Sadhwani, A.A. Kidwai, B. Jann, A. Oster*, M.Sharkansky* I .Ben-Bassat*, O. Degani*, S.Porat*, A. Fridman*, H. Shang, C. Chu, A. Ly, M. Smith, Intel Corporation, Hillsboro OR, *Intel Corporation, Haifa, Israel

Abstract: We report a compact 802.11b/g/n MIMO SoC with fully integrated transceiver, on-chip PMU including dc-dc converters, PHY, MAC, PCIe and a non-volatile memory. The transceiver includes on-chip PA, LNA and T/R switch. Fabricated in 90nm standard digital CMOS technology, this IC consumes 663/878mW (Rx/Tx 54Mbps) with an area of approx 33mm^2. A peak saturated power of 24dBm is achieved at antenna.

Tuesday May 25, 2010
01:20 PM
Room 211AB
Session: RTU2C: Millimeter-Wave Arrays
Chair: Brian Floyd, North Carolina State University
Co-Chair: C. Patrick Yue, UC Santa Barbara

RTU2C-1 01:20 PM
A 44GHz 8-Element Phased-Array SiGe HBT Transmitter RFIC with an Injection-locked Quadrature Frequency Multiplier

Sunghwan Kim*, Prasad S. Gudem**, and Lawrence E. Larson*, *Center for Wireless Communication, University of California, San Diego, CA, USA, **Qualcomm Inc., San Diego, CA, USA

Abstract: An 8-element 44GHz phased-array direct up-conversion transmitter, based on a localized injection-locked quadrature oscillator, is fabricated in a SiGe HBT process. The transmitter includes an improved injection-locked quadrature frequency doubler, an LO active phase shifter, I/Q mixers, and an RF PA driver. The transmitter has approximately 20-dB conversion gain per element, the maximum saturated RF output power is 2-dBm at 45GHz. Each element consumes 450mW. The chip size is 3mm x 2.4mm.

RTU2C-2 01:40 PM
A Thirty Two Element Phased-array Transceiver at 60GHz with RF-IF Conversion Block in 90nm Flip Chip CMOS Process

Emanuel Cohen*/**, Claudio Jakobson*, Shmuel Ravid*, and Dan Ritter**, * Mobile Wireless Group, Intel Haifa, Israel, ** Electrical Engineering Technion, Haifa, Israel

Abstract: A 60GHz 32 element bidirectional phased-array TX/RX chip with a 2 bit phase shifter and 12GHz IF converter, using 90nm CMOS process, is described. The array features 12.5 dB gain, NF of 11 dB, IP1dB of -17dbm for RX, and output Psat of 8dBm for TX, drawing 390 mA from a 1.3-V supply. The RMS amplitude and phase error of the phase shifter is 0.8dB and 5deg max respectively from 57 to 66GHz. Flip-chip assembly is used and characterized with additional test structures. Array die area is 14.5mm^2

RTU2C-3 02:00 PM

A 16-Element Phased-Array Receiver IC for 60GHz Communications in SiGe BiCMOS

S. Reynolds, A. Natarajan, M.-D. Tsai*, S. Nicolson**, J.-H. Zhan*, D. Liu, D. Kam, O. Huang*, A. Valdes-Garcia, B. Floyd, IBM T. J. Watson Research Center (Yorktown Heights, NY), *MediaTek (HsinChu, Taiwan), **MediaTek Inc. (San Jose, CA)

Abstract: A 0.12-μm SiGe phased-array Rx IC for beam-steered wireless communication in the 60GHz band is described. It has 16 RF phase-shifting front-ends with 11° digital phase resolution and hybrid passive-active RF signal combining. It achieves 7.4-7.9 dB NF (not including 12dB array gain) over the 4 IEEE channels, < -90dBc/Hz Rx phase noise at 1MHz offset, uses a double-conversion Rx core, draws 1.8W at 2.7V in 38 mm^2, and has been packaged with 16 antennas in a 288-pin organic BGA.

RTU2C-4 02:20 PM

A 24GHz Phased-Array Receiver in 0.13-μm CMOS using an 8GHz LO

S. Patnaik, R. Harjani, Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN 55455

Abstract: This paper presents a 24GHz two-channel phased-array receiver. The receiver adopts the LO-phase-shifting approach and employs a sub-harmonically injection-locked phase-shifter. A CMOS-only prototype, fabricated in a 130-nm SiGe BiCMOS technology, draws 24-mW from a 1.5-V supply and consists of a injection-locked oscillator, a down-conversion mixer and IF-buffer. The worst-case measured amplitude and phase errors are 1.5-dB and 4°. The two-channel receiver occupies an active area of 0.23-sq.mm.

RTU2C-5 02:40 PM

Wafer-Scale W-Band Power Amplifiers Using on-chip Antennas

Y. A. Atesal, B. Cetinoneri, R. A. Alhalabi, G. M. Rebeiz, University of California at San Diego

Abstract: This paper presents, for the first time, a W-band SiGe power amplifier designed and fabricated together with a high-efficiency on-chip microstrip antenna. The antenna/amplifier results in an effective radiated power (ERP=PtGt) > 10 dBm from 88 to 98GHz, with a peak of 14.6 dBm at 92GHz. The chip consumes 120 mA from a 1.7 V supply. The antenna/amplifier approach can be extended to a large number of elements (8x8) and allows for efficient wafer-scale power combining and phased-array scanning.

Tuesday May 25, 2010
01:20 PM
Room 212AB
Session: RTU2D: RF Modeling for Switch and PA Applications
Chair: Francis Rotella, Peregrine Semiconductor
Co-Chair: Yuhua Cheng, Peking University

RTU2D-1 01:20 PM
Application of BSIMSOI MOSFET Model to SOS Technology

J. W. Roach, L-W. Chen, P. G. Clarke, F. M. Rotella, Peregrine Semiconductor, San Diego, USA

Abstract: The BSIMSOI model dominates modeling of SOI MOSFETs. SOS technology has many of the same advantages as SOI for RF and low-power applications, plus enhanced electrical isolation and heat dissipation. BSIMSOI can reasonably describe state-of-the-art SOS devices as well, including partial and full depletion, if differences between SOS and SOI are accounted for. For RF switch applications, Ron and Coff are adequately represented. A spot check at low currents shows that Ft is not unreasonable.

RTU2D-2 01:40 PM
Modeling of SOI FET for RF Switch Applications

T.-Y. Lee, S. Lee, Skyworks Solutions, Inc.

Abstract: This paper presents the modeling of an SOI FET for RF switch applications. Given that the HF small-signal predictability, i.e. the insertion loss and the isolation, is a common state of the art, the study focuses on the modeling of the non-linearity of the FET. Finally a hybrid model that combines PSP as the FET core and a layout-dependent non-linear SOI substrate model is presented, and excellent non-linearity predictability was demonstrated on a real-life RF switch for cellular application.

RTU2D-3 02:00 PM
A High Power CMOS Differential T/R Switch using Multi-section Impedance Transformation Technique

H.-W. Kim, M. Ahn*, O. Lee, C.-H. Lee*, and J. Laskar, Georgia Institute of Technology, *Samsung Design Center

Abstract: A high-power CMOS SPDT antenna switch using a differential architecture and a multi-section impedance transformation technique is demonstrated. A loss of the whole design block including switch and matching networks has been analyzed, considering the integration issue of the front-end circuitries. The measured performance of the differential switch shows input 1-dB compression point (P1dB) of 33.8 dBm with insertion losses of 0.5 dB and 1.1 dB for Tx and Rx modes at 1.9GHz, respectively.

RTU2D-4 02:20 PM

Exploitation of Active Load-pull and DLUT Models in MMIC DesignA

D. M. FitzPatrick, T. Williams*, J. Lees, J. Benedikt, S.C. Cripps and P.J. Tasker, Cardiff University, *Selex-Galileo SAS Ltd.

Abstract: This paper describes how active loadpull has been applied to the design of a wide-band RFIC stage. The technique is particularly relevant in new and developing processes where accurate device models are not available. Often in RFIC design, components operate outside of the ideal operating impedance. A look-up table model technique based on measured data which can be used by conventional CAD programs is used to analyze behavior. This paper shows how the ALP system can be used in design & analysis?

RTU2D-5 02:40 PM

A Mixed-signal Load-Pull System for Base-station Applications

Mauro Marchetti*, Rob Heeres**, Michele Squillante*, Marco Pelk*, Marco Spirito*, and Leo C. N. de Vreede*, *Delft University of Technology, Mekelweg 4, 2628 CD, Delft, The Netherlands, **NXP Semiconductors, Gerstweg 2, 6534 AE, Nijmegen, The Netherlands

Abstract: The capabilities of active load-pull are extended to be compatible with the characterization requirements of high-power base-station applications. The proposed measurement setup provides ultra-fast high-power device characterization for both CW, as well as, pulsed, duty-cycle controlled, operation. The realized system has the unique feature that it can handle realistic complex modulated signals like W-CDMA with absolute control of their reflection coefficients vs. frequency.

Tuesday May 25, 2010
02:00 PM
ACC - Rooms 208AB, 209AB
Session: RTUIF: RFIC Interactive Forum
Chair: Walid Khalil, Ohio State University
Co-Chair: Patrick Yue, University of California, Santa Barbara

RTUIF-01
A 228μW Injection Locked Ring Oscillator based BPSK Demodulator in 65nm CMOS

Q. Zhu, Y. Xu, Illinois Institute of Technology

Abstract: This paper presents an ultra-low power BPSK demodulator based on injection locked oscillators (ILOs). Two ILOs are employed to convert BPSK signals to ASK signals which are demodulated by an envelope detector to baseband signals. For subGHz applications, the ILOs are implemented using ring oscillators to allow compact chip area and ultra-low power dissipation. The prototype demodulator is fabricated in a 65nm CMOS technology that consumes 228μW of power and occupies 0.014mm^2 of die area.

RTUIF-02
A 0.13-μm CMOS Wireless Reflector for Phase Sweep Cooperative Diversity

J.-F. Bousquet, S.C. Magierowski, G.G. Messier, Z. Zhao, Schulich School of Engineering, University of Calgary

Abstract: A 4GHz 1.2-V all-analog wireless reflector acting as a cooperative diversity repeater is built in 0.13-μm CMOS technology. Interfaced with a dipole antenna, the circuit achieves 22.3-dB gain for a low power consumption equal to 120 μW. By applying slow phase sweeping at the reflector node, diversity gain is achieved and the coverage area of an indoor wireless network is increased by a factor of 2.5.

RTUIF-03
Design Methodology and Comparison of Rectifiers for UHF-band RFIDs

Francesco Mazzilli*, Prakash E Thoppay*, Norbert Johl+, and Catherine Dehollain*, *Swiss Federal Institutes of Technology, Lausanne, 1015, Switzerland, +Advanced Silicon, Lausanne, 1004, Switzerland

Abstract: Rectifiers are important energy converters and henceforth crucial building blocks for RFID applications. In the first half of the work, we have presented a design methodology for matching the rectifier input impedance with the antenna to maximize the rectifier power conversion efficiency. The proposed design approach uses the fundamental transconductance (Gm(1)) analysis to estimate the rectifier input impedance.

RTUIF-04

A CMOS Ultra-wideband Radar Transmitter with Pulsed Oscillator

Sungeun Lee, Sanghoon Sim, Songcheol Hong, School of Electrical Engineering and Computer Science at KAIST, Korea

Abstract: A design of UWB radar transmitter is presented. The transmitter which uses a pulsed oscillator consists of pulse generator, switching buffers and control signal generator. The control signal generator includes modulators of BPSK and PPM for spreading the spectral lines. It is fabricated using 0.13μm CMOS technology and the chip size is 910x485 μm^2. The output spectrum is centered at the 22.0GHz with the 10-dB bandwidth 2.5GHz and the pulse width of output pulse is tunable from 630ps to 830ps.

RTUIF-05

900MHz/1800MHz GSM Base Station LNA with Sub-1dB Noise Figure and +36dBm OIP3

D. Leenaerts, J. Bergervoet, J.-W. Lobeek, M. Schmidt-Szalowski, NXP Semiconductors, Eindhoven, 5656AE, the Netherlands

Abstract: A sub-1dB NF fully integrated low noise amplifier in a 0.25μm SiGe:C BiCMOS technology targeting GSM base-station applications will be discussed. The two-stage LNA is housed in a HVSON10 package and mounted on a PCB. The LNA measures a NF of 0.75dB in the 900MHz band and 0.9dB in the 1800MHz band. The LNA is matched to 50Ω at the RF I/O pins of the IC and has integrated ESD protection on all IC pins. The LNA achieves an OIP3 of +36dBm, a 1-dB OCP of +19dBm while dissipating 190mW.

RTUIF-06

A 4.35-mW +22-dBm IIP3 Continuously Tunable Channel Select Filter for WLAN/WiMax Receivers in 90-nm CMOS

Mostafa Savadi Oskooei*,**, Nasser Masoumi**, Mahmud Kamarei**, and Henrik Sjöland*, *Department of Electrical and Information Technology, Lund University, Lund, Sweden, **School of Electrical and Computer engineering, University of Tehran, Tehran, Iran

Abstract: A low-power high linearity CMOS Gm-C channel select filter for WLAN/WiMax receivers in 90-nm CMOS technology is presented. To reduce power consumption a biquad cell with simple architecture is used. A simple but efficient technique is also used to improve the linearity. The cutoff frequency of the sixth order Butterworth LPF can be tuned from 8.1 to 13.5 MHz. The measurement results show an in-band IIP3 of +22-dBm and an IRN of 75 nV/√Hz at a power consumption of 4.35-mW from a 1-V supply.

RTUIF-07
Wideband Trans-Impedance Filter Low Noise Amplifier
M. Kaltiokallio*, A. Pärssinen**, J. Ryynänen*, *Aalto University, Finland, **Nokia Research Center, Finland

Abstract: A design of wideband low-noise amplifier, which includes transferred-impedance structures to improve interference tolerance is given. The LNA is implemented as part of simple RF receiver to demonstrate the feasibility of the transferred-impedance circuits in wideband receivers. The LNA itself achieves a gain of 24 and 20 dB, noise figure of 3.4 and 4.9 dB for the interference blocking structure turned off and on, respectively. Added selectivity of 6 dB is achieved by using the structure.

RTUIF-08
A Wideband High-Linearity Mixer in 0.5 μm InP DHBT Technology
M. Stuenkel, M. Feng, University of Illinios

Abstract: This paper presents the design, implementation and characterization of a wideband down-conversion mixer in a 0.5 μm InP DHBT process. A modified Gilbert cell topology is implemented to improve circuit linearity and to give a means by which DHBT mixers can operate at lower supply voltages. The measured circuit has a maximum conversion gain of 11.3 dB over a 3 dB bandwidth from 7 to 24GHz. The input referred 1-dB compression point is greater than -15.6 dB across the entire frequency range.

RTUIF-09
A High Gain Wideband 77GHz SiGe Power Amplifier
Roee Ben Yishay, Roi Carmon, Oded Katz and Danny Elad, IBM Haifa Research Lab

Abstract: This paper presents a fully integrated 77GHz power amplifier fabricated in a 0.13 μm SiGe BiCMOS technology. A 4-stages single ended common-emitter topology was utilized to achieve power gain of 19dB at 77GHz with 14.6dBm output power at 1dB compression, saturated power of 16dBm and 12.5% peak PAE.The PA demonstrates 3dB bandwidth of 15GHz (22%), wideband input and output matching and robust performance at 85 degrees.

RTUIF-10
A Broadband Differential Cascode Power Amplifier in 45 nm CMOS for High-Speed 60GHz System-on-Chip
M. Abbasi*, T. Kjellberg**, A. de Graauw***, E. V. Heijden***, R. Roovers***, H. Zirath*, *Chalmers University of Technology, **Chalmers Industrial Technologies, Sweden, ***NXP Semiconductors, The Netherlands

Abstract: A compact two-stage differential cascode power amplifier is designed and fabricated in a 45nm standard LP CMOS. The amplifier shows 20dB small-signal gain centered at 60GHz with a flat frequency response and 1-dB bandwidth of 10GHz in large-signal operation. The chip delivers 11.2dBm output power at 1-dB compression and up to 14.5dBm power in saturation. The amplifier operates with 2V supply and draws 90mA current which results in 14.4% PAE. The OIP3 is measured to be 18dBm.

RTUIF-11
A CMOS LC VCO with Novel Negative Impedance Design for Wide-Band Operation

Chang-Hsi Wu and Guan-Xiu Jian, Department of Electronic Engineering, Lunghwa University of Science and Technology,*RF Integrated Circuits,Wireless Communication Systems Nonlinear System Theory*, R.O.C.

Abstract: A 5.2GHz CMOS LC voltage-controlled oscillator (VCO) for UWB receiver, fabricated using CMOS 0.18μm process is presented in this paper. The tuning range of the proposed VCO is mainly broadened by novel negative resistance and tapping inductance techniques. Measured results of the proposed VCO reveal phase noise of -116.708/Hz at 1 MHz offset and tuning range of 4.567GHz~5.832GHz (24.32%) while consuming only 3.92mW under the supply voltage of 0.8V. The core area is 0.732mm x 0.633mm.

RTUIF-12
An 80GHz range Synchronized Push-push Oscillator For Automotive Radar Application

C. Ameziane, T. Taris, Y. Deval, D. Belot*, R. Plana** and J.-B. Bégueret, IMS-Bordeaux, *STMicroelectronics, **LAAS, FRANCE

Abstract: We present an 81GHz Injection Locking Oscillator, intended for automotive radar applications. The synthesis technique is based on a synchronization throw an external subharmonic signal. The reference signal, around 8GHz, is converted before being injected into the Push-push oscillator by inductive coupling. The synchronized oscillator is implemented in a 0.13μm STMicroelectronics BiCMOS technology. The ILO exhibits a locking range of 3GHz and a phase noise of -108dBc/Hz@10MHz from the carrier.

RTUIF-13
Millimeter Wave CMOS VCO with a High Impedance LC Tank

S. Chai, J. Yang, B. Ku, S. Hong., Korea Advanced Institute of Science and Technology

Abstract: The proposed VCO achieves low phase noise with high oscillation amplitude by using a high impedance resonator. The VCO shows PN of -94.83dBc/Hz@1MHz offset,-13.33dBm output power at 55.63GHz. In order to provide a comparison with a VCO with a conventional resonator, two VCOs with different resonators are designed. The proposed VCO shows 7.5dB higher output power and 11dB lower phase noise than the VCO with a conventional resonator. The proposed VCO can provide high performance for mmW applications.

RTUIF-14
Controlled Dither For Effective Fractional Delay in 90 nm Digital to Time Conversion Based DDS for Spur Mitigation

S. A. Talwalkar, T. Gradishar, B. Stengel, G. Cafaro and G. Nagaraj, Motorola, Inc., Plantation, FL

Abstract: Dithering is used in many discrete to continuous value conversion functions to provide an effective average fractional value. This paper reviews the application of time-domain dither to a digital-to-time converter (DTC) based digital synthesizer suitable for many common wireless communication systems. Controlled dithering is shown to help correct for buffer errors as well as quantization errors. Measurements of a 90 nm CMOS implementation using a 5 bit DTC show extension to effective 8 bits.

RTUIF-15
2-4 and 9-12 Gb/s CMOS Fully Integrated ILO-based CDR

O. Mazouffre*, R. Toupet*, M. Pignol**, Y. Deval1 and J. B. Begueret*, * IMS Laboratory, University of Bordeaux, Talence, France, ** CNES (Centre National d'Etudes Spatiales), Toulouse, France

Abstract: A CDR dedicated to satellite data link is presented. The clock recovery function is made-up of an Injection Locked Oscillator combined with an analog phase alignment circuit. The circuit covers two bit-rate ranges: 2.2 to 4.3 Gb/s and 9.1 to 12.1 Gb/s. It was designed in 130 nm CMOS bulk process from STMicroelectronics. The overall power dissipation is 400 mW in the first bit-rate range and 480 mW in the second including 220 mW for I/O buffers.

RTUIF-16
A 22.5-dB Gain, 20.1-dBm Output Power K-band Power Amplifier in 0.18-μm CMOS

Chi-Cheng Hung, Jing-Lin Kuo, Kun-You Lin, and Huei Wang, Dept of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University

Abstract: A fully integrated power amplifier (PA) at K-band implemented in 0.18-μm CMOS process is presented. The power amplifier performs 22.5 dB peak gain and saturation output power of 20.1 dBm. The 3-dB gain bandwidth is from 18-23GHz, while the output power at 1-dB compression point (OP1dB) from 19-22GHz is over 15 dBm. This power amplifier has the highest gain and output power in K-band using standard CMOS process.

RTUIF-17
A 40% PAE Linear CMOS Power Amplifier with Feedback Bias Technique for WCDMA Applications

H. Jeon, K..-S. Lee, O. Lee, K. H. An, Y. Yoon, H. Kim, D. H. Lee*, J. Lee**, C..-H. Lee***, J. Laskar, Georgia Electronic Design Center, USA, *Skyworks, USA, **Gwangju Institute of Science and Technology, Korea, ***Samsung Design Center, USA

Abstract: The highly efficient CMOS linear power amplifier for WCDMA applications with feedback bias technique is presented. The method involves connecting the gates of common-gate devices of the driver stage and the power stage in cascode configurations by a feedback network, and IMD sweet spot is properly used. The experimental results demonstrate a gain of 26 dB, a max output power of 26 dBm with 46.4% of peak PAE and a linear output power of 23.5 dBm with 40% PAE using a 3GPP WCDMA modulated signal.

RTUIF-18
A Switching-Mode Amplifier for Class-S Transmitters for Clock Frequencies up to 7.5GHz in 0.25μm SiGe-BiCMOS

S. Heck, M. Schmidt, A. Bräckle, F. Schuller, M. Grözing, M. Berroth, H. Gustat*, C. Scheytt*, University of Stuttgart (Institute of Electrical and Optical Communications Engineering), *IHP GmbH, Germany

Abstract: The paper presents the first voltage mode H-bridge amplifier in a complementary SiGe-technology for frequencies in the GHz range. The amplifier is suited as a driver for a high power GaN amplifier in class-S transmitters. It can be operated with pseudo-random pulse trains up to 7.5 Gbit/s. The measured broadband output power for a rectangular drive signal with a 50% duty cycle and a frequency of 2GHz is 148 mW. The PAE of the switching stage including all drivers is 30%.

RTUIF-19
SiGe Power Amplifier ICs for 4G (WIMAX and LTE) Mobile and Nomadic Applications

V. Krishnamurthy, K. Hershberger, J. Dekosky, H. Zhao, D. Poulin, R. Rood, E. Prince, VT Silicon, Inc., USA

Abstract: SiGe 4G PA development is a key element in enabling integrated 4G front end SiGe ICs. In this paper, we report a wideband SiGe 4G PA IC which meets WIMAX (802.16e) and LTE specifications. For 802.16e, the SiGe PA produces 25 dBm linear power at Vcc=3.3 V for 2.3-2.7GHz operation while meeting spectral mask and EVM<4%. For TD-LTE, Band 40 (2.3-2.4GHz) and FDD-LTE, Band 7 (2.500-2.570GHz), this SiGe PA produces 28.5 dBm linear power while meeting 3GPP specifications.

RTUIF-20
Self-Matched ESD Cell in CMOS Technology for 60GHz Broadband RF Applications

Chun-Yu Lin 1, Li-Wei Chu 1, Ming-Dou Ker 1,2, Tse-Hua Lu 3, Ping-Fang Hung 3, and Hsiao-Chun Li 3, 1 National Chiao-Tung University, Hsinchu, Taiwan; 2 I-Shou University, Kaohsiung, Taiwan; 3 Taiwan Semiconductor Manufacturing Company

Abstract: A self-matched ESD cell library has been implemented in a commercial sub-100nm CMOS process for 60GHz broadband RF applications. This ESD cell library has reached the 50-Ω input/output matching to reduce the design complexity for RF circuit designer to provide suitable electrostatic discharge (ESD) protection. Experimental results of this ESD cell library have successfully verified the ESD robustness and the RF characteristics in the 60GHz frequency band.

RTUIF-21
The Impact of MOSFET Layout Dependent Stress on High Frequency Characteristics and Flicker Noise

Kuo-Liang Yeh, Chih-You Ku, and Jyh-Chyurn Guo, Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

Abstract: Layout dependent stress in 90 nm MOSFET and its impact on high frequency performance and flicker noise has been investigated. Donut MOSFETs were created to eliminate the transverse stress from shallow trench isolation (STI). Both NMOS and PMOS can benefit from the donut layout in terms of higher effective mobility μ_{eff} and cutoff frequency f_t, as well as lower flicker noise. The measured flicker noise follows number fluctuation model for NMOS and mobility fluctuation model for PMOS, respectively. The reduction of flicker noise suggests the reduction of STI generated traps and the suppression of mobility fluctuation due to eliminated transverse stress using donut structure.

RTUIF-22
A Novel Low-Profile Low-Parasitic RF Package Using High-Density Build-Up Technology

Chien-Cheng Wei, Ming-Chien Lin, Chin-Ta Fan, Ta-Hsiang Chiang, Ming-Kuen Chiu, Shao-Pin Ru, and Albert Cardona*, Tong Hsing Electronic Industries, LTD., 55, Lane 365, Yingtao Road, Yinko, Taipei Hsien, Taiwan 239, Agile RF*, Inc 93 Castilian Drive, Santa Barbara, CA 93117

Abstract: This paper presents a low-profile, low-parasitic RF package by using the high-density build-up (HD-BU) technology. This package achieves much thinner, fine pitch, and exposed design pattern feature for outstanding electrical and thermal performance. The packaging fabrication is simple and only needs several processes. This HD-BU package provides lower parasitic than other lead-frame types due to the use of very thin bonding pads. Therefore, a capacitor chip is assembled using the proposed technology for packaging demonstration and electrical performance evaluation. Based on the experimental results, the measured capacitances at 1GHz are quite similar before and after packaging. It indicates that the HD-BU package has low parasitic capacitance even at high-frequency operation, and does not affect the electrical performance for the packaged chip. Additionally, these packages are good candidates for applications requiring low profile, low parasitic and low cost.

RTUIF-23
A High Quality Factor Varactor Technology Evaluation
R. Debroucke *, S. Jan*, J.-F. Larchanche*, C. Gaquiere, *STMicroelectronics Crolles, France; IEMN University of Lille, France

Abstract: Providing a high quality factor scalable varactor in an integrated technology is a challenge. How to insure that your device will give possible the highest quality factor? In order to answer this questions, we let the bases of a varactor gauge. For a given targeted capacitance, it could furnish a qualitative idea of the adequacy with technology performance. It could provide also an indicator for comparison with other devices. As example, we present a comparison between two varactors.

RTUIF-24
Power Improvement for 65nm nMOSFET with High-Tensile CESL and Fast Nonlinear Behavior Modeling
C. S. Chiu, K. M. Chen, G. W. Huang, K. H. Liao, S. Y. Lin, C. C. Hung*, S. Y. Huang*, C. W. Fan*, C. Y. Tzeng*, S. Chou*, National Nano Device Lab., United Microelectronics Corporation*, National Chiao Tung University**, Taiwan

Abstract: In this paper, the power gain improvements by stress contact etch stop layer (CESL) in a 65-nm nMOSFET were studied. Compared to the conventional nMOSFET, the device with CESL stress shows an extra 6% power gain enhancement for the increased stress in the channel region. This study also presents the polyharmonic distortion (PHD) model extraction by X-parameters measurement when the power transistor was designed to work far from 50Ω.

RTUIF-25
RF Benchmark Tests for Compact MOS Models
G. D. J Smit, A. J. Scholten, D. B. M Klaassen, NXP Semiconductors, The Netherlands

Abstract: We collect and derive a number of requirements for compact MOS models that are important for RF-circuit applications. We present, for the first time, a derivation for the required reciprocity of capacitances at zero bias. We also derive from first principles the expected non-quasi-static behavior of a MOSFET at Vds=0 as well as its thermal noise. Finally, we demonstrate that the CMC standard model PSP satisfies all presented requirements.

RTUIF-26
A 1.8V 74mW UHF RFID Reader Receiver with 18.5dBm IIP3 and -77dBm Sensitivity in 0.18μm CMOS
X. Sun, B. Chi, C. Zhang, Z. Wang, Z. Wang, Beijing, 100084, P. R. China

Abstract: A UHF RFID reader receiver is implemented in 0.18μm CMOS. The direct-conversion receiver consists of an LNA, passive mixers, baseband PGAs and LPFs. As high as 18.5dBm measured IIP3 of the RF front-end is achieved by using passive mixers driven by 25% duty cycle square wave LO. The receiver has a sensitivity of -77dBm in the normal mode and -87dBm in the LBT mode. The total power dissipation in the normal mode is 74mW from 1.8V power supply.

RFIC PANEL SESSIONS

Monday, May 24, 2010
12:00 PM - 01:10 PM • Room 210CD

The Challenges, Competitions and Future Prospect of 60 GHz

Chair/Moderator:
SK Yong, Marvell Semiconductor, Inc.
Myron Hattig, Intel Corporation

Panelist and Affiliation:
C. Patrick Yue, UC Santa Barbara

Panelists:
1. **Jason Trachewsky,** Senior Technical Director and Broadcom Fellow, Broadcom Corporation
2. **Scott Reynolds,** Manager, IBM TJ Watson
3. **Myron Hattig,** Director of WLAN Standards, Intel Corporation
4. **Raja Banerjea,** Principal Architect, Marvell Semiconductor, Inc.
5. **Michiaki Matsuo,** Senior Manager/Chief Engineer, Panasonic Corporation
6. **Jisung Oh,** Principle Engineer/Director, Samsung Electronics

Sponsor: **RFIC**

Panel Session Abstract: The ever growing demand for multi-gigabit data rates to support variety of new applications has pushed to the emergence of 60 GHz radio technology. Significant R&D work in the past decade have demonstrated the viability of wideband 60 GHz CMOS RFIC circuit and transceiver, which were difficult if not impossible to realize in the past, have now become a reality for commercialization. The momentum is further intensified by the heavily harmonized regulations and frequency allocation globally that allow higher EIRP limit and operation of huge unlicensed (i.e. 7 GHz) bandwidth in the 60 GHz band.

As a result, various standards (IEEE 802.11ad and IEEE 802.15.3c) and industry alliances (WirelessHD™ and WiGig Alliance) have emerged to deliver the promise of gigabit wireless solution. Multiple standard solutions could lead to two contradictory effects: On one hand, competition could lead to better 60 GHz products and drives the cost down towards commoditization. On the other hand, competition could create market confusion and co-existence issues among different products if not handled correctly. To date, among the various different standards, only 60 GHz products based on WirelessHD™ solution that supports wireless transmission of full HD contents has reported to hit the high end TV market in Jan 2009. Other 60 GHz products are under rigorous development and in the pipeline for productization. However, the question remains on their timeline in delivering the promise of gigabit experience to the customers.

In addition, Wi-Fi based IEEE 802.11n solution has started to enter the market for audio/video distribution on top of the widespread used of wireless Ethernet. Built strongly upon a broad ecosystem and interoperability among billions of Wi-Fi devices, Wi-Fi centric solution is set to evolve into gigabit data rate range with the recent development in IEEE 802.11.ac. This could potentially yet another solution that serves the similar applications and thus creates competition in market place with 60 GHz. However, the distinct characteristics of Wi-Fi (2.4/5 GHz)

and 60 GHz provide a different deployment perspective in which both technologies could be complementary rather than competing to each other. Such complementary technology requires multi-band radios that allow fast and seamless session transfer between them whenever the performance of the current radio deteriorates or an enhanced performance could be achieved.

In this panel, industry leaders and experts will discuss the challenges ahead of full scale commercialization of 60 GHz technology including implementation, tug-of-war among competitive standards, co-existence issues and future direction of 60 GHz.

RFIC PANEL SESSIONS (continued)

Tuesday, May 25, 2010
12:00 PM - 01:10 PM • Room 210CD

Future of High-Speed I/O: Electrical, Optical, or Wireless?

Chair/Moderator:
Jacques C. Rudell, University of Washington

Co-Organizer:
Sam Palermo, Texas A&M

Panelists and Affiliations:
1. **Ali Hajimiri,** Caltech
2. **Byunghoo Jung,** Purdue University
3. **Jared Zerbe,** Rambus
4. **Sam Palermo,** Texas A&M
5. **Ronald Ho,** Sun Microsystems
6. **Daniel Kucharski,** Luxtera

Sponsor: **RFIC**

Panel Session Abstract: The rising power consumption associated with microprocessors realized in nanometer length silicon processes has placed a fundamental limit on core clock rates. This has lead to new advanced microprocessor architectures which seek to increase computational power by replicating the number of cores on a single die. Processors currently under development are estimated to use as many as 128 cores integrated on the same IC, leaving the routing of data via high-speed signaling from core-to-core, core-to-cache, or core-to-off-chip memory as a critical aspect of modern microprocessor performance. What is the future of high-speed I/O? Will the future demand for higher data rate I/Os come through incremental advances of all-electrical integrated transceivers, or will a new breed of high-speed I/O come to life in the form of either integrated optical (nanophotonics) transceivers, or perhaps mmWave wireless transceivers. Come hear a panel of experts debate what the future holds for high-speed signaling.

IMS LUNCH PANEL SESSIONS

Monday, May 24, 2010
12:00 PM - 01:10 PM • Room 210AB

Hubbert's Peak, The Coal Question, and Climate Change

Chair/Moderator:
David Rutledge, **Tomiyasu Professor of Electrical Engineering,**
California Institute of Technology

Tuesday, May 25, 2010
12:00 PM - 01:10 PM • Room 201AB

Silicon at THz Frequencies: A Reality or a Dream?

Chair/Moderator:
Prof. Gabriel M. Rebeiz, University of California, San Diego

Wednesday, May 26, 2010
12:00 PM - 01:10 PM • Room 210AB

Semiconductor Technology Impact on Microwave and Millimeter Wave Markets

Chair/Moderator:
Doug Lockie, Gigabeam

12:00 PM - 01:10 PM • Room 210CD

Standardizing Attributes for RF and Microwave Components and Assemblies – The Time Is Now?

Chairs/Moderators:
Dr. Chandra Gupta, Aeroflex-KDI, **Dr. Paul Khanna**, Phase Matrix

Thursday, May 27, 2010
12:00 PM - 01:10 PM • Room 210AB

On-Die Synthesized Inductors: Boon or Bane?

Chair/Moderator:
Jim Wight, Carleton University

12:00 PM - 01:10 PM • Room 210CD

RF GaN Reliability: Where Does the Technology Stand?

Chairs/Moderators:
Frank Sullivan, Raytheon, **Bernie Geller,** Vadum, Inc.

WORKSHOPS AND SHORT COURSES

Workshops and Tutorials are offered on Sunday, Monday and Friday of Microwave Week. They are distinguished by the following features:

- Advanced Level Workshops (designated as WSA, WSB, etc.) present the state of the art to specialists who are already experienced in the topic area.
- Tutorial Level Workshops (designated as TSB, RSC, etc.) are targeted towards educating attendees in new areas of microwave technology, reviewing material that is primarily a revision of previously published information.

All Workshops and Tutorials will be held at the Anaheim Convention Center. Specific room assignments will be announced at check-in.

RFIC AND IMS SPONSORED SUNDAY WORKSHOPS

08:00 AM-12:00 PM

WSA: Software Defined Radio for Microwave Applications.

Reviewed by: **MTT-9, MTT-20**
Organizers: **Jeffrey Pawlan,** Pawlan Communications;
Hermann Boss, Rohde & Schwarz

Abstract: Software Defined Radio (SDR) is the most significant innovation and change to radio communications since 1990. From HF to microwave frequencies, it allows the use of a fixed hardware platform to change bands, frequencies, and modulation types without any change in the hardware at all. This synergistic combination of analog and digital microwave hardware combined with software has significantly improved performance, allowed for great flexibility to ever-changing modulations and standards, shortened development time, and reduced cost. This workshop will make SDR understandable and applicable to microwave engineers.

It will begin with a clear explanation of how SDR works and its evolution through several generations of refinements. You will see and hear SDR in action with several live demonstrations of operating hardware and software along with test equipment. Your future work as a microwave engineer will be put in perspective with the current and future radio requirements.

Actual space communications SDR hardware and software will be demonstrated by the second speaker who is from JPL / NASA.

Cognitive Radio, a new related field, will be presented by a third speaker. SDR makes it possible to dynamically assess spectrum activity and change the modulation format to allow multiple signals to co-exist on the same frequency without interference or jamming.

This workshop will be practical and emphasize weak signal communications and commercial applications.

Speakers:

1. **Jeffrey Pawlan,** Pawlan Communications, "Software Defined Radio for Weaksignal and Commercial Applications"
2. **James Lux,** JPL, "The Adoption of SDR by NASA for Space Communications"
3. **Vasu Chakravarthy**, Air Force Research Laboratory/Sensors Directorate "An Introduction to Cognitive Radio and its Implementation"

01:00 PM-05:00 PM

WSB: Advances in Filtering and Sampling for Integrated Transceivers

Reviewed by: **RFIC, MTT-9, MTT-20**
Organizers: **Tom Riley,** Kaben Wireless Silicon Inc.

Abstract: Blocker and interference filtering is a key issue in highly integrated Software Defined Radio (SDR) Receivers. If blockers can be removed prior to the ADC and conversion to the digital domain, power and area in the ADC can be greatly reduced. This workshop will show how Analog, sampled-time signal processing can be used to implement highly selective FIR, IIR and spatial FIR filters. N-path filtering can be used to design high bandwidth filters using low bandwidth analog components. Component mismatch, timing jitter and other sources of error that can affect receiver performance will be discussed. Linearity enhancement techniques for filters will be presented, as well as wideband RF front-end circuit techniques. For added blocker rejection, notched Delta-Sigma data converters are presented.

Following each speaker's presentation, the floor will be opened for interactive discussion with the audience.

Speakers:

1. **Tom Riley,** Kaben Wireless Silicon Inc., "Advances in Discrete-Time Analog Filtering"
2. **Bogdan Staszewski,** Technical University of Delft, "Discrete-Time Receiver"
3. **Asad Abidi,** University of California, Los Angeles, "A Discrete-Time Wideband Receiver for Software-Defined Radio"
4. **Dr. Martin Snelgrove,** Kapik Integration Inc., "Interference Mitigation in Receivers"

08:00 AM-05:00 PM

WSC: Interference, Noise and Coupling Effects in Modern SoC and SiP Products: Issues, Problems and Solutions

Reviewed by: **RFIC, MTT-6, MTT-12**
Organizers: **Jan Niehof,** NXP Semiconductors
Matthias Locher, ST-Ericsson
Oren Eliezer, Xtendwave

Abstract: The focus of this interactive workshop will be on resolving noise and self-interference problems: on-chip coupling effects, chip-package co-design, substrate issues, noise (inherent and external), coupling-aware RFIC floor planning, digitally assisted solutions for interference problems, EMC (chip and board level), design practices, and CAD/EDA modeling capabilities to effectively analyze and address these effects. Recognized companies and partnerships active in the semiconductor industry will present actual issues encountered in their designs and the solutions/design-practices used to address them, including key lessons learned. Interactive discussions will be facilitated to exchange valuable ideas for the benefit of participants and the industry at large.

Speakers:

1. **Nikos Haralabidis,** Broadcom, "Self-Interference in Multi-Standard RF SoC Transceivers"
2. **Dietolf Seippel,** Infineon, "Floor Planning of Complex Baseband-Radio SoCs in Consideration of Cross Talk Prevention"
3. **Matthias Locher,** ST-Ericsson, "A Bottom-Up Design and Verification Approach for Coexistence in Multi-System SoCs"
4. **Ayman Fayed,** Iowa State University, Oren Eliezer, Xtendwave, "System-level Methodology for the Power Management System Design in Complex SoCs: Minimize the Impact of Interference Through the Supply"
5. **Jonathan Jensen,** Intel, "Isolation and Coexistence Challenges – A Single-chip Bluetooth/WiFi Combo Example"
6. **Jan Niehof,** NXP Semiconductors, "Interference Issues and Coupling Effects in RF Products"
7. **Ravi Subramanian,** Berkeley Design Automation, "Advances in CAD: Simulation & Analysis of RF SoCs"

08:00 AM-05:00 PM

WSD: Ultra-Wideband (UWB) Technology: The State-of-the-Art and Applications

Reviewed by: **MTT-15, MTT-16**
Organizers: **Zhizhang (David) Chen,** Dalhousie University, Canada;
Hong (Jeffery) Nie, University of Northern Iowa, USA

Abstract: Since the FCC issued a Report and Order allowing license-free use of 0-960 MHz and 3.1-10.6GHz frequency bands in 2002, extensive research and development efforts have been made worldwide in utilizing these ultra-wide-band (UWB) frequency allocations for applications such as microwave imaging, high-speed short-range wireless communications, and wireless sensor networks. Despite a couple of setbacks in its commercialization, UWB technology and application continue to advance. More UWB algorithms and hardware design approaches are emerging. This workshop presents the latest developments of various UWB technologies, paying the way for ultimate realization of practical UWB systems. The workshop provide insight into (a) the operating principles and limitations of UWB systems, (b) design and test of UWB antennas, components, RF front-ends and transceivers, (c) the state-of-the-art in UWB signal processing algorithms, and (d) future trends in the UWB systems and their applications. This workshop will be beneficial to students, engineers and researchers who want to learn about the current status of UWB and related designs, tests and applications, and who want to follow and understand the recent developments and advanced applications of UWB.

Speakers:

1. **Dave Michelson,** University of British Columbia, Canada, "Deployment of UWB Wireless Systems in Industrial Environments"
2. **Zhining Chen,** Institute for Infocomm Research, Singapore, "Miniaturization of Ultra-Wideband Antennas"

3. **Ke Wu, Serge O. Tatu** and **Renato G. Bosisio,** École Polytechnique de Montréal, Canada, "Multi-Port Interferometers for UWB Transceiver Systems and Applications"
4. **Natalia Nikolova,** McMaster University, Canada, "Direct Methods for Detection and Imaging with Microwave Measurements in the Ultra-wide Band"
5. **Aly Fathy** and **Mohamed R. Mahfouz,** et. al., University of Tennessee, Knoxville, USA, "Recent Trends and Advances in UWB Positioning"
6. **Hong Nie,** University of Northern Iowa, USA, "Code Shifted Reference UWB transceiver and Its Applications for Intra-Vehicle Control and Communication"
7. **Zhizhang (David) Chen,** Dalhousie University, Canada"UWB Reference-based Impulse Radio Systems and Hardware Design Issues"

08:00 AM-05:00 PM

WSE: High Speed Signal Integrity Workshop

Reviewed by: **MTT-11, MTT-12**
Organizers: **Brett Grossman,** Intel Corporation
Mike Resso, Agilent Technologies

Abstract: The triple play of voice, video, and data continues to demand ever greater bandwidths from devices and interconnects. This requirement is driving the challenges faced by the signal integrity engineer into a realm which may seem somewhat familiar to the microwave engineer. However, the challenges associated with frequency content, coupled with the density of signals, and the need to fit into relatively low cost consumer products, are a unique set of constraints which drive these solutions.

This signal integrity workshop will feature presentations which discuss practical case studies, as well as more fundamental and theoretical signal integrity research. You are welcome to attend and listen to industry and academic experts describe several of the latest developments in the field of high speed signal and power integrity.

Speakers:

1. **Paul Huray,** University of South Carolina, "Bridging the Gap"
2. **Michael Hill,** Intel Corporation, "Microprocessor Power Integrity – Metrologies and Future Challenges"
3. **Heidi Barnes,** Verigy, "The Art of VNA Calibrations for Measuring Low Loss PCB Components"
4. **Matthew Claudius,** Intel Corporation, "End Use Model Correlation"
5. **Bob Schaefer,** Agilent Technologies, "Comparison of Fixture Removal Techniques for Connector and Cable Measurements"
6. **Jim Rautio**, Sonnet Software "Measurement and Analysis of Substrate Dielectric Constant Anisotropy"
7. **Evan Fledell,** Intel Corporation, "Passive Interconnect Frequency Domain Characterization for Mixed-Medium and Vertical Interconnect Systems"
8. **Leung Tsang,** University of Washington, "Electromagnetic Modeling of High Speed Vertical Interconnect on Chip-Package-Board"

08:00 AM-05:00 PM

WSF: GaN for High Power, High Bandwidth Applications, Finally Fulfilling the Promise

Reviewed by: **MTT-5, MTT-6, MTT-7**
Organizers: **Bill Vassilakis,** Empower RF Systems
David W. Runton, RF Micro Devices

Abstract: GaN circuits have, for a long time, promised to enable amplifier applications that have not been possible with GaAs or LDMOS such as higher temperatures of operation, large operating bandwidths, and higher operating power. Material quality problems have slowed the progress on the delivery of such applications leaving many wondering when GaN would displace incumbent technologies. GaN has also defied declining cost trends of semiconductors, due to higher processing costs, smaller wafers, and lower yields. In the commercial market, dollars per watt delivered has long dominated in the selection of technology. Other factors such as efficiency, the ability to pre-distort, and linearity have been secondary. GaN is at last emerging as a serious contender for both commercial and military applications, as we see more demand for power, efficiency and larger bandwidths of operation. As other technologies are reaching inherent limits, GaN is finally ready for prime time.

Speakers:

1. **Norihiko Ui,** Sumitomo Electric Device Innovations, "Power and High Efficiency GaN-HEMTs for Cellular Base Station Applications"
2. **Oualid Hammi** and **Fadhel M. Ghannouchi,** iRadio Lab, Department of Electrical and Computer Engineering, University of Calgary, Canada, "Power Amplifiers for Wireless Communication Infrastructure"
3. **Dr. James J. Komiak**, BAE Systems Electronic Solutions, "Progress in High Power GaN HEMT Power Amplifiers for Wideband Applications"
4. **Simon Wood,** Cree Inc., "Trends in high power GaN transistors and MMICs"
5. **Bumman Kim,** Pohang University of Science and Technology, "Highly Efficient Saturated Power Amplifier based on GaN – A class P amplifier"
6. **David W. Runton**, RF Micro Devices, "Defining Application Spaces for High Power GaN"
7. **Rik Jos,** NXP Semiconductors,"GaN HEMT and their Commercial RF Power Applications"

08:00 AM-12:00 PM

WSG: MOSFET Modeling for RFIC Design Based On the Industry-Standard PSP Model

Reviewed by: **RFIC, MTT-6**
Organizers: **Kevin McCarthy,** University College Cork;
Weimin Wu, Arizona State University

Abstract: This workshop will present an overview of the state-of-the art in MOSFET modeling for the design of CMOS Radio Frequency ICs using modern nanometer-scale CMOS. It focuses on the industry-standard PSP (MOSFET) and MOSVAR (varactor) models. The workshop will review the fundamentals of both models and demonstrate the highly-accurate RF simulation capabilities they provide for RFIC designs. The workshop will also show how the PSP model can be extended to SOI and Multi-Gate devices, which will become of increasing importance to RFIC design.

Speakers:

1. **Gert-Jan Smit,** NXP Semiconductors, "The PSP Compact MOSFET Model: Physical Background and Benefits for RFIC Design"
2. **Brandt Braswell,** Freescale Semiconductor, "Deployment of an Advanced MOSFET Model in an Industrial Context"
3. **James Victory,** Sentinel IC Technologies, "MOSVAR – A PSP-Derived MOS Varactor Model"
4. **Weimin Wu,** Arizona State University "PSP-Based Modeling of SOI and Multi-Gate MOS Devices"

08:00 AM-05:00 PM

WSH: Power Management for Integrated RF Circuits: Challenges and Solutions

Reviewed by: **RFIC, MTT-6**
Organizers: **Ayman Fayed,** Iowa State University
Waleed Khalil, Ohio State University
Oren Eliezer: Xtendwave

Abstract: The recent expansion in the use of mobile communications and multi-media devices has fueled the demand for various wireless/RF transceivers to be integrated in a single SoC with the digital processing circuitry and power management functions. As battery life in mobile devices is critical, and with these transceivers typically not operating directly from the battery, regulating and delivering power to them in an efficient manner is becoming a bottleneck. Since power delivery efficiency and implementation cost on one hand, and noise and regulation quality on the other hand are two contradictory factors in traditional power management circuits, RF loads present a great challenge due to their high sensitivity to their power supply quality. This workshop will discuss the challenges and tradeoffs that power management designers have to make when designing for RF loads while maintaining high efficiency and cost-effectiveness.

Speakers:

1. **Ayman Fayed,** Iowa State University, "Challenges in Integrated Power Management for Analog, RF, and mixed-signal SoCs"
2. **Keith Kunz,** Texas Instruments, "Integrated DC-DC Converters in Nanometer CMOS RF SOCs"
3. **Bertan Bakkaloglu,** Arizona State University, "Low-noise Switched-mode and Low-dropout Linear Regulators for RF Applications"
4. **Siamak Abedinpour,** Freescale, "An Overview of Integrated Power Management Circuits for Portable RF applications"
5. **Sam Palermo,** Texas A&M University, "Supply Regulation Techniques for Frequency Synthesizers"
6. **David Allstot, Jeffery Walling,** University of Washington, "Supply Regulators in Class-E/G/H CMOS Power Amplifiers"
7. **Ram Sadhwani,** Intel, "Direct Powering of RF and Analog Circuits from DC-DC Converters"
8. **Ahmed Emira,** Newport Media, "DC-DC Converters Noise Considerations in RF SoCs"

08:00 PM-05:00 PM

WSI: Substrate Integrated Circuits (SICs)

Reviewed by: **MTT-8, MTT-12**
Organizers: **Maurizio Bozzi,** University of Pavia, Italy
Ke Wu, Ecole Polytechnique (Université de Montréal), QC, Canada

Abstract: Substrate integrated circuits (SICs) are probably the most promising candidate for the design and implementation of low-cost and high-density millimeter-wave integrated circuits and systems in the next decades. SICs, which integrate planar and non-planar structures together, are able to offer a compact, low-loss, flexible, high integration density, and cost-effective solution for integrating active circuits, passive components and radiating elements on the same substrates including multilayered geometries regardless of technological platforms such as PCB, LTCC, MHMICs, MMICs and even CMOS processes. In this way, the concept of System-in-Package (SiP), widely adopted in the design of RF/microwave circuits, can be extended to System-on-Substrate (SoS) for up-higher frequency ranges. This technological concept can be extended to terahertz and optoelectronic domains.

The aim of this workshop is to provide an overview of the current trends of research and development in the field of SICs, including modeling methods, innovative structures, design techniques and technological issues.

Speakers:

1. **Ke Wu,** Ecole Polytechnique (Université de Montréal), Canada, "State-of-the-art and Future Perspective of Substrate Integrated Circuits"
2. **Tatsuo Itoh,** University of California, Los Angeles, USA , "Progress in Composite Right/Left Handed Structures based on Substrate Integrated Waveguide"

3. **Vicente E. Boria-Esbert,** Polytechnic University of Valencia, Spain, "Computer-Aided Design Tools of Passive Circuits in Substrate Integrated Waveguide Technology"
4. **Jens Bornemann,** University of Victoria, Canada, "Multilayered Substrate-Integrated Waveguide Couplers"
5. **Maurizio Bozzi,** University of Pavia, Italy, "Full-Wave Analysis and Equivalent-Circuit Modeling of SIW Components"
6. **Ruey-Beei Wu,** National Taiwan University, Taiwan, "Development of LTCC mm-wave Passive Components for SoP Wireless Applications"
7. **Apostolos Georgiadis,** Centre Tecnològic de Telecomunicacions de Catalunya, Spain, "Oscillator and active antenna design in SIW technology"
8. **Roberto Vincenti Gatti,** University of Perugia, Italy, "SIW Components and Solutions for Large Electronic Beam Steering Arrays"
9. **Stepan Lucyszyn,** Imperial College, United Kingdom, "Substrate Integrated Metal-Pipe Rectangular Waveguides"

08:00 AM-05:00 PM

WSJ: Re-configurable Multi-Radios at the Nanoscale

Reviewed by: **RFIC, MTT-6, MTT-20**
Organizers: **Gernot Hueber,** DICE, Linz, Austria
Robert Bogdan Staszewski, Delft University of Technology, The Netherlands
Stefan Heinen, RWTH Aachen University, Aachen, Germany

Abstract: Advances in CMOS fabrication technology have enabled the use of CMOS in today's RF transceivers for wireless communications. Multi-band and multi-mode radios covering the diversity of communication standards from 2G GSM, 3G UMTS, to 4G LTE impose unique challenges on the RF-transceiver design due to limitations of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications. Nanoscale CMOS on one hand features the possibility for implementing a significant computational power and complex functionality directly on a single IC, on the other hand it shows poor raw performance or RF circuits compared to other technologies. The focus of this workshop is on the challenges the cellular standards pose on future multi-radio integration in nanoscale CMOS, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in a multi-radio SoC or SiP. Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-ends.

Speakers:
1. **Gernot Hueber,** DICE, Austria, "Flexible RF Transceivers for 4G Systems"
2. **Ali M. Niknejad,** UC Berkeley, CA, " High Dynamic Range Wide Bandwidth Building Blocks for Multi-Mode CMOS"
3. **Vito Giannini,** IMEC, Leuven, Belgium, "The Green-Scalable Revolution of Nanoscale Software-Defined Radios"
4. **Jaques C. Rudell,** University of Washington, WA, "Nanometer CMOS Transceiver Design Enters the Era of "Co-Existence" and the SDR"

5. **Hooman Darabi,** Broadcom, Irvine, CA, "Radio Architectures for 2/3/4G Highly Integrated Cellular Applications"
6. **Francois Rivet,** IMS Lab, University of Bordeaux & Atlantic Innovation ES, France, "Towards Software Radio Receiver"
7. **Ali Hajimiri,** Caltech, CA, "Electromagnetically Reconfigurable Radios: Antenna Meets Digital"
8. **Frank Op 't Eynde,** Audax-Technologies Ltd., Wilsele, Belgium, "Unsolved Issues in SDR RF Frontends"
9. **Larry Larson,** University of California, San Diego, CA, "Low-Power Transmitters in Nanoscale CMOS"
10. **Robert Bogdan Staszewski,** TU Delft, The Netherlands, "Advances in Digital RF Architectures"

08:00 AM-05:00 PM

WSK: Multi-Mode Front End Design Challenges and Techniques

Reviewed by: **RFIC, MTT-6, MTT-20**
Organizers: **Edward Spears,** RFMD
Nick Chang, Skyworks Solutions

Abstract: With the proliferation of data services, mobile device original equipment manufacturers (OEMs) are presented with new, unprecedented challenges and demands from both mobile operators and consumers. Mobile operators require customized handsets and mobile devices to meet various consumer roaming needs, and the issue of rapid customization has fallen to OEMs who must configure these complex 3G devices to function in multiple frequency bands and operating modes (GSM, EDGE, WCDMA, HSPA+, with LTE on the horizon). As the number of bands and band combinations grow, frequency flexibility and signal routing at the platform level have increased in importance as critical parameters for 3G mobile device development. This sets up an unprecedented challenge for front-end suppliers who are challenged to design a broad portfolio of high-performance, multi-band, multimode front ends and components that offer frequency flexibility, ease of implementation, size reduction, and low current consumption. Presentations in this workshop will focus on the design challenges to meet these multi-mode front end requirements along with the required advancements in device technology and design techniques to meet the overall bandwidth and efficiency requirements. Design techniques of linearization, efficiency enhancement, power detection and controls will be covered in design examples utilizing various technologies such as GaAs HBT, CMOS, Silicon-on-Insulator and Silicon Germanium.

Speakers:
1. **Ville Vintola,** Nokia, "OEM Prospective for Multi-mode Solutions"
2. **Ray Arkiszewski,** RFMD, "GaAs HBT Multi Mode Amplifiers"
3. **David Ripley,** Skyworks Solutions, "Multi-mode, Multiband Power Amplifiers and Serial Bus Interface Standards"
4. **Larry Larson,** University of California at San Diego, "Design Techniques for Broadband Efficient Linear Power Amplifiers for Multi-Mode Wireless Applications"

5. **Dan Nobbe,** Peregrine, "Multimode Antenna Switch Modules"
6. **Nadim Khlat,** RFMD, "Tunable Front Ends Performance Benefits"
7. **Pasi Tikka,** Epcos, "Multimode Filter and Switch Modules"

08:00 AM-05:00 PM

WSL: Silicon-Based Technologies for Millimeter-Wave Applications

Reviewed by: **MTT-6, MTT-16, RFIC**
Organizers: **Jitendra Goel,** Raytheon Company
Lance Wei-Min Kuo, Raytheon Company
Didier Belot, STMicroelectronics
Eric Kerhervé, IMS Lab
Georg Boeck, Berlin Institute of Technology

Abstract: Traditionally, millimeter-wave (MMW) circuits utilizing only III-V technologies have been employed in low-volume, high-performance products. With the recent progress of highly scaled Si-based (SiGe and CMOS) technologies achieving f_t and f_{max} beyond 200 GHz, the application space of Si-based technologies has broadened from digital, analog, RF, and microwave domains to include MMW applications. The workshop will focus on MMW applications such as imaging (94 GHz and 140 GHz), automotive radar (LRR at 77 GHz and SRR at 79 GHz), and wireless high data rate communications (W-HDMI at 60 GHz). It gives an overview of recently developed architectures, circuit design techniques, and antenna configurations to meet the demanding performance specifications of MMW applications.

Speakers:
1. **Ali Hajimiri,** California Institute of Technology, "Si Millimeter-Wave Systems"
2. **Gabriel M. Rebeiz,** University of California at San Diego, "Ultra-Low Power Millimeter-Wave Phased Arrays and Gbps Communications Systems Using On-Chip Antennas"
3. **M. C. Frank Chang,** University of California, Los Angeles,"60-130 GHz Circuit/System Developments Based on Super-Scaled CMOS"
4. **Tian-Wei Huang** and **Huei Wang,** National Taiwan University, "Millimeter Wave Broadband Multi-Gigabit CMOS Transceiver Design"
5. **Scott K. Reynolds,** IBM T. J. Watson Research Center, "Millimeter-Wave Circuits and Systems Work at IBM Research"
6. **Piet Wambacq,** IMEC "CMOS Radio Integration for High-Data rate 60 GHz Applications"
7. A**li Niknejad,** UC Berkeley, "mm-Wave Medical Imaging Using a 94 GHz Time-Domain Ultrawideband Synthetic Imager (TUSI)"
8. **Ullrich Pfeiffer,** University of Wuppertal, "Silicon Process Technologies for Emerging Terahertz Applications"
9. **Pierre Busson,** STMicroelectronics, "60 GHz W-HDMI Transceiver"
10. **Joy Laskar,** Georgia Tech, "mmW Digital CMOS Radio Solutions for Ultra-Low Power, High Resolution Sensing and High Bandwidth Connectivity"
11. **Cathia Laskin,** University of Toronto, "140 GHz Imaging"

08:00 AM-05:00 PM

WSM: RF Packaging Solutions for Wireless Communication Platforms

Reviewed by: **MTT-12, MTT-20, RFIC**
Organizers: **Telesphor Kamgaing,** Intel Corporation
Vijay Nair, Intel Corporation
Clemens Ruppel, TDK-EPC

Abstract: In order to satisfy the decreasing form factor and increasing functionality demand from novel devices such as netbooks and smartphones, it is imperative to create a platform, where different radios and digital logic have to co-exist. This ultimate goal can only be achieved by overcoming various significant challenges at the silicon, packaging and testing levels. This full day workshop will focus on recent research and development work that will enable future ultra-small form factor computing and communication devices that incorporate one or multiple radios on the same platform. Various technology ingredients and packaging solutions for 60GHz, WiFi, WiMAX, Bluetooth, GPS and 3G/4G radios among others will be addressed by leading industrial and academic experts in the field.

Speakers:

1. **Vijay Nair,** Intel Corporation, "Multi-protocol Multi-radio Wireless Platform Integration Challenges"
2. **Joy Laskar,** Georgia Institute of Technology, "Development of Millimeter-Wave QFN: CMOS, PCB and Phased Array"
3. **Anh-Vu Pham,** University of California, Davis, "Development of Ultra-small Wireless Passive Modules Using 3-D Organic Metamaterials"
4. **Telesphor Kamgaing,** Intel Corporation, "Package Level Realization of Passives for Multiradio Wireless Modules"
5. **Clemens Ruppel,** TDK-EPC, "Front-End Integration for Multi-Band, Multi-Standard Mobile Phones Based on LTCC"
6. **William Chappell,** Purdue University, "Silicon on Silicon Packaging Using Self-aligned Interconnects"
7. **Walter De Raedt,** IMEC, "3D Heterogeneous Integration Techniques for Wireless Devices"
8. **Kevin Slattery,** Intel Corporation, "RF Interference in Small Form Factor Devices"

08:00 AM-05:00 PM

WSN: The State of Art of Microwave Filter Synthesis, Optimization and Realization

Reviewed by: **MTT-8, MTT-16**
Organizers: **Ming Yu,** COM DEV, Canada
John Bandler, McMaster University

Abstract: Today systems require increasingly sophisticated microwave filters and multiplexers. The designer often faces the challenges of compromising between several contrasting requirements. This workshop will present a comprehensive overview of the state of the art of microwave filter synthesis, optimization and realization. Recent advances in some of the most promising application areas of microwave filters; innovative solutions concerning both design approaches and technological achievements will also be presented.

Speakers:

1. **Dick Snyder,** RS Microwave, USA, "Phase Shift, Delay, Anomalous Dispersion, and Meta-Materials: Implications for Future Filter Designs"
2. **John W. Bandler,** McMaster University, Canada, "Advanced Optimization Techniques for Modern Filter Design—From Newton to Space Mapping"
3. **Smain Amari** and **F. Seyfert,** RMC and INRIA, France, "New Development in the Synthesis and Design of Microwave Filters of Arbitrary Bandwidth"
4. **K Zaki, C. Wang,** University of Maryland, USA, "Dielectric Resonator and LTCC Filters"
5. **Jen-Tsai Kuo,** National Chiao Tung University, Taiwan, "Microwave Planar Filter Technologies"
6. **G. Macchiarella** and **S. Tamiazzo,** Politecnico di Milano, Milano, Italy, "Advanced Filter Technologies for Wireless Base Stations"
7. **Ming Yu,** COM DEV, Canada, "Advanced Filter/Multiplexer Technologies for Satellite Transponders"
8. **Ian Hunter,** University of Leeds, UK, "Advanced Tunable and Reconfigurable Filters"
9. **Vicente E. Boria-Esbert, Carlos P. Vicente-Quiles,** University of Valencia, Spain "Prediction Models of RF Breakdown Effects in Passive Components for Satellite Payloads"

IMS SPONSORED MONDAY WORKSHOPS

08:00 AM-05:00 PM

WMA: SiGe HBTs Towards THz Operation

Reviewed by: **MTT-4, MTT-7, MTT-11**
Organizers: **Paulius Sakalas,** TU Dresden, Germany, and FPL Semiconductor Physics Institute, Lithuania; **Michael Schroter,** RFnano Corporation and UC San Diego, USA

08:00 AM-05:00 PM

WMB: Advances in Photovoltaic Solar Cell Technology and its Possible Applications in Microwave Communications Systems as an Energy Source

Reviewed by: **MTT-4, MTT-10, MTT-16**
Organizers: **Aly E. Fathy,** University of Tennessee; **Samir El-Ghazaly,** National Science Foundation; **Fuad Abulfotuh,** University of Alexandria

08:00 AM-05:00 PM

WMC: Recent Advancements and Challenges in mm-Wave Applications and Systems

Reviewed by: **MTT-6, MTT-12, MTT-16**
Organizers: **Amin Rida,** Georgia Institute of Technology; **Manos Tentzeris,** Georgia Institute of Technology; **ae-Seung Lee,** Toyota Research Institute North America

08:00 AM-05:00 PM

WMD: New Microwave Devices and Materials Based on Nanotechnology

Reviewed by: **MTT-15, IMS2010**
Organizers: **Luca Pierantoni,** Università Politecnica delle Marche, Ancona, Italy; **Fabio Coccetti,** LAAS-CNRS Toulouse, France; **Christophe Caloz,** École Polytechnique de Montréal, Montréal, Canada; **George W. Hanson,** University of Wisconsin-Milwaukee, WI, USA

08:00 AM-12:00 PM

WME: High-Power-Density Packaging of Gallium Nitride

Reviewed by: **MTT-5, MTT-6, MTT-12**
Organizers: **Rüdiger Quay,** Fraunhofer Institute Applied Solid-State Physics, Freiburg; B**ernie Geller,** Vadum Inc, North Carolina; **Frank Sullivan,** Raytheon Company

01:00 PM-5:00 PM

WMF: High Efficiency High Power Microwave Amplifiers for High Data Rate Space Communications

Reviewed by: **MTT-5, MTT-7, MTT-16**
Organizers: **Dr. Kavita Goverdhanam,** U.S. Army – CERDEC, Fort Monmouth, NJ; **Dr. Rainee N. Simons,** NASA Glenn Research Center, Cleveland, OH

08:00 AM-12:00 PM

WMG: Ultra-high Speed Microwave and Photonic Devices and Systems: How Will They be Tested?

Reviewed by: **MTT-3, MTT-11**
Organizers: **Stavros Iezekiel,** University of Cyprus; **Ron Reano,** Ohio State University

08:00 AM-05:00 PM

WMH: 3D Microwave and Millimeter-Wave Packaging

Reviewed by: **MTT-6, MTT-12**
Organizers: **John A. Pierro,** Telephonics Corporation, USA ; **Debabani Choudhury,** Intel Corporation, USA

08:00 AM-05:00 PM

WMI: Making Reliable Measurements at Millimeter and Submillimeter Wavelengths

Reviewed by: **MTT-4, MTT-11**
Organizers: **Nick Ridler,** National Physical Laboratory (NPL), UK; **Andrej Rumiantsev,** SUSS MicroTec Test Systems GmbH, Germany

08:00 AM-05:00 PM

WMJ: Recent Advances in Reconfigurable Filters

Reviewed by: **MTT-8, MTT-21**
Organizers: **Dimitrios Peroulis,** Purdue University; **Raafat Mansour,** University of Waterloo

08:00 AM-05:00 PM

WMK: RF MEMS for Antennas and Integrated RF Front End

Reviewed by: **MTT-14, MTT-16, MTT-21**
Organizers: **John Papapolymerou,** Georgia Institute of Technology; **Art Morris,** WiSpry; **Hector De Los Santos,** NanoMEMS Research; **James C. Hwang,** Lehigh University

IMS SPONSORED FRIDAY WORKSHOPS

08:00 AM-12:00 PM

WFA: The Expanding Role of GaN in RF Systems

Reviewed by: **MTT-5, MTT-6, MTT-16**
Organizers: **Jim Sowers,** Space Systems/Loral; **Jay Banwait,** Northrop Grumman

08:00 AM-12:00 PM

WFB: Wireless Power Transmission

Reviewed by: **MTT-5, MTT-16, IMS2010**
Organizers: **Debabani Choudhury,** Intel Corporation; **John A. Pierro,** Telephonics Corporation

08:00 AM-05:00 PM

WFC: Millimeter-Wave SiGe/CMOS and III-V Chips for Imaging Systems

Reviewed by: **MTT-4, MTT-6, MTT-16**
Organizers: **Gabriel M. Rebeiz,** University of California, San Diego; **Sorin Voinigescu,** University of Toronto; **Vipul Jain,** Sabertek

08:00 AM-05:00 PM

WFF: New Theories, Applications and Practices of Electromagnetic Field Simulators

Reviewed by: **MTT-1, MTT-15**
Organizers: **Zhizhang (David) Chen,** Dalhousie University, Canada; **Poman So,** University of Victoria, Canada

08:00 AM-05:00 PM

WFG: Emerging Optical Modulator Technologies for RF Photonics

Reviewed by: **MTT-3, MTT-16, IMS2010**
Organizers: **Ronald M. Reano,** Ohio State University; **Dieter Jäger,** Universität Duisburg-Essen

08:00 AM-12:00 PM

WFH: How to Start a Microwave Business

Reviewed by: **MTT-19, IMS2010**
Organizers: **Fred Schindler,** RF Micro Devices; **Mike Golio,** Golio Pubs

08:00 AM-12:00 PM

WFI: Practical Metamaterial RF and Antennas for Commercial Application

Reviewed by: **MTT-15, MTT-16, MTT-20**
Organizers: **Maha Achour,** RAYSPAN Corporation

IMS/ATRFG SPONSORED WORKSHOPS AND SHORT COURSES

(all workshops held in ACC)

Full Day **08:00am-05:00pm**

Coding	Room	Day	Description
SC-1	TBD	Sun	**Theory and Design of Phase Locked Loops** *Instructors:* **L.Dayaratna,** Lockheed Martin; **Dean Banerje**e, National Semiconductor; **Cicero S. Vaucher, NXP** Semiconductors; **P. White,** Applied Radio Labs; **Ron Reedy,** Peregrine Semiconductor
SC-2	TBD	Sun	**Low Phase Noise Oscillators: Lecture (Theory and Design) and Laboratory** *Instructor:* **Jeremy K.A. Everard,** BAE Systems/Royal Academy of Engineering Research Professor in Low Phase Noise Signal Generation, Department of Electronics, University of York, UK.

Half Day **08:00am-12:00pm**

Coding	Room	Day	Description
SC-2A	TBD	Sun	**Low Phase Noise Ocillators: Lecture Only** *Instructor:* **Jeremy K.A. Everard,** BAE Systems/Royal Academy of Engineering Research Professor in Low Phase Noise Signal Generation, Department of Electronics, University of York, UK.

Half Day **01:00pm-05:00pm**

Coding	Room	Day	Description
SC-3	TBD	Sun	**Mictowave Packaging and Manufacturing 101** Organizer: **lan Lindner,** L-3 Communications, Narda Microwave West MTT Affiliation: MTT-12

ADVANCE REGISTRATION

REGISTRATION CATEGORIES

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the **Early Bird Registration** period. It begins Tuesday, January 19th and will last through Friday, May 7th. This period provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird period is the 2nd tier or **Advance Registration** period. It extends from Saturday May 8th through Friday, May 21st, just prior to the start of **Microwave Week.** The 3rd and final tier is the **On-Site Registration** period that will remain the same as in past Symposia, starting on Saturday May 22nd, the first day of Microwave Week, and ending on Friday, May 28th.

Early Bird Period	January 19	May 7 (thru midnight PST)
Advance Period	May 8	May 21 (thru midnight PST)
On-Site Period	May 22	May 28 (throughout Microwave Week)

Symposium SUPERPASS

The Symposium **SUPERPASS**. For one low price, registrants can attend as many technical sessions as they can from any of the three contributing organizations, MTT, RFIC, and ARFTG, as well as attend one full-day workshop (or two half-day workshops, if desired). In addition, the **SUPERPASS** will allow you to attend the Awards Banquet on Wednesday and the Symposium Reception on Thursday.

The **SUPERPASS** is a **SUPER DEAL** offering a **15% discount** over the combined ala-carte pricing.

EARLY BIRD REGISTRATION

Please follow these instructions for completing the Early Bird Registration Form. Early Bird Registration rates provide significant savings from the on-site fees shown on the Registration form at the center of this Program Book and are available through midnight May 7th. Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and Exhibition Hall. This form is not used for guest tour registration, which is described elsewhere in this Program Book. Each registrant must submit a separate form with payment.

① METHODS OF REGISTRATION

Individuals can register online, by fax or by mail. All registrations must be accompanied with a payment; we accept Visa, MasterCard, American Express, and checks drawn from a U.S. bank. Registration forms received without a form of payment will be discarded. We do NOT accept phone registrations.

② PERSONAL INFORMATION

If you would like to receive information by email from the IEEE, MTT-S, or microwave companies, simply select the appropriate boxes. An optional complimentary badge for one guest allows access to the Hospitality Suite, Plenary Session, and Exhibition Hall, but does not allow access to Technical Sessions and Workshops.

③ MEMBERSHIPS

Check boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit www.ieeee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

④ **SYMPOSIA**

Microwave Week includes the IMS Technical program (www.ims2010.org), and Exhibition, as well as the RFIC Symposium (www.rfic2010.org), and ARFTG Conference (www.arftg.org).

Select the conference(s) you wish to attend. Students, Retiree's, and IEEE Life Members receive a discount on some registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full time student carrying a course load of at least nine credit hours.

- IMS Technical Sessions are held on Tuesdays, Wednesday, and Thursday. Registration includes continental breakfast, admission to the exhibits, abstract books, and a CD ROM.
- RFIC Technical Sessions are held on Monday and Tuesday. Registration includes continental breakfast, admission to the RFIC, Reception, and Exhibition
- ARFTG Technical Sessions are held on Friday. Registration includes breakfast, lunch, a CD-ROM, and admission the ARFTG Exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE Members.
- Microwave Week hosts the largest exhibition of its kind with over 400 companies. Exhibit only registration is available.

⑤ **EXTRA CD-ROMS AND DIGESTS**

Additional CD ROMS (IMS, RFIC, and ARFTG) and digests (RFIC only) are available for purchase and pickup at the conference. After the Symposium, these digests and CD ROMS will be available for purchase from IEEE.

⑥ **AWARDS BANQUET**

The MTT Awards Banquet will be held on Wednesday, May 26 from 6:30 to 10:00pm at the Hilton Anaheim. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

⑦ **BOXED LUNCHES**

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibition hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as on-site pricing will be higher. Refunds for lunches, however, will not be available since these are ordered in advance.

⑧ **WORKSHOPS**

The workshop fee includes a CD ROM and speaker's notes for that workshop. Full-day workshops include a continental breakfast, a morning refreshment break, a boxed lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, a morning refreshment break, and a boxed lunch. Afternoon workshops include a boxed lunch and an afternoon refreshment break. The All-Workshop DVD-ROM includes material for all RFIC and IMS workshops on one DVD-ROM, but the DVD-ROM price alone does not include admission to any workshops. Note that there are two other options for workshop registration. First, registrants can save by selecting a combined Workshop (one full-day or two half-day workshops) and All-Workshop DVD-ROM. And second, for those who might only be interested in the RFIC workshops, an All-RFIC Workshop-Only CD is offered.

⑨ **PAYMENT**

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express only). Bank drafts, wire transfers, cash, international money order, and purchase orders are unacceptable and will be returned. Personal checks must be encoded at the bottom with the bank, bank account number, and check number. Please make checks payable to ''2010 IEEE IMS''. Written requests for refunds will be honored if received by May 7, 2010. Refer to the Refund Policy for complete details.

ON-SITE REGISTRATION

ON-SITE REGISTRATION

On Site registration for all Microwave Week events will be available in the Anaheim Convention Center Lobby C. Registration hours are:

DAY	TIME
Saturday, May 22, 2010	02:00pm - 05:00pm
Sunday, May 23, 2010	07:00am - 06:00pm
Monday, May 24, 2010	07:00am - 06:00pm
Tuesday, May 25, 2010	07:00am - 06:00pm
Wednesday, May 26, 2010	07:00am - 06:00pm
Thursday, May 27, 2010	07:00am - 04:00pm
Friday, May 28, 2010	07:00am - 09:00am

EXHIBIT ONLY REGISTRATION

Exhibit-only registration is available.

GUEST TOUR REGISTRATION

Registration for guest tours will be available in the hospitality suite in the Garden Terrace Room at the Sheraton Park Hotel. Please refer to the Guest Tour Program section of this program book for further details and tour descriptions.

PRESS REGISTRATION

Credentialed press representatives are welcome to register without cost, receiving access to technical sessions and exhibits. Digests are not included. The Press Room will available from Tuesday thru Friday of Microwave Week.

ARFTG REGISTRATION

Late on-site registration will be available at the Anaheim Convention Center Lobby C on Friday from 7:00 to 9:00am. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

REFUND POLICY

Written requests received by May 7, 2010 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra CD-ROM's, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email address for the refund check. If registration was paid for by credit card, the refund will be made through an account credit. An account number must be provided if the initial registration was completed on-line. Address your requests to:

MTT-S REGISTRATION

Nannette Jordan
MP Associates
1721 Boxelder St. Ste. 107
Louisville, CO 80027
nannette@mpassociates.com

ON-SITE REGISTRATION (continued)

REGISTRATION FEES

On-site registration fees are as follows:

SUPERPASS	MEMBER	NON-MEMBER
All IMS, RFIC and ARFTG Sessions, Awards Banquet, Evening Social and all Workshop CD (RFIC/IMS) + Full Day (or 2 Half Day) Attendance	$1295	$1895
Student, Retiree, Life Member SuperPass	$745	
IMS		
All IMS Sessions	$525	$785
All IMS Sessions (No CD ROM)	$450	$665
Single Day Registration	$275	$385
Student, Retiree, Life Member All IMS Sessions	$85	
RFIC Symposium		
All RFIC Sessions	$270	$400
RFIC Reception Only	$65	$85
ARFTG Conference		
All ARFTG Sessions	$260	$390
Student, Retiree, Life Member All ARFTG Sessions	$160	
Exhibition Only		
Exhibition Only Pass	$25	$25
Extra CDs and Digests		
IMS CD ROM	$80	$150
RFIC Digest	$80	$150
RFIC CD ROM	$80	$150
ARFTG CD ROM	$80	$150
ARFTG Conference Compendium CD ROM 1982-2006	$65	$90
Evening Events		
Awards Banquet (Wednesday Night)	$75	$75
Evening Social (Thursday Night)	$20	$20
Box Lunches		
Lunches Per Day	$20	$20
Workshop and Short Courses		
Full Day	$205	$305
Half Day	$155	$230
Full Day Short Courses	$365	$540
Full Day Short Courses with/Lab	$415	$590
Half Day Short Courses	$275	$410
All Workshops DVD (RFIC/IMS)	$245	$355
All Workshops DVD (RFIC/MS) plus Full Day (or 2 Half Day) Workshop Attendance	$405	$595
All RFIC Workshop Only CD-ROMs (no attendance included)	$150	$210

UNITED STATES VISA ADVISORY

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment and pay fees. An interview is required as a standard part of processing for most visa applicants.
- Plan on having finger scans as part of the visa application process. Two index-finger scans are normally collected by the consular officer at the visa interview window. However; in some countries, they may be collected prior to the actual visa interview.

VISA WAIVER PROGRAM (VWP): Citizens of the following countries can travel to the U.S. without a visa for tourism or business for 90 days or less under the Visa Waiver Program (VWP) if they meet other travel requirements. As of June 26, 2005, all VWP travelers must have a machine-readable passport to enter the United States without a visa.

Andorra	France	Lithuania	Singapore
Australia	Germany	Luxembourg	Slovakia
Austria	Hungary	Malta	Slovenia
Belgium	Iceland	Monaco	South Korea
Brunei	Ireland	the Netherlands	Spain
Czech Republic	Italy	New Zealand	Sweden
Denmark	Japan	Norway	Switzerland
Estonia	Latvia	Portugal	United Kingdom
Finland	Liechtenstein	San Marino	

Some citizens of Canada and Bermuda do not need a visa to visit the United States. Contact your nearest U.S. embassy or consulate for guidance. Travelers should be aware that by requesting admission under the Visa Waiver Program, they are generally waiving their right to review or appeal a CBP (Customs and Border Protection) officer's decision as to their application for admission at the port of entry.

Effective January 20, 2010, the Department of Homeland Security is transitioning to enforced compliance of the Electronic System for Travel Authorization (ESTA) requirement for VWP travelers. Therefore, VWP travelers who have not obtained approval through ESTA should expect to be denied boarding on any air carrier bound for the United States. ESTA applications may be completed FREE online at the official DHS website, which is: https://esta.cbp.dhs.gov

PASSPORTS: A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, https:/www.cbp.gov, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

VISA LETTERS: A visa support letter can be provided for authors and registered attendees upon request. Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing. Spouses requiring visa assistance must be registered for an IMS Guest Program Event. Check the IMS 2010 website (www.ims2010.org) for Guest Program details. For additional assistance, please contact L.R. Whicker @ lrwassoc@carolina.rr.com

DISCLAIMER: This information is provided in good faith but travel regulations do change. The only authoritative sources of information are the U.S. Government websites at www.unitedstatesvisas.gov and http://travel.state.gov/visa/visa_1750.html.

TRANSPORTATION

FLYING TO ANAHEIM/ORANGE COUNTY:

Anaheim/Orange County has four nearby convenience airports to choose from:

JOHN WAYNE ORANGE COUNTY AIRPORT (SNA)

18601 Airport Way, Santa Ana, CA 92707 (949) 252-5200
Drive time: 20 minutes (13 miles/20.92km) to Anaheim

Approximate rates to & from Anaheim:

Shuttle Services:.....starting at $10 per person/one way
Disneyland Express Bus: .....$15 per person/one way
Taxi: metered rates:.....ranging from $45-$75 per car or van load/one way
Rental Car, Van or SUV:.....$50-$95 per car/daily
Limousine Service: .....approx. $115
Town car or SUV: .....approx. $85

LOS ANGELES INTERNATIONAL AIRPORT (LAX)

World Way, Los Angeles, CA 90045 (310)646-5252
Drive time: 50 minutes (35 miles/56.33km) to Anaheim

Approximate rates to & from Anaheim:

Shuttle Services:.....starting at $16 per person/one way
Disneyland Express Bus: .....$20 per person/one way
Taxi: metered rates:.....ranging from $90-$130 per car or van load/one way
Rental Car, Van or SUV:.....$50-$130 per car or van/daily
Limousine Service: .....approx. $160
Town car or SUV: .....approx. $100

LONG BEACH AIRPORT (LGB)

4100 Donald Douglas Dr., Long Beach, CA 90808 (562)570-2619
Drive time: 30 minutes (18 miles/28.97km) to Anaheim

Approximate rates to & from Anaheim:

Shuttle Services: .....starting at $35 for the first person + $9-10 each additional person/one way
Taxi: .....metered rates, ranging from $50-$80 per car or van/one way
Rental Car, Van or SUV:.....$75-$100 per car or van/daily
Limousine Service: .....approx. $110, per car/one way
Town car or SUV:.....approx. $90

ONTARIO INTERNATIONAL AIRPORT (ONT)

2500 Airport Dr., Ontario, CA 91761 (909)937-2700
Drive time: 45 minutes (36 miles/57.94km) to Anaheim

Approximate rates to & from Anaheim:

Shuttle Services..... starting at $43 for the first person + $9-10 each additional person/one way.
Taxi: metered rates:.....ranging from $95-$135 per car or van/one way.
Rental Car, Van or SUV: .....$45-$95 per car or van/daily.
Limousine Service: .....approx. $170
Town car or SUV: .....approx. $110

For more information on these airports and ground transportation please visit: www.anaheimoc.org

TRANSPORTATION (continued)

DRIVING DIRECTIONS TO THE ANAHEIM CONVENTION CENTER:

FROM POINTS NORTH

Take I-5 South. Take the HARBOR BLVD. exit. Keep RIGHT at the fork in the ramp. Merge onto S. HARBOR BLVD. Cross W. Katella Ave. Turn RIGHT onto CONVENTION WAY. Anaheim Convention Center is straight ahead.

FROM POINTS SOUTH

Take I-5 North. Take the KATELLA AVE. exit toward DISNEY WAY. Turn SLIGHT LEFT onto ANAHEIM WAY. Turn LEFT (west) onto E. KATELLA AVE. (becomes W. Katella Ave.) Turn LEFT onto S. HARBOR BLVD. Turn RIGHT onto CONVENTION WAY. Anaheim Convention Center is straight ahead.

FROM POINTS EAST

Take CA-91 West. Merge onto CA-57 South toward SANTA ANA. Take the KATELLA AVE. exit. Turn RIGHT (west) onto E. KATELLA AVE. (becomes W. Katella Ave.) Turn LEFT onto S. HARBOR BLVD. Turn RIGHT onto CONVENTION WAY. Anaheim Convention Center is straight ahead.

BUS AND RAIL INFORMATION ROUTES:

Local bus service is provided by Orange County Transportation Authority. OCTA can be reached at (714) 636-RIDE (7433) or www.octa.net/busrail. The following bus routes have stops near the Anaheim Convention Center (ACC):

Route 50 Long Beach – Anaheim via Katella Ave.: stops on W. Katella Ave. between S. Harbor Blvd. & West St., short walk South to Anaheim Convention Center entrance.

Route 205 Laguna Hills – Anaheim: stops on W. Katella Ave. between S. Harbor Blvd. & West St., short walk South to Anaheim Convention Center entrance.

Route 430 Anaheim Metrolink/Amtrak Station – Anaheim Resort: stops at S. Harbor & W. Katella Ave., and also stops at West St. & W. Katella Ave., short walk South to ACC.

AIR TRAVEL AND RENTAL CAR DISCOUNTS

For your convenience, airline tickets and car rentals may be booked through IEEE's corporate travel agency, World Travel Inc. Hours of operation are 08:00 to 17:30 EDT, Monday through Friday.

For more information please visit the IEEE Travel Program Website at www.ieee.org/web/aboutus/travel/index.htm

Email: ieee@worldtravelinc.com
Phone: +1 800.TRY.IEEE (+1 800.879.4333) in the US and Canada;
+1 717.556.1100 elsewhere

PLEASE REFERENCE IEEE's account 1iV9

SOCIAL EVENTS

SUNDAY, MAY 23, 2010

RFIC Reception • 07:00pm-09:00pm
Anaheim Convention Center, Room 213BCD

Immediately following the RFIC Plenary Session is the RFIC Reception to be held in adjacent ROOM 213BCD at the Anaheim Convention Center. This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

MONDAY, MAY 24, 2010

IMS 2010 Welcome Reception • 06:00pm-08:00pm
Hilton Hotel, Sunset Deck

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by IMS 2010.

TUESDAY, MAY 25, 2010

Special Luncheon for Chuck Swift • 12:00pm-02:00pm
Anaheim Convention Center, Room AR1 & 2

The IMS 2010 will hold a Special Luncheon on May 25, 2010, to celebrate Chuck Swift's 52 years of service in support of the Los Angeles Chapter of the Microwave Theory and Techniques Society. The chapter has sponsored monthly technical meetings since 1952 and periodic national/international 3-5 day meetings since 1970, such as the IMS meeting being held in Anaheim on May 23-28, 2010. Chuck formed his business, C. W. Swift & Associates, in July 1958. Since 1958, Chuck, his business and his family have supported 450 meetings and 7 IMS symposia. IMS 1989 stands out as the best performance, where Chuck put on a show of shows. The Luncheon will be held on Tuesday May 25 from 12:00 (noon) to 2:00 pm, in the Convention Center, in Rooms AR1 & 2 (near the Arena). The Luncheon is a full sit-down lunch.

Admission is $35 per person; sign-up is through the IMS 2010 Registration.

Women in Microwaves Engineering (WIM) Reception • 05:30pm-07:30pm
Uva Bar, 1580 Disneyland Drive, Downtown Disney

Meet with old friends as well as make new connections to the growing community of women who make a career in the field of high-technology. Enjoy good food, cool beverages and warm conversation at the WIM Social Event. Join us at the outside patio area of the Uva Bar in the center of the Downtown Disney entertainment district.

Student Reception • 07:00pm-09:00pm
Hilton Hotel, Room California B

Mix and mingle with fellow students from across the globe!

TUESDAY, MAY 25, 2010 (continued)

Ham Radio Social – 06:00pm-09:00pm
Hilton Hotel, California A

While enjoying a buffet and open bar, the attendees will have the opportunity to see the accomplishments of amateur radio operators who have skillfully designed and built transceivers for use from VHF to high millimeter wave bands. Some of these transceivers were made from surplus and commercially available components and some are state-of-the-art new designs including SDR. Several will be on display and their builders will be there to answer questions.

All conference attendees are welcome. You will find that amateur radio operators are utilizing their allocated frequency spectrum for very important uses and you may be interested in obtaining your license so you too can test your new designs and microwave propagation.

WEDNESDAY, MAY 26, 2010

Industry Hosted Cocktail Reception • 05:00pm-6:00pm
Anaheim Convention Center Exhibition Floor

Symposium Exhibitors will host a cocktail reception. Complimentary beverage tickets will be included in the registration packages.

MTT-S Awards Banquet • 07:00pm-10:00pm
Hilton Hotel, California Room

The MTT-S Awards Banquet includes a fine dinner, major society awards presentation, and entertainment. This years entertainment will be provided by String Theory. String Theory is an exceptional music performance drawing on the very space of the performance by transforming architecture into musical instruments and then playing the building. The result is a visually stunning landscape in which the performance unfolds. Tickets can be purchased at the time of registration.

THURSDAY, MAY 27, 2010

MTT-S STUDENT AWARDS LUNCHEON • 12:00pm-02:00pm
Hilton Hotel, California B

All students are invited to attend this luncheon which recognizes recipients of the MTT-S Undergraduate Scholarships, MTT-S Graduate Fellowships, IMS2010 Student Volunteers, IMS2010 Student Paper Awards, and the winners and participants of the IMS2010 Student Design Competitions.

MTT-S Graduates of the Last Decade (GOLD) Reception • 05:30pm-07:00pm
300 Anaheim

IEEE Graduates of the Last Decade (GOLD) was created in 1996 as a membership program to help students transition to young professionals within the larger IEEE community. MTT-S GOLD activities began at the IMS2007 meeting in Honolulu, HI. GOLD makes up approximately 10% of the MTT-S population and are a valuable part of the community. Join us for food, beverages and bowling at 300 Anaheim! Directions and additional information can be found at http://www.three-hundred.com/anaheim.html.

GUEST PROGRAM

HOSPITALITY SUITE: Enjoy Southern California hospitality by joining us in the Hospitality Suite in the Garden Room of the Sheraton Hotel. Grab your guest badge and come have breakfast in the morning or snacks later in the day. Meet friends, make friends, kick back and relax. There will be a special area for children with toys and games. Guest Tours will depart from the Hospitality Suite.Open Sunday, May 23 through Thursday, May 27 7:30am to 3:30pm.

GUEST TOURS / RECREATIONAL ACTIVITIES

Guests can register for the tours both online and at the Hospitality Suite located in the Garden Room at the Sheraton Park Hotel. To register for tours online please visit: http://www.pra-tours.com/IEEE.

LOS ANGELES COUNTY MUSEUM OF ART, PETERSEN AUTOMOTIVE MUSEUM & LA BREA TAR PITS — Sunday, May 23, 2010

Suggested Itinerary

10:00 AM ..... Depart Sheraton Park Hotel
11:30 AM ..... Arrive LACMA and Petersen – Free time to explore both museums
1:30 PM ..... Lunch at LACMA
2:30 PM ..... Arrive Page Museum and La Brea Tar Pits- guided tour
4:00 PM ..... Depart Museum
5:30 PM ..... Return to Sheraton Park Hotel

Time: **10:00 AM-5:30 PM** Price: **$125 per person**

NEWPORT HARBOR CRUISE — Sunday, May 23, 2010

Suggested Itinerary

1:30 PM ..... Depart Sheraton Park Hotel
2:00 PM ..... Newport Harbor Cruise
2:45 PM ..... Free time to explore Balboa Island
4:00 PM ..... Board coach and depart for hotel
4:30 PM ..... Return to Sheraton Park Hotel

Time: **1:30 PM-4:30 PM** ..... Price: **$64 per person**

QUIET ON THE SET! — Monday, May 24, 2010

Suggested Itinerary:

9:00 AM ..... Depart Sheraton Park Hotel
9:45 AM ..... Arrive Warner Bros. Studio
10:00 AM ..... Watch film on the Studio's history
10:30 AM ..... Docent guided tram tour
12:45 PM ..... Lunch at Warner Brothers cafeteria Commissary
1:45 PM ..... Depart Warner Bros. Studio
2:30 PM ..... Return to Sheraton Park Hotel

Time: **9:00 AM-2:30 PM** **Price: $138 per person**

A PRESIDENTIAL PEEK — Monday, May 24, 2010

Suggested Itinerary:

1:00 PM ..... Depart Sheraton Park Hotel
1:30 PM ..... Docent guided tour of the Nixon Library, based on (2) hours
3:30 PM ..... Free time on own at the Nixon Library
4:30 PM ..... Depart the Nixon Library
5:00 PM ..... Return to Sheraton Park Hotel

Time: **1:00 PM-5:00 PM** Price: **$60 per person**

IN VINO VERITAS - WINE COUNTRY OF TEMECULA — Tuesday, May 25, 2010

Suggested Itinerary:

8:15 AM ..... Depart Sheraton Park Hotel
9:45 AM ..... Ponte Winery
11:45 AM ..... Free time in the Visitor's Center
12:15 PM ..... Depart Ponte Winery
12:30 PM ..... Lunch and tasting at Wilson Creek Winery & Vineyards
2:30 PM ..... Free time in Visitor's Center
3:00 PM ..... Depart Temecula
4:30 PM ..... Return to Sheraton Park Hotel

Time: **8:15 AM-4:30 PM** Price: **$140 per person**

BRUSHSTROKES OF LAGUNA — Tuesday, May 25, 2010

Suggested Itinerary:

10:30 AM ..... Depart Sheraton Park Hotel
11:00 AM ..... Art walk with local artist, based on (1½) hours
12:30 PM ..... Free time for browsing and shopping in Laguna Beach
2:00 PM ..... Depart Laguna Beach
2:30 PM ..... Return to Sheraton Park Hotel

Time: **10:30 AM-2:30 PM** Price: **$96 per person**

THE GLITZ AND GLAMOUR . . . AN INSIDE LOOK — Wednesday, May 26, 2010

Suggested Itinerary:

10:00 AM ..... Depart Sheraton Park Hotel
11:00 AM ..... Arrive Hollywood, begin Historic Hollywood tour
12:15 PM ..... Tour ends – free time in Hollywood
1:00 PM ..... Depart Hollywood
1:15 PM ..... Lunch at uWink
2:15 PM ..... Free time on Rodeo Drive
3:30 PM ..... Depart for Hotel
4:30 PM ..... Return to Sheraton Park Hotel

Time: **10:00 AM- 4:30 PM** Price: **$108 per person**

WINDOWS OF DISCOVERY AT BOWERS MUSEUM

Wednesday, May 26, 2010

Suggested Itinerary:

11:15 AM ..... Depart Sheraton Park Hotel
11:30 AM ..... Free time at Bowers Museum
1:30 PM ..... Depart the Bowers Museum
1:45 PM ..... Return to Sheraton Park Hotel

Time: **11:15 AM-1:45 PM** Price: **$60 per person**

LANDMARKS OF LONG BEACH

Thursday, May 27, 2010

Suggested Itinerary:

8:45 AM ..... Depart from Sheraton Park Hotel
9:15 AM ..... Arrive Aquarium of the Pacific Self Guided Tour
10:45 AM ..... Depart for Queen Mary
11:00 AM ..... Arrive Queen Mary Self Guided Tour
12:00 PM ..... Lunch at Promenade Cafe
1:30 PM ..... Ghost and Legends Show
2:15 PM ..... Board coach and depart for hotel
2:45 PM ..... Return to Sheraton Park Hotel

Time: **8:45 AM-2:45 PM** Price: **$135 per person**

SECRETS OF THE SEA

Thursday, May 27, 2010

Suggested Itinerary:

9:00 AM ..... Depart Sheraton Park Hotel
9:30 AM ..... Arrive at Crystal Cove Beach Walk
11:30 AM ..... Board coach and depart for hotel
12:00 PM ..... Return to Sheraton Park Hotel

Time: **9:00 AM-12:00 PM** Price: **$97 per person**

THE GETTY CENTER

Friday, May 28, 2010

Suggested Itinerary:

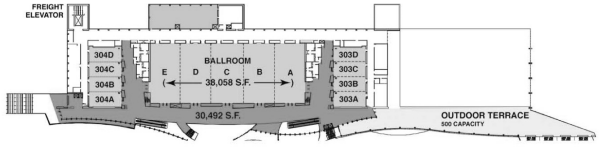
9:30 AM ..... Depart Sheraton Park Hotel
10:30 AM ..... Self-guided tour at the Getty Center, based on (3) hours Lunch on Getty Center lawn
1:30 PM ..... Depart the Getty Center
2:30 PM ..... Return to Sheraton Park Hotel

Time: **9:30 AM-2:30 PM** Price: **$81 per person**

ANAHEIM
ORANGE COUNTY
VISITOR & CONVENTION BUREAU

800 W. Katella Avenue | P.O. Box 4270
Anaheim, CA 92803 | 714.765.8888
meeting.inquiry@anaheimoc.org
anaheimoc.org

ANAHEIM
CONVENTION
CENTER



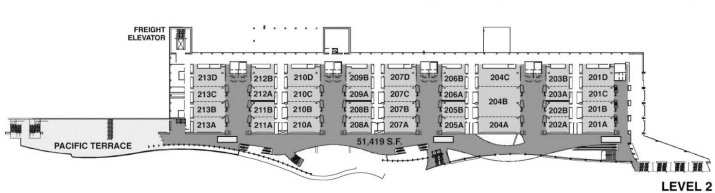
Specification Summary:

- Exhibit space: more than 800,000 sf
- Meeting & Ballroom space: 152,821 sf
- Prefunction areas: more than 200,000 sf

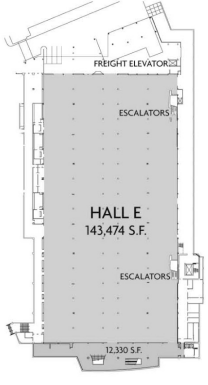
Exhibit Halls: 813,607 total sf

	Hall A	Hall B	Hall C	Hall D	Hall E
	718 10'x10' Booths 736 Total Booths	718 10'x10' Booths 736 Total Booths	759 10'x10' Booths 791 Total Booths	1140 10'x10' Booths	650 10'x10' Booths
Ceiling Heights	18' 6" – 24'	20' 6" – 25'	20' 6" – 25'	25'	13' 8"
Theater (Capacity)	12,000	12,250	12,900	15,000	N/A
Banquet (Capacity)	9,000	9,200	9,700	13,800	8,000

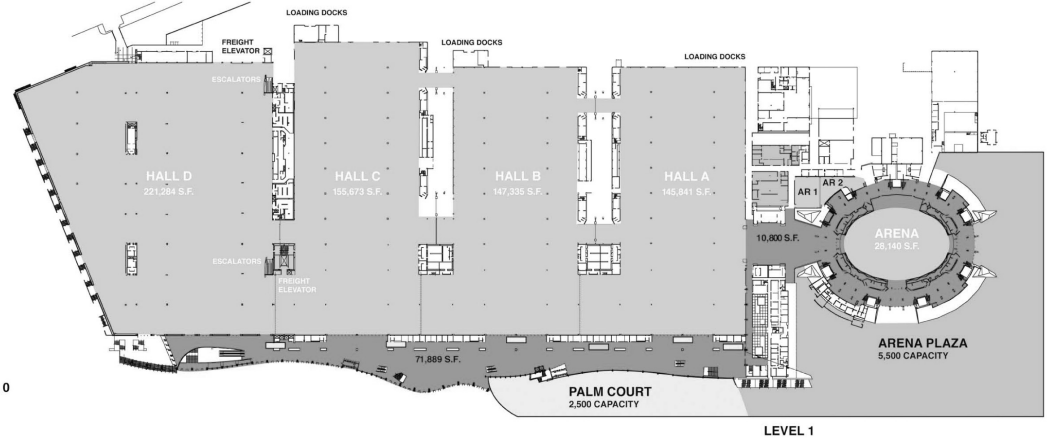
Specifications are subject to change. A copy of the Anaheim Convention Center "Policies, Rules and Regulations" is available upon request.



LEVEL 2



LEVEL 0



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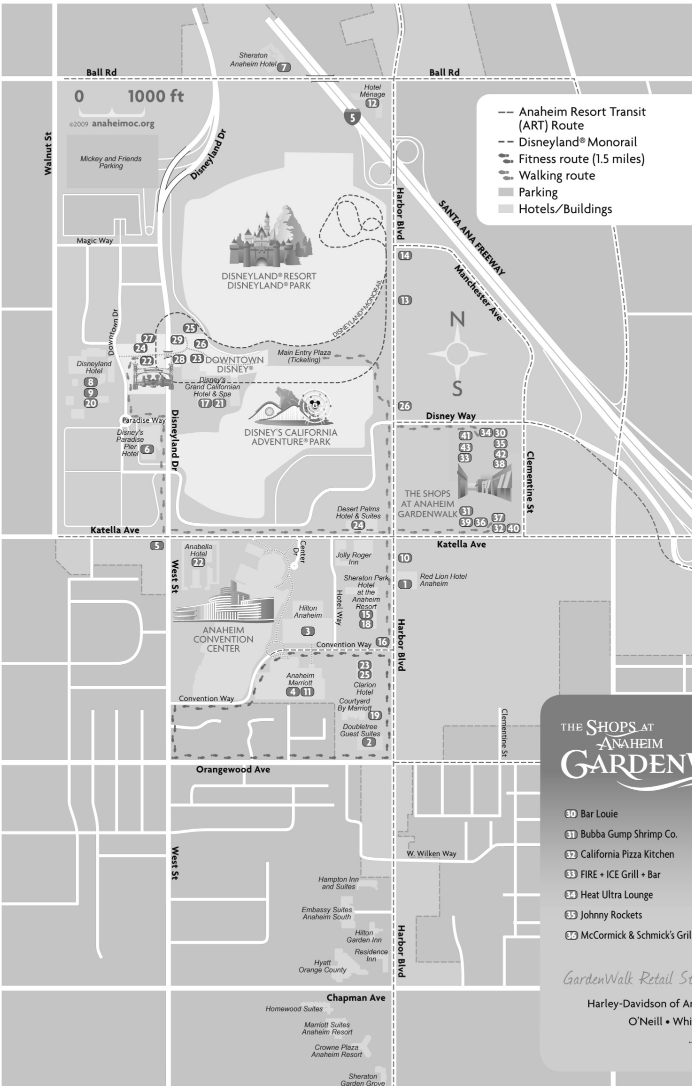


- Anaheim Resort Transit (ART) Route
- Disneyland® Monorail
- Fitness route (1.5 miles)
- Walking route
- Parking
- Hotels/Buildings

ANAHEIM
ORANGE COUNTY
VISITOR & CONVENTION BUREAU

Restaurants

1. 18 Fifty Bar and Grill
2. Agio Ristorante
3. Baja Fresh/Mix Restaurant Sbarro/Frozen Assets Yogurt
4. Café Del Sol
5. Coco's Bakery Restaurant
6. Disney's PCH Grill
7. Garden Court Bistro
8. Goofy's Kitchen
9. Hook's Pointe & Wine Cellar
10. IHOP
11. JW's Steakhouse
12. k'ya Anaheim
13. McDonald's
14. Mimi's Cafe
15. Molly's Kitchen
16. Morton's The Steakhouse
17. Napa Rose
18. Overland Stage Southwestern Grill & BBQ Company
19. Ruth's Chris Steak House
20. Steakhouse 55
21. Storyteller's Cafe
22. Tangerine Grill & Patio
23. The Mexicana Cafe & Cantina
24. The Sandbox Bar & Grille
25. Tivoli Gardens Café
26. Tony Roma's

Downtown Disney

22. AMC Theatre
23. Catal Restaurant & Uva Bar
24. ESPN Zone
25. House of Blues
26. Naples Ristorante e Pizzeria
27. Rainforest Cafe
28. Ralph Brennan's Jazz Kitchen
29. Tortilla Jo's

THE SHOPS AT ANAHEIM GARDENWALK

30. Bar Louie
31. Bubba Gump Shrimp Co.
32. California Pizza Kitchen
33. FIRE + ICE Grill + Bar
34. Heat Ultra Lounge
35. Johnny Rockets
36. McCormick & Schmick's Grille
37. P.F. Chang's China Bistro
38. Pop the Cork Wine Bar
39. Roy's Hawaiian Fusion Cuisine
40. The Cheesecake Factory
41. Cinemafusion 14/IMAX
42. 24 Hour Fitness
43. 300 Anaheim Bowling & Entertainment Center

GardenWalk Retail Stores

Harley-Davidson of Anaheim • Lux/Aveda Salon & Spa
O'Neill • White House/Black Market
...and more!

www.anaheimoc.org

Anaheim/OC Walking & Area Map

DINE+SHOP+PLAY

Stroll 1 block EAST on Katella

For more information and hours of operation please contact:

Anaheim/Orange County Visitor & Convention Bureau
(Located at the Anaheim Convention Center)
Phone: 714.765.8888
visitorinfo@anaheimoc.org
www.anaheimoc.org

For advanced restaurant reservations call 714-765-8899 ext 2000 or visit the kiosk located in the main lobby of the Anaheim Convention Center

Orange County California Beaches

Within a short drive from the Anaheim, Orange County's 42 miles of picturesque coastline offer colorful beach towns know for their artist havens, posh yacht harbors and trendy surf culture.

Seal Beach: Charismatic film location and northern gateway to coastal O.C. named after the seals that once frequented its coastline. (17 miles away)

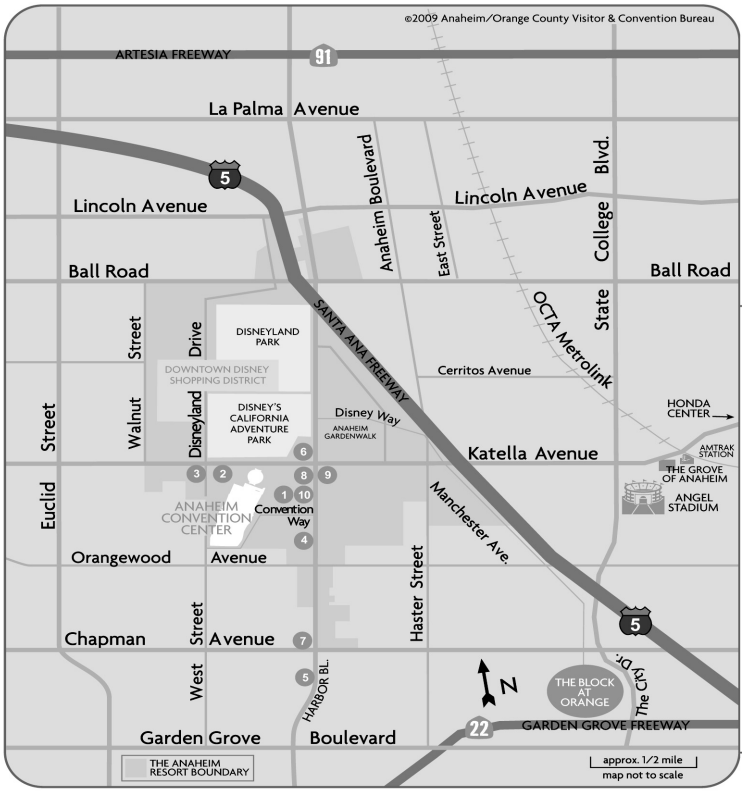
Huntington Beach: Surf City USA® embodies SoCal's surf culture. (24 miles away)

Newport Beach: Home of the largest small-craft yacht harbor in the U.S., as well as the body boarding mecca "Wedge." (18 miles away)

Laguna Beach: Home to several notable festivals, the city's coastline has inspired artists since the late 1800's. (28 miles away)

Dana Point: Rich marine life, aquatic fun and California history– named after famous author Richard Henry Dana. (33 miles away)

San Clemente: Spanish-style architecture throughout this quaint beach. (36 miles away)



RFIC Attendee Hotels

1. Hilton Anaheim Headquarter Hotel
2. Anabella Hotel
3. Best Western Stovall's Inn
4. Clarion Hotel Anaheim Resort
5. Crowne Plaza
6. Desert Palms
7. Hyatt Regency Orange County
8. Portofino Inn & Suites
9. Red Lion Anaheim Maingate Hotel
10. Sheraton Park Hotel at the Anaheim Resort

IEEE
468 Walden Trail
Waxhaw, NC 28173

2010 RFIC Symposium
Anaheim, CA
May 23-25, 2010

PROGRAM