



**2009 IEEE Radio Frequency  
Integrated Circuits Symposium  
Boston, Massachusetts  
June 7-9, 2009**



**IEEE**

# **PROGRAM**

**Boston Convention and Exhibition Center**

*Sponsored by*  
**IEEE Microwave Theory and Techniques Society  
IEEE Electron Devices Society  
and  
The IEEE Solid-State Circuits Society**



## **RFIC Plenary and Reception Sunday Night (June 7, 2009)**

After a busy day of outstanding RFIC Workshops (see page 10-55) the Plenary Session and RFIC Reception will be held on Sunday evening – June 7, 2009. These activities are the highlight of technical activities include the Plenary Session at 5:30pm in the Westin Boston Waterfront Hotel, Grand Ballroom A. The Plenary Session will include two outstanding speakers (See page 8-9) and the Student Paper Award ceremony. Immediately following the RFIC Plenary Session at 7:00pm is the RFIC Reception in the Westin Boston Waterfront Hotel, Grand Ballroom B & C. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The Reception is sponsored by the RFIC Steering Committee and Platinum Sponsors:



# cā d e n c e

### **RFIC Week Activities (June 6-10)**

#### **Saturday June 6, 2009**

02:00pm - 06:00pm Registration – BC&EC

#### **Sunday June 7, 2009**

07:00am - 06:00pm Registration – BC&EC

07:00am - 09:00am Attendee Breakfast – BC&EC, Room 258AB

08:00am - 05:00pm Workshops and Tutorials – BC&EC

05:30pm - 06:40pm RFIC Plenary – WBWH, Grand Ballroom A

07:00pm - 09:00pm RFIC Reception – WBWH, Grand Ballroom B & C

#### **Monday June 8, 2009**

07:00am - 05:00pm Registration – BC&EC

07:00am - 09:00am Attendee Breakfast – BC&EC, Room 258AB

08:00am - 05:10pm RFIC Technical Sessions (see pages 10-41)

08:00am - 09:40am RM01A RM01B RM01C RM01D

10:10am - 11:50am RM02A RM02B RM02C RM02D

01:20pm - 03:00pm RM03A RM03B RM03C RM03D

03:30pm - 05:10pm RM04A RM04B RM04C RM04D

#### **Tuesday June 9, 2009**

07:00am - 05:00pm Registration – BC&EC – BC&EC, Room TBD

07:00am - 09:00am Attendee Breakfast – BC&EC, Room 253ABC

08:00am - 04:00pm RFIC Oral and IF Technical Sessions (see pages 42-55)

08:00am - 09:20am RTU1A RTU1B RTU1C

10:20am - 11:40am IRTU2A, RTU2B, RTU2C

01:20am - 02:40pm RTU3A RTU3B RTU3C

02:00pm - 04:00pm RTU1F

This Program can be found on the RFIC website <http://www.rfic2009>. IMS sessions and exhibits are held on Tuesday - Thursday. IMS program can be found on the IMS website [www.ims2009.org](http://www.ims2009.org).

# TABLE OF CONTENTS

The RFIC Symposium will be held in Boston Massachusetts at the Boston Convention & Exhibition Center On June 7-9, 2009 in conjunction with the International Microwave Symposium. It opens Microwave week 2009, the largest RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF Systems, circuit device, and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Table of Contents . . . . .	p. 1
Message from General Chair . . . . .	p. 2
Message from Technical Program Chair . . . . .	p. 3
Steering Committee . . . . .	p. 4
Advisory Board . . . . .	p. 4
Executive Committee . . . . .	p. 4
Technical Program Committee . . . . .	p. 5
RFIC Schedule 2009 . . . . .	p. 6-7
Plenary Session . . . . .	p. 7-9
Session: RMO1A: Cellular IC I . . . . .	p. 10-11
Session: RMO1B: Advanced Millimeter-Wave Circuits . . . . .	p. 12-13
Session: RMO1C: Broadband IC I . . . . .	p. 14-15
Session: RMO1D: Transformer Based VCOs . . . . .	p. 16-17
Session: RMO2A: RFID and Low-Power Wireless Applications . . . . .	p. 18-19
Session: RMO2B: High-Frequency CMOS RF Receivers . . . . .	p. 20-21
Session: RMO2C: PA Modulator Components . . . . .	p. 22-23
Session: RMO2D: RF Modeling and Design Automation . . . . .	p. 24-25
Session: RMO3A: Cellular IC II . . . . .	p. 26-27
Session: RMO3B: 60-GHz Phased Arrays . . . . .	p. 28-29
Session: RMO3C: Handset PA's & Concepts . . . . .	p. 30-31
Session: RMO3D: Advanced VCO Topologies . . . . .	p. 32-33
Session: RMO4A: WLAN and WiMax . . . . .	p. 34-35
Session: RMO4B: RF Front End Building Blocks . . . . .	p. 36-37
Session: RMO4C: Frequency Generation Circuits: PLLs and Synthesizers . . . . .	p. 38-39
Session: RMO4D: Submicron RFIC MOS and Novel Devices . . . . .	p. 40-41
Session: RTU1A: Broadband PA's and MIMO . . . . .	p. 42
Session: RTU1B: New Ideas in CMOS RF Front-End Circuits . . . . .	p. 43
Session: RTU1C: Advanced Device Characterization and Non-Linear Circuit Analysis . . . . .	p. 44
Session: RTU2A: Wideband and Direct Digital Frequency Synthesizers . . . . .	p. 45
Session: RTU2B: Millimeter-Wave Imaging and Communication Systems . . . . .	p. 46
Session: RTU2C: Broadband IC II . . . . .	p. 47
Session: RTU3A: Millimeter-Wave VCOs . . . . .	p. 48
Session: RTU3B: Integrated Filters for RF Applications . . . . .	p. 49
Session: RTU3C: On-wafer Wireless Testing and Passive RFIC Components . . . . .	p. 50
Session: RTUIF: Interactive Forum . . . . .	p. 51-55
Panel Sessions . . . . .	p. 56-58
Workshops and Short Courses . . . . .	p. 59-70
Registration Information . . . . .	p. 71-74
Social Events . . . . .	p. 75-76
Guest Programs . . . . .	p. 77-79
BC&EC Floor Plans . . . . .	p. 80

# Message from the General Chair



**Tina Quach**

On behalf of the Steering Committee, I would like to welcome you to the RFIC Symposium!

The 2009 RFIC Symposium maintains its reputation as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development for wireless and wireline communication ICs. Running in conjunction with the International Microwave Symposium and Exhibition, the RFIC Symposium adds to the excitement of Microwave Week with three days focused exclusively on RFIC technology and innovation. The RFIC symposium will be held at the Boston Convention Center, June 7-9, 2009. The symposium begins on Sunday, June 7th with workshops targeted at RF technology, design, and system issues. The workshop organizers have put a

strong emphasis in future RF integration, as well as a variety of

Power Amplifier designs including CMOS technology; advanced design techniques for mobile handsets and different solutions for PA and TX architectures. Don't miss out on this great opportunity to expand your horizons! Sunday evening activities continue at 5:30pm with RFIC Plenary Session at the Westin Water Front Hotel, Grand Ballroom A. Two renowned speakers will share their views on the direction and challenges that the RF IC industry will be facing. The first speaker, Christopher Snowden, Ph.D., Vice-Chancellor and Chief Executive of the University of Surrey, Guildford, UK, will discuss "Cost-effective Semiconductor Technologies for RF and Microwave Applications." The second speaker, George W. Everhart, CEO of Alien Technology Corporation, will cover "Real-world RFID deployments: What makes them work?" Following the Plenary Session, the RFIC Reception will be hosted in the Westin Water Front Hotel, Grand Ballroom B and C. This social event is a key component of the conference with the opportunity to connect with old friends and new acquaintances and catch up on the wireless industry.

The technical program includes oral sessions, an Interactive Forum (poster session), and two exciting lunch panel sessions. The oral presentation sessions start on Monday, June 8th with four parallel sessions of five papers per session throughout the morning and the afternoon. The oral sessions continue on Tuesday, June 9th with four papers per session and one hour break to synchronize with the IMS technical Program. The poster session will be held on Tuesday afternoon. The poster session is the perfect place to have an opportunity to have more detailed technical discussions with the authors. Panel Sessions are also planned at lunch time on Monday and Tuesday. The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall.

The RFIC organization is thankful to the IMS2009 team, without whom we could not make this conference successful. Most of all, we are particularly thankful to all the technical contributors to the RFIC Symposium. We look forward to your participation. Please continue to make this conference so vibrant within the wireless industry!

I look forward to seeing you in Boston!

Tina Quach  
General Chair  
2009 IEEE RFIC Symposium

## Message from the Technical Program Committee Chairs



Yann Deval



David Ngo

On behalf of the Technical Program Committee, welcome to the 2009 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. This is a leading-edge IEEE technical conference dedicated to the advancement of integrated circuits and sub-systems for RF, wireless, broadband communications, and many other emerging applications. The RFIC Technical Program

Committee has worked diligently in selecting the best papers and assembling an excellent quality technical program this year. The symposium's main features include tutorial workshops, Plenary, Interactive Forum and several technical sessions. There will also be a student paper contest. The three best student papers will be selected by the Technical Program Committee and the awards will be presented in the Plenary Session. This year the RFIC Symposium begins on Sunday, June 7th with workshops at the advanced and tutorial level addressing RF technology, design and integration, at both system and circuit levels. The Plenary Session will be held on Sunday evening, following the workshops. The RFIC Reception will follow immediately after the plenary session, providing a relaxing time for all to mingle with old friends and catch up on the latest news. In addition to the technical sessions on Monday and Tuesday, the RFIC Symposium also features two exciting panel sessions and many workshops. Monday's lunch panel session entitled "Who will win the battle for the gigabit wireless in your home: Wireless HD, 802.11n, Wireless USB, or UWB?" has panelists from both industry and academia debating the future of high data rate wireless networks. Tuesday's lunch panel session, "60GHz CMOS radio: reality or fiction?" is posed to stimulate interactive discussions with the audience. The workshops on Sunday cover a wide range of topics from system to device technologies.

The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to make the RFIC Symposium the venue of choice for both industry and academia to meet, discuss results and exchange ideas. The 2009 RFIC Technical Program Committee will keep working tirelessly toward the goal of strengthening the technical quality and scope of the program, while maintaining and improving the legacy left by the previous Symposia. This would not be possible without holding the interest of professionals like you and gaining the trust of all the authors who submitted their work to the RFIC Symposium.

We hope you enjoy the 2009 RFIC Symposium!

Yann Deval and David Ngo  
Technical Program Chairs  
2009 IEEE RFIC Symposium

## **Steering Committee**

Tina Quach, Freescale Semiconductor Inc., *General Chair*

Yann Deval, Univ. of Bordeaux, IMS Labs, *TPC Chair*

David Ngo, RFMD, *TPC Co-Chair*

Jacques C. Rudell, Univ. of Washington, *Finance Chair*

Bertan Bakaloglu, Arizona State Univ., *Workshops Chair*

Kevin McCarthy, Univ. College Cork, *Digest & CD ROM Chair*

Albert Jerng, Ralink, *Publicity Chair*

Yuhua Cheng, SHRIME Peking Univ., *Panel Sessions Chair*

Albert Wang, UC Riverside, *Transactions/Guest Editor*

Kevin Kobayashi, RFMD, *Student Papers Chair*

Brian Floyd, IBM, *Secretary*

Noriharu Suematsu, Mitsubishi Electric, *Asia Pacific Liaisons*

Luciano Boglione, Univ. of Massachusetts, *IMS Liaisons*

Takao Inoue, Univ. of Texas, Austin, *Webmaster*

Larry Whicker, LRW Associates, *Conference Coordinator*

## **Advisory Board**

Natalino Camilleri • Fazal Ali • Eliot Cohen

Reynold Kagiwada • Sayfe Kiaei • Louis Lou

David Lovelace • Vijay Nair • Steve Lloyd

## **Executive Committee**

Joseph Staudinger • Stefan Heinen • Luciano Boglione

Jenshan Lin • Tina Quach

## **SSCS Liaison**

Kenneth O

# Technical Program Committee

- Fazal Ali, *Qualcomm*  
 Walid Ali-Ahmad, *MediaTek Singapore*  
 Kirk Ashby, *Microtune, Inc.*  
 Bertan Bakkaloglu, *Arizona State University*  
 Jean-Baptiste Begueret,  
*University of Bordeaux, IMS Lab*  
 Didier Belot, *ST Microelectronics*  
 Paul Blount, *Custom MMIC Design*  
 Georg Boeck, *TU Berlin,*  
*Microwave Engineering*  
 Luciano Boglione,  
*University of Massachusetts Lowell*  
 Natalino Camilleri, *Alien Technology*  
 Sudipto Chakraborty, *Texas Instruments*  
 Glenn Chang, *MaxLinear*  
 Jing-Hong Chen, *Analog Devices*  
 Nick Cheng, *Skyworks Solutions*  
 Yuhua Cheng, *Sbrime Peking University*  
 Stephen Dow, *ON Semiconductor*  
 Brian Floyd,  
*IBM T. J. Watson Research Center*  
 Ranjit Gharpurey,  
*University of Texas, Austin*  
 Aditya Gupta, *Anadigics*  
 Timothy Hancock, *MIT Lincoln Lab*  
 Andre Hanke,  
*Infineon Technologies AG*  
 Stefan Heinen,  
*Infineon Technologies AG*  
 Frank Henkel, *LMST GmbH*  
 Tian-Wei Huang,  
*National Taiwan University*  
 Stavros Iezekiel, *University of Leeds*  
 Lars Jansson,  
*Tumbledown Technical Inc.*  
 Albert Jerng, *Ralink*  
 Waleed Khalil, *Ohio State University*  
 Jaber Khoja, *Microtune, Inc.*  
 Sayfe Kiaei, *Arizona State University,*  
*Connection One*  
 Bumman Kim,  
*Pohang University of Science and Technology*  
 Kevin Kobayashi, *RF Micro Devices, Inc.*  
 Chang-Ho Lee, *Samsung*  
 Domine Leenaerts, *NXP Semiconductor*  
 Donald Y.C. Lie, *Texas Tech. University*  
 Fujiang Lin, *IME Singapore*  
 Jenshan Lin, *University of Florida*  
 Louis Liu, *Northrop Grumman Corporation*  
 Ting-Ping Liu,  
*Winbond Electronics, Shanghai*  
 David Lovelace, *ON Semiconductor*  
 Danilo Manstretta, *University of Pavia*  
 Kevin McCarthy, *University College Cork*  
 Srenik Mehta, *Atheros Communications*  
 Jyoti Mondal, *Freescale Semiconductor Inc.*  
 Stefano Pellerano, *Intel Corporation*  
 Sanjay Raman, *Virginia Tech*  
 Madhukar Reddy, *MaxLinear*  
 Bill Redman-White, *NXP Semiconductor*  
 Eli Reese, *TriQuint Semiconductor*  
 Mark Roberto, *Intel Corporation*  
 Francis Rotella,  
*Peregrine Semiconductor*  
 Jacques Rudell, *University of Washington*  
 Carlos Saavedra,  
*Queen's University Walter, Canada*  
 Derek Shaeffer, *Beceem Communications, Inc.*  
 Osama Shana'a, *MediaTek Corporation*  
 Eddie Spears, *RFMD*  
 Joseph Staudinger, *Freescale Semiconductor Inc.*  
 Bob Stengel, *Motorola*  
 Noriharu Suematsu, *Mitsubishi Electric*  
 Julian Tham, *Arda Technologies*  
 Bruce Thompson, *Motorola Labs*  
 Freek van Straten, *NXP Semiconductor*  
 Albert Wang,  
*University of California, Riverside*  
 Patrick Yue,  
*University of California, Santa Barbara*  
 Gary Zhang, *Skyworks Solutions*

## RFIC Schedule 2009

The RFIC Symposium will be held in Boston, MA in the Boston Convention & Exhibition Center (BC&EC). The headquarters hotel is the Westin which is adjacent to the BE&EC. The RFIC Plenary and Reception will be held on Sunday June 7 starting at 5:30pm.

The RFIC Symposium is held as part of Microwave week. The RFIC Symposium is followed by the IMS Symposium and Exhibition and by ARFTG. Attendees of RFIC are invited to attend the IMS Plenary Session which will be held on Monday evening, June 8, 2009.

### Saturday June 6 2009

02:00pm - 06:00pm      Registration – BC&EC

### Sunday June 7, 2009

07:00am - 06:00pm      Registration – BC&EC  
07:00am - 09:00am      Attendee Breakfast – BC&EC, Room 258AB  
08:00am - 05:00pm      Workshops and Tutorials – BC&EC  
05:30pm - 06:40pm      RFIC Plenary – Westin Hotel, Grand Ballroom A  
07:00pm - 09:00pm      RFIC Reception – Westin Hotel, Grand Ballroom B & C

### Monday June 8, 2009

07:00am - 05:00pm      Registration – BC&EC  
07:00am - 09:00am      Speakers Breakfast – BC&EC, Room TBD  
07:00am - 09:00am      Attendee Breakfast – BC&EC, Room 253ABC  
07:00am - 05:00pm      Speakers Prep Room – BC&EC, Room TBD  
08:00am - 05:10pm      RFIC Technical Sessions (see pages 10-41)  
08:00am - 09:40am      RM01A, RM01B, RM01C, RM01D  
09:40am - 10:10am      Break  
10:10am - 11:50am      RM02A, RM02B, RM02C, RM02D  
11:50am - 01:20pm      RFIC Panel and Lunch  
01:20pm - 03:00pm      RM03A, RM03B, RM03C, RM03D  
03:00pm - 03:30pm      Break  
03:30pm - 05:10pm      RM04A, RM04B, RM04C, RM04D  
05:30pm-06:45pm      IMS Plenary Session



## **RFIC Schedule** (Continued)

### **Tuesday June 9, 2009**

07:00am - 05:00pm	Registration – BC&EC, Room TBD
07:00am - 09:00am	Speakers Breakfast – BC&EC, Room TBD
07:00am - 09:00am	Attendee Breakfast – BC&EC, Room 253ABC
07:00am - 05:00pm	Speakers Prep Room – BC&EC, Room TBD
08:00am - 04:00pm	RFIC Oral and IF Sessions (see pages 42-55)
08:00am - 09:20am	RTU1A, RTU1B, RTU1C
09:20am - 10:20am	Break and IMS Exhibit
10:20am - 11:40am	RTU2A, RTU2B, RTU2C
11:40am - 01:20pm	RFIC and IMS Panels, and IMS Exhibit
01:20pm - 02:40pm	RTU3A, RTU3B, RTU3C
02:00pm - 04:00pm	RTU1F
02:40pm - 03:40pm	Break and IMS Exhibits

## **Plenary Schedule**

### **Sunday, June 7, 2009**

**05:30 PM**

#### **Westin Hotel – Grand Ballroom A**

#### **Session RSU5A: RFIC Plenary**

Chair: Tina Quach, Freescale Semiconductor Inc.

Session Co-Chairs: Yann Deval, University of Bordeaux,

IMS Lab

David Ngo, RFMD

- |         |                                                                                                                                                |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 05:30pm | Welcome message from General and TPC Chairs, Announcement of Student Paper Awards                                                              |
| 05:45pm | <b>RSU5A-1:</b> Cost-Effective Semiconductor Techniques for RF and Microwave Applications, <b>Christopher M. Snowden</b> , Univ. of Surrey, UK |
| 06:15pm | <b>RSU5A-2:</b> Real World RFID Developments: What Makes them Work <b>George W. Everhart</b> , Allen Technology Corp.                          |



## Plenary Speaker 1:

Christopher M. Snowden –  
Vice-Chancellor and Chief Executive,  
University of Surrey, Guildford. Surrey. UK

### **Cost-effective Semiconductor Technologies for RF and Microwave Applications**

**Abstract:** Microwave systems designers have a wide choice of semiconductor technologies for applications up to 100 GHz. While there is a natural tendency to choose integrated silicon as the technology of choice for most RFIC applications below 2 GHz and for many applications at higher frequencies, there are many other options available which can offer cost-competitive and performance-enhancing solutions.

This presentation will examine the current state-of-the-art in microwave and RF semiconductor technologies set against economic pressures which demand the lowest cost solution while meeting technical performance requirements, reliability and reproducibility. The presentation will examine factors affecting the wafer cost or equivalent die cost for various microwave technologies and the significance of mask set costs for some choices. The need for high yields and larger diameter wafer technology to reduce die costs led to 6" (150mm) wafer diameters becoming an industry standard for compound semiconductors.

The presentation will conclude by offering some insight into emerging technologies and their potential performance advantages for microwave and RF applications.

### **About Christopher M. Snowden:**

Christopher Snowden is Vice-Chancellor and Chief Executive of the University of Surrey, Guildford, UK and a microwave engineer with wide experience of the international microwave and semiconductor industry.

He is currently a non-executive Director of Intense Ltd, which designs and manufactures photonic products such as laser arrays for the professional printing industry. He is also an advisor to DMD Ltd and Filtronic plc. He has previous experience as a Non-Executive of several other technology companies.

Prior to his appointment at Surrey he was Chief Executive Officer of Filtronic ICS. He joined Filtronic plc in 1998 as Director of Technology before being promoted to Joint Chief Executive Officer in 1999.

Professor Snowden is a Member of the UK's Council of the Engineering and Physical Sciences Research Council, the UK's Engineering and Technology Board (ETB), the Defence Scientific Advisory Council, the Board of Universities UK (UUK), and Deputy-President of the Institute of Engineering and Technology. He is Vice-President of the Royal Academy of Engineering and Chair of the Engineering Policy Committee.

Professor Snowden is a Fellow of the Royal Society, Fellow of the Royal Academy of Engineering, Fellow of the IEEE, a Fellow of the IET and a Fellow of the City and Guilds Institute. He was awarded the Royal Academy of Engineering's Silver Medal in 2004 for his 'outstanding contributions to the microwave semiconductor industry'. He was a Distinguished Lecturer for the IEEE Electron Devices Society for seven years until 2005. He was awarded the 1999 Microwave Prize of the IEEE Microwave Theory and Techniques Society.



## Plenary Speaker 2:

George W. Everhart –  
Chief Executive Officer,  
Alien Technology Corporation

### **Real-world RFID Deployments: What Makes Them Work**

**Abstract:** Although there have been a variety of RFID pilots that have failed to reach a full implementation, there have been many real-world deployments which have been fully deployed and are providing a strong improvement in efficiency and effectiveness, netting a sound ROI. This talk will site a couple of examples of these successful deployments and recount some characteristics, both technical and otherwise, that are critical for these successes. These examples will also provide insight as to some of the remaining challenges for broad industry adoption.

### **About George W. Everhart**

George W. Everhart joined Alien in January 2007. Mr. Everhart has over 25 years of executive leadership experience with specific expertise in leading high growth phases of industry leading technology companies. Everhart has held CEO and sales and marketing executive positions with both small startup companies in emerging markets, and large multinational companies, experiencing a rapid pace of growth. He has extensive experience in global markets as well as the domestic U.S. market.

Everhart recently held CEO positions with early stage startup companies, SealedMedia and Onesecure, where he led successful company funding and expansion and established both companies as recognized leaders in their markets. Previously, Everhart was Sr.VP, Worldwide Sales & Service for 3COM Corporation, managing the Americas, Asia/Pacific, and EMEA (Europe, Middle East & Africa) business activities as well as the 1,000 person global service organization. Prior, Everhart was President & CEO, Fujitsu PC Corporation, where he led the company's market entry and rapid growth in the notebook PC business. Everhart also held a series of executive leadership positions with Apple Computer during the company's fast growth years, 1987-1996, including VP US Sales, VP & GM PC Business Division, and VP Business & Government Sales. Everhart's early career included marketing, sales, and business management positions with The Braegen Corporation and Memorex Corporation.

Mr. Everhart has been active in industry, government, and education associations as well holding both board and advisory positions. He was a member of the "Highway One Committee" to assist in the automation of Congress. He currently is a member of the Board of Fellows at Santa Clara University.

Mr. Everhart holds a Bachelors degree in Psychology, and a Masters degree in Business Administration from Santa Clara University.

**Monday June 8, 2009**  
**08:00 AM**  
**BC&EC - Room 204AB**  
**Session: RM01A: Cellular IC I**  
Chair: Didier Belot, ST Microelectronics  
Co-Chair: Andre Hanke, Infineon

**RM01A-1      8:00 AM**

**RF Receiver Front-End with +3dBm Out-of-Band IIP3 and 3.4dB NF in 45nm CMOS for 3G and Beyond**

Naveen K. Yanduru\*, Danielle Griffith\*, Kah-Mun Low\*, Poras Balsara\*\* \*Texas Instruments Inc., Dallas, TX 75243, USA, \*\*The University of Texas at Dallas, Richardson, TX 75080, USA

**Abstract:** A receiver front-end in 45nm standard CMOS is presented. The receiver achieves WCDMA system performance without an inter-stage SAW filter. High out-of-band linearity is achieved by reducing the RF circuitry and filtering the blockers after direct conversion. For the receiver at 1.9GHz, a +3.1dBm IIP3 is achieved for blockers that are 40MHz and 80MHz away from the RF carrier. NF is 3.4dB, IIP2 is +51dBm and current is 19.5mA for I,Q paths. LO is provided using on chip VCO and quadrature divider.

**RM01A-2      8:20 AM**

**A SAW-Less CDMA Receiver Front-End with Single-Ended LNA and Single-Balanced Mixer with 25% Duty-Cycle LO in 65nm CMOS**

Himanshu Khatri\*, Li Liu\*\*, Tony Chang\*\*, Prasad S. Gudem\*\*, and Lawrence E. Larson\*,  
\*University of California San Diego, La Jolla, CA, 92093, USA, \*\*, Qualcomm Inc., San Diego, CA, 92121, USA

**Abstract:** A fully integrated SAW-less direct conversion CDMA receiver with single-ended LNA and modified single-balanced passive mixer is manufactured in a 65 nm digital CMOS process. The measured receiver gain at 1.96 GHz was 37 dB, NF was 3 dB, IIP2 was (TB) was 65 dB.

### **RM01A-3      8:40 AM**

#### **A 0.13- $\mu$ m CMOS Multi-Band WCDMA/HSDPA Receiver Adopting Silicon Area Reducing Techniques**

Hyunwon Moon, Juyoung Han\*, Seung-Il Choi, Dongjin Keum\*, Byeong-Ha Park MSC Design Team, System LSI, Samsung Electronics, Korea, \*RF Development Team, System LSI, Samsung Electronics, Korea

**Abstract:** A multi-band WCDMA/HSDPA direct-conversion receiver to cover all six 3GPP bands is implemented in a 0.13 $\mu$ m CMOS process. The proposed integrated inductor structure and the mixed-type DC offset correction technique are very useful to reduce the increase of silicon area generated by realizing a multi-band multi-mode RF transceiver. The measured full-path receiver performance is NF of <3dB, IIP3 of >-17dBm, and IIP2 of >+30dBm for all six bands. The current consumption is about 45mA at 2.8V supply.

### **RM01A-4      9:00 AM**

#### **A Tunable 300-800MHz RF-Sampling Receiver Achieving 60dB Harmonic Rejection and 0.8dB Minimum NF in 65nm CMOS**

Z. Ru, E. Klumperink, C. Saavedra\*, B. Nauta University of Twente, Netherlands, \*Queen's University, Canada

**Abstract:** A 300-800MHz CMOS radio receiver aiming at software-defined radio is proposed. It exploits an LNA preceded by a tunable LC filter with one external coil to achieve voltage amplification for low NF and low-pass filtering to improve the 3rd and 5th harmonic rejection of an RF-sampling receiver to >60dB. The balun-LNA provides partial IM3 compensation, to drive a wideband sampling downconverter. The measured gain is 22-28dB while NF ranges from 0.8-4.3dB. The core consumes 6mW and clock takes 12mW.

### **RM01A-5      9:20 AM**

#### **The First Experimental Demonstration of a SASP-based Full Software Radio Receiver**

F. Rivet\*, Y. Deval\*, JB. Begueret\*, D. Dallet\*, P. Cathelin\*\*, D. Belot\*\* \*IMS Laboratory, 351 Cours de la Liberation, 33405 Talence Cedex, France, \*\*STMicroelectronics, Central R&D, 38926 Crolles Cedex, France

**Abstract:** This paper presents the principles of a Sampled Analog Signal Processor (SASP) dedicated to Software Radio mobile device. The SASP aims to select a spectral envelope of a RF signal among all RF signals. It processes analogically the RF signal spectrum. It replaces the classical mixing and filtering operations. It dramatically reduces the A/D conversion frequency from GHz to MHz frequencies. Design strategy, applications and for the very first time, measurements are presented.

**Monday June 8, 2009**

**08:00 AM**

**BC&EC - Room 205A**

**Session: RM01B: Advanced Millimeter-Wave Circuits**

Chair: Paul Blount, Custom MMIC Design Services

Co-Chair: Kevin Kobayashi, RFMD

**RM01B-1 8:00 AM**

**Current Combining 60GHz CMOS Power Amplifiers**

M. Bohsali and A. M. Niknejad BWRC, University of California at Berkeley

**Abstract:** Two 60GHz power amplifiers are presented in standard 90nm CMOS using integrated power combining and matching networks. The power amplifiers incorporate 4-way/2-way power splitters and combiners into their matching networks rather than using separate structures, and achieve 1dB output power of 12.1/10.1 dBm and saturation output power of 14.2/11.6 dBm respectively with saturation efficiency of 18.1/17.7% respectively when operated with a 1V supply.

**RM01B-2 8:20 AM**

**60GHz 45nm PA for Linear OFDM Signal with Predistortion Correction achieving 6.1% PAE and -28dB EVM**

E. Cohen\*, S. Ravid\*, D. Ritter\*\* \*Mobile Wireless Group, Intel Haifa, Israel, \*\*Electrical Engineering Technion, Haifa, Israel

**Abstract:** 45nm CMOS 60 GHz PA optimized for linear modulation with 6dbm saturated power and 13dB gain is presented when biased at 70uA/um. A maximum PAE of 19.4% 8dBm Psat and 18dB gain is achieved for 200uA/um bias point. The PA was tested using a digital predistortion algorithm and OFDM packets, and achieved PAE of 6.1% with -28dB EVM and 9% with -20dB EVM at output powers of -2dBm and +1dBm respectively.

### **RM01B-3      8:40 AM**

#### **60GHz and 80GHz Wide Band Power Amplifier MMICs in 90nm CMOS Technology**

N. Kurita, H. Kondoh Central Research Laboratory, Hitachi, Ltd., Japan

**Abstract:** 60GHz and 80GHz-band power amplifier (PA) MMICs have been developed on a standard 90nm CMOS technology for use in RF front-ends of wide-band, low-cost communication and/or radar systems. Two PAs have three- and five-stage single-ended architectures, respectively. Under 1.0V bias supply, they have achieved saturation powers  $P_{sat}$  of 12.6dBm and 10.3dBm with linear gains of 10.0dB and 12.2dB, respectively, the highest  $P_{sat}$  reported to our best knowledge.

### **RM01B-4      9:00 AM**

#### **Low-Loss 0.13- $\mu$ m CMOS 50-70 GHz SPDT and SP4T Switches**

Y. A. Atesal, B. Cetinoneri, G. M. Rebeiz, University of California, San Diego

**Abstract:** This paper presents 50-70 GHz tuned  $\lambda/4$  single-pole double-throw (SPDT) and single-pole four-throw (SP4T) switches in a 0.13 $\mu$ m CMOS process. High substrate resistance is used for low insertion loss. The SPDT and SP4T switches result in a measured insertion loss of 2.0 and 2.3 dB at 60 GHz, with an isolation of > 32 dB and > 22 dB, respectively. To our knowledge, this paper presents the lowest loss 60 GHz SPDT and SP4T switches and the highest isolation SPDT switch in any CMOS technology to-date.

### **RM01B-5      9:20 AM**

#### **A Tunable Flipflop Based Frequency Divider up to 113GHz in SiGe:C Bipolar Technology**

S.Trotta\*, J. John\*\* \*Freescale Semiconductor Inc., Schatzbogen 7, D-81829 Munich, Germany,

\*\*Freescale Semiconductor Inc., 2100 East Elliot Road, 85284, Tempe, AZ, USA

**Abstract:** We present a tunable flipflop based frequency divider designed in a 200GHz fT SiGe bipolar technology. A new technique for tuning the sensitivity of the divider in the frequency range of interest is presented. The new technique also allows increasing the maximum toggle frequency of the divider. The chip is operational from 60GHz up to the record frequency of 113GHz. At 125°C the maximum speed is 96GHz. At a 3.3V power supply, the circuit, including the output buffer, consumes 35mA.

**Monday June 8, 2009**  
**08:00 AM**  
**BC&EC - Room 206AB**  
**Session: RM01C: Broadband IC I**  
Chair: Chris Rudell, Univ. of Washington  
Co-Chair: Ranjit Gharpurey, Univ. of Texas, Austin

**RM01C-1      8:00 AM**

**A DC-102GHz Broadband Amplifier in 0.12 $\mu$ m SiGe BiCMOS**

Joohwa Kim and James F. Buckwalter, Department of Electrical and Computer Engineering, University of California, San Diego, CA, 92093, USA

**Abstract:** RM0-1 An ultra-wideband amplifier scheme is realized with two cascaded stages that are equalized for high-bandwidth and low gain ripple. The amplifier is implemented in a 0.12 $\mu$ m SiGe BiCMOS process and achieves a 3dB bandwidth of 102GHz. The gain is 10dB with less than 1.5dB gain-ripple and group-delay variation under +/- 6ps over the entire 3dB bandwidth. The chip occupies an area of 0.29mm<sup>2</sup> including the pads and consumes 73mW from a 2V supply.

**RM01C-2      8:20 AM**

**A 1.8mW Wideband 57dB $\Omega$  Transimpedance Amplifier in 0.13 $\mu$ m CMOS**

F. Aflatouni, H. Hashemi, Department of Electrical Engineering-Electrophysics, University of Southern California, Los Angeles, CA, USA

**Abstract:** In optical links for on-chip or chip to chip data transfer, system components should be designed to be low power while occupying small areas. This paper presents a low power transimpedance amplifier (TIA) that is suitable to operate up to 10Gb/s in presence of 370fF input capacitance. The 0.13 $\mu$ m CMOS TIA consumes 1.8mW to provide 57 dBohm transimpedance gain, while occupying 0.015 mm<sup>2</sup> area. The measured input referred current noise of the TIA is less than 30pA/sqrt(Hz) across 8 GHz.



### **RM01C-3      8:40 AM**

#### **1 - 10GHz Inductorless Receiver in 0.13 $\mu$ m CMOS**

Liuchun Cai, Ramesh Harjani, University of Minnesota, Minneapolis, MN 55455

**Abstract:** We describe inductorless wideband radio receiver architecture from 1GHz to 10GHz. Two receiver RF frontends designs are presented and compared: a traditional inductor peaking LNA and mixer (IPLM) and a capacitive peaking LNA and mixer circuit (CPLM). Measurement results indicate that CPLM has better linearity, comparable noise figure and uses only 17% more power. Silicon area for CPLM is only 22% of IPLM. Both designs can be mated with an inductorless PLL also shown here.

### **RM01C-4      9:00 AM**

#### **A 2Gbps RF-Correlation-Based Impulse-Radio UWB Transceiver Front-End in 130nm CMOS**

L. Zhou, Z. Chen, G.-C. Wang, F. Tzeng, V. Jain, and P. Heydari, University of California, Irvine

**Abstract:** The design of a carrier-less RF-correlation-based IR-UWB TRX front-end in 130nm CMOS is presented. Timing synchronization and coherent demodulation are implemented directly in the RF domain, enabling energy-efficient wireless communication at Gb/s data rates. Occupying mm<sup>2</sup> chip area, the TRX achieves a maximum data rate of 2Gbps and an RX sensitivity of -64dBm with a BER of 10<sup>-5</sup>, while requiring only 51.5pJ/pulse in the TX mode and 72.9pJ/pulse in the RX mode.

### **RM01C-5      9:20 AM**

#### **A Multi-modulation Low-power FCC/EC-compliant IR-UWB RF Transmitter in 0.18- $\mu$ m CMOS**

D. Barras, G. von Bueren, W. Hirt\*, H. Jaeckel, Electronics Laboratory, Swiss Federal Institute of Technology (ETH Zurich), 8092 Zurich, Switzerland, \*IBM Research, Zurich Research Laboratory, 8803 Rüschlikon, Switzerland

**Abstract:** A multi-modulation RF transmitter IC intended for Impulse-Radio UWB is presented. The modulation rates extend up to 10Mpulses/s for BFSK, 500Mchips/s for shaped BPSK bursts and 1Gchips/s for unshaped BPSK bursts. This PLL-based TX achieves a power consumption of 81pJ/chip. The generated RF signals have spurious-free PSD and comply with U.S. and European regulations.

**Monday June 8, 2009**

**08:00 AM**

**BC&EC - Room 203**

**Session: RM01D: Transformer Based VCOs**

Chair: Timothy Hancock, MIT Lincoln Laboratory

Co-Chair: Tian-Wei Huang, National Taiwan University

**RM01D-1 8:00 AM**

**A 24 GHz Low Power VCO With Transformer Feedback**

C. A. Lin, J. L. Kuo, K. Y. Lin, H. Wang, Dept. of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan

**Abstract:** A K-band low power VCO fabricated by 0.13 $\mu$ m CMOS technology is developed. By employing a NMOS cross-coupled pair with a transformer feedback, low phase noise under low dc power condition can be achieved at higher frequency. The VCO exhibits a 2.2 GHz frequency tuning range. The output power and the phase noise at 1 MHz offset are -10 dBm and -113 dBc/Hz, respectively. The dc power consumption is 0.6 V/3 mW. To author's knowledge, this performance achieves the best FOM in CMOS K- band VCOs.

**RM01D-2 8:20 AM**

**A 1.7-mW, 16.8% Frequency Tuning, 24-GHz Transformer-Based LC-VCO using 0.18- $\mu$ m CMOS Technology,**

Y.-H. Kuo, J.-H. Tsai\*, T.-W. Huang, National Taiwan University, \*Yuan Ze University, Taiwan

**Abstract:** A low-power, wide-tuning-range voltage-controlled oscillator (VCO) using 0.18- $\mu$ m CMOS technology is presented in this paper. The proposed transformer-based LC-VCO has 16.8% frequency tuning range without switching techniques. To achieve wide-tuning- range and low-power in the same time, the current-reused topology is selected to demonstrate a low-power consumption of 1.7 mW. The VCO oscillation frequency at 22.6 GHz has a phase noise of -95dBc/Hz at 1 MHz offset.

### **RMO1D-3      8:40 AM**

#### **A 92.6% Tuning Range VCO Utilizing Simultaneously Controlling of Transformers and MOS Varactors in 0.13 $\mu\text{m}$ CMOS Technology**

Y. Takigawa, H. Ohta, Q. Liu, S. Kurachi\*, N. Itoh\*, T. Yoshimasu, Waseda University, \* Toshiba Corporation, Japan

**Abstract:** A Novel resonant circuit consisting of transformer-based variable inductors and MOS varactors is proposed to implement an ultra-wideband VCO IC. The VCO exhibits a frequency tuning range as high as 92.6 % spanning from 1.2 GHz to 3.27 GHz by simultaneously controlling the variable inductors and MOS varactors with a single control voltage. The measured phase noises at 1 MHz offset from the carriers are -124 dBc at 1.2 GHz and - 120 dBc at 3.1 GHz, respectively.

### **RMO1D-4      9:00 AM**

#### **1.1 to 1.9GHz CMOS VCO for Tuner Application with Resistively Tuned Variable Inductor**

S. J. Cheng, Y. Zheng\*, C. H. Heng, National University of Singapore, \*Institute of Microelectronics, Singapore

**Abstract:** A VCO is fabricated in 0.35 $\mu\text{m}$  CMOS technology for tuner application as a proof of concept for a novel method of resistively tuning the inductance of an LC VCO. By employing a transformer as inductor, L is varied by changing the secondary coil current using active resistors. This eliminates the need for using multiple inductors, resulting in large savings in area. It achieves a tuning range of 1.06 to 1.88GHz (56%) and phase noise of -116.1dBc/Hz. It draws about 6.8mA from a 3V supply.

### **RMO1D-5      9:20 AM**

#### **An Ultra-Low-Power CMOS Complementary VCO Using Three-Coil Transformer Feedback**

C.-K. Hsieh, K.-Y. Kao, and K.-Y. Lin, Graduate Institute of Communication Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, 10617, R.O.C

**Abstract:** A ultra-low-power VCO based on the complementary cross-coupled structure with the three-coil transformer feedback is proposed and realized in 0.18 $\mu\text{m}$  CMOS. This VCO has a 1 MHz offset phase noise of -118.5 dBc/Hz and consumes only 0.66 mW dc consumption. The FOM of this VCO is better than -195 dBc/Hz from 8.09 to 8.42 GHz, and the highest FOM of -198.6 dBc/Hz occurs at 8.2 GHz. The chip size is 530x430 $\mu\text{m}^2$ .

**Monday June 8, 2009**  
**10:10 AM**  
**BC&EC - Room 204AB**  
**Session: RMO2A: RFID and Low-Power Wireless Applications**

Chair: Natalino Camilleri, Alien Technology  
Co-Chair: Glenn Chang, MaxLinear

**RMO2A-1 10:10 AM**

**Software Configurable 5.8 GHz Radar Sensor Receiver Chip in 0.13 $\mu$ m CMOS for Non-contact Vital Sign Detection**

Changzhi Li, Xiaogang Yu, Dong Li, Lixin Ran, and Jenshan Lin, University of Florida, Zhejiang University

**Abstract:** A direct conversion 5.8 GHz radar sensor chip with 1GHz bandwidth was designed and fabricated. This radar sensor chip is software configurable to set the operation point and detection range for optimal performance. Important design issues for direct conversion on-contact vital sign detection sensors, such as the effect of baseband flicker noise and gain budget, have been discussed. Experiments have been performed successfully in lab environment to detect the vital signs of human subject.

**RMO2A-2 10:30 AM**

**An Asymmetric RF Tagging IC for Ingestible Medication Compliance Capsules**

H. Yu, C. M. Tang, R. Bashirullah, University of Florida, Gainesville, FL, USA

**Abstract:** An asymmetric RF tagging IC fabricated in 130nm CMOS is powered by low frequency AC signals inside biological equivalent phantom solutions to create externally detectable RF bursts in the 915MHz ISM band. Such a device can be attached to the outer surface of standard ingestible capsules as a cost-effective method for medication compliance monitoring.

### **RM02A-3      10:50 AM**

#### **A Novel CMOS Transmitter Front-end for Mobile RFID Reader**

Tongqiang Gao, Jingchao Wang, Chun Zhang, Baoyong Chi, Zhihua Wang Tsinghua University, Department of Electronic Engineering, Beijing, China

**Abstract:** In this paper, design considerations are expatiated to a novel structure of transmitter front-end for mobile RFID reader with 0.18 $\mu$ m CMOS process. The transmitter front-end consists of an up-conversion mixer, a linear PA and a non-linear PA. Controlled by the reader's working status, the implemented transmitter can provide high efficient carrier or highly linear ASK-modulation data at separate period. Test results verify the feasibility of the transmitter scheme.

### **RM02A-4      11:10 AM**

#### **A RF Transceiver with Auto Signal Detection and Combined PGA/RSSI**

#### **in 0.18 $\mu$ m CMOS for V2.1 Bluetooth Applications**

Wei-Yi Hu, Jia-Wei Lin, Kuo-Chi Tien\*, Yong-Hsiang Hsieh\*, Chao-Liang Chen\*, Hung-Ta Tso\*, Yi-Shun Shih\*, Shao-Chueh Hu\*, Sao-Jie Chen, National Taiwan University, \*MuChip Corp. Ltd.

**Abstract:** A RF front-end transceiver is implemented in 0.18 $\mu$ m CMOS for v2.1 Bluetooth application. All detections and calibrations are realized without baseband's feedback using an incoming GFSK signal detection, auto LNA gain mode selection and auto gain calibration with combined PGA/RSSI function. The DEVm performance of transmitter is less than 6% and a 7.5dB system NF is achieved in receiver. Continuous current consumption of RX and TX are 32mA and 42mA respectively from a 1.8V internal regulator.

### **RM02A-5      11:30 AM**

#### **An Ultra-Low-Power 868/915 MHz RF Transceiver for Wireless Sensor Network Applications**

R. van Langevelde, M. van Elzakker, D. van Goor, H. Termeer, J. Moss\* and A.J. Davie, Philips Research Europe, Eindhoven, The Netherlands, \*Philips Research UK, Cambridge, United Kingdom

**Abstract:** This paper describes an ultra-low-power transceiver operating in the 868/915 MHz frequency band using binary FSK at 45 kbit/s data rate. It achieves -89 dBm receiver sensitivity and -6 dBm transmit output power while consuming 1.6 mA and 1.8 mA, respectively, from a 1.2 to 1.5 V supply. It is fabricated in 0.13 $\mu$ m CMOS occupying 1.5 mm<sup>2</sup>, and it uses only 4 external components. The transceiver offers a small form factor, low cost and low power solution for wireless sensor network applications.

**Monday June 8, 2009**

**10:10 AM**

**BC&EC - Room 205A**

**Session: RMO2B: High-Frequency CMOS RF Receivers**

Chair: Walid Ali-Ahmad, MediaTek

Co-Chair: Sayfe Kiaei, Arizona State University

**RMO2B-1 10:10 AM**

**Low-Voltage, Inductorless Folded Down-Conversion Mixer in 65nm CMOS for UWB Applications**

S. K. Hampel, O. Schmitz, M. Tiebout\*, I. Rolfes, Leibniz Universität Hannover, Germany,

\*Infineon Technologies Austria AG, Austria

**Abstract:** The paper presents a low-voltage down-conversion mixer in 65nm CMOS for UWB applications. The inductorless folded circuit topology provides a peak gain of 14.5dB with 1dBm LO power and an 3dB-bandwidth from 1 to 10.5GHz. The input compression is better than -16.5dBm with an oIP3 of 7dBm at 2GHz. The circuit provides a minimum DSB noise figure of 6.5dB with a flicker-noise corner frequency of 2MHz. The mixer draws 12mA DC current from a 1.2V supply voltage resulting in a power dissipation of 14.4mW.

**RMO2B-2 10:30 AM**

**A 14-GHz CMOS Receiver with Local Oscillator and IF Bandpass Filter for Satellite Applications**

W. Chen, T. Copani, H. Barnaby, S. Kiaei, Connection One, Arizona State University, Tempe, AZ

**Abstract:** This paper presents a 14-GHz transformer-coupled receiver front-end with LO and IF band-pass filter for satellite applications. The monolithic transformer's parameters were optimized through theoretical analysis of the circuit performance. The system was fabricated in a 0.13 $\mu$ m CMOS process. The receiver conversion gain is 20dB and the NF is 7dB at 400-MHz IF frequency. The LO shows -112dBc/Hz@1MHz phase noise from a 14-GHz carrier. The IC draws 40 mA total current from a 1.2 V supply.

### **RM02B-3      10:50 AM**

#### **A Two-Channel Ku-Band BiCMOS Digital Beam-Forming Receiver for Polarization-Agile Phased-Array Applications**

B. Cetinoneri, Y. A. Atesal, G. M. Rebeiz, University of California, San Diego

**Abstract:** A 15 GHz two-channel receiver in 0.18- $\mu\text{m}$  SiGe BiCMOS process is presented for digital beam-forming applications. The receiver is based on a dual-down-conversion architecture and results in a channel gain of 47.1 dB at 15 GHz, a NF of 3.1 dB, and an OP1dB of -11 dBm. The channel-to-channel coupling is  $< -48$  dB. The chip consumes 70 mA (3.3 V) per channel and is 2.6x2.2 mm<sup>2</sup>, including pads. To our knowledge, this is the first high-performance Ku-band beam-forming chip in SiGe BiCMOS technology.

### **RM02B-4      11:10 AM**

#### **High Performance CMOS Receiver for Local Positioning Systems**

M. Krcmar, V. Subramanian, G. Boeck, Microwave Engineering Lab, Berlin Institute of Technology, Berlin, 10587, Germany

**Abstract:** A fully integrated CMOS receiver consisting of an LNA and a mixer has been designed and fabricated in IBM BiCMOS 7WL 180 nm technology. An on chip balun loading the second stage of the LNA was implemented as well for single to differential conversion. Excellent experimental results were demonstrated: a conversion gain (CG) of 28 dB, a noise figure (NF) of 3.3 dB and an input third order interceptionpoint (IIP3) of -11 dBm while consuming only 50 mW.

### **RM02B-5      11:30 AM**

#### **A CMOS Ku-band Single-Conversion Low-Noise Block Front-End for Satellite Receivers**

Z. Deng, J. Chen, J. Tsai, A. M. Niknejad, University of California at Berkeley, USA

**Abstract:** This paper presents a Ku-band single-conversion low-noise block front-end in a 0.18- $\mu\text{m}$  CMOS technology. The front-end down-converts the input signal from the Ku-band (10.5-13 GHz) to the L-band (0.75-2.25 GHz). The in-band noise figure is between 2.8 to 4.2 dB. It achieves a gain of 50 dB with -dB variation. The in-band OIP3 is above 17 dBm and output 1-dB compression point is above 9 dBm. The front-end consumes total of 75 mA from a 1.8 V supply. The die area is 0.8 x 1.8mm<sup>2</sup>.

**Monday June 8, 2009**

**10:10 AM**

**BC&EC - Room 206AB**

**Session: RM02C: PA Modulator Components**

Chair: Freek van Straten, NXP Semiconductors

Co-Chair: Joseph Staudinger, Freescale Semiconductor Inc.

**RM02C-1 10:10 AM**

**A Hybrid Envelope Modulator Using Feedforward Control for OFDM WLAN Polar Transmitter**

C. Lee, C. Chen and S. Wu, STC, ITRI, Taiwan, R.O.C.

**Abstract:** This paper presents a feedforward control for hybrid envelope modulator for applications in 802.11g OFDM WLAN polar transmitter. The feedforward control is constituted by hysteresis comparator and duplicate-linear amplifier that possess low power dissipation. For achieving high speed and high efficiency, the hybrid envelope modulator combines with a linear amplifier and a switch amplifier.

**RM02C-2 10:30 AM**

**A Spurious Emission Reduction Technique for Power Amplifiers Using Frequency Hopping DC-DC Converters**

J.-H. Chen, P.-J. Liu\*, Y.-J. E. Chen

Department of Engineering Science and Ocean Engineering, National Taiwan University, Taipei, Taiwan, \*Graduate Institute of Electronics Engineering, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan

**Abstract:** This paper presents a spurious emission suppression technique for RF power amplifiers using frequency-hopping DC-DC converters. The frequency-hopping technique changes the switching frequency of the DC-DC converter dynamically and reduces the peak spur created by using a DC-DC converter with a radio frequency power amplifier. The use of this technique can also reduce the size of the external passive components used for reducing the ripple voltage of the DC-DC converter.



### **RM02C-3      10:50 AM**

#### **A Highly-Linear Radio-Frequency Envelope Detector for Multi-Standard Operation**

J. Cha, W. Woo\*, C. Cho\*, Y. Park\*, C.-H. Lee\*, H. Kim\*\*, and J. Laskar, Georgia Institute of Technology, \*Samsung Design Center, \*\*Samsung Electro-Mechanics

**Abstract:** A highly-linear RF envelope detector for amplitude modulation of multiple wireless standards is presented. The RF envelope detector employs a differential voltage-to-current converter and a current-mode full-wave rectifier to enhance linearity of output envelope signal. It is shown that the proposed RF envelope detector linearly tracks 5-MHz sine-wave envelope at 1.9-GHz RF carrier as well as WCDMA and WiMAX envelopes at 1.95 GHz and 2.4 GHz, respectively.

### **RM02C-4      11:10 AM**

#### **A 1.55 GHz to 2.45 GHz Center Frequency Continuous-Time Bandpass Delta-Sigma Modulator for Frequency Agile Transmitters**

M. Schmidt, M. Grözing, S. Heck, I. Dettmann, M. Berroth, D. Wiegner\*, W. Templ\*, A. Pascht\*, University of Stuttgart, \*Alcatel-Lucent Bell Labs Stuttgart, Germany

**Abstract:** This paper presents a 4th order continuous-time bandpass delta-sigma modulator (CT-BPDSM) with a programmable center frequency ranging from 1.55 GHz to 2.45 GHz. The modulator is suited to be applied in multi-standard class-S power amplifiers. The circuit is implemented in a 200 GHz- $f_T$  SiGe-technology. The measured SNR at 2.2 GHz center frequency is 45.5 dB in a bandwidth of 20 MHz. The measured uplink UMTS-FDD ACLR of the modulator output signal is 48.4 dB in the first adjacent channel.

### **RM02C-5      11:30 AM**

#### **A 25-dBm High-Efficiency Digitally-Modulated SOI CMOS Power Amplifier for Multi-Standard RF Polar Transmitters**

S. Pornpromlikit, J. Jeong\*, C. D. Presti, A. Scuderi\*\*, and P. M. Asbeck, University of California at San Diego, \*Kwangwoon University, \*\*STMicroelectronics, s.r.l., USA

**Abstract:** A digitally-modulated power amplifier (DPA) is demonstrated in a 0.13- $\mu\text{m}$  SOI CMOS technology, to be used in a multi-standard RF polar transmitter. The amplitude modulation is done by digitally controlling the number of activated unit amplifiers whose currents are summed at the output. The measured DPA delivers a 24.9-dBm peak output power at 900 MHz with a maximum power efficiency of 62.7%. It also exhibits high-efficiency performance for other carrier frequencies with a reconfigured matching.

**Monday June 8, 2009**

**10:10 AM**

**BC&EC - Room 203**

**Session: RM02D: RF Modeling and Design Automation**

Chair: Kevin McCarthy, University College Cork

Co-Chair: Francis Rotella, Peregrine Semiconductor

**RM02D-1 10:10 AM**

**Effect of Substrate Contact Shape and Placement on RF Characteristics of 45 nm Low Power CMOS Devices**

Usha Gogineni, Hongmei Li\*, Susan Sweeney\*, Jing Wang\*\*, Basanth Jagannathan\*\*, Jesus del Alamo, Massachusetts Institute of Technology, Cambridge, MA, \*IBM Microelectronics, Essex Jct, VT, \*\*IBM Microelectronics, Hopewell Junction, NY

**Abstract:** The substrate resistance ( $R_{sx}$ ) of 45nm CMOS devices shows a strong dependence on the distance between the device edge and substrate ring and also on the number of sides the device is surrounded by the contact ring. Unilateral gain is modulated by  $R_{sx}$  and gate-body capacitance at low to medium frequencies ( $< 20\text{GHz}$ ) and by the  $R_{sx}$  to drain junction capacitance pole at mm wave frequencies. The impact of  $R_{sx}$  on  $f_T$ , maximum available gain, high frequency noise and power characteristics. minimal.

**RM02D-2 10:30 AM**

**Design and Modeling of Planar Transformer-based Silicon Integrated Passive Devices for Wireless Applications**

C.-H. Huang, T.-C. Wei, T.-S. Horng, S.-M. Wu\*, J.-Y. Li\*\*, C.-C. Chen\*\*, C.-C. Wang\*\*\*, C.-T. Chiu\*\*\*, and C.-P. Hung\*\*\*, National Sun Yat-sen University, National University of Kaohsiung\*, ITRI\*\*, Advanced Semiconductor Engineering\*\*\*, Taiwan

**Abstract:** This paper presents design and modeling techniques for Above-IC silicon process integrated passive devices (IPDs) that can be stacked with RF chips in a highly integrated 3D IC for wireless applications. The research starts to study modeling techniques for high efficiency planar transformers as near 90%. Based upon the proposed and modeled high-efficiency planar transformers, this paper explores novel designs of various passive devices including baluns, bandpass filters and power combiners.

### **RM02D-3      10:50 AM**

#### **Characterisation and Macro-modeling of Patterned Micronic and Nano-Scale Dummy Metal-Fills in Integrated Circuits**

S.Wane, D. Bajon\*, NXP Semiconductors Caen, France, \*ISAE/Toulouse University Toulouse, France

**Abstract:** A wideband characterization and macro-modeling of patterned micronic and nano-scale dummy metal-fill is presented and impacts of metal-fill topologies on electrical performances are investigated. The validity of the proposed macro-modeling methodology is demonstrated by comparison with high frequency measurement of test case structures including on-chip interconnects and RF inductive loops. Compact broadband SPICE models are derived using fully scalable closed-form semi-analytical expressions.

### **RM02D-4      11:10 AM**

#### **Mosaic Placement of Very High Density 3D Capacitors for Efficient Decoupling Functionality in the RF Domain**

O. Tesson, F. Le Cornec, S. Jacqueline, NXP Semiconductors Caen, France

**Abstract:** A layout driven approach used to fill empty space within MCM, with 3D high density decoupling capacitors is proposed. In a first time, a description of the innovative 3D unit cell is done based on process considerations. Then the method including the whole design flow is described and validated with the help of specific test cases and RF characterization data up to 6 GHz. A physical model is also proposed and implemented in the flow in order to compare simulated and measured data.

### **RM02D-5      11:30 AM**

#### **On Modeling Parasitic Control Loops in RF SoCs: RF Cross-Coupling and Spurious Analysis**

K. Muhammad, Chih-Ming Hung, Hunsoo Choo, Erkin Cubukcu, Texas Instruments Inc., Dallas, TX 75243

We address the issue of design verification of single-chip RF SOC's in the presence of unintentional cross-couplings and leakages due to proximity of aggressors and victims. We extend a previously presented VHDL based simulation methodology to allow building complex RF SOC's based on behavioral models. This approach has been successfully applied to investigate system behavior in the presence of aggressing nodes that create parasitic control loops due to unintentional and undesirable couplings.

**Monday June 8, 2009**  
**01:20 PM**  
**BC&EC - Room 204AB**  
**Session: RM03A: Cellular IC II**  
Chair: Jyoti P. Mondal, Freescale Semiconductor Inc.  
Co-Chair: Fazal Ali, Qualcomm

**RM03A-1 01:20 PM**

**Asynchronous Modulator for Linearization and Switch-mode RF Power Amplifier Applications**

T. Johnson, K. Mekechuk, D. Kelly, J. Lu, Pulsewave RF, Inc., USA

**Abstract:** An implementation of an asynchronous modulator which encodes a modulated RF signal into a two level pulse train is described. The modulator is designed for RF switch mode amplifier applications and feedback linearization using conventional linear power amplifiers. The modulator is implemented in 0.18 $\mu$ m SiGe BiCMOS and operates over a frequency range from 750 MHz to 2.2 GHz. Experimental results are shown for a power amplifier module where the modulator is configured in a feedback loop.

**RM03A-2 01:40 PM**

**A Low Power 100 MHz – 2.5 GHz Digital-to-Time Conversion Based Transmitter for Constant-Envelope Direct Digital Modulation**

Bob Stengel, S. A. Talwalkar, Tom Gradishar, Gio Cafaro, Motorola, Inc., Plantation, FL

**Abstract:** This paper reports a flexible direct digital modulation based low power transmitter in 90 nm CMOS that supports constant- envelope modulation using phase or frequency modulation for carrier frequencies from 100 MHz to 2.5 GHz with power drain of 130 mW and area of 0.7 mm<sup>2</sup>. For 8-PSK modulation upto 20 M symbol/s the RMS phase error is less than 4 deg. GSM phase error at 800-900 MHz and 1900 MHz is less than 1 deg RMS. APCO-25 FSK error is less than 2% from 150-900 MHz.

### **RM03A-3      02:00 PM**

#### **A 65nm CMOS Low-Noise Direct-Conversion Transmitter with Carrier Leakage Calibration for Low-Band EDGE Application**

S. F. Chen, Y. B. Lee, Eric Sun, B. J. Kuo, G. K. Dehng, MediaTek Inc., Taiwan.

**Abstract:** A low-noise EDGE transmitter implemented in a 65nm CMOS process using direct-conversion architecture for low-band application is presented. The transmitter consists of a programable-gain I/Q modulator, a frequency divider and a power director for carrier leakage calibration. The out-of-band noise at 20MHz offset is less than -163dBc/Hz. The carrier leakage after calibration can reach -50dBc. The design consumes 21mA at 1.5V supply and 40mA at 2.7V supply and is housed in a 40-pin CFN package.

### **RM03A-4      02:20 PM**

#### **A Low-Cost Quad-Band Single-Chip GSM/GPRS Radio in 90nm Digital CMOS**

K. Muhammad, C.-M. Hung, D. Leipold, T. Mayhugh, I. Elahi, I. Deng, C. Fernando, M.-C. Lee, T. Murphy, J. L. Wallberg, R. B. Staszewski, S. Larson, T. Jung, P. Cruise, V. Roussel, S.K. Vemulapalli, R. Staszewski, O.E. Eliezer, G. Feygin, K. Kunz, K. Maggio, Texas Instruments Inc., Dallas, TX 75243

**Abstract:** We present a quad-band single-chip GSM/GPRS radio in 90nm digital CMOS process based on the Digital RF Processor technology. This chip integrates all functions from physical layer to the protocol stack and peripheral support in a single RF SoC. The transceiver exceeds all 3GPP specifications demonstrating a receive NF of 1.8 dB and a margin of 8dB on TX spectral mask at 400 KHz offset in GSM850/900 bands. The transceiver is best-in-class in area and occupies only 3.8 mm<sup>2</sup> of silicon area.

### **RM03A-5      02:40 PM**

#### **A Multi-band High Performance Single-chip Transceiver for WCDMA/HSDPA**

C. S. Chiu\*, B. S. Heng\*\*, E. S. Khoo\*\*, S. R. Karri\*\*, B. J. Kuo\*, C. H. Shen\*, T. Y. Sin\*\*, C. Y. Wang\*, W. Yang\*\*, H. L. Zhang\*\*, Walid Y. Ali-Ahmad\*\*, C. L. Heng\*\*, G. K. Dehng\*, \*MediaTek Inc., Hsinchu, Taiwan, 300, R.O.C., \*\*MediaTek Singapore, Ayer Rajah, Crescent, Singapore 139964

**Abstract:** A multi-band single-chip RFIC has been implemented in 0.18μm SiGe BiCMOS process for WCDMA/HSDPA applications. The direct-conversion receiver achieves competitive system performance: -110.5dBm sensitivity, 20dB and 12dB blocking margin for ACS case 1 and case 2, respectively, and excellent in-band blocking margins. The direct-modulation transmitter achieves more than 90dB dynamic range, and excellent EVM performance: <3.5%. In Band I, the RX and TX sections draw each 35mA and 65mA, respectively.

**Monday June 8, 2009**  
**01:20 PM**  
**BC&EC - Room 205A**  
**Session: RM03B: 60-GHz Phased Arrays**  
Chair: Brian Floyd, IBM  
Co-Chair: Georg Boeck, TU-Berlin

**RM03B-1      01:20 PM**

**A Bidirectional TX/RX Four Element Phased-array at 60GHz with RF-IF Conversion Block in 90nm CMOS Process**

E. Cohen\*, C. Jakobson\*, S. Ravid\*, D. Ritter\*\*, \* Mobile Wireless Group, Intel Haifa, Israel, \*\* Electrical Engineering Technion, Haifa, Israel

**Abstract:** A 60 GHz 4 element bidirectional phased-array TX/RX chip with a 2 bit phase shifter and IF converter to/from 12GHz, using 90nm CMOS process, is described. The array features 7 dB gain, measured NF of 9 dB, IP1dB of -19dbm for RX, and output Psat of +3.5dBm for TX, drawing 60 mA from a 1.3-V supply. The RMS amplitude and phase error of the phase shifter is 0.7dB and 2deg max respectively from 57 to 66 GHz. Total die area 1.6x1mm<sup>2</sup> with half of the area being the IF converter block.

**RM03B-2      01:40 PM**

**A 60GHz Digitally-Controlled RF-Beamforming Receiver Front-end in 65nm CMOS**

Y.Yu, P.G.M. Baltus, A.J.M. de Graauw\*, E. van der Heijden\*, M. Collados\*, C. Vaucher\*, A.H.M. van Roermund, Eindhoven University of Technology, Eindhoven, The Netherlands; \*NXP Semiconductors, Research, Eindhoven, The Netherlands

**Abstract:** Phased arrays form a crucial step towards high data rate 60GHz wireless communication. This paper presents a fully integrated digitally controlled 60GHz RF-beamforming receiver front-end in CMOS. Using digitally controlled active phase shifters, each path of the scalable architecture achieves 10dB power gain, 7.2dB noise figure, a 360° phase shift range in 22.5° steps at 61GHz, and a 3dB-bandwidth of 5.4GHz, while only dissipating 78mW in each path. Chip area is 1.6mm<sup>2</sup>.

**RM03B-3      02:00 PM****A 60-GHz Band CMOS Phased Array Transmitter Utilizing Compact Baseband Phase Shifters**

S. Kishimoto, N. Orihashi, Y. Hamada, M. Ito, K. Maruhashi, NEC Corporation, Japan

**Abstract:** A 60-GHz band phased array transmitter is developed based on 90-nm CMOS process featuring compact baseband phase shifters with ideally zero power consumption. The phase shifter changes an RF signal phase every 90 deg by switching baseband signal paths. The transmitter has 6 RF front-ends and 6 phase shifters to implement beam steering function for a 1 x 6 array antenna system. By controlling phase shifters, the beam steering from 0 deg to 60 deg is observed.

**RM03B-4      02:20 PM****Embedded DiCAD Linear Phase Shifter for 57-65GHz Reconfigurable Direct Frequency Modulation in 90nm CMOS**

T. LaRocca, J. Liu, F. Wang, F. Chang, University of California at Los Angeles

**Abstract:** A digitally controlled artificial dielectric (DiCAD) differential transmission line is designed to perform agile linear phase shift over 100deg with thermometer-coded 16step control. It also operates with a 16 gain-step VGA to enable re-configurable and direct-frequency modulation at 60GHz with  $256^2$  states (1.1deg angular and 0.0007 magnitude resolutions) and -31dB static EVM for multiple PSK/QAM modulations. The modulator uses  $0.33\text{mm}^2$  core area in 90nm CMOS and consumes 10mA at 1V.

**RM03B-5      02:40 PM****60GHz Passive and Active RF-Path Phase Shifters in Silicon**

Ming-Da Tsai, Arun Natarajan\*

MediaTek Inc., Taiwan 300, R.O.C., \*IBM T.J. Watson Research Center, New York 10598

**Abstract:** Integrated 60-GHz active and passive phase shifters for RF-path phase-shifting phased array transceivers are demonstrated in this paper. The active and passive phase shifters are based on vector-interpolation and reflection-type architecture, respectively. Measurements over process and temperature are also discussed and comparisons are drawn between active and passive phase shifting approach for 60GHz phased arrays.

**Monday June 8, 2009**

**01:20 PM**

**BC&EC - Room 206AB**

**Session: RM03C: Handset PA's & Concepts**

Chair: Nick Cheng, Skyworks Solutions

Co-Chair: Eddy Spears, RF Micro Devices

**RM03C-1 01:20 PM**

**A Highly Efficient GSM/GPRS Quad-band CMOS PA Module**

C.-H. Lee, Y. Kim\*, J. J. Chang, K. S. Yang, K. H. An, I. Lee\*, K. Kim\*, J. Nam\*, H. Kim\*,  
Samsung Design Center, USA, \* Samsung Electro-Mechanics Corporation, Korea

**Abstract:** The highly efficient CMOS Power Amplifier Module (PAM) is designed for quad-band cellular handsets comprising GSM850, EGSM, DCS, PCS and supports Class 12 General Packet Radio Service (GPRS) multi-slot operation. This module integrates a power amplifier(PA) with a complete power control and protection in a standard RF CMOS process and also contains a high-Q integrated passive device (IPD) for an output-matching network guaranteeing high power-added efficiency (PAE).

**RM03C-2 01:40 PM**

**Scalable CMOS Power Devices with 70% PAE and 1, 2 and 3.4 Watt Output Power at 2GHz**

Mustafa Acar, Mark P. van der Heijden, Iouri Volokhine\*\*, Melina Apostolidou, Jan Sonsky\*\*, and Jan S. Vromans, NXP Semiconductors Research, Eindhoven, The Netherlands, \*\*, NXP-TSMC Research Center, Leuven, Belgium

**Abstract:** This paper reports RF power devices achieving 70% power-added efficiency (PAE) with 1, 2 and 3.4W output power at 2GHz. The power devices operate as sub-optimum class-E power amplifiers, having the advantage of 1.6 times higher output power with a slightly lower PAE than conventional class-E. The power devices use high voltage extended-drain NMOS (ED-NMOS) transistors in standard 65nm CMOS. A scalable layout design that we used preserves the high PAE for the various output power levels.

**RM03C-3 02:00 PM**

**Asymmetric Multilevel Outphasing Architecture for Multi-standard Transmitters**

SungWon Chung, Philip A. Godoy, Taylor W. Barton, Everest W. Huang, David J. Perreault, Joel L. Dawson, Massachusetts Institute of Technology, USA



**Abstract:** We describe a new outphasing transmitter architecture in which the supply voltage for each PA can switch among multiple levels. It is based on a new asymmetric multilevel outphasing (AMO) modulation technique which increases efficiency over a much wider output power range than the standard LINC system while maintaining high linearity. Simulations in 65nm CMOS show an efficiency improvement from 17.7% to 40.7% for HSUPA at 25.3dBm output power and from 11.3% to 35.5% for WLAN 802.11g at 22.8dBm.

## **RM03C-4      02:20 PM**

### **Distributed Power Amplifier with Electronic Harmonic Filtering**

B. Thompson, B. Stengel, S. Olson, D. Scagmelli\*, A. Joseph\*, J. Dunn\*, Motorola Inc.,  
\*IBM Microelectronics

**Abstract:** Providing all band power amplification and harmonic rejection are objectives with orthogonal implementations. This paper is a review of a new Distributed Power Amplifier (DPA) architecture using programmable frequency dispersion. This frequency domain dispersion is designed to achieve electronic harmonic filtering within the intended frequency band. Tunable reactive components are not practical in a high power transmitter network. Vector signal combining is used to provide harmonic filtering.

**RM03C-5** This paper presents a new balanced architecture to improve the power added efficiency (PAE) of a 3G handset power amplifier without trading-off its stringent linearity requirement. It is modified from the structure of our Switched Load Insensitive Power Amplifier (LIPA®). Power amplifiers using the modified balanced structure retain the main features of the LIPA and provide boosted PAE performance in low and high power mode. The novel balanced structure is implemented into 4x4mm<sup>2</sup> power amplifier

## **RM03C-5      02:40 PM**

### **Dual Mode Efficiency Enhanced Linear Power Amplifiers Using a New Balanced Structure**

Gary Zhang, Shiao Chang, Sunny Chen and Jing Sun, Skyworks Solutions Inc, 5221 California Ave., Irvine, CA 92617 (Gary Zhang), 2427, W. Hillcrest Dr., Newbury Park, CA 91320, USA, (the rest)

**Abstract:** This paper presents a new balanced architecture to improve the power added efficiency (PAE) of a 3G handset power amplifier without trading-off its stringent linearity requirement. It is modified from the structure of our Switched Load Insensitive Power Amplifier (LIPA®). Power amplifiers using the modified balanced structure retain the main features of the LIPA and provide boosted PAE performance in low and high power mode. The novel balanced structure is implemented into 4x4mm<sup>2</sup> power amplifier.

**Monday June 8, 2009**  
**01:20 PM**  
**BC&EC - Room 203**  
**Session: RM03D: Advanced VCO Topologies**  
Chair: Waleed Khalil, Ohio State University  
Co-Chair: Timothy Hancock, MIT Lincoln Laboratory

**RM03D-1     01:20 PM**

**A Low-Power Dual-Band Oscillator Based on Band-Limited Negative Resistance**

B. Catli, M. M. Hella, Rensselaer Polytechnic Institute

**Abstract:** This paper presents a 2.1/3.9 GHz oscillator in a GaAs technology. The dual band operation is based on switching the negative resistance bandwidth of a capacitively degenerated common collector stage, while using a multi-resonant point tank, thus the band switching mechanism is moved to the active core of the oscillator. The measured phase noise for both bands is 136dBc/Hz@1MHz with a power consumption of 5.1mW, and a FOM of 195.39/-200.72 for 2.1/3.9GHz respectively.

**RM03D-2     01:40 PM**

**Low Phase Noise Gm-Boosted Differential Colpitts VCO with Suppressed AM-to-FM Conversion**

J.P. Hong and S.G. Lee, Information and Communications University (ICU), Korea

**Abstract:** A gm-boosted differential Colpitts VCO is proposed, which allows lower oscillation start-up current and suppressed AM-to-FM conversion by the switching transistors. The proposed architecture allows wider range of saturation mode operation for the switching transistors which helps to suppress the AM-to-FM conversion. Measurement shows, at 1.84GHz(1.75~1.93 GHz), the phase noise of -105 and -128 dBc/Hz (FOM=191.2) at 100KHz and 1MHz offset, respectively, while dissipating 1.8 mA from 0.9-V supply.

### **RM03D-3      02:00 PM**

#### **An SoC with Automatic Bias Calibration of an RF Oscillator**

Imran Bashir, R. Bogdan Staszewski, Oren Eliezer, Poras T. Balsara, Texas Instruments Inc., USA, University of Texas at Dallas, USA

**Abstract:** We present a novel scheme for calibrating RF oscillator current to ensure device reliability and improve performance of a wireless SoC. The proposed method calculates variance of the digitized phase error samples by a time-to-digital converter (TDC) in an all-digital phase-locked loop (ADPLL) to estimate oscillator noise as a function of the current setting. This concept is incorporated on a commercial single-chip radio SoC fabricated in 90-nm CMOS and is used in GSM/EDGE mobile handsets.

### **RM03D-4      02:20 PM**

#### **A Low-Power, Small Area Quadrature LC-VCO Using Miniature 3D Solenoid Shaped Inductor**

A. Tanabe, K. Hijioka, H. Nagase, Y. Hayashi, LSI Fundamental Res. Lab., NEC Electronics Corp., Japan

**Abstract:** A low-power, small area quadrature 5GHz LC-VCO includes 20GHz oscillator and 1/4 divider has been fabricated using miniature 3D solenoid shaped inductor in 90nm CMOS. Owing to the small area and small magnetic energy of the 3D inductor, small chip area of 2597mm<sup>2</sup> which is 1/10 of the reported smallest LC-VCOs and 2.8mW power consumption have been achieved without degrading Figure of Merit. This miniature LC-VCO is suitable for low-power, low-cost wireless transceivers and RF SoCs.

### **RM03D-5      02:40 PM**

#### **A Gate-Modulated CMOS LC Quadrature VCO**

K.-W. Cheng and D. J. Allstot, University of Washington, Seattle, WA, USA

**Abstract:** A QVCO based on the time-varying gate-modulated coupling of two LC tank VCOs (GM-QVCO) is introduced. In addition to comparable phase noise performance, the GM-QVCO also exhibits superior quadrature phase accuracy, and suitability for low power supply voltage designs that use cascode current sources and active loads. It draws 2.4mA from a 1.8V power supply, displays a phase noise of -122dBc/Hz@1MHz offset, and has a quadrature phase error of 0.4°.

**Monday June 8, 2009**  
**03:30 PM**  
**BC&EC - Room 204AB**  
**Session: RM04A: WLAN and WiMax**  
Chair: Srenik Mehta, Atheros Communications  
Co-Chair: Julian Tham, Arda Technologies

**RM04A-1 03:30 PM**

**Full Integrated 23dBm Transmit Chain With On-chip Power Amplifier and Balun for 802.11a Application in Standard 45nm CMOS process**

A. A. Kidwai, A. Nazimov\*, Y. Eilat\*, O. Degani\*, Intel Corporation, Hillsboro OR, \*Intel Corporation, Haifa Israel

**Abstract:** A fully integrated transmit chain for 802.11a band with on-chip power amplifier and on-chip balun matching network in 45nm standard digital CMOS process demonstrates saturated power of +23dBm. The average efficiency is +5% and peak efficiency is +15%. A standalone class AB CMOS power amplifier with on-chip BALUN matching network was also produced and detailed characterization data is presented. Using digital predistortion, an EVM of -28dB is achieved at 19dBm for 5GHz band for standalone PA.

**RM04A-2 03:50 PM**

**A Tri-Band MIMO Transceiver for Mobile WiMAX with an Image Rejection Ratio Tunable SSB Mixer**

K. Oishi, D. Yamazaki, N. Hasegawa\*, N. Kobayashi\*, M. Kudo\*, T. Sasaki\*, S. Sakamoto\*\*, S. Yamaura, Fujitsu Laboratories Ltd., \*Fujitsu Microelectronics Ltd., \*\*Fujitsu Microelectronics Solutions Ltd., Japan

**Abstract:** A tri-band (2.3/2.5/3.5 GHz) MIMO transceiver for mobile WiMAX is presented. We adopted a double conversion transceiver that can switch lower and upper local modes to create an effective multiband transceiver. For the RX, the image rejection ratio (IRR) tunable single side-band (SSB) mixer was used to achieve over 50 dB IRR. The RCE for 2.5 GHz at -71.5 dBm input was below -28.7 dB and maximum input level up to -20 dBm was achieved. The TX had a dynamic range of over 56 dB.

#### **RMO4A-3     04:10 PM**

##### **Innovative Architecture for Dual-band WLAN and MIMO Front-end Module Based on a Single Pole Three Throw Switch-plexer**

Chun-Wen Paul Huang, William Vaillancourt, Philip Antognetti, Tony Quaglietta, Mike McPartlin, Mark Doherty, and Christophe Masse, SiGe Semiconductor, Andover, MA 01810, USA

**Abstract:** An innovative architecture for a dual-band front-end module for WiFi / MIMO radios is presented. The FEM only consists of a dual-band PA and a SP3T switch-plexer. The switchplexer has a SP3T switch and an integrated Rx diplexer, which features 0.1 dB compression at  $> 33$  dBm with  $< 1$  dB loss for Tx paths and  $< 2$  dB loss with selectivity  $> 15$  dB for Rx. These features reduce complexity and post PA loss of the FEM, resulting in 18 dBm with EVM  $< 3\%$  and  $< -50$  dBm/MHz harmonics in a 4 x 4 mm package.

#### **RMO4A-4     04:30 PM**

##### **A Compact Low Power SDR receiver with 0.5-20MHz Baseband Sampled Filter**

A. Geis\*, \*\* J. Ryckaert\*, J. Borremans\*, G. Vandersteen\*\*, Y. Rolain\*\*, J. Craninckx\*, \*IMEC, Belgium, \*\*Vrije Universiteit Brussels, Belgium

**Abstract:** A flexible low power receiver chain based on a wideband front-end in combination with a novel triangular-wave integration sampling baseband section, with strong embedded anti-alias protection, is proposed for multi-mode SDR receivers. The 90nm CMOS receiver operates from 200MHz up to 5.5GHz with a clock-tunable baseband bandwidth from 500kHz to 20MHz. It has 5.5 to 6dB NF, -0.9dBm IIP3 and 20 to 65dB of gain. Current consumption is 14.5mA from a 1.2V supply.

#### **RMO4A-5     04:50 PM**

##### **Wi-Fi/WiMAX Dual Mode RF MMIC Front-end Module**

P. H. Wu, S. M. Wang and M. W. Lee, Industrial Technology Research Institute, Taiwan

**Abstract:** A dual-mode RF front-end module is designed and implemented for Wi-Fi/WiMAX applications. It consists of a front-end MMIC and a dual-band power amplifier MMIC, both fabricated by 0.5 $\mu$ m E/D-mode p-HEMT process. The front-end MMIC integrates a single-pole triple-throw antenna switch, two low noise amplifiers, a low pass filter and a diplexer in single chip. Overall module size is compact 7mm x 10mm, well tested with Wi-Fi/WiMAX OFDM signals

**Monday June 8, 2009**  
**03:30 PM**  
**BC&EC - Room 205A**  
**Session: RM04B: RF Front End Building Blocks**  
Chair: Osama Shana'a, MediaTek  
Co-Chair: Danilo Manstretta, University of Pavia

**RM04B-1      03:30 PM**

**A DC-to-22 GHz 8.4mW Compact Dual-feedback Wideband LNA in 90 nm Digital CMOS**

M. Okushima\*, J. Borremans, D. Linten, G. Groeseneken, IMEC, Leuven, Belgium, \*currently at: Core Development Division, NEC Electronics corp., Japan

**Abstract:** A dual-feedback topology to extend bandwidth of resistive feedback LNAs is proposed in this paper. Active source follower shunt-shunt feedback using a shunt peaking inductor, combined with series-shunt inductor extend 3-dB and input bandwidth. A prototype in 90nm digital CMOS achieves a high 3-dB bandwidth of 29GHz with adequate input matching up to 22GHz. The miniature area (0.017mm<sup>2</sup>) and low power consumption (8.4mW) make it a very attractive for low-cost very wideband LNA solution.

**RM04B-2      03:50 PM**

**A 24-GHz Transformer-Based Single-In Differential-Out CMOS Low-Noise Amplifier**

Jin-Fu Yeh, Chu-Yun Yang, Hsin-Chih Kuo, and Huey-Ru Chuang, Institute of Computer and Communication Engineering, Department of Electrical Engineering, National Cheng Kung University, Tainan, Taiwan, R.O.C

**Abstract:** This paper presents a 24-GHz single-in differential-out (SIDO) 0.13- $\mu$ m CMOS LNA. The SIDO LNA utilizes a trifilar transformer inserted between the first and the second stages for the single-to-differential signal conversion. The fabricated LNA exhibits a differential gain of 14.7 dB, a 3-dB bandwidth of 3.5 GHz (from 22.9 to 26.4 GHz), a noise figure of 4.3 dB, and an input 1-dB compression point of -13 dBm at 24 GHz. The gain and phase difference are 0.6 dB and 0.47°, respectively.

**RM04B-3      04:10 PM****A 3-to-5 GHz UWB LNA with a Low-Power Balanced Active Balun**

Sanghoon Joo, Tae-Young Choi, Jae-Young Kim\*, Byunghoo Jung, Purdue University in West Lafayette, USA, \*ETRI, South Korea

**Abstract:** A 3-to-5 GHz UWB LNA with a low-power balanced active balun is presented. The LNA employs an NMOS feedback for wideband matching and current reuse scheme for reducing power consumption. The balun uses a differential amplifier with a cascoded cross coupled pair to mitigate the gain and phase imbalances. The LNA and balun achieve the best figure of merit among the presented designs. The gain and phase mismatches of the balun from 0.5 GHz to 10 GHz are 0.4 dB and 1.8°, respectively.

**RM04B-4      04:30 PM****A 50-dB Image-Rejection SiGe-HBT Based Low Noise Amplifier in 24-GHz Band**

T. Masuda, N. Shiramizu, T. Nakamura, and K. Washio, Hitachi, Central Research Laboratory

**Abstract:** A low noise amplifier with high image-rejection function in 0.18- $\mu\text{m}$  SiGe BiCMOS technology were developed to create a 24-GHz band RF receiver frontend. The proposed configuration using notch feedback circuit attributed to have higher image-rejection ratio (IRR) in the quasi-millimeter-wave frequency region. The LNA has a 14-dB gain at 27.2 GHz and a more than 50-dB IRR at 21.6 GHz. While an IIP3 of -13.5 dBm is achieved, the power consumption is also low, 8 mW, with a 1.2 V power supply.

**RM04B-5      04:50 PM****A 1.3 V, 65nm CMOS, Coilless Combined Feedback LNA with Integrated Single Coil Notch Filter**

Dirk Bormann, Tobias D. Werth, Christoph Schmits\*\*, and Stefan Heinen, RWTH Aachen University, Chair of Integrated Analog Circuits and RF Systems, \*Ruhr-Universitaet Bochum, Lehrstuhl fuer Integrierte Systeme, Germany

**Abstract:** An LNA with integrated notch filter is demonstrated. It consists of a coilless two-stage LNA with capacitive feedback and an integrated Q-enhanced notch filter. Thus, this circuit is capable for use in FDD systems like UMTS or WCDMA without additional off-chip interstage filter, especially for highly integrated multi-band multi-standard transceivers as only one area consuming coil is used. The circuit was implemented on a 65nm CMOS process.

**Monday June 8, 2009**  
**03:30 PM**  
**BC&EC - Room 206AB**  
**Session: RM04C: Frequency Generation Circuits: PLLs**  
**and Synthesizers**  
Chair: Stefano Pellerano, Intel Co.  
Co-Chair: Bertan Bakkaloglu, Arizona State University

**RM04C-1      03:30 PM**

**A 750uW 1.575GHz Temperature-Stable FBAR-Based PLL**

Julie R. Hu, Wei Pang\*, Richard C. Ruby\*, and Brian P. Otis, University of Washington, Seattle, WA, \*Avago Technologies, Inc., San Jose, CA

**Abstract:** A 1.575GHz phase-locked loop (PLL) using a bulk acoustic wave resonator (FBAR) based VCO is presented. Close-in phase noise is suppressed by the loop, while high-offset noise is suppressed by the extremely high Q ( $> \$2000$ ) VCO. This technique results in a 750uW PLL with phase noise of -82 and -138dBc/Hz at 1kHz and 1MHz offset, respectively. A temperature-compensated FBAR stack is described, allowing quartz locking over a -10 to 100 degree C temperature variation.

**RM04C-2      03:50 PM**

**A 0.1-5GHz Dual-VCO Software-Defined  $\Sigma\Delta$ ; Frequency Synthesizer in 45nm Digital CMOS**

P. Nuzzo\*, K. Vengattaramane\*#, M. Ingels\*, V. Giannini\*, M. Steyaert#, J. Craninckx\*, \*NES/Wireless, IMEC #Katholieke Universiteit Leuven, Belgium

**Abstract:** A wide-band frequency synthesizer architecture for SDR applications is presented based on a dual-VCO  $\Sigma\Delta$ ; PLL with a wide-range modulus programmable divider. The design combines high flexibility with a scalable implementation exploiting the capabilities of advanced digital technologies. The prototype in 1.1-V 45-nm digital CMOS achieves a 4.3 to 10GHz tuning range with programmable KVCO, bandwidth and current consumption. Measured phase noise is -122dBc/Hz at 2-MHz offset from a 7.2GHz carrier.



### **RM04C-3      04:10 PM**

#### **A 3GHz Wideband $\Sigma\Delta$ ; Fractional-N Synthesizer with Voltage-Mode Exponential CP-PFD**

Hiva Hedayati and Bertan Bakkaloglu, Department of Electrical Engineering, Arizona State University, Tempe, AZ 85287 USA

**Abstract:** A 3GHz wideband  $\Sigma\Delta$ ; fractional-N synthesizer with an exponential settling voltage-mode PFD is presented. The 1MHz band-width Type-I PLL loop utilizes the exponential small-signal settling characteristics of a voltage-mode NMOS (follower) LDO based PFD-CP to reduce in-band quantization noise leakage by 15dB without the need for a noise suppression DAC. The PLL is fabricated on a 0.18  $\mu$ m less than 20-mA current consumption from 1.8-V power supply.

### **RM04C-4      04:30 PM**

#### **An Integrated 18 GHz Fractional-N PLL in SiGe BiCMOS Technology for Satellite Communications**

F. Herzel, S. A. Osmany, K. Schmalz, W. Winkler, J. C. Scheytt, T. Podrebersek\*, R. Follmann\*, H.-V. Heyer\*\*, IHP, \*IMST GmbH, \*\*Kayser-Threde GmbH

**Abstract:** We present a single-chip fractional-N PLL for space applications. The design employs a high-current charge pump with optimum output biasing and a low-current charge pump for extension of the tuning range. We show that the extension of the tuning range does not increase phase noise and reference spurs. The PLL is tunable from 17.5 GHz to 18.9 GHz, and the phase noise at 1 MHz offset is below -110 dBc/Hz. Loop bandwidth and phase noise are almost independent of the output frequency.

### **RM04C-5      04:50 PM**

#### **A 1.2-mW CMOS Frequency Synthesizer with Fully-Integrated LC VCO for 400-MHz Medical Implantable Transceivers**

A. Italia, G. Palmisano, University of Catania, Italy

**Abstract:** An ultra low-power frequency synthesizer for 400-MHz medical implantable transceivers was designed in a 0.13- $\mu$ m CMOS technology. The circuit is implemented by means of an integer-N PLL, which features a fully-integrated LC VCO and 160/480-kHz programmable channel steps. The frequency synthesizer achieves a phase noise of -99 dBc/Hz at 100-kHz offset frequency. The measured settling time is 500  $\mu$ s and the reference spurs are lower than -52 dBc. The circuit consumes 1.2 mW from a 1.2-V supply.

**Monday June 8, 2009**  
**03:30 PM**  
**BC&EC - Room 203**  
**Session: RM04D: Submicron RFIC MOS and Novel Devices**  
Chair: Aditya Gupta, ANADIGICS  
Co-Chair: Eli Reese Triquint

**RM04D-1     03:30 PM**

**Temperature Compensated BAW Resonator and its integrated Thermistor for a 2.5GHz Electrical Thermally Compensated Oscillator**

David Petit, Etienne César\*\*, Pierre Bar, Sylvain Joblot, Guy Parat\*\*\*, Olivier Berchaud\*\*, Jacques Verdier\*, Jean-François Carpentier, STMicroelectronics, Crolles, France,  
\*INL, Villeurbanne, France, \*\*ST-NXP Wireless, Grenoble, France, \*\*\*CEA, LETI, Grenoble

**Abstract:** This paper presents a miniaturized 2.5 GHz frequency source based on compensated BAW resonator with its integrated temperature molybdenum sensor assembled on the differential Colpitts oscillator. The presence of silicon dioxide layer having a positive temperature coefficient compared to other layers is used to reduce the resonator's drift. A demonstration oscillator achieves a frequency drift of 40 ppm over a temperature range from -35°C to +85°C.

**RM04D-2     03:50 PM**

**RF Reliability of Short Channel NMOS Devices**

D. Stephens\*, T. Vanhoucke\*\* and J.J.T.M. Donkers\*\*, NXP-TSMC Research Center, \*High Tech Campus 37, 5656 AE Eindhoven, The Netherlands, \*\*Kapeldreef 75, 3001, Leuven, Belgium

**Abstract:** Abstract: The complexities associated with performing accurate large-signal measurements have been prohibitive in determining device level reliability under RF stress. In this work, a large-signal measurement setup is adapted to perform RF stress measurements on a 45nm n-channel metal-oxide semiconductor transistor. For the first time, a device level comparison of degradation under RF and DC stress conditions is performed.

### **RMO4D-3     04:10 PM**

#### **Flicker Noise in Nanoscale pMOSFETs with Mobility Enhancement Engineering and Dynamic Body Biases**

Kuo-Liang Yeh, Chih-You Ku, Wei-Lun Hong, and Jyh-Chyurn Guo, Institute of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan

**Abstract:** The uniaxial compressive strain from e-SiGe combined with dynamic body biases effect on flicker noise of pMOSFETs is presented in this paper. This compressive strain contributes higher mobility but the worse flicker noise becomes a potential killer to RF analog circuits. Forward body biases can reduce the flicker noise but its effect is degraded in strained pMOSFETs. The increase of Hooge parameter  $aH$  is the key factor responsible the degraded flicker noise in strained pMOSFETs.

### **RMO4D-4     04:30 PM**

#### **High Frequency Noise in Deep-Submicrometer nMOSFETs under Different Hot Carrier Stresses**

Hao Su, Hong Wang, Zhiyong Sun, Tao Xu, Microelectronic Centre, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Republic of Singapore

**Abstract:** Degradation mechanisms contributing to the increased high frequency noise of deep-submicrometer NMOSFETs after different hot-carrier (HC) stresses are investigated. It is demonstrated that device noise parameters, such as NFmin and  $R_n$  degraded most under maximum substrate-current ( $I_{B,max}$ ) stress. However, hot electron and hot hole injection has much lower degradation on device noise performance.

### **RMO4D-5     04:50 PM**

#### **K-band Diamond MESFETs for RFIC technology**

P. Calvani \*, A. Corsaro \*, M. C. Rossi \*, G. Conte \*, E. Giovine \*\*, W. Ciccognani, \*\*\*, E. Limiti \*\*\*, \* University of Roma Tre, Rome, Italy, \*\* Istituto di Fotonica e Nanotecnologie, CNR, Rome, Italy, \*\*\* University of Rome; Tor Vergata, Rome, Italy

**Abstract:** Submicron gate-length metal-semiconductor field effect transistors (MESFETs) were fabricated on hydrogen-terminated diamond. Devices were realized to be employed in Microwave Integrated Circuits for satellite communications and high frequency power amplification, areas where diamond promises the replacement of vacuum electronics. Fabricated MESFETs showed high drain-source current and large transconductance values with a cut off frequency of 10 GHz and a maximum oscillation frequency of 35 GHz

**Session: RTU1A: Broadband PA's and MIMO**

Chair: Noriharu Suematsu, Mitsubishi Electric

Co-Chair: Bruce Thompson, Motorola ARTC

**RTU1A-1 8:00 AM****A 4-Antenna Transmitter in 0.18 $\mu$ m CMOS using Space-Time Block Codes**

N. M. Neihart, K. W. Cheng\*, J. S. Walling\*, S. Yoo\*, and D. J. Allstot\*, Iowa State University, \*University of Washington

**Abstract:** The first implementation of a fully-integrated (0.18 $\mu$ m CMOS), configurable, 4-antenna transmitter using space-time block codes as a means for reducing the required output power of the PA, and thereby improving system efficiency, is described. Measured results show optimum efficiency is obtained for the 3-antenna system capable of delivering 27.7dBm into 50 Ohm using three class-AB PA cells each delivering 20dBm into 50 Ohm with PAE of 23%. The overall system efficiency delivering 27.7dBm is 39%.

**RTU1A-2 8:20 AM****Fully Integrated Dual-Band Power Amplifiers with On-chip Baluns in 65nm CMOS for an 802.11n MIMO WLAN SoC**

A. Afsahi\*, \*\*, A Behzad\*\*, V. Magoon\*\*, L. E. Larson\*, \*University of California at San Diego, \*\*Broadcom Corp., USA

**Abstract:** Fully integrated dual-band power amplifiers with on-chip baluns for 802.11n MIMO WLAN applications are presented. With a 3.3v supply, the PAs produce a saturated output power of 28.3dBm and 26.7dBm with peak drain efficiency of 35.3% and 25.3% for the 2.4 GHz and 5GHz bands, respectively. By utilizing multiple fully self-contained linearization algorithms, an EVM of -25dB is achieved at 22.4dBm for the 2.4GHz band and 20.5dBm for the 5GHz band while transmitting 54Mbps OFDM. The chip is fabricated

**RTU1A-3 8:40 AM****Multi-Decade GaN HEMT Cascode-Distributed Power Amplifier with Baseband Performance**

Kevin W. Kobayashi, \*YaoChung Chen, \*Ioulia Smorchkova, \*Benjamin Heying, \*Wen-Ben Luo, \*William Sutton, \*Mike Wojtowicz, and \*Aaron Oki, RF MICRO DEVICES, Torrance, CA, 90505, \*Northrop Grumman Space &amp; Technology, One Space Park, Redondo Beach, CA, 90278

**Abstract:** We report the first multi-decade bandwidth GaN HEMT Cascode-distributed power amplifier designs which achieve performance from base-band to over 20 GHz. The amplifiers achieve 1-4 Watts of saturated CW power from 100MHz to over 20GHz at an operating voltage of 30V. Typical OIP<sub>3</sub> > 40 dBm and NF of 3 dB were also achieved. Compared to equivalent GaAs PHEMT DAs, the GaN HEMT DAs obtain 6 dB higher output power and 5.8-6.6dB higher OIP<sub>3</sub> while achieving comparable gain, noise figure, and bandwidth.

**RTU1A-4 9:00 AM****A 90nm CMOS Power Amplifier for 802.16e (WiMAX) Applications**

O. Degani, E. Cossoy, S. Shahaf, D. Chowdhury, C. D. Hull, C. Emanuel, R. Shmuel Mobility Wireless Group, Intel Corp., Israel

**Abstract:** We demonstrate a 90nm CMOS power amplifier with integrated BALUN for 2.3-2.7GHz WiMAX (802.16e) band. The PA gain and Psat are +18dB and +32dBm, respectively, using a 3.3V supply, with peak PAE of 48%. Digital pre distortion technique is used to enhance the PA linearity. Compliance with the FCC 10MHz WiMAX mask is demonstrated at +25dBm with power efficiency of ~25%. Under these conditions, The measured EVM for 64QAM OFDM signal is -30dB and the measured second harmonic level is -31[dBm/MHz].

**Session: RTU1B: New Ideas in CMOS RF Front-End Circuits**

Chair: Frank Henkel, IMST GmbH

Co-Chair: Reynold Kagiwada, Northrop Grumman

**RTU1B-1 8:00 AM**

**Active Feedback Interference Cancellation in RF Receiver Front-Ends**

T.D. Werth, C. Schmits\*, S. Heinen, Chair of Integrated Analog Circuits RWTH Aachen University,

\*Institute for Integrated Systems Ruhr-Universitaet Bochum, Germany

**Abstract:** A feedback interference cancellation circuit using a control loop to reject blockers in wireless receivers is presented. The concept is based on a translational loop which subtracts a blocker replica in a feedback loop fashion. In contrast to feedforward methods loop selectivity does not depend on exact gain matching of two paths but on the open loop gain which is easier to adjust. The concept and measurement results from a prototype chip in 65 nm CMOS are presented showing the feasibility.

**RTU1B-2 8:20 AM**

**A 1.3V 26mW 3.2GS/s Undersampled LC Bandpass Sigma-Delta ADC for a SDR ISM-band Receiver in 130nm CMOS,**

N. Beilleau, H. Aboushady, F. Montaudon\* and A. Cathelin\*, University of Paris VI, Pierre et Marie Curie, Paris, France, \*STMicroelectronics, Grenoble, France.

**Abstract:** This paper presents the implementation of an undersampled LC bandpass Sigma-Delta ADC with a raised-cosine feedback DAC. It converts a signal centered in the ISM band at 2.442GHz with a sampling frequency of 3.256GHz. This circuit has been fabricated in a 130nm CMOS process, occupies an area of 0.27mm<sup>2</sup> and is operating at a supply voltage of 1.3V. The SNDR measured are 34dB, 37dB and 42dB for respective bandwidths of 25MHz, 10MHz and 1MHz. The power consumption is 26mW and the FoM is 2.3pJ/bit.

**RTU1B-3 8:40 AM**

**An Inductorless High Dynamic Range 0.3-2.6 GHz Receiver CMOS Front-End**

N. Poobuapheun\*, \*\*, W.H. Chen\*, Z. Boos\*\*\*, and A.M. Niknejad\*, \*University of California at Berkeley,

\*\* Maxim Integrated Products, Inc., \*\*\* Infineon Technologies, Munich, Germany,

**Abstract:** This paper presents a wideband receiver front-end implemented in 0.13μm CMOS technology that consists of a low-noise amplifier, a quadrature mixer, and a frequency divider. Multi-gated transistors have been used to enable linearity tuning. The circuit employs no inductors and operates from 0.3 - 2.6 GHz with a tunable baseband bandwidth. The front-end achieves 38 dB voltage conversion gain, 3.6 dB DSB NF, nominal -6.5 dBm IIP3 and +4 dBm when tuned. The chip consumes 35 mA from a 1.5 V supply.

**RTU1B-4 9:00 AM**

**A 90nm CMOS Highly Linear Clock Bootstrapped RF Sampler Operating at Wide Frequency Range of 0.5GHz to 5GHz**

M.Sato, H.Abe, M.Hamada\*, H.Majima\*, T.Kuroda,H.Ishikuro, Keio University, \*Toshiba Corp

**Abstract:** This paper reports a highly linear RF sampler with wide operating frequency range and power supply range. A clock bootstrapping circuit is proposed to decrease both the on-resistance and off-leakage of advanced MOSFETs while considering the device reliability. The proposed RF sampler circuit has been implemented in 90nm CMOS process, and excellent IIP3 has been obtained at wide frequency range up to 5GHz and 2GHz when the power supply is 1.2V and 0.5V, respectively.

**Session: RTU1C: Advanced Device Characterization and  
Non-Linear Circuit Analysis**

Chair: Yuhua Cheng, Peking University

Co-Chair: Louis C Liu, CT Communication Technologies

**RTU1C-1 8:00 AM**

**MMW Lab In-Situ to Extract Noise Parameters of 65nm CMOS  
Aiming 70~90GHz Applications**

Y. Tagro\*, D. Gloria\*, S. Boret\*, G. Dambrine\*\*, \*STMicroelectronics, \*\*IEMN

**Abstract:** Design and use of an In-Situ Tuner (IST) aiming On-Wafer multi-impedance method are presented. The conventional method using Off-Wafer Tuner is limited by the frequency range and has losses between this external Tuner and the DUT. Here, IST is placed near the DUT to achieve higher Gamma and to cancel losses between the impedance generator and the device. The IST's architectures presented and the noise de-embedding is described extracting the 4 noise parameters of a 65nm Si-MOS-FET in 70~90GHz.

**RTU1C-2 8:20 AM**

**40 ns Pulsed I/V Set-up and Measurement Method Applied to InP  
HBT Characterization and Electro-thermal modeling**

A. Saleh, M. Abou Chahine, T. Reveyrand, G. Neveux, D. Barataud, J.M. Nebus, R. Quéré,  
Y. Bouvier\*, J. Godin\*, and M. Riet\*, University of Limoges XLIM,\* Alcatel-Thales III-V Lab, France

**Abstract:** This paper presents a novel pulsed I/V measurement methodology applied to HBT's characterization using very narrow 40 ns pulse widths. The proposed measurement technique is applied here to the characterization and electro-thermal modeling of InGaAs/InP DHBTs from Alcatel Thales III-V Lab. Measurements and simulations are then done to study electro-thermal effects in bipolar current mirrors.

**RTU1C-3 8:40 AM**

**Background Estimation of Power Amplifier Nonlinearities for OFDM  
Signals**

P. V. Kolinko, L. E. Larson, University Of California San Diego, California Institute for  
Telecommunications and Information Technology (CALIT2).

**Abstract:** A method of estimating the third-order distortion coefficient of a memoryless amplifier is presented for the case of an OFDM signal. The estimate is obtained from correlation of PN sequences BPSK modulated onto the OFDM pilots with in-band pilot distortion products at the amplifier output. The method can be used for real-time estimation of nonlinearities without affecting the communication. An 8-10dB improvement in ACPR was obtained, after digital predistortion using the above estimates.

**RTU1C-4 9:00 AM**

**A Rigorous Analysis of Local Oscillator Pulling in Frequency and  
Discrete-time Domain**

C. J. Li, F. K. Wang, T. S. Horng, K. C. Peng\*, Department of Electrical Engineering, National Sun Yat-sen University, Taiwan, \*Department of Computer and Communication Engineering, National Kaohsiung First University of Science and Technology, Taiwan

**Abstract:** This study presents injection pulling effects on a local oscillator (LO) for wireless applications. A phase-locked loop under injection is analyzed in frequency domain to account for the inherent band-pass filtering on an injection signal. A discrete-time analysis is also provided to predict output spectra of the LO pulled by a sinusoidal and modulated injection signal. Comparison between theoretical predictions and experimental results shows excellent agreement.

## Session: RTU2A: Wideband and Direct Digital Frequency Synthesizers

Chair: Domine M. W. Leenaerts, NXP Semiconductors

Co-Chair: Sanjay Raman, DARPA / VT

### RTU2A-1 10:20 AM

#### A 366 mW Direct Digital Synthesizer at 15 GHz Clock Frequency in SiGe Bipolar Technology

B. Laemmle, C. Wagner\*, H. Knapp\*\*, L. Maurer\*\*\*, R. Weigel, University Erlangen Nuremberg,

\*Johannes Kepler University Linz, \*\*Infineon AG, \*\*\*, DICE, Germany/Austria

**Abstract:** A direct digital synthesizer (DDS) with 6bit amplitude and 8bit phase resolution is presented. The phase-to-amplitude mapping circuit is implemented as a differential pair in saturation. The use of a modern SiGe bipolar technology enables both a low powerconsumption of 366 mW and a high clock frequency of 15 GHz. The chip is fabricated in a 0.35  $\mu\text{m}$  200-GHz fT SiGe bipolar technology and occupies only 1024x1128  $\mu\text{m}^2$ .

### RTU2A-2 10:40 AM

#### A 24-bit 5.0 GHz Direct Digital Synthesizer MMIC with Direct Digital Modulations and Spur Randomization

X. Geng, F. F. Dai, J. D. Irwin, R. C. Jaeger, Auburn University, USA

**Abstract:** This paper presents a low power, 5.0GHz SiGe DDS MMIC with 24-bit phase and 10-bit amplitude resolutions, with both direct frequency and phase modulation capabilities. The device contains a 24-bit ripple carry accumulator, a 12-bit ripple carry adder, a 10-bit segmented sine-weighted DAC and an LSB phase dithering scheme for spur randomization. It occupies 3.0x2.5mm<sup>2</sup> and consumes 4.7W under a 3.3V single power supply. The measured Nyquist and narrow band SFDR are 38dBc and 60dBc with 5.0GHz clock

### RTU2A-3 11:00 AM

#### A Digital Frequency Synthesizer for Cognitive Radio Spectrum Sensing Applications

T. Rapinaja, K. Stadius, L. Xu, S. Lindfors\*, R. Kaunisto\*\*, A. Pärssinen\*\*, J. Rynänen, Department of Micro- and Nanosciences/SMARAD2, Helsinki University of Technology, Finland, \*Currently at Texas Instruments, Finland, \*\*Nokia Research Center, Finland

**Abstract:** A frequency synthesizer architecture targeted for spectrum sensing applications is presented. It achieves wide operational bandwidth, extremely high frequency resolution, short settling time as well as low power and area consumption. The synthesizer was implemented in 65-nm CMOS process and it occupies 0.12 mm<sup>2</sup> area, covers a frequency range range of 0.1 GHz to 4.267 GHz with 5.38 Hz frequency resolution, and dissipates 8.4 mW power. The settling time for any arbitrary frequency jump is 30 ns.

### RTU2A-4 11:20 AM

#### A Single-Chip 0.125-26GHz Signal Source in 0.18 $\mu\text{m}$ SiGe BiCMOS

S. Yu, Y. Baeyens\*, J. Weiner\*, U. Koc\*, M. Rambaud\*, F. Liao\*, Y. Chen\*, P. Kinget, Columbia University,

\*Bell Laboratories, Alcatel-Lucent

**Abstract:** We present a 4.4mm<sup>2</sup> single-chip synthesized signal source with 0.125 to 26-GHz output frequency realized on a 0.18 $\mu\text{m}$  SiGe BiCMOS technology. A core fractional-N synthesizer uses four VCO's and has a 4 to 8-GHz synthesizable range. Additional frequency division and multiplication are used to generate frequencies below 4GHz and above 8GHz, respectively. The noise performance achieves -116.7dBc/Hz at 1-MHz offset for 6-GHz output frequency and -80.6dBc/Hz in-band noise.



**Session: RTU2B: Millimeter-Wave Imaging and Communication Systems**

Chair: Luciano Boglione, University of Massachusetts Lowell

Co-Chair: Jenshan Lin, University of Florida

**RTU2B-1 10:20 AM**

**A CMOS Focal-Plane Array for Heterodyne Terahertz Imaging**

U.R. Pfeiffer, E. Öjefors, A. Lisaukas\*, D. Glaab\*, H.G. Roskos\*, High-Frequency and Communication Technology, University of Wuppertal, Germany, \*Physikalisches Institut, Johann Wolfgang Goethe-Universität Frankfurt, Germany

**Abstract:** In this paper we present a focal-plane array (FPA) for heterodyne imaging at 0.65-THz in a low-cost 0.25- $\mu\text{m}$  CMOS process technology. The  $3 \times 5$  pixel array is fully integrated on chip and consists of differential patch antennas, NMOS square-law mixers, and 4 3-dB low-IF amplifiers. The NMOS square-law mixers are based on distributed resistive self-mixing and facilitate mixing well beyond the cut-off frequency of the technology. First 0.65-THz heterodyne imaging results are presented.

**RTU2B-2 10:40 AM**

**High-Performance W-Band SiGe RFICs for Passive Millimeter-Wave Imaging**

Jason W. May, Gabriel M. Rebeiz, University of California, San Diego, USA

**Abstract:** A W-band square-law detector was implemented in a commercial SiGe process and integrated with a SiGe LNA and SPDT switch. The combined LNA+Detector is 0.26 mm<sup>2</sup>, achieves a responsivity of  $\sim 4$  MV/W at 94 GHz with an NEP  $< 0.02$  pW/sqrt(Hz), and consumes 29 mA from a 1.2 V supply. The chip can achieve a temperature resolution of 0.2 K with a 30 ms integration time. This is, to our knowledge, the first W-band SiGe passive millimeter-wave imaging chip with state-of-the-art temperature sensitivity.

**RTU2B-3 11:00 AM**

**W-band 65-nm CMOS and SiGe BiCMOS Transmitter and Receiver with Lumped I-Q Phase Shifters**

I. Sarkas\*, M. Khanpour\*, A. Tomkins\*, P. Chevalier\*\*, P. Garcia\*\* and S. P. Voinigescu\*

\*University of Toronto, Canada, \*\*STMicronics, France

**Abstract:** This paper describes 80-94 GHz and 70-77 GHz I-Q phase shifters and the corresponding transmitter and receiver ICs, fabricated in 65-nm CMOS and SiGe BiCMOS technologies, respectively. The CMOS transmitter operates with a saturated output power of +3 dBm, peak gain of 3.8 dB and power consumption of 142 mW. The SiGe BiCMOS receiver has a peak gain of 17 dB and power consumption of 128 mW from 1.5 V and 2.5 V supplies.

**RTU2B-4 11:20 AM**

**A 60-GHz CMOS Receiver With an On-Chip ADC**

M. Varonen, M. Kallio, V. Saari, O. Viitala, M. Kärkkäinen, S. Lindfors\*, J. Rynänen, K.A.I. Halonen, TKK Helsinki University of Technology, \*Texas Instruments, Finland

**Abstract:** A broadband 60-GHz receiver implemented in a 65-nm baseline CMOS technology is presented. A millimeter-wave front-end, including a single-ended low noise amplifier and a balanced resistive mixer, an IF-stage and an analog baseband circuit with an analog-to-digital converter are integrated on a single chip. The receiver achieves a measured 7.0-dB noise figure at 60 GHz and the voltage gain can be controlled between 45 to 79 dB. The measured 1-dB input compression point is  $-38.5$  dBm.



**Session: RTU2C: Broadband IC II**

Chair: Albert Jerng, Ralink

Co-Chair: Albert Wang, UC Riverside

**RTU2C-1 10:20 AM**

**A 5-Gbps Optical Receiver with Monolithically Integrated Photodetector in 0.18- $\mu$ m CMOS**

T. Kao, A. Chan Carusone, Edward S. Rogers, Sr., Department of Electrical & Computer Engineering, University of Toronto

**Abstract:** This paper describes an optical receiver with monolithically integrated photodetector in 0.18- $\mu$ m CMOS technology using a combination of spatially modulated light detection and an analog equalizer. A transimpedance amplifier employing negative Miller capacitance is introduced to increase its bandwidth without causing gain peaking. Occupying a core area of 0.72 mm<sup>2</sup>, the fully integrated optical receiver achieves 4.25 Gbps and 5 Gbps with a power consumption of 144 mW and 183 mW respectively.

**RTU2C-2 10:40 AM**

**A 4-channel 24-27 GHz CMOS Differential Phased-Array Receiver**

T. Yu, G. M. Rebeiz, University of California at San Diego

**Abstract:** The paper presents a 24-27 GHz 4-channel CMOS differential phased array receiver front-end with integrated baluns, ESD protection and VGAs. The differential implementation of the phased array significantly reduces the substrate coupling effects. The measured array performance shows a gain of 15 dB, a NF of 7.8 dB, an IIP3 of -12 dBm and a 4-bit phase control with an rms gain and phase errors of < 0.35 dB and < 6 degrees. The chip consumes power of 230 mW with an area of 4mm<sup>2</sup>.

**RTU2C-3 11:00 AM**

**A Single-Chip 24 GHz SiGe BiCMOS Transceiver for FMCW Automotive Radars**

D. Saunders, S. Bingham, G. Menon\*\*, D. Crocket, J. Tor, R. Mende\*, M. Behrens\*, N. Jain\*\*, A. Alexanian\*\*\*, Rajanish\*\*, US Monolithics, USA, \*Smart Microwave Sensors, Germany, \*\*Anokiwave, USA, \*\*\*RFmaker, USA

**Abstract:** The design and measured results of a highly integrated FMCW radar transceiver are presented. The transceiver includes a +7dBm transmitter, dual I/Q receivers with 10dB NF/18 dB gain, 24 GHz LO with -82 dBc/Hz phase noise at 100 kHz, PLL, 15-bit DAC, instrumentation amplifiers, and serial programming interface – all designed to operate from -40 to +125°C at 3.5V, 275 mA. Fabricated using Jazz Semiconductor's 0.18  $\mu$ m SiGe BiCMOS process and packaged in a standard plastic 32-pin 5 mm x 5 mm

**RTU2C-4 11:20 AM**

**An 8-18GHz 0.18W Wideband Recursive Receiver MMIC with Gain-Reuse**

D. Ma, F. F. Dai, R. C. Jaeger and J. D. Irwin, Department of Electrical and Computer Engineering, Auburn University, USA

**Abstract:** This paper presents an 8-18GHz wideband receiver with super-heterodyne topology. To save power, the IF output of the first mixer is fed to its tunable input stage for IF amplification in a recursive manner, which significantly enhances the gain tuning without increasing the power. The receiver is implemented in 0.13 $\mu$ m SiGe BiCMOS technology and this is the first fully integrated single-chip receiver MMIC with the coverage of the entire X-band and Ku-band realized on a commercial SiGe process.

**Session: RTU3A: Millimeter-Wave VCOs**

Chair: Timothy Hancock, MIT Lincoln Laboratory

Co-Chair: Stephen Dow, On Semiconductor

**RTU3A-1 01:20 PM****A Low Power mm-wave Oscillator Using Power Matching Techniques**

L. Li, P. Reynaert, M. Steyaert, KU Leuven ESAT-MICAS, Leuven, Belgium

**Abstract:** A low power 90nm CMOS mm-wave oscillator using a power matching technique is presented. It uses an inductive divider to create impedance matching for the amplifier. With the technique, the effect of the varactor loss on the phase noise is reduced and the oscillator power efficiency is increased. The oscillator achieves a phase noise of -95dBc/Hz@1MHz offset from 64GHz, consuming 3.16mW from a 0.6V supply. The figures-of-merit are FOM -186 and FOMT -185. The tuning range is from 61.1 to 66.7GHz.

**RTU3A-2 01:40 PM****A 24 GHz VCO with 20 % Tuning Range in 130-nm CMOS using SOP Technology**

M. Tormanen, H. Sjolund, Lund University

**Abstract:** A 24 GHz System-on-Package (SOP) VCO is demonstrated. The core operates at 6 GHz and employs a high-Q on-carrier inductor. Using two cascaded on-chip frequency doublers the centre frequency is 24.6 GHz with a 20 % tuning range. The phase noise is below -107 dBc/Hz at 1 MHz offset over the tuning range, with a FOM between 188 and 192 dB at a power consumption of 6.9 mW.

**RTU3A-3 02:00 PM****A Dual Band mm-Wave CMOS Oscillator with Left-Handed Resonator**

S-W. Tam, H-T. Yu, Y. Kim, E. Socher, M-C.F. Chang, T.Itoh, University of California, Los Angeles

**Abstract:** A new technique using left-handed resonator to generate multi-band mm-wave carrier signal is proposed in this paper. The left-handed resonator exhibits non-linear dispersion characteristic which enables uneven spacing between resonant frequencies. A dual band mm-wave oscillator in 90nm CMOS technology is implemented to demonstrate this new technique. Using a mode selection switch, the proposed oscillator operates at 21.3GHz and 55.3GHz respectively with a total power consumption of 14mW.

**RTU3A-4 02:20 PM****A 56GHz LC-Tank VCO with 17% Tuning Range in 65nm Bulk CMOS for Wireless HDMI Applications**

José Luis González Jiménez\*, Franck Badets\*\*, Baudouin Martineau\*\*, Didier Belot\*\*, \*Universitat Politècnica de Catalunya, Barcelona, Spain, \*\*STMicroelectronics, Crolles, France

**Abstract:** A voltage controlled oscillator (VCO) with 56GHz central frequency and 17% tuning range is presented. The oscillation frequency is tuned both by an analog input and a three-bit digital control bus using the same type of differential varactors. It achieves a record FOMT (considering tuning range) of 186.8 dBc/Hz and it is able to address the full wireless HDMI band. The VCO is implemented in a 65nm bulk CMOS process and dissipates 15 mW from a 1.2 V supply

**Session: RTU3B: Integrated Filters for RF Applications**

Chair: Jean-Baptiste Begueret, IMS

Co-Chair: Donald Lie, Texas Tech University

**RTU3B-1 01:20 PM****Non-Decimation FIR Filter for Digital RF Sampling Receiver with Wideband Operation Capability**

Changjoon Park, Jehyung Yoon, and Bumman Kim, Department of Electrical Engineering, Pohang University of Science and Technology, Gyeongbuk 790-784, Republic of Korea.

**Abstract:** In order to realize a discrete-time filter for wideband signal processing, a new finite impulse response filter (FIR) has been developed. The filter maintains the moving average effect, but the decimation function is removed in order to realize a cascaded filter. By cascading the proposed FIR filter with a conventional FIR filter, about -60 dB attenuation across 50 MHz signal bandwidth is possible. This bandwidth is wide enough to process the signals of the next generation systems

**RTU3B-2 01:40 PM****A 250-MHz Cut-off Charge-Domain Baseband Filter with Improved Stopband Attenuations**

A. Yoshizawa, S. Iida, Sony Corporation, Tokyo, Japan

**Abstract:** A discrete-time charge-domain baseband filter with a wide bandwidth and improved stopband attenuation characteristics has been implemented with a 90nm CMOS technology. The proposed zero splitting technique allows the discrete-time charge-domain filter to have attenuation notches at non-integer-divided frequencies of the sampling frequency. Measurements show that the 250-MHz cut-off filter achieves an attenuation of 42 dB at 580 MHz, while dissipating 16.6 mW from a 1.2-V supply voltage.

**RTU3B-3 02:00 PM****A 6th Order 1.6 to 3.2GHz Tunable Low-Pass Linear Phase gm-C Filter for Fiber Optic Adaptive EDC Receivers**

D. Baranauskas, D. Zelenin, M. Bussmann\*, S. Elahmadi\*, J. Edwards\*, C. Gill\*, K. Tran\*, L. Linder\*, H. Tan\*, Pacific Microchip Corp., \*Menara Networks

**Abstract:** A 6th order low-pass 1.6 to 3.2GHz Gm-C filter for fiber optic adaptive EDC receivers cascades three Bi-Quads permitting reduction of group delay variation down to 10ps. Cut-off frequency is tuned by switching CMOS varactors polarity. THD is below -40dB at 0.9Vpp-diff output. CTF is implemented in a 0.18 $\mu$ m SiGe process, it occupies 0.17mm<sup>2</sup> and consumes 0.3W from 3.3V supply.

**RTU3B-4 02:20 PM****Compact Circulator Based Phase Shifter at C-Band in BiCMOS**

U. Mayer, F. Ellinger, R. Eickhoff, Chair for Circuit Design and Network Theory, Dresden University of Technology, Dresden, Germany

**Abstract:** This paper presents an active BiCMOS circulator based phase shifter suitable for spatial diversity transceivers in the C-band. Up to 10 GHz, a phase control range of at least 90° and a gain of 0  $\pm$  0.5 dB can be realized. The circuit uses a single supply of 1.8 V and draws a maximum current of 4.6 mA. The proposed phase control principle neither needs inductors nor varactors yielding a simple phase control and very compact core size of only 0.023 mm<sup>2</sup>.

**Session: RTU3C: On-wafer Wireless Testing and Passive RFIC Components**

**Chair:** Gary Zhang, Skyworks Solutions

**Co-Chair:** Chang-Ho Lee, Samsung

**RTU3C-1 01:20 PM**

**On-Wafer Wireless Testing and Mismatch Monitoring Using RF Transmitters with Integrated Antennas**

Piljae Park, Luis Chen, Le Wang, Stephen Long, Hyunkyu Yu\*, and C. Patck Yue, University of California, Santa Barbara, \*ETRI

**Abstract:** This paper presents fully integrated transmitters with integrated antennas for on-wafer wireless testing. The proposed transmitters can replace the I/O pins during testing and can act as a wafer monitoring circuit. Two RF transmitters are implemented to demonstrate the feasibility of wireless testing. The first transmitter is designed to minimize circuit complexity, area and Tx energy per bit. The second design is an image-rejection transmitter serving as a process variations monitoring circuit.

**RTU3C-2 01:40 PM**

**CMOS-MEMS Variable Capacitors with Low Parasitic Capacitance for Frequency-Reconfigurable RF Circuits**

J. Reinke, A. Jajoo, L. Wang, G. K. Fedder, and T. Mukherjee, Carnegie Mellon University

**Abstract:** The design and characterization of a CMOS-MEMS variable capacitor is presented. Measured results demonstrate a tuning ratio of 6.9:1, a quality factor of 28 at 3 GHz, and a self-resonant frequency of 11 GHz, with sub-50 fF parasitic capacitance. Simulations of two frequency-reconfigurable circuits, a low-noise amplifier and a power amplifier, show the importance of low parasitic capacitance for practical reconfigurable front-end designs.

**RTU3C-3 02:00 PM**

**A High Magnetic Coupling, Low Loss, Stacked Balun in Digital 65nm CMOS**

S. Akhtar, R. Taylor\*, P. Litmanen, Texas Instruments Inc., USA

**Abstract:** We present a high magnetic coupling, low loss, stacked balun using a thick aluminum bonding metal layer over a thick copper layer. The thick copper is used to realize a differential primary input winding that resides directly underneath a single ended spiral secondary winding using the aluminum. Occupying an area of 0.078mm<sup>2</sup> on a digital 65nm process with no additional masks, a 5 turn primary with a 3 turn secondary has a measured coupling of 0.94 and a total balun loss of 1.55dB at 1845MHz.

**RTU3C-4 02:20 PM**

**High Current 3D Symmetrical Inductor Integrated in an Advanced HR SOI CMOS Technology Targeting RF Power Applications**

F. Ganesello, D. Gloria, O. Bon\*, B. Rauber and C. Raynaud\*, STMicroelectronics, TR&D, TPS Lab, 850 avenue Jean Monnet, 38926 Crolles (France), \*CEA Leti, avenue des martyrs, 38000 Grenoble (France)

**Abstract:** During past years, high resistivity SOI CMOS technology has emerged as a promising one for the integration of RF applications. In this trend, 3D symmetrical inductor (3DSI) has been proposed on SOI to lower the amount of area consumed by inductor. Unfortunately in advanced CMOS technology 3DSI suffer from limited current capability since they use the lower levels of the BEOL (which are thinner). This paper presents a novel class of high current 3DSI aiming to resolve this issue.

**Session: RTUIF: Interactive Forum**

Chair: David Ngo, RFMD

Co-Chair: Tina Quach, Freescale Semiconductor Inc.

Yann Deval, University of Bordeaux, IMS Lab

**RTUIF-01**

**A Dual-Band CMOS CDMA Transmitter Without SAW and Driver Amplifier**

M. Farazian, B. Asuri\*, Y. Zhao\*, L. E. Larson, Center for Wireless Communication, University of California San Diego, \* Qualcomm Inc., USA

**Abstract:** A SAW-less dual-band I/Q transmitter without a Driver Amplifier is designed for dual-band (PCS/IMT, cellular) CDMA applications. The receive band noise is better than -159 dBc/Hz. It can provide up to +5 dBm output power and meets the ACPR and dynamic range requirements of both PCS/IMT and cellular CDMA. The measured S22 is better than -10 dB for both bands and it requires no external matching components. The transmitter is implemented in a 65nm digital CMOS technology and occupies 1.0 mm<sup>2</sup>.

**RTUIF-02**

**A 50 dB Dynamic Range, 11.3 GSPS, Programmable FIR Equalizer in 0.18μm SiGe BiCMOS Technology for High Speed EDC Applications**

K. Tran, J. Edwards, L.F. Linder, C. Gill, M. Bussmann, S. Elahmadi, H. Tan Menara Networks Inc., Irvine, CA, USA

**Abstract:** Fiber optic signals transmitted over long lengths of single mode fiber (> 80km) suffer from various forms of dispersion. This translates into signal distortion in the electrical domain. Equalizers such as a FIR filter is used to transform severely distorted NRZ data into predictable pre-defined target signals that allow for robust clock / data recovery. There are several key features of the FIR in support of the performance needed for this application. A new T/H circuit enables the performance.

**RTUIF-03**

**A 1.2-V Single-Sideband Upconverter System with High Spurious Suppression for UWB Frequency Synthesizers**

Siu-Kei TANG, Kong-Pang PUN, The Chinese University of Hong Kong

**Abstract:** This paper presents a precise single-sideband (SSB) upconverter system for use in UWB Mode 1 frequency synthesizers. A divide-by-two circuit and a notch filter are employed to generate accurate quadrature sinusoids at the required offset frequency with low harmonic distortion for precise SSB mixing. Double degeneration technique is applied to linearize the SSB upconverter for minimizing non-linearities and unwanted spurs.

**RTUIF-04**

**A 12.5Gbps Analog Timing Recovery System for PRML Optical Receivers**

J. Edwards\*, C. Gill\*, K. Tran\*, L. Linder\*, M. Bussmann\*, S. Elahmadi\*, H. Tan\*, D. Zelenin\*\*, D. Baranauskas\*\*, \*Menara Networks, Irvine, CA, USA, \*\*Pacific Microchip, Los Angeles, CA, USA

**Abstract:** This paper describes a timing recovery system (TRS) based on an analog approximation of the minimum mean squared error (MMSE) algorithm. The TRS has been fabricated in a 0.18μm, 150GHz SiGe BiCMOS process as part of a high performance Class-2 Partial Response Maximum Likelihood (PRML) dispersion tolerant optical receiver.

## RTUIF-05

### CMOS UWB Pulse Generator Co-Designed with Package Transition

S. Bourdel, J. Gaubert, O. Fourquin, R. Vauche, N. Dehaese, Aix-Marseille University, IM2NP, and CNRS, IM2NP (UMR 6242), Campus de Saint-Jérôme, Avenue Escadrille Normandie Niemen - Case 142, F-13397 Marseille Cedex, France

**Abstract:** The design of an UWB pulse generator is presented in the context of low cost applications. The pulse generator is fully integrated in a 0.13 $\mu\text{m}$  CMOS technology and achieves 1Vpp magnitude pulses with only 2.25pJ of energy consumed by pulse and 1.2V voltage supply. The generation method used in this design is well suited for packaged IC using wire bond interconnections and a co-design approach is proposed to preserve the signal integrity while increasing the pulse magnitude up to 1.4Vpp.

## RTUIF-06

### A 0.17-nJ/Pulse IR-UWB Receiver Based on Distributed Pulse Correlator in 0.18- $\mu\text{m}$ Digital CMOS

J.Hu, Y.Zhu, S.Wang, H.Wu, University of Rochester, NY

**Abstract:** This paper presents a low power IR-UWB receiver based on a reconfigurable, high speed analog correlator called distributed pulse correlator (DPC). The DPC incorporates built-in local template pulse generators, and hence significantly reduces the power consumption and circuit complexity of the analog correlation receiver. A chip prototype of the IR-UWB receiver was implemented in 0.18- $\mu\text{m}$  digital CMOS, and achieved an energy efficiency of 0.17-nJ/pulse at 250-MHz pulse rate in the measurement.

## RTUIF-07

### A Quadrature Charge-Domain Filter with Frequency Down-Conversion and Filtering for RF Receiver

Ming-Feng Huang, and Lai-Fu Chen, SoC Technology Center, Industrial Technology Research Institute, Taiwan, R.O.C.

**Abstract:** A quadrature charge-domain filter (QCDF) for frequency down-conversion and filtering is proposed. After measurement of QCDF by a 1072-MS/s sampling rate, a stop-band attenuation and bandwidth were 53-dB and 44-MHz, respectively. For quadrature performance after down-conversion, this QCDF provided -27.67-dB EVM upon a 64-QAM signal with 54-Mb/s. This chip consumed 7.7-mA power current upon a 1.2-V supply and occupied 0.08-mm<sup>2</sup> in 90-nm CMOS process.

## RTUIF-08

### A UHF Variable Gain Amplifier for Direct-Conversion DVB-H Receivers

Masoud Meghdadi, Mehrdad Sharif-Bakhtiar, AliMedi, Sharif University of Technology

**Abstract:** A CMOS fully differential UHF variable gain amplifier for use in a direct-conversion DVB-H receiver is presented. High linearity is achieved by reducing the trans-conductance of the input transistors for lower gain settings. Implemented in TSMC 0.18- $\mu\text{m}$  CMOS process, the inductorless RF VGA covers voltage gains from 15.5 dB to -6.5 dB with a maximum IIP3 of +24 dBm. The amplifier achieves a 3-dB bandwidth of 1.4 GHz and a minimum noise figure of 5.8 dB while drawing 3.6 mA from a 1.8 V supply.

## RTUIF-09

### A CMOS Resistive Feedback Single to Differential Low Noise Amplifier with Multiple-Tuner-Outputs for a Digital TV Tuner

Donggu Im, \*Ilku Nam, Seong-Sik Song, Hong-Teuk Kim, System IC Business Team, RF Part, LG Electronics Inc., Korea, \*School of EE, Pusan National University, Korea

**Abstract:** A CMOS resistive feedback single to differential low noise amplifier (S-to-D LNA) with single-ended multiple tuner outputs (MTOs) is implemented for a digital TV tuner. In order to achieve wideband output balancing with high gain, low noise figure and high linearity, the S-to-D LNA exploiting the resistive feedback with enhanced loop gain is designed. The single-ended MTOs are made by



combining the differential output without second-order distortion for supporting multiple tuner applications.

### **RTUIF-10**

#### **Two 24 GHz Receiver Front-ends in 130-nm CMOS using SOP Technology**

M. Tormanen, H. Sjolund, Lund University

**Abstract:** Two 24 GHz 130-nm CMOS receiver front-ends using System-on-Package (SOP) technology are demonstrated. CMOS dies featuring a two-stage LNA, a passive mixer, and output buffers are flip-chipped to a glass carrier featuring low loss baluns. One design uses glass baluns for both RF and LO input, whereas the other uses an active RF balun on-chip. The fully differential front-end measures; 20.7dB conversion gain, 7.8dB NF, -23.3dBm CP1dB, -12.6dBm IIP3, 16.3dBm IIP2, and 44dB LO to RF isolation.

### **RTUIF-11**

#### **A 0.13 $\mu$ m CMOS 2.5Gb/s FSK Demodulator Using Injection-Locked Technique**

Chao-Shiun Wang, Kun-Da Chu and Chong-Kuang Wang, Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan

**Abstract:** A low-power gigabits FSK demodulator using injection-locked technique is employed for 60GHz wireless communication systems. Fabricated in 0.13 $\mu$ m CMOS technology, this FSK demodulation only occupies a chip area of 0.5x0.65mm<sup>2</sup>. The demodulation input sensitivity is -16dBm at BER less than 10<sup>-9</sup> for uncoded 2.5Gbps 2<sup>31</sup>-1 PRBS data with 1GHz frequency deviation while consuming 6mW from a 1.2V supply.

### **RTUIF-12**

#### **A 5GHz LC VCO with Extended Linear-Range Varactor in Purely Digital 0.15 $\mu$ m CMOS Process**

Aleksander Dec, Hiroshi Akima, and Ken Suyama, Epoch Microelectronics, Inc., Tarrytown, NY, USA

**Abstract:** MOSFET varactors with two different threshold voltages are used for extending linear tuning range of a voltage controlled oscillator (VCO). This method is suitable for VCOs implemented in purely digital CMOS processes where MIM-capacitors are not available and only MOS transistors can be used for tuning element. The effectiveness of this technique is demonstrated in a 5GHz LC VCO with divide-by-2, output buffer, and integrated low-dropout voltage regulator.

### **RTUIF-13**

#### **A 5GHz Band Low Noise and Wide Tuning Range Si-CMOS VCO**

Tuan Thanh Ta, Suguru Kameda, Tadashi Takagi, and Kazuo Tsubouchi, Research Institute of Electrical Communication, Tohoku University, Japan

**Abstract:** In this work, a fully integrated 5GHz VCO is presented. The VCO is designed with 0.18 $\mu$ m mixed signal CMOS process. To achieve low phase noise, varactor circuit is designed to cancel effects of 1/f noise and fluctuation of capacitance due to harmonics. The proposed VCO has tuning range from 5.1-6.1GHz (17.9%) and phase noise lower than -110.8dBc/Hz at 1MHz offset over the full tuning range. Figure-of-Merit-with-Tuning-range of the proposed VCO is -182dBc/Hz.

### **RTUIF-14**

#### **Injection Locked Oscillator Arrays for Spectrum Analysis**

T.D. Gathman, J.F. Buckwalter, University of California at San Diego

**Abstract:** Injection locked oscillator arrays are described as a means of quasi-real-time spectrum analysis. Two oscillators with closely spaced frequencies at 5.1 and 5.8 GHz were designed such that single or simultaneous injection locking may occur depending on the injected frequency and power. Injection

sensitivity, isolation, and phase noise characteristics are described and measured. Only NMOS devices were used in a 0.12 $\mu$ m SiGe BiCMOS process

### **RTUIF-15**

#### **Design of a CMOS 12 GHz Rotary Travelling Wave Oscillator with Switched Capacitor Tuning**

F. Ben Abdeljelil (1,2), W. Tatinian (1), L. Carpineto (2), G. Jacquemod (1), (1) LEAT, UMR CNRS-UNSA 6071, Sophia Antipolis, France, (2) Entropic Communications, Sophia-Antipolis, France

**Abstract:** This paper presents the design methodology, simulation and measurement results of a CMOS 12GHz Rotary Travelling Wave Voltage Controlled Oscillator. The different simulations (electrical using SPICE and electromagnetical using HFSS) are presented. These results are compared to a theoretical approach and measurements. The oscillator has been fabricated in a 0.13 $\mu$ m RF-CMOS technology. The phase noise at a 1MHz offset from the carrier is -105dBc/Hz and the tuning range is 1.2GHz.

### **RTUIF-16**

#### **A Fast Automatic Frequency Calibration (AFC) Scheme for Phase-Locked Loop (PLL) Frequency Synthesizer**

Chan-Young Jeong, Dong-Ho Choi, Changsik Yoo, Integrated Circuit Lab, Department of ECE, Hanyang University, Seoul, Korea

**Abstract:** A noble automatic frequency calibration (AFC) scheme is proposed for phase-locked loop (PLL) based frequency synthesizer. For fast AFC operation, the frequency control code is updated right after the frequency difference is detected. The uncertainty of the phase relationship between the reference clock and VCO output is eliminated by comparing the divided VCO clock with two-phase reference clocks. The AFC is applied to a CMOS frequency synthesizer.

### **RTUIF-17**

#### **Multiple Supply (Class-G) Linear Modulator and PA for Non-CE Modulation**

J. S. Walling\*, S. T. Taylor\*\*, D. J. Allstot\*, \*University of Washington, Department of Electrical Engineering, \*\* Intel Corp.

**Abstract:** A class-G PA consisting of a class-E PA and class-G supply modulator is fabricated in a 130nm process. It operates from 1.65 and 3.3 V supplies and the die area is 2x2mm. It achieves a Pout of 29.2dBm with a PAE of 72%. It amplifies signals with p-to-a ratios of ~3-20dBm, or act as power control for constant envelope signals. It achieves an EVM value of 4.6%-rms for a root-raised cosine filtered, QPSK modulated signal and an average efficiency of 45%, compared to 17% for a similar class-B PA.

### **RTUIF-18**

#### **A Non-Uniform GaN Power TWA for 2 to 10 GHz Suitable for Square-Wave Operation**

C. Meliani, E. Ersoy, N. Chaturvedi, S. Freyer, J. Wuerfl, W. Heinrich, and G. Traenkle, Ferdinand-Braun-Inst. fuer Hoechstfrequenztechnik, Berlin - Germany

**Abstract:** A broadband GaN monolithic power amplifier covering the 2 to 10 GHz band is presented. It is based on a non-uniform traveling-wave architecture using 4 transistor cells with 4x125 mm gate width each. The amplifier achieves 7 to 11 dB small signal gain in the frequency band between 2 and 10 GHz. The circuit delivers between 2.5 and 4.5 W over the bandwidth from 2 GHz up to 10 GHz. In addition, large signal operation with square wave signals have been demonstrated at 1 and 2 Gbps.

### **RTUIF-19**

#### **A GSM-EDGE Power Amplifier with a BiFET Current Limiting Bias Circuit**

G. De la Rosa, D. Osika, N. Scheinberg, ANADIGICS Inc, Warren, NJ, 07059, USA



**Abstract:** A dual mode BiFET GSM-EDGE Power amplifier with built in current limiting circuitry is presented. The amplifier incorporates a bias circuit on the power stage that limits the base current of the HBT cells thus limiting the collector current to a predetermined level of 2.1 Amps. This novel scheme increases the ruggedness of the power amplifier when subjected to high mismatch conditions while maintaining matched load GMSK PAE and EDGE linearity. The amplifier operates in the 850/900 band.

## **RTUIF-20**

### **A Low-complexity GSM Baseband Detector for RF BIST**

I. Elahi, K. Muhammad, Texas Instruments Inc., USA

**Abstract:** We present a low-complexity digital baseband detector for GSM applications for functional RF BIST of the receiver section of a complex transceiver SoC implemented in 90-nm digital CMOS process. The detector can be used as a pass/fail criterion during factory testing using a Tx-Rx RF loopback mode or with an inexpensive signal generator. It can also be used for testing of the analog and digital base-band data paths of the receiver without requiring any external equipment.

## **RTUIF-21**

### **Including Pattern-Dependent Effects in Electromagnetic Simulations of On-Chip Passive Components**

S. Kapur, D. E. Long, T. L. Hsu\*, S. Chen\*, C. P. Jou\*, S. Liu\*, G. S. Chang\*, C. H. Yeh\*, H. T. Yang\*, Integrand Software, Inc., USA, \*Taiwan Semiconductor Manufacturing Corporation, Taiwan, R.O.C.

**Abstract:** In advanced IC processes, the physical properties of wires (width, thickness, and resistance) depends on the surrounding wiring. We modified the EMX electromagnetic simulator to allow width-and spacing-dependent properties to be given in the process description. EMX automatically modifies the drawn layout to mimic the fabrication process. We validate our approach by comparing to measurements and show a significant improvement in simulation accuracy for inductors and interdigitated capacitors.

## **RTUIF-22**

### **Scalable Electromagnetic Segmentation Methodology for Accurate Investigation of Inductive Couplings**

H. Kampe, S. Wane, Olivier Tesson, Hugues Murray\*, Philippe Descamps\* and Patrick Martin\*, NXP Semiconductors, \*LaMIPS: NXP-CRISMAT UMR 6508 CNRS ENSICAEN UCBN Microelectronic Laboratory, France

**Abstract:** Electromagnetic-based segmentation methodology is proposed for design, analysis and simulation of inductive couplings in RFICs. The methodology efficiency is demonstrated through its application to component and function-bloc test-carriers. The obtained results are successfully correlated to measurement results and other relevant methods and techniques. Guidelines and design rules towards standard segmentation-based scalable wideband model synthesis for EMI-aware design analysis are discussed.

## **RTUIF-23**

### **Accurate Closed-Form Capacitance Extraction Formulas for Metal Fill in RFICs**

S. G. Gaskill, V. S. Shilimkar, A. Weisshaar, Oregon State University

**Abstract:** Metal fill patterning in modern IC processes forces many floating metal structures to exist in the final design. The number of these structures makes electrostatic capacitance extraction difficult and the capacitance impact may be neglected or incorrectly approximated. In this paper closed-form, semi-empirical formulas are presented for a single layer of floating metal fill between two parallel plates. Maximum error was less than 1% for a wide range of metal fill dimensions in a 0.18 $\mu$ m process.

## RFIC PANEL SESSIONS

Monday, June 8 2009  
12:00 PM - 01:15 PM • Room 205B

### **RPM-A: Who Will Win the Battle for the Gigabit Wireless in your Home: WirelessHD, 802.11n, Wireless USB, or UWB?**

*Organizers:*     **C. Patrick Yue**, UC Santa Barbara  
                      **Albert Jerng**, Ralink

*Moderator:*     **C. Patrick Yue**, UC Santa Barbara

*Panel:*            **Srenik Metha**, Atheros  
                      **Huei Wang**, National Taiwan University  
                      **Joy Laskar**, Georgia Tech  
                      **Hung Nguyen**, Sigma Designs  
                      **Jeff Gilbert**, SiBeam  
                      **Jim Lansford**, Alereon

**Abstract:** The extraordinary growth in the HD multimedia market, during the last few years, has created an eminent need for truly seamless interconnectivity of the various home entertainment appliances, broadband content streaming machines and personal computing devices. According to DisplaySearch, the worldwide sales of HDTV topped US\$100B for the first time in 2007 with 200M units. Meanwhile, set-top box revenue reached 41M units in 2007 according to Instat. IDC projected a large leap in worldwide laptop shipments, from 108 million in 2007 to 148.2 million in 2008. Strategy Analytics estimated that 30M units of Blu-ray players will be sold in 2008, out of which 20M units are Play Stations 3 by Sony. Apple reported that since the launch of iStore, between July and September, more 100M iPhone software applications (US\$40M sales) have been downloaded - an unprecedented adoption rate by any measure. The common theme that all these trends shares is a massive increase in the amount of digital content and the desire to share them seamlessly.

To cater the connectivity demand, industry heavyweights and entrepreneurial warriors are pursuing a wide range of new technologies. Among them, the so-called "Gigabit Wireless" has received a great deal of attention because it can potentially solve the "spaghetti wire" problem. While the state-of-the-art WiFi using IEEE 802.11n can already offer data rate in excess of 480Mbps, a substantial gap still remains to reach the uncompressed HD video data rate requirement - ~3 Gbps. On the other hand, it remains an open question whether a multi-node networking protocol is indeed needed, or a simpler point-to-point wireless link will suffice.

The Gigabit Wireless experts on this panel - including technology leaders, academes - will assess the market potential, examine the technology landscape, and project the deployment horizon. The competing standards such as 60-GHz WirelessHD, IEEE 802.11n, wireless USB, UWB, etc. will be addressed.

## **RFIC PANEL SESSIONS (continued)**

Tuesday, June 9 2009  
12:00 PM - 01:15PM • Room 107B

### **RPTU-A: Will RFCMOS be Practical for 60GHz Radio and Beyond?**

*Organizer:*     **Lee Yang**, SMIC  
                     **Yang Xu**, IIT

*Moderator:*    **Yang Xu**, IIT

*Panel:*           **Simon Wong**, Stanford  
                      **Lawrence Larson**, UCSD  
                      **S. P. Voinigescu**, Univ. of Toronto  
                      **Ali Niknejad**, UCB  
                      **Helen Kim**, MIT Lincoln Labs  
                      **Basanth Jagannathan**, IBM

**Abstract:** The 60-GHz band is a free/unlicensed band which features a large amount of bandwidth and a large worldwide overlap. The large bandwidth means that a very high volume of information can be transmitted wirelessly. The large worldwide overlap results in interoperability around the globe. Multiple applications can benefit from this--wireless HDTV, wireless laptop docking stations, extremely fast downloading of files via wireless Gigabit Ethernet, wireless USB or other protocols, wireless telecommunications backhauls, etc.

Radio frequency (RF) ICs continue to benefit from advances in CMOS process technologies. Over the years, we have seen monolithic CMOS transceiver chips handling wider bandwidths to address the needs of cellular handsets. And packing more on-chip to offer system-on-a-chip (SoC) solutions for a variety of cellular and wireless bands. In reality, CMOS RF SoC chips are incorporating all the radio building blocks including the power amplifier, phase-locked loop (PLL) filter, and the antenna switch. Thus, CMOS continues to make strong inroads into the microwave territory, going well beyond 5 GHz. Now, the availability of unlicensed bands around 7 GHz and 60 GHz is motivating designers to make a giant leap and migrate deeper into this turf. These bands are intended to facilitate emerging applications like point-to-point wireless LANs, broadband Internet access, as well as automotive applications like short- (24 GHz) and longrange (77 GHz) radars for collision avoidance. Operation in these frequency bands was once the exclusive domain of III-V-compound semiconductors, such as gallium arsenide (GaAs) and indium phosphide (InP). However, aggressive scaling and corresponding improvements in CMOS and silicon germanium (SiGe) technologies is making history. What may have been considered unthinkable a decade ago is now becoming a reality. CMOS will continue its march into the microwave and millimeter wave turf slowly but steadily. And, the performance will only get better with time. However, for critical functions, it will depend on other technologies such as SiGe technology. Also, the debating never stops and a lot of people think that it could take some time for CMOS 60 GHz radios to be ready for the market. The need for multiple sources of chips and interoperability testing will stretch out the technology's time-to-market.

In this panel, we will gather the experts in the field of 60GHz radio development and discuss the status and challenges of 60GHz radio. The alternative technologies and circuit implementation trade-offs will also be debated in this panel.

## **IMS PANEL SESSIONS**

Tuesday, June 9, 2009  
12:00 PM - 01:10 PM • Room 109AB

### **System-On-Chip vs. System-On-Package for Emerging 3D Microsystems**

Wednesday, June 10, 2009  
12:00 PM - 01:10 PM • Room 107ABC

### **SiGe/CMOS RF-IC Phased Arrays: Will They be Used in Defense and Commercial Systems?**

Wednesday, June 10, 2009  
12:00 PM - 01:10 PM • Room 104ABC

### **Faster than Fiber: Enabling Multi-Gigabit Wireless Communication Links**

Thursday, June 11, 2009  
12:00 PM - 01:10 PM • Room 104ABC

### **A Return to the Classic Heterodyne Architecture for Integrated Transceivers?**

## WORKSHOPS AND SHORT COURSES

Workshops and Tutorials are offered on Sunday, Monday and Friday of Microwave Week. They are distinguished by the following features:

- Advanced Level Workshops (designated as WSA, WSB, etc.) present the state of the art to specialists who are already experienced in the topic area.
- Short Courses (designated as SC-1, SC-2, etc.) are targeted towards educating attendees in new areas of microwave technology, reviewing material that is primarily a revision of previously published information.

### RFIC SPONSORED SUNDAY WORKSHOPS AND SHORT COURSES

**08:00 AM-05:00 PM**

**BC&EC – Room 156AB**

#### **WSA: Advances in CMOS RF Power Amplifiers for Cellular and IEEE 802 Connectivity Radios**

*Full-day workshop reviewed by RFIC.*

*Organizers:* **Malcom Smith**, Amalfi Semiconductor, **Upkar Dhaliwal**, Future Wireless Technologies; MTT-20, **Stewart Taylor**, Intel

*Sponsor:* **RFIC**

**Workshop Abstract:** This workshop will present the latest design and developments in RF Module/RFIC power amplifiers, as well as covering the RF system requirements for Cellular and IEEE 802 connectivity power amplifiers. Until very recently CMOS power amplifiers were not mature enough to compete against other non-silicon technologies and could not be used widely in handheld cell-phones. With some new developments in device technologies, circuit solutions as well as system-level improvements, several companies have announced CMOS power amplifiers products with the ability to be used in mass-market handsets, PC cards, laptops and netbooks. Challenges remain in terms of output power, mismatch handling, thermal and DC performance for the power amplifier so that it may be integrated with the rest of the RF and in future with the baseband. This workshop will present and discuss the advantages, disadvantages and future of CMOS and silicon-based power amplifiers for Cellular (2G – GSM, EDGE, CDMA) (3G UMTS, HSDPA, DO1x) and IEEE 802 (WLAN/WiFi, WiMAX/WiBRO) connectivity power amplifiers.

*Speakers & Topics:*

1. **Michael Bailey**, Amalfi Semiconductor: “Utilizing Bulk CMOS Transistors for High Frequency Power Amplifiers”
2. **Ali M. Niknejad**, Berkeley Wireless Research Center (BWRC): “Low Voltage Transformer Coupled CMOS PAs”
3. **Rahul Magoon**, Axiom Microdevices: “The Integration of Cellular CMOS PAs with RF, Mixed Signal, and Digital Circuits on a Single Die Radio: Challenges and Opportunities”
4. **Susanne Paul**, Black Sand Technologies: “Class P Architectures in Linear 3G CMOS Power Amplifiers”

5. **Bumman Kim**, Pohang University of Science and Technology: “CMOS Linear Power Amplifier Design”
6. **Antonino Scuderi**, STMicroelectronics, Catania, Italy: “Multimode Digital CMOS PA for Polar Architectures”
7. **Dan Nobbe**, Peregrine Semiconductor: “Radio Frequency Front End Integration in UltraCMOS”
8. **Peter Gammel**, SiGe Semiconductor: “High Performance, Low Cost .35 $\mu$ m SiGe BiCMOS Dual-Band Integrated RF front end ICs for WLAN Applications”
9. **Chris D. Hull**, Intel Corporation: “A WiMAX Power Amplifier in 90nm CMOS Technology”

**08:00 AM-05:00 PM**

**BC&EC – Room 151AB**

### **WSB: Current and Future Trends in Frequency Generation Circuits**

*Full-day workshop reviewed by RFIC.*

*Organizers:* **Waleed Khalil**, Intel; RFIC TPC, **Ahmed Helmy**, Intel

*Sponsor:* **RFIC**

**Workshop Abstract:** In order to adapt to the highly competitive IC market, chip suppliers are racing to reduce the total chip count by integrating many functionalities onto a single IC. However, one of the few elements that escaped this integration and remains to be off-chip is the timing source. In both wireless and wired systems, the reference source requires varying degrees of accuracy and stability over time and temperature. More often these accuracy requirements can only be met by using externally compensated reference sources such as (TCXOS) or (VCXOS), which occupy a large fraction of the board space. Hence a large emphasis is placed on eliminating these components by either integrating their functionality on-chip or replacing them with a much smaller footprint solution. This workshop will review various aspects in the design of stable and low phase noise oscillator circuits. Solutions that are gaining more popularity such as (DCXOS), MEMS and self-referenced oscillators will also be presented.

*Speakers & Topics:*

1. **Michael M. Driscoll**, Northrop Grumman : “Introduction to the Design and Performance of Quartz Crystal Oscillators”
2. **Michael McCorquodale**, Mobius Microsystems : “Self-Referenced CMOS Oscillators”
3. **Ayman Ahmed**, Si-Ware Systems : “Temperature Compensation Techniques of Crystal-less Reference Oscillators”
4. **Justin Black**, Harmonic Devices Inc.: “Emerging Piezoelectric MEMS Resonators for Clock Synthesis”
5. **Eric Klumperink**, University of Twente : “Recent Advances in Low-Jitter CMOS Clock Generation Stimulated by FoM Definitions”
6. **Kenneth. K. O**, University of Florida : “Millimeter-wave Signal Generation in CMO
7. **Mona M. Hella**, Rensselaer Polytechnic Institute : “Recent Advances in Multi-Standard Oscillator Design”

**WSC: Advances in PA and TX Architectures**

*Full-day workshop reviewed by RFIC.*

*Organizers:*       **Patrick Reynaert, K.U.Leuven**, Belgium, **Dominique Schreurs, K.U.Leuven**, Belgium; AdCom, MTT-11, IMS TPC

*Sponsor:*         **RFIC**

**Workshop Abstract:** Although most PA and TX architectures (Doherty, Polar, outphasing, LINC, ...) have been envisioned several decades ago, there is not a clear winner today. Technology considerations (GaN, CMOS, SiGe,...), system level considerations (output power, bandwidth,...), implementation and packaging issues and the specific cost or business model (base stations, terminals,...), make the optimal choice less obvious. This workshop will cover the different solutions that exist today for PA and TX architectures. It will discuss the different trade-offs and implementation issues of the various architectures, crucial information when selecting the architecture of choice. All speakers will also give an outlook of new PA architectures that are being developed in their field.

*Speakers & Topics:*

1. **Steve C. Cripps**, Cardiff University, United Kingdom: "Old Dogs and New Tricks in the Pursuit of Higher RFPA Efficiency"
2. **John Gajadharsing**, NXP, Netherlands: "Recent Advances in Doherty Amplifiers for Wireless Infrastructure"
3. **Leo de Vreede**, T.U.Delft, The Netherlands: "Enhanced LINC/Chireix Power Amplifiers"
4. **Dave Kelly**, PulseWave RF, USA: "Carrier Frequency Switch Mode Amplification and Linearization"
5. **Georg Fischer**, University of Erlangen / Alcatel-Lucent, Germany: "Practical design and implementation challenges of the Class-S PA"
6. **Earl McCune**, Panasonic Emerging Advanced RF Laboratory (PEARL), USA: "Polar modulation and power amplifiers"
7. **Patrick Reynaert**, K.U.Leuven ESAT-MICAS, Belgium: "CMOS RF Power Amplifiers"
8. **Gottfried Magerl**, TU Vienna, Austria: "Class F Amplifiers"
9. Panel discussion with speakers and attendees.

**08:00 AM-05:00 PM**

**BC&EC – Room 157C**

## **WSD: Self-Interference and Co-Habitation Considerations in Complex SoC and SiP Integrated Solutions**

*Full-day workshop reviewed by RFIC.*

*Organizers:* **Jan Niehof**, NXP Semiconductors., **Oren Eytan Eliezer**, Texas Instruments.

**Paul Blount**, Custom MMIC Design Services; RFIC TPC.

*Sponsor:* **RFIC**

**Workshop Abstract:** With the integration of RF, mixed signal and digital building blocks on a single die, combined with the trend of increased frequencies (both in the RF and in the digital circuitry), it is essential to consider various on-chip coupling effects in the early design phases of the RF SoC or SiP. Additionally, provisions should be made for mitigating the impact of peripheral interactions (e.g., package, antenna), as well as the potential for self-interference, such that these are either eliminated or can be resolved on the fabricated product without hardware redesign. The focus of this interactive workshop will be on resolving self-interference problems: on-chip coupling effects, chip-package co-design, substrate issues, coupling-aware RFIC floor planning, digitally assisted solutions for interference problems, design practices, modeling and CAD/EDA capabilities to address coupling effects. Recognized companies and partnerships active in the semiconductor industry will present actual issues encountered in their designs and the solutions/design-practices used to address them. Interactive discussions will be facilitated to exchange valuable ideas for the benefit of participants and the industry at large.

### *Speakers & Topics:*

1. **Jonathan Jensen**, Intel: “Single Chip Radio Design; Thinking Beyond the Circuits and the Silicon”
2. **Stephane Bronckers**, IMEC: “A Novel Methodology to Predict the Impact of Substrate Noise in Complex Analog/RF Systems”
3. **Scott Morris**, RFMD: “Innovative Techniques for Shielding RF Components at the Package Level”
4. **Matthias Locher**, ST-Ericsson: “Bottom-up Coexistence Physical Design and Verification Approach for Multi-Standard SoCs”
5. **Nikos Haralabidis**, Broadcom: “SoC System and Physical Design Approach for Co-Existence of Transceivers of Multiple Standards”
6. **Jan Niehof**, NXP Semiconductors: “Dealing with Physical Design Issues in Complex RF Applications”
7. **José Luis González**, Universitat Politècnica de Catalunya: “Substrate Noise Interference in RF Integrated Circuits”
8. **Francois Clement**, Coupling Wave Solutions: “Electrical Signal Integrity Analysis in Mixed-Signal and RF ICs”
9. **Oren Eliezer**, Texas Instruments: “A Design Approach and Techniques for the Mitigation of Self-Interference in Transceiver SoCs”



**WSE: Advanced BAW-Enabled Wireless Transceivers:  
From Devices to System Architecture**

*Full-day workshop reviewed by RFIC.*

*Organizers:*       **Andreas Kaiser**, IEMN-ISEN, **Andreia Cathelin**, ST Microelectronics,  
                             **Edgar Schmidhammer**, EPCOS AG

*Sponsor:*           **RFIC**

**Workshop Abstract:** Bulk Acoustic Wave (BAW) resonators are now being used in functions such as filters or duplexers, namely for US-based PCS system. Key-advantages of this technology are reduced size and cost at good performance. This workshop will discuss recent advances in the technology and at the device level, such as zero temperature drift, multiple frequency bands on the same wafer, improved power durability, and increased quality factors. Combined with advanced packaging technologies, modules with high functionality can be realized. Beyond replacing other filtering technologies, BAW technology can have a significant impact on system architectures, and will allow novel approaches namely for low power radios. BAW resonators also have a strong potential as high-precision frequency references where they could advantageously replace quartz resonators for this purpose. All these points, as well as design tools and methodology, will be described by the speakers in this workshop.

*Speakers & Topics:*

1. **Alexandre Reinhardt**, CEA-LETI, “BAW Technology for Advanced RF Architectures”
2. **Florin Constantinescu**, Politehnica University Bucharest, Romania, “Circuit and Field Models of Power BAW Resonators”
3. **Arto Nurmela**, VTT, “Power Durability and Non-Linear Effects in BAW Resonators”
4. **Eric Kerhervé**, IMS Bordeaux, “An Operant Methodology to Handle BAW Designs: Application to a WCDMA/UMTS Duplexer”
5. **Eric Tournier**, LAAS, “Phase Noise of FBAR/SMR Resonators - Application to Frequency Generation and Measurement”
6. **Andreia Cathelin**, STMicroelectronics, “BAW Enabled Advanced Digital RF Transmitter Architectures for Wireless Systems”
7. **Alexandre Volatier**, Triquint Semiconductor, “A High Performance PCS Front End Module Incorporating a BAW Duplexer and a Tri-Mode Power Amplifier for a Fully Integrated CDMA/WCDMA Transmit Module Solution”
8. **Rich Ruby**, Avago, “Future Extensions of FBAR Technology”
9. **Jan Rabaey**, University of California - Berkeley, “Innovative Use of BAW Resonators in Low-Power Transceivers”

**WSF: Devices and Design Techniques for Advanced Handset/Mobile PAs**

*Full-day workshop reviewed by RFIC.*

*Organizers:*       **Nick Cheng**, Skyworks Solutions; RFIC TPC, **David Ngo**, RF Micro Devices; RFIC TPC Co-Chair

*Sponsor:*         **RFIC**

**Workshop Abstract:** During the past decade, cellular handsets have moved from single-band, single-mode platforms to very complex multiband, multimode architectures that optimize carrier capacity flexibility, support numerous geographic air-interface standards and enable more multimedia features. The ever-increasing complexity in cellular handsets has been imposing more and more stringent requirements on power amplifiers. Advancements in both device technology and design techniques have been escalating in addressing critical issues such as efficiency, linearity, noise, harmonics, switching transient, to name a few. Several presentations in this workshop will cover future handset trends, requirements on advanced power amplifiers and choice of device technology. Furthermore, design techniques of linearization, efficiency enhancement, power detection and controls will be covered with design examples demonstrated on various technologies such as GaAs HBT, CMOS, Silicon-on-Insulator and Silicon Germanium.

*Speakers & Topics:*

1. **Ville Vintola, Nokia**, “Handset Trends and Advanced PA Requirements”
2. **Peter Zampardi**, Skyworks Solutions, “Device Technology for Handset Power Amplifiers”
3. **Ali Hajimiri**, California Institute of Technology, “Fully Integrated CMOS PAs for the Handsets”
4. **Ali Tombak**, RFMD, “Highly Integrated Wireless Handset Front-End Modules Based on Bulk Silicon and Silicon-on-Insulator (SOI) Technologies”
5. **Youngwoo Kwon**, Seoul National University, “Low-Power PAE Enhancement for 3G Handset Power Amplifiers”
6. **Donald Lie**, Texas Tech University, “SiGe PA for WLAN/WiMax and Handset Applications”
7. **Leo de Vreede**, Delft University of Technology, “Out-Of-Band Linearization of Semiconductor Devices”
8. **David Ripley**, Skyworks Solutions, “Power Detection and Control for Handset Power Amplifiers”

**WSG: Challenges for Future RF Integration**

*Full-day workshop reviewed by RFIC.*

**Organizers:** **Gernot Hueber**, DICE GmbH & Co KG, **R. Bogdan Staszewski**, Texas Instruments, **Stefan Heinen**, RWTH Aachen University; MTT-23, RFIC TPC

**Sponsor:** **RFIC**

**Workshop Abstract:** Current and future transceivers for mobile terminals are facing increasing complexity because of the market's demands for lower cost, lower power consumption, and higher data-rate. As a result, multi-band and multi-mode radios covering the diversity of communication standards impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications. The focus of this workshop will be on the challenges the cellular standards pose on future transceiver integration, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in SoC approaches including novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules, and the integration of digital signal processing into the traditionally purely analog front-end. However, the utilization of digital signal processing capabilities is in line with the ongoing trend towards SoCs in minimum-feature-sized CMOS in the cellular market. Moreover, advances in the field of RF front-end modules and novel analog signal processing architectures are covered to give a consolidated outlook on future concepts for cellular radios.

*Speakers & Topics:*

1. **Larry Larson**, University of California, San Diego, USA, "Multi-Mode/Multi-Band Transmitters and Power Amplifiers"
2. **Bertan Bakkaloglu**, Arizona State University, USA, "Reconfigurable Transmitters and Power Management"
3. **Geoff Dawe**, BitWave Semiconductor, Lowell, MA USA, "Software Defined (Configured) Radio Transceivers"
4. **Ranjit Gharpurey**, University of Texas at Austin, USA, "Interference Cancellation and Linearity Enhancement in Wireless Receiver Front-ends"
5. **Aarno Pärssinen**, Nokia Research Center, Helsinki, Finland, "RF System and Architecture Challenges for Multi-Standard Mobile Devices"
6. **Sebastian Hoyos**, Texas A&M University, USA, "Multi-Path Receivers Architectures for Wideband Multi-Standard Radios"
7. **Aaron Partridge**, SiTime, Sunnyvale, CA USA, "System Architecture For Embedded MEMS Frequency References"
8. **Yann Deval**, IMS Laboratory, Talence Cedex, France, "Toward Software Radio Receiver"
9. **Robert Bogdan Staszewski**, Texas Instruments, Dallas, TX USA, "Advances in Digital RF Architectures"

**08:00 AM-12:00 PM**

**BC&EC – Room 152**

## **WSH: System-Level Design and Implementation of Gb/s 60GHz Radios**

*Half-day workshop reviewed by RFIC.*

*Organizers:*       **Alberto Valdes Garcia**, IBM Research, Yorktown Heights, NY, USA ,  
                             **Su-Khiong Yong**, Samsung Electronics, San Jose, CA, USA

*Sponsor:*           **RFIC**

**Workshop Abstract:** In recent years, the design of active and passive mm-wave components in general, and in the 60GHz band in particular, has become a center of gravity for academic and industrial research. The time has come to move beyond circuit components and fulfill the motivation for the development of this technology: the deployment of commercial solutions capable of delivering Gb/s wireless links in a variety of applications. A successful Gb/s 60GHz radio module is the result of holistic design. These contemporary systems push the boundary not only of RF design, but also of DSP techniques, and communication systems. This workshop brings to IMS-RFIC 2009 the experts leading the standards, design and system integration for 60GHz commercial solutions. The physical layer design and specifications for key applications, such as high-definition video and fast download, are covered considering both single-carrier and OFDM modulations. The pros and cons of each signaling scheme for different usage scenarios are analyzed. The impact of RF circuit non-idealities in these systems is also addressed. Full system implementation examples, including radio and baseband, are presented and illustrated with 60GHz end-to-end systems and link experiments. One of the specific challenges and opportunities of 60GHz is the directionality of the transmitted energy that can be enhanced and steered through the use of beamforming. While different RF implementations of phased-arrays are available in contemporary literature, the impact of beamforming on a high data rate communication system is less understood. This workshop will cover this crucial aspect from a system viewpoint. All of the presentations will address how these important aspects of 60GHz systems are addressed by the emerging standards such as the IEEE 802.15.3c 60GHz standard.

### *Speakers & Topics:*

1. **Shu Kato**, NICT/Tohoku University, Japan, “Overview of 60GHz Standardization and Single-Carrier System Design for Fastdown-Load Applications”
2. **Yasunao Katayama**, IBM Tokyo Research Laboratory, Japan, “End-to-end 60GHz Single-Carrier System Implementation and Link Experiments”
3. **Su-Khiong Yong**, Samsung Electronics, USA, “OFDM System Design for 60GHz High-Definition Video Applications”
4. **Chang-Soon Choi**, IHP Microelectronics GmbH, Germany, “60-GHz SiGe BiCMOS Radio and OFDM Baseband Implementation for Gbps WLAN Applications”
5. **André Bourdoux**, IMEC, Belgium, “Beamforming at 60GHz: Challenges and Solutions”

**01:00 PM-05:00 PM**

**BC&EC – Room 152**

## **WSI: Technology and Power Combining Techniques for Millimeter-Wave Applications**

*Half-day workshop reviewed by RFIC.*

**Organizers:** **Didier Belot**, STMicroelectronics; RFIC TPC, **Eric Kerhervé**, IMS Lab  
**Sponsor:** **RFIC**

**Workshop Abstract:** This workshop highlights the difficulties in designing silicon power amplifiers at MMW and RF frequencies. The presentations will focus on the limitations of CMOS, BiCMOS, bipolar and other advanced silicon technologies. In a second part, innovative design approaches such as power-combining techniques will be discussed in order to address the drastic specifications of radio communications from mobile phone standards (GSM, UMTS, WIMAX, WLAN...) to MMW standards (60GHz WMAN, 77GHz radar ...).

*Speakers & Topics:*

1. **Georg Boeck**, TU Berlin , “PAs for MMW Applications: A Comparison of Technologies and Achievements”
2. **Ullrich Pfeiffer**, University of Wuppertal , “Innovative Power Combining Structures for MMW PA”
3. **Debopriyo Chowdhury**, University of California , “Matching Techniques from RF to MMW Silicon PA”
4. **Christine Raynaud**, STMicroelectronics - CEA LETI , “Advanced CMOS (sub-0.25 $\mu$ m) Technologies for RF and MMW PA”
5. **Domine Leenaerts**, NXP Semiconductors, Research , “Power Amplifier Design in CMOS Technology for Cellular and WLAN”

**08:00 AM-12:00 PM**

**BC&EC – Room 51**

## **WSJ: Active Radio Circuits for Bio & Medical Applications**

*Half-day workshop reviewed by RFIC.*

**Organizers:** **Jacques Rudell**, University of Washington, Seattle, WA USA, **Donhee Ham**, Harvard University, Cambridge, MA USA, **Brian Otis**, University of Washington, Seattle, WA USA  
**Sponsor:** **RFIC**

**Workshop Abstract:** Scientists and engineers have spent the better part of the last century developing more efficient radio circuits, systems and software for wireless communication. Recently, the scientific community has begun exploring the use of radio-frequency circuits for biomedical applications. These bio-compatible radio circuits can be categorized into two sub-topics. The first is the use of radios to communicate sensed information from the human body to the outside world. The second is the use of traditional radio circuits for medical analysis. Two speakers in this workshop will explore using radio circuits for biomedical sensing and diagnosis, such as early-cancer detection and Protein and DNA analysis. Two additional speakers will describe current work on communication with radio links for body area networks (BAN) and implantable devices.

*Speakers & Topics:*

1. **Arjang Hassibi**, University of Texas, Austin “Challenges in CMOS Integrated Biosensors”
2. **Brian P. Otis**, University of Washington, Seattle, “BANning Low Power Radio Design”
3. **Joel L. Dawson**, Massachusetts Institute of Technology, Cambridge, MA, “A New Architecture for Implantable Transceivers”
4. **Donhee Ham**, Harvard University, Cambridge, MA , “NMR-Based CMOS RF Biomolecular Sensor”

**01:00 PM-05:00 PM**

**BC&EC – Room 156C**

**WSK: Digitally Assisted Analog and RF Circuits**

*Half-day workshop reviewed by RFIC.*

*Organizers:* **Joel L. Dawson**, Massachusetts Institute of Technology, **Stewart Taylor**, Intel, **Josie Ammer**, Qualcomm

*Sponsor:* **RFIC**

**Workshop Abstract:** The purpose of this workshop is to push forward the discipline of digitally assisted analog and RF design by taking a snapshot of the cutting-edge work going on in this field. Rather than hunt through the various journals and conference proceedings to piece together design trends, we offer attendees the chance to hear oral presentations from several of the leading experts in this young field. The workshop format is particularly advantageous for this topic, as in our view many of the breakthroughs in digitally assisted RF will find inspiration from similar work going on in analog design, and vice versa. Attendees will get a chance to hear about and ask questions concerning published work, and will also get a glimpse at cutting-edge but as-yet-unpublished work. Most importantly, attendees are encouraged to share their own thoughts and expertise concerning the techniques that are discussed. We expect the open exchange to benefit presenters and listeners alike.

*Speakers & Topics:*

1. **Joel L. Dawson**, Massachusetts Institute of Technology, “Digitally Assisted Architectures for RF Transceivers”
2. **Boris Murmann**, Stanford University, “Overview of Digital Correction Techniques for High-Speed Data Converters”
3. **Oren Eliezer**, Texas Instruments, “Software-Based Dynamic Compensation for Analog Impairments and for Interference Effects in Wireless Transmitters”
4. **Larry Larson**, University of California at San Diego, “Digitally Assisted Transmitter Technology for Wireless Transmitters”
5. **Michael P. Anthony**, Intersil Corporation , “Mixed Digital/Analog Correction of Mismatch and Process Variability in a Pipeline ADC”

## IMS/RFIC SPONSORED SUNDAY WORKSHOPS AND SHORT COURSES

**01:00 PM-05:00 PM**

**BC&EC – Room 153C**

### **WSL: State-of-the-Art of Low-Noise III-V Narrow-Bandgap and Silicon FET Technologies for Low-Power Applications**

*Half-day workshop reviewed by MTT-14, MTT-7, MTT-23.*

*Organizers:* **Francois Danneville**, IEMN-DHS, UMR CNRS, France; MTT-14, IMS TPC  
**Paulius Sakalas**, CEDIC, Dresden University of Technology, Germany;  
MTT-14

*Sponsor:* **IMS/RFIC**

This workshop aims to investigate various state-of-the-art low-noise FET technologies for low-power applications: (i) narrow-bandgap III-V HEMTs technologies (on InP or GaAs substrate) (ii) Si CMOS Technology. The first part will focus on InGaAs/InAlAs and Antimonide-Based Compound Semiconductor (ABCS) InAs/AlSb HEMTs. Devices specifically designed to operate at lower DC power consumption, or for low-noise operation, will be presented along with corresponding characterizations (models extraction). Their capability will be shown through ultra-low power MMIC (or hybrid) circuits, including low-noise amplifiers (operating at room and cryogenic temperatures) and switches in cm/mm-wave range. Strengths and limitations of such technologies will also be addressed. The second part will focus on Si CMOS technology. Millimeter-wave LNA will be presented with recent advances concerning CMOS mm-wave building blocks. Special attention will be paid on particular techniques taking advantage of CMOS technology while circumventing its weaknesses. Finally, a new scheme to optimize RF noise of MOSFETs through channel engineering will be described in detail.

#### *Speakers & Topics:*

1. **Jan Grahn**, Chalmers University of Technology, Göteborg, Sweden, “Narrow-Bandgap InGaAs/InAlAs and InAs/AlSb HEMTs for Low-Noise and Low-Power Applications”
2. **Jonathan Hacker**, Teledyne Scientific, “Antimonide Based Compound Semiconductors (ABCS) for Ultra-Low Power Applications”
3. **Tatsuya Hirose**, Fujitsu Ltd., “InP HEMT and Si-CMOS Device and Circuit Design for mm-Wave Low-Noise Applications”
4. **Ali Niknejad**, University of California - Berkeley, “Recent Advances in CMOS mm-Wave Building Blocks”
5. **Francois Danneville**, IEMN-DHS, UMR CNRS, “Noise Properties of Low-Power Si MOSFETs Through Different Channel Engineering”

## **IMS/ATRFG SPONSORED WORKSHOPS AND SHORT COURSES**

(all workshops held in BC&EC)

### **Full Day Workshop 08:00am-05:00pm**

CodingRoom	Day	Description
SC4 51	Sun	Doherty RF Power Amplifiers, Theory and Practice
SC5 50&51	Mon	Low Phase Noise Oscillators, Lecture and Laboratory
WMA 151AB	Mon	Tunable RF-Components and Modules For Wireless Communication Systems
WMB 157C	Mon	Parameter Extraction Strategies for Compact Transistor Models
WMC 153AB	Mon	Power Amplifier Linearization: From Advanced Analog and Digital Techniques to Practical Real-Time Implementations
WMD 156AB	Mon	Digital Receiver Systems for Defense and Related Commercial Applications
WME 153C	Mon	Subharmonically Pumped Mixers (SHP Mixers): Design Theory and Systems Applications
WMF 157AB	Mon	Is GaN Ready for System Insertion?
WMG 156C	Mon	New Component Technologies for Vehicular Radar Applications
WMH 152	Mon	Radio-Frequency Applications of Nanotechnology: Towards a New Generation of Extremely Integrated Devices and Systems
WFA 151B	Mon	EM-Based Microwave Optimization Technology: State of the Art and Applications
WFB 152	Mon	Modern RFID: Inkjet Printing of “Green” RFID and RFID-enabled Sensors on Flexible Substrates
WFC 156C	Mon	Recent Advances in Microwave Power Applications and Techniques (RAMPAnT)
WFD: 153AB	Mon	Emerging Applications of RF-MEMS
WFE 156A	Mon	Stability of Nonlinear Microwave Circuits and Systems: Concepts, Analysis, and Design

### **Half Day Workshop 08:00am-12:00pm**

CodingRoom	Day	Description
SC1 50	Sun	Advances in the Design of Electrically Small Antennas
SC5A 50	Mon	Low Phase Noise Oscillators, Theory and Design Only
WWB 152	Wed	RF Design Components of Magnetic Resonance Scanners

### **Half Day Workshop 01:00pm-05:00pm**

CodingRoom	Day	Description
SC2 50	Sun	RFID Transponders and Systems Design
SC3 51	Sun	Short-Range Wireless Networking Standards
WMI 154	Mon	Gigabit Packaging of Wireless 60GHz Links
WWC 152	Wed	Advanced Measurement Techniques, Adapted for Different Memory Effects
WWD 151AB	Wed	RF MEMS Testing, Reliability, and Power Handling



---

## REGISTRATION CATEGORIES

---

NEW for 2009, the Registration process is now split into three tiers in order to better serve attendee needs. The 1st tier is the Early Bird Registration, Monday, February 2 through Friday, May 15. This period provides an opportunity to register for the Symposium at the lowest possible cost. The 2nd tier or Advance Registration is Saturday, May 16 through Friday, June 5. The 3rd and final tier is the On-Site Registration, from the first day of Microwave Week, ending on Friday, June 12.

- Early Bird, Feb 2-May 15 (midnight EST)
- Advance, May 16-June 5 (midnight EST)
- On-Site, June 6-June 12 (through Microwave Week)

### NEW Symposium SUPERPASS

Also NEW for 2009 is the Symposia SUPERPASS. For one low price, registrants can attend as many technical sessions as they can from any of the three contributing organizations, MTT, RFIC, and ARFTG, as well as attend one full-day workshop (or two half-day workshops, if desired). In addition, the SUPERPASS will allow you to attend the Awards Banquet on Wednesday and a new Thursday Evening Social. The SUPERPASS is a SUPER DEAL offering a 15% discount over the combined ala-carte pricing.

### EARLY BIRD REGISTRATION

Early Bird Registration rates provide significant savings from the on-site fees shown on the enclosed registration insert. Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and Exhibition Hall. This form is not used for guest tour registration, see page 74 for information on registration for tours and special events. Each registrant must submit a separate form with payment. Registration by telephone is available for handicap, special needs, or information; please call 303-530-4562.

### ① METHODS OF REGISTRATION

Individuals can register online, by FAX, or by mail. All forms of registration, including mail registrations must be received at MP Associates by the deadline; otherwise, advance or on-site fees will be charged. If the registration is sent by FAX, do not send it by mail. Additional items can be added on site after advance registration. For phone numbers outside the US, please include a country code. An optional complimentary badge for one guest allows access to the Hospitality Suite, Plenary Session, and Exhibition Hall, but does not allow access to Technical Sessions and Workshops.

### ② MEMBERSHIP

Check boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and wish to take advantage of member rates, call 1.800.678.IEEE or visit [www.ieee.org/services/join](http://www.ieee.org/services/join) prior to registering.

### ③ SYMPOSIA

Microwave Week hosts three conferences: the International Microwave Symposium (IMS), the RF Integrated Circuits Symposium (RFIC), and the Automatic RF Techniques Group Conference (ARFTG). Membership in IEEE or ARFTG entitles students, retirees, and Life Members discounts on some registration fees (member price applies where discount not indicated).

- IMS Technical Sessions are held on Tuesdays, Wednesday, and Thursday. Registration includes breakfast, admission to the exhibits, abstract books, and a CD-ROM.

---

## REGISTRATION CATEGORIES (continued)

---

- RFIC Technical Sessions are held on Monday and Tuesday. Registration includes breakfast, admission to the RFIC, Reception, and Exhibition
- ARFTG Technical Sessions are held on Friday. Registration includes breakfast, a CD-ROM, and admission to the ARFTG Exhibition. ARFTG conference member rates are available to ARFTG and IEEE members.
- Microwave Week hosts the largest exhibition of its kind with over 500 companies. Exhibit only registration is available on site for \$25.

### Special Offers:

- Free Wednesday afternoon exhibit only registration admits you to Exhibit Hall from 12:00pm to 07:00pm, includes the Industry Hosted Reception.
- Free Thursday one day Technical Registration for retirees.

### ④ EXTRA CD-ROMS AND DIGESTS

Additional CD-ROMs (IMS, RFIC, and ARFTG) and digests (RFIC only) are available for purchase and pickup at the conference. After the Symposium, these digests and CD-ROMs will be available for purchase from IEEE.

### ⑤ AWARDS BANQUET

The MIT Awards Banquet will be held on Wednesday, 07:00pm to 10:00pm, in the BC&EC Grand Ballroom. Banquet details are presented on page 79. The new Thursday Evening Social will feature a cruise in Boston Harbor. For details see page 76.

### ⑥ BOXED LUNCHES

Optional boxed lunches are available for purchase by all attendees and for those attending the panel sessions or exhibition hall during lunchtime. Refunds for lunches are not available.

### ⑦ WORKSHOPS and SHORT COURSES

The workshop fee includes a CD-ROM and speakers' notes for that workshop. Full-day workshops include a continental breakfast, a morning refreshment break, a boxed lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, a morning refreshment break, and a boxed lunch. Afternoon workshops include a boxed lunch and afternoon refreshment break. The All-Workshop DVD-ROM fee includes material for all RFIC and IMS workshops on one DVD-ROM, but the DVD-ROM price alone does not include admission to any workshops. Note that there are two NEW options for 2009. \*First, registrants can save by selecting a combined Workshop (one full day or two half-day workshops) and All Workshop DVD-ROM. And second, for those who might not be able to attend the RFIC workshops, an All RFIC Workshop Only CD-ROM is now offered. The short course fee includes a CD-ROM (color PDF notes and in some cases software) and speakers' hardcopy notes for that short course. Breakfast, lunch, and breaks are included the same way as for workshops.

### ⑧ REMITTANCE

Individual remittance must accompany the registration form and is payable in US dollars only, using a personal check drawn on US bank, traveler's check, international money order, or credit card (VISA, Mastercard, or American Express only). Personal checks must be encoded at the bottom with the bank, bank account number, and check number. Bank drafts, wire transfers, cash, and purchase orders are UNACCEPTABLE and will be returned. Make checks and money orders payable to "IEEE/MIT-S". Written requests for refunds will be honored if received by May 1 2009. See page 74 for full refund policy. IMS Alumni Between Jobs Please email inquiries for fee consideration to: [alumni.request@ims2009.org](mailto:alumni.request@ims2009.org).

---

## ON-SITE REGISTRATION

---

### ON SITE REGISTRATION

On Site registration for all Microwave Week events will be available in the BC&EC Main Lobby. Registration hours are:

Saturday, June 6, 2009	02:00pm - 06:00pm
Sunday, June 7 2009	07:00am - 06:00pm
Monday, June 8, 2009	07:00am - 05:00pm
Tuesday, June 9 2009	07:00am - 05:00pm
Wednesday, June 10 2009	07:00am - 06:30pm
Thursday, June 11 2009	07:00am - 03:00pm
Friday, June 12 2009	07:00am - 09:00am

### EXHIBIT ONLY REGISTRATION

Exhibit-only registration is available on site for \$25.

### GUEST TOUR REGISTRATION

Registration for guest tours can be made in advance at [ims2009.org/guest\\_html](http://ims2009.org/guest_html) and will be available on site in the BC&EC lobby. Please refer to the Guest Program section (pages 77 to 79) of this program book for further details and tour descriptions.

### PRESS REGISTRATION

Credentialed press representatives are welcome to register without cost, receiving access to technical sessions and exhibits. Digests are not included. The Press Room is located in the BC&EC and will be open from Tuesday thru Friday.

### ARFTG REGISTRATION

Late on-site registration will be available at the BC&EC lobby on Friday from 07:00am to 11:00am. If at all possible, please pre-register earlier in the week to avoid last minute queues.

### REFUND POLICY

Written requests received by May 1 2009 will be honored. **Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled.** This policy applies to the registration for the symposium sessions, workshops, digests, extra CD-ROMs, awards banquet and boxed lunches. Please state the pre-registrants name and provide an postal address for the refund check. If registration was paid for by credit card, the refund will be made through an account credit. An account number must be provided if the initial registration was completed on-line. Address your requests to:

**Nannette Jordan**  
**MP Associates, Inc.**  
**1721 Boxelder Ste. 107**  
**Louisville, CO 80027**  
**[nannette@mpassociates.com](mailto:nannette@mpassociates.com)**

## ON-SITE REGISTRATION (continued)

REGISTRATION FEES	IEEE or ARFTG Membership	Student Retiree Life Member	Non- Member
<b>Super Pass</b> All IMS, RFIC and ARFTG Sessions, Award Banquet, Thursday Evening Social and all Workshop DVD (RFIC/IMS) plus Full Day (or 2 Half Day) Workshop Attendance	\$1,295	\$745	\$1,895
<b>IMS</b> All IMS Sessions All IMS Sessions (No CD ROM) Single Day Registration	\$525 \$450 \$275	\$85	\$785 \$665 \$385
<b>RFIC Symposium</b> All RFIC Sessions RFIC Reception Only	\$270 \$65		\$400 \$85
<b>ARFTG Conference</b> All ARFTG Sessions	\$260	\$160	\$390
<b>Exhibition</b> Exhibition Pass Only	\$25		\$25
<b>Extra CDs and Digests</b> IMS CD ROM RFIC Digest RFIC CD ROM ARFTG CD ROM ARFTG Conference Compendium CD ROM 1982-2006	\$80 \$80 \$80 \$80 \$65		\$150 \$150 \$150 \$150 \$90
<b>Evening Events</b> Awards Banquet Evening Social (Thursday Night)	\$75 \$20		\$75 \$20
<b>Box Lunches</b>	\$20		\$20
<b>Workshop and Short Courses</b> Full Day Half Day Full Day Short Courses Full Day Short Courses SC-5 (with lab) Half Day Short Courses All Workshops DVD (RFIC/IMS) All Workshops DVD (RFIC/MS) plus Full Day (or 2 Half Day) Workshop Attendance All RFIC Workshop Only CD-ROMs (no attendance included)	\$205 \$155 \$365 \$415 \$275 \$245 \$405 \$150	\$140 \$105 \$250 \$300 \$190 \$155 \$280 \$105	\$305 \$230 \$540 \$590 \$410 \$355 \$595 \$210

---

## **SOCIAL and SPECIAL EVENTS**

---

**SUNDAY, JUNE 7 2009**

**RFIC Symposium Reception • 07:00pm-10:00pm  
Westin Grand Ballroom B&C**

Immediately following the RFIC Plenary Session, all RFIC Symposium attendees are invited to attend a complimentary reception hosted by RFMD. This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends make new acquaintances and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

**MONDAY, JUNE 8 2009**

**Technical Attendees Breakfast • 07:00am-09:00am  
BC&EC**

This breakfast is for all persons registered as technical participants in the IMS, RFIC and ARFTG events. Technical coded badge required for admission.

**IMS 2009 Golf Tournament • 07:00am-02:00pm  
Granite Links Golf Club, Quincy, MA**

Start your week off right; relax with fellow conference attendees at the IMS 2009 Golf Tournament. Register at [www.ims2009.com/golf/ims2009](http://www.ims2009.com/golf/ims2009)

**MTT-S Welcome Reception • 07:00pm-11:00pm  
BC&EC Ballroom East**

All Microwave Week attendees and exhibitors are invited to attend a complimentary reception hosted by MTT-S immediately following the IMS Plenary Session in the adjoining Ballroom. The Plenary and Reception are open to all IMS attendees.

**TUESDAY, JUNE 9 2009**

**IEEE MTT-S Women in Microwaves Reception • 06:00pm-08:00pm  
Westin Commonwealth Ballroom A**

Meet and interact with industry professionals who share a mutual interest in promoting the WIM forum.

**Ham Radio Social – 07:00pm-10:00pm  
Westin Commonwealth Ballroom C**

CQ, CQ, CQ, Calling All Hams: IMS2009 will host a social on Tuesday evening for ham radio operators. Dale Clement, AF1T will give a unique talk titled, “See How Antennas Work”, using live physical examples on the 70 cm band. Bring your QSL card for display!

For those Attendees who are involved with Amateur Radio, Boston is radio-active. You should plan on bringing a radio for 2M, 440MHz, and 900MHz. Repeaters for the symposium will be Boston at 145.230 (PL 88.5), Waltham at 449.075 (No PL), and Waltham at 927.1375 (PL 131.8).

---

## **SOCIAL and SPECIAL EVENTS** (continued)

---

### **WEDNESDAY, JUNE 10 2009**

#### **Industry Hosted Cocktail Reception • 05:00pm-6:30pm BC&EC Exhibit Hall**

Symposium exhibitors will host a cocktail reception in the exhibit hall of the Convention Center. Refreshments and hors d'oeuvres will be served throughout the exhibit area courtesy of the exhibitors beginning at 05:00pm. The reception is open to all registered attendees.

#### **MTT-S Awards Banquet • 07:00pm-10:00pm BC&EC Ballroom**

Continuing a tradition for the Boston IMS, the MTT-S Awards Banquet, scheduled for June 10, 2009 will again feature a distinguished speaker. Dr. Spencer Wells, a National Geographic Explorer-in-Residence, will describe how The Genographic Project is seeking to chart the migratory history of the human species using DNA contributed by hundreds of thousands of people from around the world

### **THURSDAY, JUNE 11 2009**

#### **MTT-S STUDENT AWARDS LUNCHEON • 12:00pm-02:00pm Westin**

All students and advisors are invited to attend this luncheon which recognizes recipients of the MTT-S Undergraduate Scholarships, MTT-S Graduate Fellowships, IMS2009 Student Volunteers, IMS 2009 Student Paper Awards, and the winners and participants of the IMS2009 Student Design Competitions. The luncheon is complementary to all students, their advisors, competition judges, and presenters.

#### **GOLD Reception • 06:00-08:00pm The Fish Exchange Building, 1 Fish Pier**

The Graduates of Last Decade (GOLD) committee will host a complimentary reception. From the BC&EC walk northeast on D street to the end of the Fish Pier.

#### **Thursday Evening Social Cruise • 07:00pm-09:00pm**

Thursday evening will be the time to take a break from the sessions and workshops to enjoy Boston from a wonderful vantage point. We invite you to join us for a couple of hours on Thursday evening for a cruise of Boston Harbor. Let us share with you the views of Boston's skyline and the harbor islands from our ship, while relaxing with something to drink, something to eat, and music to serenade us while we cruise the evening away. Our ship sails from the World Trade Center in the Seaport District, a short two block walk from the convention center. The ship is outfitted with table seating, perimeter seating, an enclosed deck, semi enclosed deck, and the enormous top deck will ensure a wonderful time on the water.

---

## GUEST PROGRAM

---

### **HOSPITALITY SUITE: Westin Boston Waterfront, Harbor Ballroom 1 – Conference Level**

A hospitality suite is planned for all guests of IMS 2009 technical attendees. Guests are invited to relax, enjoy a bite to eat and take advantage of the activities planned throughout the city of Boston. All tours will depart from the guest hospitality suite and a representative from the city will be available for questions about Boston. A continental breakfast and light refreshments will be served daily.

The hospitality suite will be open from Sunday, June 7 through Thursday, June 11 from 07:00am-04:00pm and is reserved for guests of attendees only. IMS 2009 attendees are encouraged to take advantage of the food, beverage and services available at the Boston Convention and Exposition Center (BC&EC).

### **TOURS AND SPECIAL EVENTS:**

#### **Sunday, June 7 2009 HARVARD UNIVERSITY AND THE JFK LIBRARY – WITH STOP AT 12:30pm-05:00pm HARVARD MUSEUM OF NATURAL HISTORY TO VIEW GLASS FLOWERS**

You will explore the world famous Harvard University area where the young JFK lived and studied. You will stroll through Harvard Yard, the original campus of the oldest university in the country. You will have time to browse in Harvard Square, with its shops, boutiques, and over 25 bookstores. Following Harvard Square, your guests will stop at the Harvard Museum of Natural History to view the showplace that houses unique glass flowers. Since the 1880's the Botanical Museum of Harvard University has been the showplace of the unique "garden in glass." True to life glass models of over 700 plant species have inspired reactions ranging from amazed admiration to disbelief. The accuracy of their forms corroborated by botanists, attests to the artistic and scientific skill of their creators, Leopold Blaschkka and his son Rudolf. Their family, originally from Venice, included numerous artistic technicians who had, through many generations, developed great proficiency in the working of glass, enamel and metals. In addition to being a popular attraction, the glass flowers collection serves as a useful adjunct to the study of botany and is regularly used for that purpose by the students of Harvard and other colleges in the Boston area. Your tour will continue as you travel from Cambridge to the shoreline of Dorchester Bay, where you will visit the spectacular John F. Kennedy Library, designed by I.M. Pei.

**COST:** \$55.00 per person. *Price includes roundtrip transportation via executive coach, professional guide service, admissions and taxes*

#### **Monday, June 8 2009 01:00pm-03:00pm**

#### **BOSTON DUCK TOURS: THE RIDE OF YOUR LIFE**

Unless you fought in World War II, you probably haven't ridden on a "DUKW" before. This "duck" is an authentic renovated amphibious landing vehicle, retrofitted to take you on a special historical tour of Boston, with a special splashdown right into the Charles River for a breathtaking waterside view of Boston, the kind of view that you can't get anywhere else.

**COST:** \$42.00 per person. *Price includes private duck rental, professional guide service and taxes*

#### **Monday, June 8 2009 8:30am-05:00pm**

#### **A TOUR OF NEWPORT AND ITS MANSIONS**

Newport, Rhode Island, is rich in both history and culture. A town which was established in the colonial era, made a name for itself during America's Gilded Age, and since has become the yachting capital of the world. Today, the town thrives as a hub for American culture and visitors are faced with an abundance of activities, quaint B&B's, museums, shops, beaches, and outstanding restaurants. Newport is not to be missed.

After touring these homes, guests will explore Newport Harbor and will enjoy a luncheon at one of the town's most charming restaurants. The group will then take pleasure in a tour of the famed 10 mile Ocean Drive for a view of the area's estates and gardens which dot this beautiful shoreline.

**COST:** \$115.00 per person *Price includes roundtrip transportation via executive coach, professional guide service, admissions, tours, luncheon and taxes*

---

## **GUEST PROGRAM** (continued)

---

**Monday, June 8 2009**

**COMPLETE TOUR OF BOSTON: 350 YEARS IN A DAY  
WITH GUIDED TROLLEY TOUR**

**09:00am-01:00pm**

Boston is comprised of many neighborhoods, each with its own architecture and atmosphere. You'll have an overview of the city when you see the major neighborhoods and the historic sites that make Boston such a fascinating place to visit. You'll see Beacon Hill, Boston's most prestigious address, and visit the Back Bay, an elegant section of Boston which, one hundred years ago, was built according to the plan of Paris' Bois de Boulogne. To enhance the tour, your guests will be guided in an Old Town Trolley.

**COST:** \$40.00 per person. *Price includes roundtrip transportation via Trolley, professional guide service, admissions and taxes*

Note: This tour involves a considerable amount of walking on hills and cobblestones. Participants should be aware of these conditions and are advised to wear walking shoes.

**Tuesday, June 9 2009**

**WRENTHAM VILLAGE OUTLETS**

**10:00am-05:00pm**

Wrentham Village is one of the easiest to negotiate and most attractive outlet shopping areas in the country. With 170 outlet stores, one can find impressive savings at Barneys New York Outlet, Bebe, Donna Karan, Gap Outlet, Hugo Boss, Kenneth Cole, Liz Claiborne, Nike, Polo Ralph Lauren, Reebok, Sony, Timberland, Versace, Williams-Sonoma and much more! There are shops of every kind, as well as many areas to relax and enjoy refreshments during your visit. You will be given a map, as well as a variety of coupons prior to your arrival. Wrentham is located approximately 45 minutes from Boston and the drive is well worth it! Here you can truly "shop 'til you drop"!

**COST:** \$35.00 per person. *Price includes roundtrip transportation, professional guide, coupons, maps and taxes*

**Tuesday, June 9 2009**

**THE BOSTON FREEDOM TRAIL WALKING TOUR**

**09:30am-01:30pm**

In 1958, local journalist William Schofield had the idea that Boston's sites could be more accessible to residents and visitors, and conceived of the Freedom Trail. Follow the Red Bricks Road! The Freedom Trail is a 2.5 mile red brick or red painted line that travels through Beacon Hill, downtown Boston, the North End and Charlestown. This tour will be enhanced as your guests go on a ride on Boston's famed Swan Boats!

**COST:** \$36.00 per person. *Price includes Professional guide service, refreshments and ride on swan boats.*

Note: This tour involves a considerable amount of walking on hills and cobblestones. Participants should be aware of these conditions and are advised to wear walking shoes.

**Tuesday, June 9 2009**

**BOSTON RED SOX-FENWAY PARK**

**07:00pm**

Enjoy a Red Sox game at America's most beloved stadium. Your senses will light up as you step ontoYawkee Way and catch a smell of a "Fenway frank," hear the cheers of the most dedicated fans, and see the most authentic stadium in America. Visit the home of the 2004 and 2007 World Champion Red Sox team as they battle it out with their opponent. This is the park where the Babe pitched, the Kid hit, Yaz dazzled, and famed players such as Yuke and Big Papi Ortiz still thrill young fans today.

**COST:** \$165.00 per person (bleachers) *Limited number of seats are available*



---

## **GUEST PROGRAM** (continued)

---

**Tuesday, June 9 2009**

**BOSTON POPS PERFORMANCE**

**08:00pm performance**

Boston Pops Performance on this evening is a Judy Garland program consisting of all of her well-known songs with special guest, Linda Eder, a fabulous Broadway singer who will accompany the orchestra with her fabulous vocals. All guests are on their own for transportation to Symphony Hall.

**COST:** \$51.00 per person. *Price includes seats only. Limited number of seats are available.*

**Wednesday, June 10 2009**

**GLOUCESTER AND ROCKPORT**

**09:00am-05:00pm**

**- SCENIC CAPE ANN**

You'll see some of the Northeast's most beautiful coastline, as well as the "Man at the Wheel" — the fisherman's Memorial Statue on Gloucester harbor. Gloucester balances its intertwined past and future with assurance and skill. The city, long renowned among artists for the purity of its light, has traditionally been the home of internationally known painters like Winslow Homer, Edward Hopper and Fitzhugh Lane and sculptors like Walker Hancock.

**COST:** \$98.00 per person. *Price includes roundtrip transportation via executive motor coach, professional guide service, lobster lunch and all taxes.*

**Thursday, June 11 2009**

**BIKE YOUR WAY THROUGH THE STREETS FOR BOSTON**

**09:30am-01:30pm**

**- SHOP TILL YOU DROP**

Why see the city through the windows of a bus, when you can see the city in a much more intimate way... on bike!! Without question this biking experience provides the best way to see all that Boston has to offer in a fun and exciting setting. Boston is notorious for its vast history, its quaint community districts and its traffic! Why put yourself through that? On bike you will have better access to all of the sites of the city. The signature city view tour allows you to pedal from historic Fenway Park, home of the World Champion Boston Red Sox, through modern and dynamic Back Bay, into historic Beacon Hill, with a stop for a cup of coffee and a pastry in the Italian North End. You will see parts of Boston off the beaten path and experience the diversity of Boston's contemporary and classic neighborhoods. You are sure to enjoy this unique way of seeing the city.

**COST:** \$100.00 per person. *Price includes bike delivery to hotel, professional tour guide service, bike and helmet rental, and customized city tour of Boston, water, taxes and gratuities.*

**Thursday, June 11 2009**

**LEXINGTON AND CONCORD**

**09:00am-01:30pm**

**— THE SHOT HEARD 'ROUND THE WORLD**

You will see many historic sites on this visit to Lexington and Concord. This tour includes a stop at historic Lexington Green, the site of the initial skirmish of the Revolutionary war.

**COST:** \$52.00 per person. *Price includes roundtrip transportation via executive motor coach, professional guide service, admissions and taxes.*

**Thursday, June 11 2009**

**MASTERPIECES OF ART**

**10:00am-02:00pm**

**WITH LUNCH AT BRAVO RESTAURANT**

Bostonians have always supported the arts and the Museum of Fine Arts is a grand example of this commitment. You will view the incomparable collections of paintings, sculpture, decorative arts, drawings and photographs, representing Eastern and Western cultures from ancient times to the present. To make these collections even more meaningful, our fine arts lecturer will interpret. The masterpieces of art as they were perceived by various artists and cultures throughout the ages. **COST:** \$107.00 per person. *Price includes roundtrip transportation via executive coach, services of a professional guide, admissions, docent tour of the Museum of Fine Arts, Lunch at Bravo Restaurant at MFA.*

**Thursday, June 11 2009**

**BOSTON DUCK TOURS:**

**01:00pm-03:00pm**

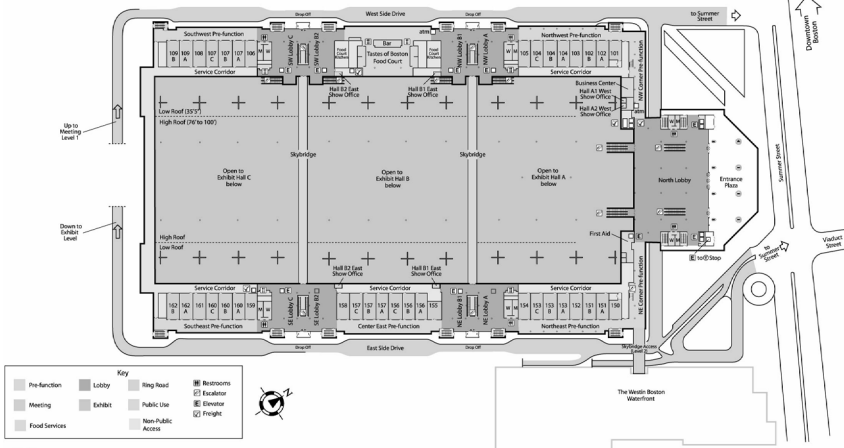
**THE RIDE OF YOUR LIFE**

For details see "Boston Duck Tours" on page 77.



**Boston Convention & Exhibition Center**  
 415 Summer Street  
 Boston, Massachusetts 02210  
 ph: 617.954.2800 fc: 617.954.3326  
 www.AdvantageBOSTON.com

### Meeting Level 1

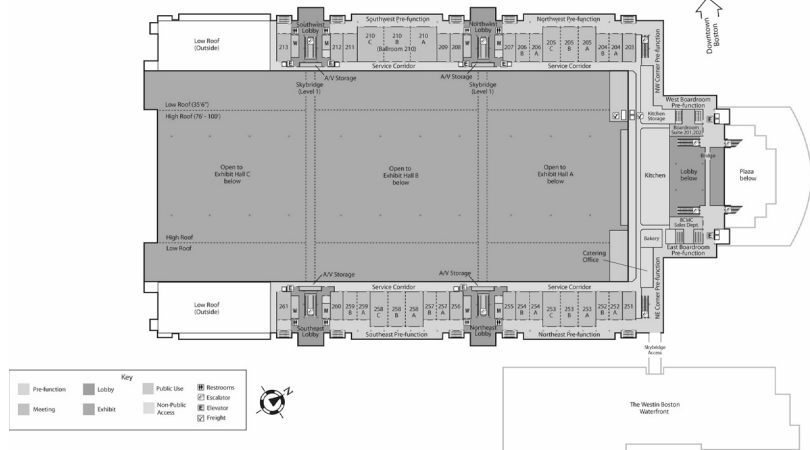


The Massachusetts Convention Center Authority owns and operates the Boston Convention & Exhibition Center and the Hyatt Convention Center.



**Boston Convention & Exhibition Center**  
 415 Summer Street  
 Boston, Massachusetts 02210  
 ph: 617.954.2800 fc: 617.954.3326  
 www.AdvantageBOSTON.com

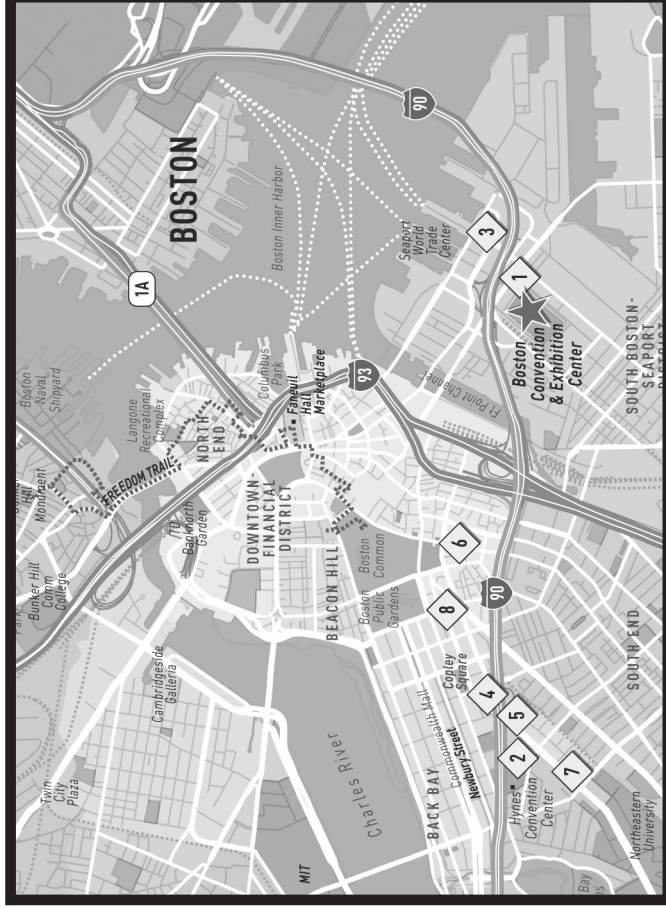
### Meeting Level 2



The Massachusetts Convention Center Authority owns and operates the Boston Convention & Exhibition Center and the Hyatt Convention Center.

# RFIC Attendee Hotels

1. Westin Waterfront  
(Headquarter Hotel)
2. Sheraton Boston  
(Co-Headquarters Hotel)
3. Renaissance Boston Waterfront
4. Westin Copley Place
5. Boston Marriott Copley Place
6. Courtyard Marriott Boston Tremont
7. Midtown Hotel
8. Boston Park Plaza



**IEEE**

468 Walden Trail  
Waxhaw, NC 28173

**2009 RFIC Symposium**

Boston, MA  
June 7-9, 2009



**PROGRAM**

Nonprofit Org.  
U.S. POSTAGE  
PAID  
PERMIT NO. 35  
PITTSBURGH, PA