2008 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium

Atlanta, Georgia – June 15-17

IEEE

PROGRAM

Georgia
World Congress Center

Sponsored by
IEEE Microwave Theory and Techniques Society
IEEE Electron Device Society
and
The IEEE Solid-State Circuits Society

RFIC Plenary and Reception – Sunday Night (Sunday June 15, 2008)

After a busy day of outstanding RFIC Workshops (see page 77 - 89), the Plenary Session and RFIC Reception will be held on Sunday evening – June 15, 2008. These activities are the highlight of technical activities include the Plenary Session at 17:30 in the Georgia World Congress Center (GWCC) Room – A411. The Plenary Session will include two outstanding speakers (See pages 7-9), and the Student Paper Award ceremony. The RFIC Reception will follow at 19:00 in the GWCC - Room A412. This social event is a key component of the RFIC Symposium, providing the opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration. The Reception is sponsored by the RFIC Steering Committee and two industrial sponsors.

Platinum Sponsor: RFMD

Gold Sponsor: ANSOFT

RFIC Week Activities (June 14-17)

Saturday June 14, 2008

14:00 - 18:00	Registration – GWCC

Sunday June 15, 2008

07:00 - 18:00	Registration – GWCC
08:00 - 17:00	Workshops and Tutorials – GWCC
17:30 - 19:00	RFIC Plenary GWCC – Room A411
19:00 - 21:00	RFIC Reception GWCC – Room A412

Monday June 16, 2008

07:00 - 18:00	Registration – GWCC
07:00 - 08:00	Attendee Breakfast GWCC – Hall A3
08:00 - 17:00	RFIC Oral Technical Sessions (see pages 10 -41)
08:00 - 09:40	RMO1A RMO1B RMO1C RMO1D
10:10 - 11:50	RMO2A RMO2B RMO2C RMO2D
13:20 - 15:00	RMO3A RMO3B RMO3C RMO3D
15:30 - 17:10	RMO4A RMO4B RMO4C RMO4D

Tuesday June 17, 2008

07:00 - 18:00	Registration – GWCC
07:00 - 08:00	Attendee Breakfast GWCC – Hall A3
08:00 - 17:00	RFIC Oral and IF Technical Sessions (see pages 42 -72)
08:00 - 09:40	RTU1A RTU1B RTU1C RTU1D RTU1E
10:10 - 11:50	IMS Plenary (RFIC Attendees are invited)
13:20 - 15:00	RTU3A RTU3B RTU3C
15:30 - 17:00	RTU4B RTU4C
14:00 - 16:00	RTUIF

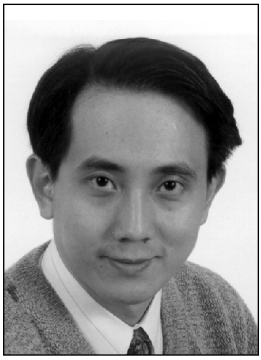
This Program can be found on the RFIC Web site www.rfic2008.org. IMS Sessions and Exhibit are held on Tuesday - Thursday from 08:00 - 17:10. IMS Program details are found on www.ims2008.org. RFIC spouses/guests may take advantage of the IMS Guest Program listed on the IMS Web site.

TABLE OF CONTENTS

The RFIC Symposium will be in Atlanta, Georgia on June 15-17, 2008 in conjunction with the IEEE International Microwave Symposium. It opens Microwave Week 2008, the largest world-wide RF/Microwave meeting of the year.

The RFIC Symposium brings focus to the technical accomplishments in RF systems, circuit, device and packaging technologies for mobile phones, wireless communication systems, broadband access modems, radar systems and intelligent transport systems.

Message from the General Chair



Jenshan Lin

Welcome to the 2008 RFIC Symposium!

The 2008 RFIC Symposium maintains its reputation as one of the foremost IEEE technical conferences dedicated to the latest innovations in RFIC development for wireless and wireline communication IC's. Running in conjunction with the International Microwave Symposium and Exhibition, the RFIC Symposium adds to the excitement of Microwave Week with three days focused exclusively on RFIC technology and innovation. The RFIC symposium will be held at the Georgia World Congress Center, 15-17 June, 2008. The symposium begins on Sunday, 15 June with workshops targeted at RF technology, design, and system issues. Sunday evening activities continue at 5:30pm with the Plenary Session where 2 speakers will share their views on the direction and challenges that the RFIC industry will be facing. The first speaker, Robert Van Buskirk, President of Multi-market Products Group at RFMD Inc., will discuss "Best of Both Worlds: Multi-market Diversity Embedded in a Scale RF Semiconductor Business." The second speaker, Zoltan J. Cendes, Ph.D., Founder, Chairman, and CTO of Ansoft Corporation, will discuss "First Pass System Success – When First Pass Silicon Success is Not Enough." Following the Plenary Session, the RFIC Reception will be hosted in the Georgia World Congress Center as well. This social event is a key component of the conference with the opportunity to connect with old friends and new acquaintances and catch up on the wireless industry. The technical program includes oral sessions, an Interactive Forum (poster session), and two lunch time panel sessions. The oral presentation sessions start on Monday, 16 June with four parallel sessions in the morning and in the afternoon. The oral sessions continue on Tuesday, 17 June. The poster session will be held on Tuesday afternoon. The poster session is the perfect place to have an opportunity to have more detailed technical discussions with the authors. In the tradition of the RFIC Symposium, the Tuesday morning activity will be paused during the International Microwave Symposium Plenary Session, from 10:10 - 11:50. Panel Sessions are also planned at lunch time on Monday and Tuesday. The RFIC Symposium concludes on Tuesday allowing participants to attend the IMS and ARFTG as well as plenty of time to visit the exhibit hall. The RFIC organization is thankful to the IMS2008 team, without whom we could not make this conference successful. Most of all, we are particularly thankful to all the technical contributors to the RFIC Symposium. We look forward to your participation. Please continue to make this conference so vibrant within the RFIC industry!

Enjoy the conference!

Jenshan Lin
General Chair
2008 IEEE RFIC Symposium

Message from the Technical Program Committee Chairs

Tina Quach

Yann Deval

On behalf of the Technical Program Committee, welcome to the 2008 IEEE RFIC Symposium. The RFIC Symposium is a leading-edge IEEE technical conference dedicated to the advancement of integrated circuits and subsystems for RF, wireless, broadband communications, and many other emerging applications. The RFIC Technical Program Committee has worked diligently to select the best papers to assemble a high quality technical program this year. These papers will be presented in several technical sessions. The RFIC Symposium also features a student paper contest. The three best student papers will be selected by the Technical Program Committee and the awards will be presented in the Plenary Session. This year the RFIC Symposium begins on Sunday, June 15th with workshops at the advanced and tutorial level addressing RF technology and design and integration, at both system and circuit levels. The Plenary Session will be held on Sunday evening, following the workshops. Two leading experts from the RFIC industry will share their views during the plenary session. The RFIC Reception will follow immediately after the plenary session, providing a relaxing time for all to mingle with old friends and catch up on the latest news. In addition to the technical sessions on Monday and Tuesday, the RFIC Symposium also features 2 panel sessions and 12 workshops. The Monday lunch panel session entitled "Millimeter-wave IC: Is silicon winning? Is GaAs still alive?" has panelists from both industry and academia debating the future of Millimeter wave IC using GaAs and Si technologies. The Tuesday lunch's panel session is a co-sponsor program with the IMS. The title "Cognitive Radio for Open Access and White Space" is posed to stimulate interactive discussions with the audience! The workshops on Sunday cover a wide range of topics from system to device technologies. This year, by popular demand, the hottest and latest subcommittee is added to the RFIC Technical Program. This subcommittee focuses on Millimeter Wave ICs using Silicon substrates.

The interest in RFIC technology, and the venue offered by the Symposium to showcase the latest advancements, continues to make the RFIC Symposium the venue of choice for both industry and academia to meet, discuss results and exchange ideas. The 2008 Technical Program Committee keeps working diligently toward the goal of strengthening the technical quality and scope of the program, while maintaining and improving the legacy left by the previous Symposia. This would not be possible without holding the interest of professionals like you and gaining the trust of all the authors who submitted their work to the RFIC Symposium.

We hope you enjoy the 2008 RFIC Symposium!

Tina Quach and Yann Deval
Technical Program Chairs
2008 IEEE RFIC Symposium

Steering Committee

Jenshan Lin, University of Florida
General Chair

Tina Quach, Freescale Semiconductor Inc.
TPC Co-Chair

Yann Deval, University of Bordeaux, IMS Lab
TPC Co-Chair

David Ngo, RFMD
Finance Chair

Jacques C. Rudell, Intel Corporation
Workshops Chair

Bertan Bakkaloglu, Arizona State University
Digest & CD-ROM Chair

Albert Jerng, Ralink
Transactions/Guest Editor

Derek Shaeffer, Beceem Communications, Inc.
Invited Papers Chair

Kevin Kobayashi, RFMD
Panel Sessions Chair

Noriharu Suematsu, Mitsubishi Electric
Publicity Chair

Yuhua Cheng, SHRIME, Peking University
Student Paper Chair

Kevin McCarthy, University College Cork
Secretary

Larry Whicker, LRW Associates
Conference Coordinator

Takao Inoue, University of Texas at Austin
Webmaster

Advisory Board

Fazal Ali • Eliot Cohen • Reynold Kagiwada
Sayfe Kiaei • Louis Liu • David Lovelace
Vijay Nair • Steve Lloyd

Executive Committee

Natalino Camilleri • Joseph Staudinger • Stefan Heinen
Luciano Boglione • Jenshan Lin

SSCS Liaison

Kenneth O

Technical Program Committee

Fazal Ali, *Qualcomm*

Walid Ali-Ahmad, *Mediatek Singapore*

Kirk Ashby, *Microtune, Inc.*

Bertan Bakkaloglu,
Arizona State University

Jean-Baptiste Begueret,
*University of Bordeaux,
IMS Lab*

Didier Belot, *ST Microelectronics*

Paul Blount, *Custom MMIC Design*

Georg Boeck, *TU Berlin,
Microwave Engineering*

Luciano Boglione,
University of Massachusetts, Lowell

Natalino Camilleri,
Alien Technology

Sudipto Chakraborty,
Texas Instruments

Glenn Chang, *MaxLinear*

Jing-Hong Chen, *Analog Device*

Nick Cheng, *Skyworks Solutions*

Yuhua Cheng, *Shrime Peking University*

Stephen Dow, *ON Semiconductor*

Brian Floyd, *IBM
T. J. Watson Research Center*

Ranjit Gharpurey,
University of Texas, Austin

Aditya Gupta, *Anadigics*

Timothy Hancock, *MIT Lincoln Lab.*

Andre Hanke, *Infineon Technologies*

Stefan Heinen, *Infineon Technologies*

Frank Henkel, *IMST GmbH*

Tian-Wei Huang,
National Taiwan University

Stavros Iezekiel,
University of Cyprus

Lars Jansson,
Tumbledown Technical Inc

Albert Jerng, *Ralink*

Waleed Khalil, *Intel*

Jaber Khoja, *Microtune, Inc.*

Sayfe Kiaei, *Connection One,
Arizona State University*

Bumman Kim, *Postech*

Kevin Kobayashi,
RFMD

Larry Kushner, *Kenet, Inc.*

Chang-Ho Lee, *Samsung*

Domine Leenaerts,
NXP Semiconductor

Donald Y.C. Lie,
Texas Tech. University

Louis Liu,
Northrop Grumman Corporation

Ting-Ping Liu
Winbond Electronics

David Lovelace,
ON Semiconductor

Danilo Manstretta,
University of Pavia

Adrian Maxim,
Silicon Lab. Austin, TX

Kevin McCarthy,
University College Cork

Srenik Mehta,
Atheros Communications

Jyoti Mondal,
Freescale Semiconductor Inc.

David Ngo, *RFMD*

Stefano Pellerano, *Intel Corporation*

Allen Podell, *Allen Podell*

Sanjay Raman, *Virginia Tech*

Madhukar Reddy, *Maxlinear*

Bill Redman-White,
NXP Semiconductor

Eli Reese, *TriQuint Semiconductor*

Francis Rotella,
Peregrine Seimconductor

Jacques Rudell, *Intel Corporation*

Carlos Saavedra, *Queen's University*

Derek Shaeffer, *Beceem*

Joseph Staudinger, *Freescale
Semiconductor Inc.*

Bob Stengel, *Motorola Labs*

Noriharu Suematsu, *Mitsubishi Electric*

Julian Tham, *ARDA Technologies*

Bruce Thompson, *Motorola Labs*

Freek van Straten, *NXP Semiconductor*

Albert Wang, *UC Riverside*

Patrick Yue, *UCSB*

Gary Zhang, *Skyworks Solutions*

RFIC Schedule 2008

The RFIC Symposium will be held in the Atlanta Georgia in the Georgia World Congress Center (GWCC). The headquarters hotel is the Omni Hotel at CNN Center. The RFIC Plenary and Reception will be held on Sunday June 15, 2008 at the GWCC. The Plenary will be in room A411 and the Reception will follow in Room A412.

The RFIC Symposium is held in conjunction with the International Microwave Symposium (IMS). Attendees of the RFIC Symposium are invited to attend the IMS Plenary Session on Tuesday June 17 and MTT Social Events.

Saturday June 14, 2008

14:00 - 18:00	Registration – Georgia World Congress Center (GWCC)

Sunday June 15, 2008

07:00 - 18:00	Registration – GWCC
08:00 - 17:00	Workshops – GWCC
08:00 - 17:00	Tutorials – GWCC
17:30 - 19:00	RFIC Plenary GWCC – Room A411
19:00 - 21:00	RFIC Reception GWCC- Room A412

Monday June 16, 2008

07:00 - 17:00	Registration – GWCC
07:00 - 08:00	Speakers Breakfast GWCC
07:00 - 08:00	Registered Attendee Breakfast GWCC – Hall A3
07:00 - 17:00	Speakers Preparation GWCC
08:00 - 09:40	RFIC Oral Technical Sessions GWCC – See Listings
09:40 - 10:10	Break – GWCC
10:10 - 11:50	RFIC Oral Technical Sessions GWCC – See Listings
11:50 - 13:20	RFIC Panel – GWCC Room A412
13:20 - 15:00	RFIC Oral Technical Sessions GWCC – See Listings
15:00 - 15:30	Break – GWCC
15:30 - 17:10	RFIC Oral Technical Sessions GWCC – See Listings
18:00 - 20:00	IMS2008 Reception OMNI Hotel Grand Ballroom

RFIC Schedule (Continued)

Tuesday June 17, 2008

07:00 - 17:00	Registration – GWCC
07:00 - 08:00	Speakers Breakfast GWCC
07:00 - 08:00	Registered Attendee Breakfast GWCC Hall A3
07:00 - 17:00	Speakers Preparation GWCC
08:00 - 09:40	RFIC Oral Technical Sessions GWCC – See Listings
09:40 -10:10	Break GWCC-Exhibits Area
10:10 - 11:50	IMS Plenary Session GWCC – Sydney Marcus Auditorium
11:50 - 13:20	IMS/RFIC Panel – GWCC - Room A305
14:00 - 17:00	RFIC Interactive Forum (RTUP) GWCC – Hall A3
13:20 - 15:00	RFIC Oral Technical Sessions GWCC – See Listings
15:00 - 15:30	Break GWCC – Exhibits Area
15:30 - 17:10	RFIC Oral Technical Sessions GWCC – See Listings

Plenary Schedule

Sunday, June 15, 2008 - 17:30
GWCC – Room A411
Session RSU5A: RFIC Plenary

Chair: Jenshan Lin, University of Florida
Co-Chairs: Tina Quach, Freescale Semiconductor Inc. and Yann Deval, University of Bordeaux, IMS Lab

17:30 Welcome message from General and TPC Chairs, Announcement of Student Paper Awards

17:45 **RSU5A-1:** Best of Both Worlds: Multi-market Diversity Embeded in a Scale RF Semiconductor Business
Robert Van Buskirk, President Multi-market Products Group (MPG), RFMD, Inc.

18:15 **RSU5A-2:** First Pass System Success – When First Pass Silicon Success is Not Enough
Zoltan J. Cendes – Founder, Chairman and CTO, Ansoft Corporation

RFIC Plenary Session

Best of Both Worlds: Multi-market Diversity Embedded in a Scale RF Semiconductor Business

Robert Van Buskirk –
President, Multi-market Products Group (MPG), RFMD Inc.

Many RF semiconductor companies seek a balance between scale-driven, high volume business demands and more diverse, lower volume business requirements. Successful RF companies can manage these potentially conflicting business goals and realize significant advantages through the balance of scale and multi-market diversity. Using the acquisition of Sirenza Microdevices by RFMD in November 2007 as a platform to discuss this balance, the significant competitive advantages for a multi-market business embedded in a scale RF business will be addressed. This talk will explore the benefits of these unique competitive advantages and give concrete examples of how growth can be accelerated by leveraging the "Best of Both Worlds."

About Robert Van Buskirk:

Robert Van Buskirk has served as the President of RFMD's Multi-market Products Group (MPG) since the successful completion of the Sirenza Microdevices acquisition in November 2007. Prior to joining RFMD he was Sirenza's President and Chief Executive Officer and a member of the Board of Directors from May 1999 through November 2007. Before joining Sirenza, Mr. Van Buskirk held the position of Executive Vice President of Business Development and Operations from August 1998 to May 1999 at Multilink Technology Corporation, a company specializing in the design, development, and marketing of high bit-rate electronic products for advanced fiber-optic transmission systems. Prior to his position at Multilink, Mr. Van Buskirk held various management positions at TRW, a semiconductor wafer manufacturer, including Executive Director of the TRW GaAs Telecom Products business from 1993 to August 1998. Mr. Van Buskirk holds a B.A. from California State University at Long Beach.

RFIC Plenary Session

First Pass System Success – When First Pass Silicon Success is Not Enough

Dr. Zoltan J. Cendes –
Founder, Chairman and CTO,
Ansoft Corporation

Advances in the performance and accuracy of design automation software and electromagnetic modeling have enabled RFIC designers to apply their skills to achieve first pass silicon success for complex mixed-signal radio circuits. Now, coupling between circuit simulation and parameterized electromagnetics allows them to include detailed analysis of packaging and printed circuit board parasitic coupling to analyze system performance. A silicon vendor may produce a wireless SoC that performs flawlessly at the packaged part level. Once that part is placed on a system PCB, the complex interactions among traces on the board, the coupled impedances between package pins and the PCB, and nonlinear effects in the circuit itself can combine to generate spurious radiation and corrupt signal/power integrity. These undesired effects can be predicted by applying full electromagnetic simulation of the package and board in concert with a top-level transient or harmonic balance simulation at the circuit level. We present here an overview of key simulation technologies and discuss how they can be applied to achieve first pass system success for complex electronic products.

About Zoltan J. Cendes

Dr. Zoltan Cendes is Founder, Chairman and CTO of Ansoft Corporation, Pittsburgh, PA and is an Adjunct Professor at Carnegie Mellon University, Pittsburgh, PA. As Ansoft's chief technology officer he is responsible for managing the company's research and development. He has served as Professor of Electrical and Computer Engineering at Carnegie Mellon University, as an Associate Professor of Electrical Engineering at McGill University, Montreal, Canada, and as an Engineer in the Corporate Research and Development Center of the General Electric Company in Schenectady, NY. Cendes received his MS and doctoral degrees in electrical engineering from McGill University. Dr. Cendes is a Fellow of the IEEE, has served on the Editorial Board of IEEE Spectrum, on the International Steering Committee of the COMPUMAG Conference and as an IEEE Antennas and Propagation Society (IEEE AP-S) Distinguished Lecturer.

Monday June 16, 2008
8:00
GWCC – Room A411
Session RM01A: Cellular Transceivers

Chair: Jyoti P. Mondal, Freescale Semiconductor
Co-Chair: Didier Belot, ST Microelectronics

RM01A-1 8:00
(INVITED) Self-shielded EGPRS Transceiver

A. W. Hietala, S. R. Humphreys, R. Arkizewski, S. Morris, RFMD

Abstract: The next generation of GSM/EDGE transceivers from RFMD is described. The transceiver is a single die in 0.18μm CMOS. A VLIF receiver at 175kHz is implemented with automatic image calibration. An FN offset PLL with digital AFC allows wider bandwidth operation and the ability to change the IF to avoid channel dependent spurious. An AM Loop is added to reduce variations in power as well as to limit PA current and voltage. The solution consists of two conformal shielded modules from DigRF to antenna.

RM01A-2 8:20
A Digital ΔΣ RF Signal Generator for Mobile Communication Transmitters in 90nm CMOS

A. Frappé, B. Stefanelli, A. Flament, A. Kaiser, A. Cathelin*, IEMN - ISEN, Lille, France, *STMicroelectronics, Grenoble, France

Abstract: The proposed digital RF signal generator in 90nm CMOS uses 1-bit ΔΣ modulation and targets mobile communication terminals. A 50MHz bandwidth centered on 1GHz can be achieved when the circuit is clocked at 4GHz. Signals up to 3GHz can be synthesized when using the first image band. The peak output power into a 100 ohm diff. load is 3.1dBm with 53.6dB SNDR. The digital core employs redundant arithmetic and precomputed non-exact quantization and consumes 49mW. Active area is $0.15mm^2$.

RM01A-3 8:40
Active Mitigation of Induced Phase Distortion in a GSM SoC

O. Eliezer, B. Staszewski, S. Bhatara, I. Bashir, P. Balsara(*),
Texas Instruments , (*)The University of Texas at Dallas

Abstract: A novel technique for the mitigation of self-interference in a GSM transmitter is presented. It was designed to mitigate the impact of interference caused by the transmitter's high frequency signals to the on-chip circuitry responsible for generating PLLs crystal-based reference clock, resulting in degraded phase-error performance. The presented technique, leveraging on specific features of the All-Digital PLL, was demonstrated in a GSM SoC based on the DRP in 90nm CMOS.

RM01A-4 9:00
A L1-Band Dual-Mode RF Receiver for GPS and Galileo in 0.18μm CMOS

J.-G. Jo, J.-H. Lee, D. J. Park*, Y. G. Pu*, S.-C. Shin, K.-Y. Lee*,
S.-E. Park**, S.-J. Lee**, C. Yoo, Dept. of Electronics and Comp. Eng.
Hanyang Univ. Seoul, Korea, * Dept. of Electronics Eng. Konkuk Univ.
Seoul, Korea, **, CoreLogic Inc. Seoul, Korea

Abstract: A dual-mode RF receiver with low-IF architecture has been developed for L1-band GPS and Galileo in a 0.18μm CMOS process. The channel selecting bandpass filter centered at 4.092MHz has programmable bandwidth (2-, 4-, and 6-MHz), which allows the reception of GPS and Galileo signals. A fractional-N phase locked loop generates local oscillator, allowing multiple reference frequencies. The noise figure of the receiver is 4.5dB while consuming 45mW from a 1.8V supply.

RM01A-5 9:20
An Adaptive Multi-Mode RF Front-End for Cellular Terminals

G. Hueber, J. Zipper, R. Stuhlberger, A. Holm*, DICE, Austria,
*Infineon Technologies, Germany

Abstract: This paper presents a fully-integrated performance-on-demand receiver front-end for GSM/EDGE/W-CDMA/CDMA2000 multi-mode cellular applications. The design's noise figure, linearity and selectivity are adapted depending on current environmental conditioned the selected standard to guarantee lowest overall power consumption. The single-chip zero-IF receiver comprises two self-matched LNAs for high/lowband, the demodulator and a fully-integrated DS-fractional- N PLL, ADCs, BB-Filter, and a DFE.

Monday June 16, 2008
8:00
GWCC – Room A405
Session RM01B: Broadband Circuit Techniques

Chair: Ranjit Gharpurey, University of Texas, Austin
Co-Chair: Madhukar Reddy, Maxlinear, Inc

RM01B-1 8:00
A 3.1-9.5 GHz Agile UWB Pulse Radio Receiver with Discrete-Time Wideband-IF Correlation in 90nm CMOS

F. Zhang, R. Gharpurey*, P. Kinget, Columbia University,
*University of Texas

Abstract: An 8-channel 3.1-9.5 GHz UWB pulse radio receiver is realized using a double-conversion architecture with discrete-time wideband IF correlation. The pulse templates for correlation are pre-stored in memories which allows fast band switching and agile interferer avoidance since no PLL resettling is required. The receiver chip is implemented in a standard 90 nm CMOS process and occupies 1mm^2.

RM01B-2 8:20
A 3 to 5-GHz UWB Pulse Radio Transmitter in 90nm CMOS

Anuranjan Jha*, Ranjit Gharpurey**, Peter Kinget*, *Columbia University, New York, NY, **University of Texas, Austin, TX

Abstract: We describe a dual conversion, 3-5 GHz UWB pulse radio transmitter architecture using interleaved, IF Digital-to-Analog Converters (DACs) followed by a partial-order hold reconstruction filters that eliminate sampling images, and an RF upconverter. 1.25 nJ is spent per pulse for a pulse-repetition rate (PRR) of 100 MHz while achieving a broadband image cancellation of 30dBc.

RM01B-3 8:40
A 6-9GHz WiMedia UWB RF Transmitter in 90nm CMOS
Z. Zhang, K. Mertens, M. Tiebout, S. Ek,S. Marsili, D. Matveev, C. Sandner, Infineon Technologies Austria AG, Austria

Abstract: A 6-9GHz RF transmitter fabricated in a standard digital 90nm CMOS technology and targeted for WiMedia UWB bandgroup 3 and 6 is presented. The transmitter features high linearity, low spurious emission, low power and small chip area. Measured data show -5.7dBm output power, -1.41dBm OIP3, -47dBc LO leakage and -33.8dBc sideband rejection with only 72mW from a 1.2V power supply at a minimal chip area of 0.24mm^2 active area.

RM01B-4 9:00
An Ultra-wideband Transmitter Based on a New Pulse Generator
M. Cavallaro, E. Ragonese, G. Palmisano, University of Catania, DIEES, viale A. Doria 6, Catania, 95126, Italy

Abstract: The paper describes an ultra-wideband transmitter which incorporates an innovative carrier-based pseudo-Gaussian pulse generator satisfying FCC rules with no-filter and high spectral efficiency.The design includes a BPSK modulator, a ramp generator and an output buffer.The transmitter is designed for run up to 500Mpps in the UWB 3-5 GHz band and implemented in 0.28μm CMOS technology with a core chip size of .06mm^2. It allows the use in various UWB applications.Pulse generator dissipation is 1.9mW

RM01B-5 9:20
A 19pJ/pulse UWB Transmitter with Dual Capacitively-Coupled Digital Power Amplifiers
P. P. Mercier, D. C. Daly, A. P. Chandrakasan, Massachusetts Institute of Technology

Abstract: A fully integrated pulsed-UWB transmitter that communicates in the 3-to-5 GHz 802.15.4a bands is presented. The all-digital architecture generates FCC-compliant UWB pulse bursts using discrete four-level pulse shaping. BPSK-modulation is achieved without the use of a balun through dual capacitively-coupled digital power amplifiers. The transmitter consumes zero static bias power and achieves an energy efficiency of 19-to-113pJ/pulse at data rates from 15.6Mbps-to-100kbps.

Monday June 16, 2008
8:00
GWCC– Room A406-7
Session RM01C: CMOS Millimeter-wave Amplifiers

Chair: Patrick Yue, UC Santa Barbara
Co-Chair: Luciano Boglione, University of Massachusetts, Lowell

RM01C-1 8:00
(INVITED) Deep-Submicron Digital CMOS Potentialities for Millimeter-wave Applications

Andreia Cathelin[(1)], Baudouin Martineau[(1,2)], Nicolas Seller[(1,3)], Frederic Gianesello[(1)], Christine Raynaud[(1,4)], Didier Belot[(1)], [(1)]STMicroelectronics, France, [(2)]IEMN, France, [(3)]IMS Laboratory, France, [(4)]CEA-LETI, France

Abstract: This paper presents the potentialities of deep submicron CMOS technologies for millimeter-wave applications. The target applications are firstly overviewed. Then, the nanometer bulk and SOI CMOS technology offer is presented, presenting integration solutions that take benefit of the intrinsic performances of the active device while minimizing the loss effects introduced by the BEOL. Finally, perspectives regarding future challenges in terms of system integration are discussed.

RM01C-2 8:20
A Tapered Cascaded Multi-Stage Distributed Amplifier with 370GHz GBW in 90nm CMOS

A. Arbabian, A. M. Niknejad, University of California at Berkeley

Abstract: A tapered cascaded multi-stage distributed amplifier (T-CMSDA) has been designed and fabricated in a 90nm digital CMOS process. The amplifier achieves a 3-dB bandwidth of 73.5 GHz with a pass-band gain of 14dB. This results in a gain-bandwidth (GBW) product of 370 GHz. The realized zero-dB BW is 83.5 GHz and the input and output matching stay better than -9dB up to 77 and 94 GHz, respectively. The chip consumes an area of 1.5mm by 1.15mm while drawing 70mA from a 1.2V supply.

RMO1C-3 8:40

An ultra low power LNA with 15dB gain and 4.4db NF in 90nm CMOS Process for 60 GHz Phase Array Radio

Emanuel Cohen*, Shmuel Ravid*, Dan Ritter**, Mobile Wireless Group, Intel Haifa, Israel , ** Electrical Engineering Technion, Haifa, Israel

Abstract: A 60 GHz LNA in a 90nm CMOS process is presented. It features 15 dB of gain, a measured noise figure of 4.4 dB, while consuming 4mW. The LNA uses spiral inductors and has a die area with/without pads of $0.32x0.44mm^2$/$0.14x0.27mm^2$ respectively. First pass success was achieved by using inductors with grounded guard ring. The paper compares transistor sizes and circuit topologies showing that a common source topology with a $10x1\mu$ transistor width gives the best performance over all other options.

RMO1C-4 9:00

60GHz CMOS Differential and Transformer-Coupled Power Amplifier for Compact Design

Tim LaRocca, Mau-Chung Frank Chang, University of California at Los Angeles

Abstract: A 57-65GHz differential and transformer-coupled power amplifier using a commercial 90nm digital CMOS process is presented. On-chip transformers combine bias, stability and input/interstage matching networks for a compact design with an area of $0.15mm^2$. The three-stage amplifier consumes 70mA under 1.2V supply voltage. The small-signal gain generally exceeds 15dB with saturated output power levels over 12dBm and associated peak power-added efficiency (PAE) greater than 20% (14% across the band).

RMO1C-5 9:20

A 60-GHz Fully-Integrated Doherty Power Amplifier Based on 0.13-µm CMOS Process

Byron Wicks*, Efstratios Skafidas*, Rob Evans*, National ICT Australia

Abstract: A sixty-gigahertz (60-GHz) Doherty power amplifier (PA) has been designed and implemented on 0.13 µm RF-CMOS for use in an integrated 60-GHz transceiver. The fully-integrated design implements the main and auxiliary amplifiers, matching networks, and input and output transmission line networks on-chip. The prototype operating from a 1.6-V supply exhibits an output referred P1dB of 7.0 dB, a PSAT of +7.8 dBm, with peak power gain of 13.5 dB, a 3-dB bandwidth of 6.7 GHz, and 3.0 % PAE. The die area is $1.8mm^2$. This amplifier achieves the highest reported figure of merit for power amplifiers of any published millimeter-wave PA on CMOS.

Monday June 16, 2008
8:00
GWCC– Room A404
Session RM01D: RF Front-end Design Techniques

Chair: Donald Y.C. Lie, Texas Tech University
Co-Chair: Jean-Baptiste Begueret, IMS Lab

RM01D-1 8:00
Perspective of RF Design in Future Planar and FinFET CMOS

J. Borremans*, B. Parvais, M. Dehan, S. Thijs, P. Wambacq*, A. Mercha, M. Kuijk*, G. Carchon, S. Decoutere, IMEC, Leuven, Belgium, *also Vrije Universiteit Brussel, Brussels, Belgium

Abstract: This work evaluates the perspective of RF design in planar bulk vs. FinFET SOI for (sub-)45 nm CMOS on a key RF circuit: a Low-Noise Amplifier. Planar and FinFET devices with channel lengths down to 40 nm are compared in both wideband and narrowband designs up to 14 GHz to illustrate the RF and ESD protection performance perspective. Planar devices push the RF performance. FinFETs lag somewhat behind, but show promising performance.

RM01D-2 8:20
A Broadband Low-Noise Singel-Ended Input Differential-Output Amplifier with IM2 Cancelling

D. Manstretta, Dipartimento di Elettronica, Università degli Studi di Pavia, Pavia, Italy

Abstract: A broadband single-ended input differential output low noise amplifier exploiting IM2 cancelling has been designed in a 90nm CMOS technology. A feedback path from the common mode output to the input effectively cancels the 2nd order distortion with negligible effect on the noise performance. Measured IIP2 varies from 17dBm with the feedback disabled to 35dBm when the feedback is enabled. Measured gain and noise figure are respectively 10dB and 5dB with 7.5mW power consumption.

RM01D-3 8:40

Linearization of Differential CMOS Low Noise Amplifier Using Cross-Coupled Post Distortion Canceller

Tae-Sung Kim, Byung-Sung Kim, Sungkyunkwan University, South Korea

Abstract: A post-linearization technique for the differential CMOS LNA is presented. The proposed method uses an additional cross-coupled FET pair which generates the third-order inter-modulation (IM3) current to cancel out the IM3 current of the differential amplifier while minimizing the degradation of noise figure and avoiding the gain reduction. The designed LNA is fabricated using 0.18um CMOS process and measured results show +13.2-dBm IIP3 with 13.7-dB gain and 1.68-dB NF at 2 GHz.

RM01D-4 9:00

A New Method of TX Leakage Cancelation in W/CDMA and GPS Receivers

V. Aparin, QUALCOMM Inc., San Diego

Abstract: The theory and practical implementation of a new TX cancelation method in CDMA and GPS receivers are described. The method is similar to the continuous-time LMS algorithm, but uses the TX LO as the reference signal and low-pass filters instead of the integrators. The method was implemented as part of a 0.18μm CMOS cellular-band receiver to cancel the TX leakage at the LNA input. The measured maximum rejection of the TX leakage is approximately 20dB, the LNA NF is 1.8dB, and the dc current is 4mA

RM01D-5 9:20

A 2.5mW Inductorless Wideband VGA with Dual Feedback DC-Offset Correction in 90nm CMOS Technology

Y. Wang, B. Afshar, T. Cheng, V. Gaudet*, A. M. Niknejad, Berkeley Wireless Research Center, University of California at Berkeley, *Univeristy of Alberta, Canada

Abstract: A low power inductorless wideband VGA for baseband receivers has been designed in a 90nm CMOS. The VGA was implemented using four-stage modified Cherry-Hooper amplifier with a novel dual feedback DC-offset canceling network, which simultaneously corrects DC offsets and extends bandwidth. The VGA has been measured using on-chip probing and achieves a 2.2GHz bandwidth with 60dB gain tuning range, consumes 2.5mW under a 1V supply and occupies only 0.01mm^2 die area.

Monday June 16, 2008
10:10
GWCC– Room A411
Session RMO2A: WLAN and WiMAX Transceivers

Chair: Srenik Mehta, Atheros Communications
Co-Chair: Bill Redman-White, NXP

RMO2A-1 10:10
A 65nm Low-power CMOS Transceiver for 802.11n Portable Application

Y.M. Chiu, T.M. Chen, P.Y. Chen, R. Kuan, Y.C. Shih, Y.J. Lin, C.L. Li, Realtek Semiconductor Corp., Hsinchu, Taiwan

Abstract: Low-power transceiver for 802.11N IN 65NM CMOS technology is presented. It supports 2X2 MIMO to satisfy the requirement of the draft 802.11N standard. In receiver chain it shows 5.3DB low noise figure. in transmit chain an on-chip PA driver delivers 9DBM output P1DB. -20 to 100°C operation temperature is achieved. A Fractional-N synthesizer is used to support variable reference frequency when using the RF IC in different application. It consumes 35.5MA for receiver chain & 77MA for transmit chain.

RMO2A-2 10:30
A MISO CMOS Transceiver For WLAN 802.11b/g/n Applications

C.J. Chang, P.C. Wang, W.M. Chiu, P.J. Chiu, C.C. Wang, Y.M.Chang, C.Y. Chen, K.T. Chen, C.H. Lu, S.M. Lin, C.P. Lin, K.U Chan, Y.H.Lin and C.C.Lee, Realtek Semiconductor Corp., Hsinchu, 300, Taiwan

Abstract: A 2.4GHz Fully-Integrated MISO Transceiver consisting of two receivers and one transmitter is implemented in 0.18μm CMOS technology. To alleviate the cost of external front-end components, the RF transmit/receive (T/R) switch and a power-efficient linear CMOS PA are fully integrated on-chip. It shows 3.5dB low noise figures in the receivers respectively. Also, the transmitter delivers an average power of 15.6dBm OFDM (64QAM, 54MBPS) signal with EVM of -28.7dB.

RM02A-3 10:50

A 0.13μm CMOS Transmitter with 72-dB RF Gain Control for Mobile WiMAX/WiBro Applications

H.-H. Kuo, Y.-H. Li, and Y.-H. Pang, SoC Technology Center, Industrial Technology Research Institute, HsinChu 310, Taiwan

Abstract: A direct conversion transmitter for Mobile WiMAX/WiBro is developed. It is composed of a reconstruction filter, an I/Q modulator, a four-stage RF PGA, and a PA driver. A 72-dB gain control range in 1-dB step is available by the RF PGA and the max. relative gain error is less than 0.5dB. The transmitter has a max. voltage gain of 4.3dB and OP1dB of 9.6dBm. The best measured EVM is 1.5% with -5dBm output power. The chip is fabricated in a 0.13μm 1P8M CMOS process and consumes 164mW DC power.

RM02A-4 11:10

2.5-GHz Fully-Integrated WiMAX Transceiver IC for a Compact, Low-Power Consumption RF Module

D. Yamazaki, N. Kobayashi, K. Oishi*, M. Kudo*, T. Arai, N. Hasegawa, K. Kobayashi, Fujitsu Laboratories Ltd., Fujitsu Ltd., Japan

Abstract: We fabricated a fully integrated WiMAX transceiver in a 90-nm CMOS that can reduce balun and matching network components on an RF module board. Output linearity up to 12 dBm and a wide variable gain range of 60 dB was achieved using a single signal interface with a PA Driver for the transmitter. We improved the matching network in the LNA to get an S11 of less than -20 dB between 2.5 and 2.7 GHz. The characteristics of the transceiver mean that it is suitable for WiMAX.

RM02A-5 11:30

A Fully Integrated Tri-Band, MIMO Transceiver RFIC for 802.16e

F. Beaudoin*, T. Zortea**, G. Deliyannides, M. Hiebert, M. McAdam, M. Venditti*, V. Choudary, B. Guay, H. Djahanshahi, T. McKeen, A. Hafez, PMC-Sierra, Inc., Burnaby, BC, Canada, *PMC-Sierra, Inc., Montreal, QC, Canada, **PMC-Sierra, Inc., Allentown

Abstract: A 0.18μm CMOS tri-band MIMO transceiver for fixed and mobile WiMAX applications is presented. The transceiver supports operation in the 2.3-2.7 GHz, 3.3-3.8 GHz, or 4.9-5.95 GHz bands. A novel DC-offset removal scheme is used to enConversion architecture. The transmitter exhibits an EVM of -38 dB, -36 dB, and -33 dB @ 0 dBm output power for the 2G, 3G, and 5G bands respectively. In full MIMO operation at 3.5 GHz, the TX dissipates 402 mW and 450 mW in RX mode.

Monday June 16, 2008
10:10
GWCC– Room A405
Session RMO2B: High Frequency VCOs

Chair: Stephen Dow, ON Semiconductor
Co-Chair: Timothy Hancock, MIT Lincoln Laboratory

RMO2B-1 10:10
60GHz VCOs with Transmission Line Resonator in a 0.25μm SiGe BiCMOS Technology

H. Veenstra, M.G.M. Notten, Philips Research, Eindhoven, The Netherlands

Abstract: In this paper, two varactorless 60GHz LC-VCOs are compared. One VCO uses a spiral inductor, the other VCO uses a shorted coplanar transmission line on a ground shield as inductor. The oscillator pulling sensitivity is compared. The spiral inductor offers a higher quality factor and self-resonant frequency, but poor substrate isolation. The VCO with shorted stub achieves a measured 22.6dB lower power level of the main oscillator sideband for a given interference level.

RMO2B-2 10:30
A Low Phase Noise LC-VCO with a High-Q Inductor Fabricated by Wafer Level Package Technology

K. Ohashi, Y. Kobayashi, H. Ito[1], K. Okada, H. Hatakeyama[2], T. Aizawa[2], T. Ito[2], R. Yamauchi[3], K. Masu, Integrated Research Institute, [1]Precision and Intelligence Laboratory, Tokyo Institute of Technology, [2]Electron Device Laboratory, Fujikura Ltd., [3]Fujikura Ltd.

Abstract: This paper proposes a low phase noise LC-VCO using a high-Q inductor fabricated by wafer level package (WLP) technology. Measured Q of inductor is 40 at around 1.9GHz. Capacitor-coupled varactors and filtering techniques are used to suppress flicker noises of transistors in a VCO. A phase noise is -134.4dBc/Hz at a 1MHz offset for 1.9GHz, which corresponds a FoM of -193dBc/Hz. The VCO with a WLP inductor improves phase noise of 6.4dB as compared to VCOs with conventional on-chip inductors.

RMO2B-3 10:50
The Process Variability of a V-band LC-VCO in 65nm SOI CMOS

Daeik D. Kim, Choongyeun Cho, Jonghae Kim, IBM Semiconductor Research and Development Center

Abstract: The process variability of a V-band LC-VCO implemented in 65nm SOI CMOS is examined. A complementary LC-VCO design, test set up, and measurements are presented. One lot of 300mm wafers in 65nm SOI are measured for statistics. There are 8 wafers in the lot, and 67 VCOs per wafer. The VCO frequency tuning range statistics, analog variability, yield estimation, and intra- vs. inter-wafer variations are analyzed and discussed. The VCO shows 90% yield from 65.1 to 67.9GHz.

RMO2B-4 11:10
Simultaneous Sub-harmonic Injection-Locked mm-Wave Frequency Generators for Multi-band Communications in CMOS

S-W. Tam, E. Socher, A.Wong, Y. Wang, L. D. Vu and M. F. Chang, University of California, Los Angeles

Abstract: A technique for generating multiple mm-wave carrier frequencies is introduced, using simultaneous sub-harmonic injection locking of multiple VCOs to a single reference frequency. A prototype of 30GHz and 50GHz sub-harmonic injection-locked VCOs is realized in a 90nm digital CMOS process and able to lock from 2nd to 8th harmonic of the reference frequency with locking range reaching 5.6GHz. and We also achieves demonstrate Simultaneous locking to the 3rd and 5th harmonics of a 10GHz reference.

RMO2B-5 11:30
VCO design for 60 GHz Applications Using Differential Shielded Inductors in 0.13μm CMOS

J. Borremans*, M. Dehan, K. Scheir*, M. Kuijk, P.Wambacq*, IMEC, Leuven, Belgium, *also Vrije Universiteit Brussel, Brussels, Belgium

Abstract: Two low-area VCOs are presented covering the license-free 60 GHz band, using differential shielded (slow-wave) transmission line inductors. We discuss design and provide compact modeling of these tanks, compatible with stringent metal density rules of scaled CMOS. Measured phase noise below -90 dBc/Hz at 1 MHz offset is achieved, at a consumption of 3.9 mW at 1 V. The tuning range exceeds 10%, for a tuning voltage restricted from ground to the supply.

Monday June 16, 2008
10:10
GWCC– Room A406-7
Session RM02C: Advanced Handset Power Amplifiers

Chair: Nick Cheng, Skyworks
Co-Chair: Bruce Thompson, Motorola, Inc

RM02C-1 10:10
A 65nm CMOS 30dBm Class-E RF Power Amplifier With 60% Power Added Efficiency

M. Apostolidou*, M.P. van der Heijden*, D.M.W. Leenaerts*, J. Sonsky**, A. Heringa** and I. Volokhine**, * NXP Semiconductors Research, Eindhoven (the Netherlands), **NXP-TSMC Research Center, Eindhoven (the Netherlands) – Leuven (Belgium)

Abstract: A 30dBm single-ended class-E RF PA is fabricated in 65nm CMOS technology. The PA consists of a driver followed by is a cascode stage formed by a standard thin-oxide device and a high voltage extended-drain thick-oxide device. Both devices are implemented in a standard sub-micron CMOS technology without using extra masks or processing steps. The proposed PA uses an innovative self-biasing technique and achieves a PAE of 60% at a Pout of 30dBm and a PAE of 40% at 16dB back-off at 2GHz.

RM02C-2 10:30
Design and Linearization of Class-E Power Amplifier For Non-constant Envelope Modulation

C.-T. Chen, C.-J. Li, T.-S. Horng, J.-K. Jau*, and J.-Y. Li*, National Sun Yat-Sen University, Taiwan, *Industrial Technology Research Institute, Taiwan

Abstract: A design and linearization techniques for efficient but nonlinear Class-E power amplifier applied to linear RF transmitters. A predistorted envelope modulation scheme is proposed to linearize the Class-E PA. The Class-E PA is designed with consideration of finite DC-feed inductance for wide supply-voltage modulation bandwidth. A digital envelope predistorter (DEP) is designed to provide the predistored envelope modulation for both RF-input and supply-voltage signals fed to the Class-E PA.

RMO2C-3 10:50
Efficient Three-State WCDMA PA Integrated With High-Performance BiHEMT HBT / E-D pHEMT Process
T. Apel, T. Henderson, Y. Tang, O. Berger, TriQuint Semiconductor

Abstract: Power amplifiers for WCDMA applications must provide competitive power efficiency at low power levels as well as at full power. This paper presents a novel approach to obtain high PAE performance over a wide power band from three power states. It uses a novel BiHEMT process to co-integrate InGaP/GaAs HBT technology with InGaAs/AlGaAs E/D-Mode pHEMT into a single process. No bias reference voltage is required. Typical ultra-low power mode quiescent current is 5 mA.

RMO2C-4 11:10
Switch-Mode Power Amplifier Linearization
D.E. Kelly, K. Mekechuk, and T. Miller, PulseWave RF

Abstract: A continuous time band-pass delta sigma modulator fabricated in a 0.18μm SiGe BiCMOS process was designed to accept analog intermediate frequency input up to 100 MHz and generate output up to 2.2 GHz. This modulator was inserted into a closed loop system containing multiple stages of switching amplifiers in cascade, to demonstrate linearization viability. Laboratory data show > 20 db of linearization is achieved with this technique processing multi-carrier cdma 2000 and WCDMA signals.

RMO2C-5 11:30
A 0.18μm CMOS Fully Integrated RF DAC and VGA For WCDMA Transmitters
S. Mehdizad Taleie*, Y. Han**, T. Copani**, B. Bakkaloglu**, S. Kiaei**, *Qualcomm, Inc., **Arizona State University

Abstract: A digital IF to RF converter architecture with an RF VGA targeted for WCDMA transmitters is presented. The RFDAC consists of a 1.5-bits current steering DAC with an embedded semi-digital FIR filter and a mixer with an LC load. The VGA controls the output power in 10dB steps. The prototype is fabricated in a 0.18um CMOS technology and achieves 0dBm output power at 2GHz and 33dB image rejection. The measured rms EVM and ACPR meet the WCDMA requirements. The chip draws 123.9 mA from a 1.8V supply.

Monday June 16, 2008
10:10
GWCC– Room A404
Session RM02D: Advanced Passive Circuits and Components

Chair: Chang-Ho Lee, Samsung
Co-Chair: Gary Zhang, Skyworks

RM02D-1 10:10
(INVITED) High-Performance RF Passives Using Post-CMOS MEMS Techniques for RF SoC

Xinxin Li, Lei Gu and Zhengzheng Wu, State Key Lab of Transducer Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences

Abstract: Real-world realization of RF SoC has been hindered by lack of high-performance, compact and tunable RF passive devices that are truly CMOS-compatible. This paper presents recent advances in low-temperature metal MEMS techniques developed to design and fabricate various high-performance RF passives for post-CMOS integration with RF SoC. Constructed with electroplated metal, the RF MEMS passives are suspended above the low-resistivity silicon substrate to depress both ohmic and substrate losses.

RM02D-2 10:30
An Area Efficient High Turn Ratio Monolithic Transformer For Silicon RFIC

Chee Chong Lim**, Qiu-ping**, Kiat Seng Yeo, Kok Wai Chew*, Suh Fei Lim*, Chirn Chye Boon and Manh Anh Do, Nanyang Technological University at Singapore (NTU), *Chartered Semiconductor Manufacturing (Chrt), **NTU & Chrt

Abstract: A novel way of manufacturing an on-chip transformer that produces high inductance ratio with excellent area efficiency is presented. This technique uses an electrical all-round coupling effect of a conductor A, with large effective width, and a densely routed conductor B. The conductor B can also be doubled up as a monolithic RF choke on silicon. This work compares unit inductance of various transformers for area efficiency. This technique is fully compatible to foundry standard CMOS processes.

RMO2D-3 10:50

Miniaturized Multi-Band Filter Banks for Extravehicular Radio (EVA) Applications

Philip J. Stephanou, Justin P. Black, and Andrew L. Benjamin*, Harmonic Devices Inc., *NASA Johnson Space Center

Abstract: NASA seeks to employ MEMS S-band filters to reduce the size, weight, and power of its reconfigurable, fault-tolerant, next-generation Extravehicular Activity (EVA) radio. We describe a novel double-layer contour-mode piezoelectric aluminum nitride (AlN) resonator topology that is amenable for use in GHz filter banks. Measured results of a 1.7 GHz resonator are presented, showing a motional resistance of 60 ohms and an electromechanical coupling coefficient of 0.9%.

RMO2D-4 11:10

A Low-Distortion, Low-Loss Varactor Phase-Shifter Based on a Silicon-on-Glass Technology

S. Kim, J.H. Qureshi, K. Buisman, L.E. Larson and L.C.N. de Vreede Center for Wireless Communication, University of California San Diego, La Jolla, CA, DIMES, Delft Institute of Microsystems and Nanoelectronics, TUDelft, The Netherlands

Abstract: A varactor-tuned continuously variable phase shifter based on an all-pass network is presented. Design equations for this phase shifter network are derived and presented. The phase shifter achieves an IIP3 of 52dBm with 10MHz tone-spacing at 2GHz and loss of 2.3-3.7dB with continuous 180 degrees phase shift at 2GHz. The total chip size including pads is 2900μm X 2200μm.

Monday June 16, 2008
13:20
GWCC– Room A411
Session RM03A: High-Frequency CMOS Mixers and Data-Converters

Chair: Frank Henkel, IMST GmbH
Co-Chair: Jaber Khoja, Microtune Inc.

RM03A-1 13:20
A 1GHz Bandwidth Low-Pass ΔΣ ADC with 20GHz to 50GHz Adjustable Sampling Rate

A. Hart and S. P. Voinigescu, University of Toronto, Canada

Abstract: This paper presents a wideband continuous-time ΔΣ-modulator intended for multi-gigabit OFDM receiver applications. Two versions of the circuit were fabricated in a 130-nm SiGe BiCMOS process with 170GHz ft in order to investigate the effect of finite gain and delay on dynamic range. The ADC achieves an SNDR of 44.3dB over a 500MHz passband and an SNDR of 37.1dB over a 1GHz passband while consuming 350mW from a 2.5V supply (650mW including clock distribution).

RM03A-2 13:40
A Resistively Degenerated Wide-Band Passive Mixer with Low Noise Figure and +60dBm IIP2 in 0.18μm CMOS

N. Kim, *V. Aparin, L.E. Larson, University of California at San Diego, *Qualcomm, Inc.

Abstract: A wide-band CMOS passive Mixer with 8dB Double Side Band (DSB) Noise Figure (NF) and 24dB voltage gain with +60dBm of un-calibrated IIP2 and +9dBm of IIP3 at 2GHz. A source degeneration method to improve NF and linearity is introduced and analyzed. Gm boosting methods, such as input cross-coupling, current reuse, complementary input, and back gate connection, are used. The Mixer consumes only 10mW from 2V power supply for I and Q both channels including trans-impedance amplifier stages (TIA)

RMO3A-3 14:00

High Linearity SiGe-MMIC Q-MOD Having Self Mixer Current Control Circuit with Output Power Detector for 0.4-5.8GHz Cognitive Radio

S. Shinjo, K. Tsutsumi, F. Onoma, N. Suematsu, H. Harada*, Mitsubishi Electric Corp, *National Institute of Information and Communications Technology

Abstract: A 0.4-5.8GHz high linearity SiGe-MMIC Q-MOD with a self mixer current control circuit is described. This circuit, which consists of an output power detector and an envelope current feedback circuit, is applied to unit mixers, and it automatically controls the mixer current according to the power level. It is shown by both simulation and measurement that the Q-MOD employing the proposed unit mixers realized the P1dB improvement compared with the conventional Q-MOD at the frequency of 0.4-5.8GHz.

RMO3A-4 14:20

A High IIP2 Multi-Standard CMOS Mixer for GSM, UMTS and IEEE802.11b-g-a Applications

Mohammad B. Vahidfar, Omid Shoaei *, Francesco Svelto, Unieversita degli studi di Pavia, 27100 Pavia, Italy, *University of Tehran, Iran

Abstract: The tough IIP2 required by cellular phone and 3G application can not be met without employing analog techniques for improving IIP2. A high IIP2 multi standard mixer, supporting GSM, DSC, PCS, UMTS and IEEE802.11b-g-a standards, is presented in this paper. The proposed is integrated in a 65nm CMOS technology by 1.2V supply. The IIP2 performance of the mixer is better than 65dBm in all bands except the IEEE802.11 band which is 54dBm,while the mixer current consumption is lower than 7.5mA.

RMO3A-5 14:40

Low-Power 1V 5.8GHz Bulk-Driven Mixer with On-Chip Balun in 0.18μm CMOS

D. Van Vorst, S. Mirabbasi, University of British Columbia, Department of Electrical and Computer Engineering, Canada

Abstract: Two bulk-driven down-conversion mixers with on-chip baluns are presented. The inclusion of the passive balun improves gain and provides impedance matching. Implemented in 0.18μm CMOS, the mixers operate in the 5.8GHz ISM band and consume 1mW from a 1ply. The mixer in which the RF signal is applied to the gates of the mixing transistors achieves a measured input-referred P1dB of -14dBm, an IIP3 of -5.2dBm, a gain of 13.6dB, a NF of 26dB, and an LO-to-RF isolation of greater than 50dB.

Monday June 16, 2008
13:20
GWCC– Room A405
Session RM03B: UWB Front-end ICs

Chair: Albert Wang
University of California, Riverside
Co-Chair: Stefan Heinen, Infineon Technologies AG

RM03B-1 13:20
(INVITED) 10GBASE-T for 10Gb/s Full Duplex Ethernet LAN Transmission over Structured Copper Cabling

S. K. Gupta, J. Tellado, S. Begur, F. Yang, M. A. Inerfield, D. Dabiri, J. Dring, S. Goel, K. Muthukumaraswamy, F. McCarthy, G. Golden, J. Wu, S. Arno and S. Kasturia, Teranetics Inc., Santa Clara, CA

Abstract: This paper reviews key features of the 10GBASE-T standard for full duplex 10Gb/s transmission over structured copper cabling in the LAN environment. Tradeoffs in implementing 10GBASE-T transceivers are discussed. We then present the first implementation of 10GBASE-T in digital CMOS technology (130nm). This transceiver also supports lower speeds for backward compatibility with legacy Ethernet ports and consumes 10.5W when operating at 10Gb/s over at 100m unshielded twisted pair cable.

RM03B-2 13:40
A 38-Gb/s 2-tap Transversal Equalizer in 0.13-μm CMOS using a Microstrip Delay Element

G. Ng, A. C. Carusone, University of Toronto

Abstract: This paper describes a single-ended integrated transversal 2-tap feed-forward equalizer implemented using a commercial 0.13-μm CMOS process. Equalization of a 38-Gb/s data stream over SMA cables with 14.3 dB of channel loss is demonstrated on-wafer. The equalizer features a microstrip transmission line as the delay element and "line inductors" for improved impedance matching. The IC measures 1.5mm x 0.26mm, and consumes 30 mW of power from a 1.2 V supply.

RM03B-3 14:00
A 35-GHz Differential Distributed Loss-Compensation Amplifier

James F. Buckwalter, University of California - San Diego

Abstract: The demand for 40+Gb/s broadband drivers and equalizers for electrical and optical links compels on-chip transmission line loss compensation. A distributed loss-compensation scheme is presented for synthetic transmission lines. The distributed loss-compensated amplifier is implemented in a 120nm BiCMOS process. A 3dB bandwidth of 35GHz is measured with gain ripple of ±1dB while consuming only 18mW.

RM03B-4 14:20
Wide-band CMOS Loop-Through Amplifier for Cable TV Tuner

S. Jin, T. Oh, K. Hong, H. Kim, B. Kim*, System IC Team, LG Electronics, Inc., Seoul, Korea , *Pohang University of Science and Technology, Pohang, Korea

Abstract: A fully integrated loop-through amplifier (LTA) for Cable TV tuner is presented in a 0.18μm CMOS process. It covers the whole frequency band from 48MHz to 860MHz and allows a second TV and multiple tuners. This circuit employs a parallel connection of common-gate and common-source (CG-CS) amplifiers for broadband matching. The performances are enhanced by current amplification for high linearity and by noise canceling for low noise figure.

RM03B-5 14:40
A Novel Wide-Band Envelope Detector

Yan-Ping Zhou, Guochi Huang, Sangwook Nam* and Byung-Sung Kim, Sungkyunkwan University, Suwon, Korea, *Seoul National University, Seoul, Korea

Abstract: In this paper, we present a novel wide-band envelope detector. To enhance the frequency performance of the envelop detector, we utilize gyrator-C active inductor loads in the OTA for wider bandwidth. Additionally, it is shown that the high speed rectifier of the envelope detector requires high bias current. The experimental results show that the proposed envelope detector can work from 100-Hz to 1.6-GHz with an input dynamic range of 50-dB at 100-Hz and 40-dB at 1.6-GHz, respectively.

Monday June 16, 2008
13:20
GWCC– Room A406-407
Session RMO3C: Silicon Millimeter-Wave

Chair: Kevin Kobayashi, RFMD
Co-Chair: Paul Blount, Custom MMIC Design Services

RMO3C-1 13:20
A Q-Band (40-45 GHz) 16-Element Phased-Array Transmitter in 0.18-μm SiGe BiCMOS Technology

K.-J. Koh, J. W. May, G. M. Rebeiz, University of California at San Diego

Abstract: A 16-element phased-array transmitter based on 4-bit RF phase shifters is designed for Q-band applications. The phased-array shows 12.5±1.5dB of power gain per channel at 42.5GHz with a 3dB gain bandwidth of 40-45.6GHz ≤8.8° of RMS phase error, of RMS gain error and an OIP3 of 6±1.5 dBm per channel. The transmitter also resuts in≤1.2dB RMS gain variation and o RMS phase mismatch between 16 channels. The chip consumes 720mA/5V with 2.6x3.2 mm^2 of area in a 0.18um SiGe BiCMO

RMO3C-2 13:40
A 1.2V, 140GHz Receiver with On-Die Antenna in 65nm CMOS

S. T. Nicolson*, A. Tomkins*, K. W. Tang*, A. Cathelin**, D. Belot**, and S. P. Voinigescu*, *Edward S. Rogers, Sr. Dept. of Electrical & Computer Engineering, University of Toronto, Toronto, Canada, **STMicroelectronics, Crolles, France

Abstract: This paper presents a 1.2V, 100mW, 140GHz receiver with on-die antenna in a 65nm GP CMOS process with digital BEOL. The receiver has conversion loss of 19dB at 140GHz with 102GHz LO, and occupies only 580μm x 700μm. The LNA achieves 8dB gain at 140GHz, 10GHz bandwidth, at least -1.8dBm of Psat, and maintains 3dB gain at 125°C. The antenna meets all density requirements, has -25dB gain, and occupies 180μm x 100μm. Design techniques which maximize the mm-wave performance of CMOS are also discussed.

RMO3C-3 14:00,
A 77GHz 4-Channel Automotive Radar Transceiver in SiGe

H. P. Forstner, H. Knapp, H. Jäger*, E. Kolmhofer*, J. Platz*, F. Starzer**, M. Treml**, J. Böck, K. Aufinger, R. Lachner, T. Meister, H. Schäfer, D. Lukashevich, A. Fischer*, F. Reininger, L. Maurer*, J. Minichshofer, D. Steinbuch***, Infineon Technologies AG, Germany, *DICE GmbH, Austria

Abstract: A fully integrated 4-channel automotive radar transceiver chip, integrated in a 200-GHz SiGe:C production technology, is presented. With a typical transmit power of 2x +8dBm at the antenna ports and all functions active, the chip draws a current of about 600mA from a single 5.5V supply. The design permits FMCW operation in the 76 to 77GHz band at chip-backside temperatures from -40°C to +125°C.

RMO3C-4 14:20
A 91 GHz Receiver Front-End in Silicon-Germanium Technology

Jihwan Kim*, Javier Alvarado Jr.* **, and Kevin T. Kornegay*,
*Electronic Design Center, Georgia Institute of Technology Atlanta, GA
**Raytheon Company, RF Electronics, Tucson, Arizona

Abstract: A W-band receiver front-end, including a low-noise amplifier(LNA), a coupled-wire Marchand balun and a double-balanced mixer, has been designed and fabricated in IBM's 8 HP is 0.12μm, 200 GHz-f_T, SiGe technology. The circuit operates in the 87-94 GHz frequency with a peak conversion gain of 36.3dB and a minimum single sideband(SSB) noise figure of 10 dB. At 91 GHz the measured 1dB input compression point is -36dBm. The entire circuit occupies 1.82mm^2 including bond pads and dissipates 109.7mW.

RMO3C-5 14:40
A W-Band SiGe 1.5V LNA for Imaging Applications

J. W. May, G. M. Rebeiz, University of California at San Diego

Abstract: We present a 4-stage SiGe W-Band Amplifier for imaging applications designed in a 200 GHz Ft SieE BiCMOS process (IBM 8HP). The amplifier has 19 dB gain at 85-89 GHz, 3-dB Bandwidth of 17 GHz, NF of 8-10 dB over the measurement band, and consumes only 25 mW of DC power. The small amplifier (0.1mm^2 without pads) is ideal for 8 or 16-element imaging arrays on a single chip. To our knowledge, this is the first demonstration of a high-gain, high-bandwidth W-band amplifier using SiGe technology.

Monday June 16, 2008
13:20
GWCC– Room A404
Session RM03D: Next Generation RF Models and Devices

Chair: Kevin Mc Carthy, University College Cork
Co-Chair: Bumman Kim, Pohang University of Science and Technology

RM03D-1 13:20
(INVITED) The New CMC Standard Compact MOS Model PSP: Advantages For RF Applications

A.J. Scholten, G.D.J. Smit, B.A. De Vries, L.F. Tiemeijer, J.A. Croon, D.B.M. Klaassen, X. Li*, W. Wu*, and G. Gildenblat*, NXP-TSMC Research Center, Eindhoven, The Netherlands,, *Department of Electrical Engineering, Arizona State University, Tempe

Abstract: First the surface-potential-based compact MOS model, PSP, is introduced. After a discussion of the general advantages of this surface-potential-based compact MOS model, the PSP model is benchmarked against measurements from the 45nm technology node. Finally, we zoom in on the modeling in PSP of a number of effects that are of special importance for RF applications: distortion and noise.

RM03D-2 13:40
Experimental Characterization and Simulation of RF Intermodulation Linearity in a 90 nm RF CMOS Technology

Xiaoyun Wei, Guofu Niu, Ying Li, Ming-Ta Yang*, Stewart S. Taylor**, Electrical and Computer Engineering Department, Auburn University, *Spice Modeling Dept., TSMC, Taiwan, **Communications Circuits Lab, Intel Corporation

Abstract: This work examines the intermodulation linearity of 90nm RF CMOS using IP3 measurement, BSIM4 based simulation, and first order theory. VGS, VDS, and device width dependencies are examined. Guidelines to accurately identifying the sweet spot biasing current for larger devices used in RFIC design are provided.

RM03D-3 14:00
Statistical Variations in VCO Phase Noise due to Upconverted MOSFET 1/f Noise

M. Erturk+*, T. Xia+, R. L. Wolf*, D. P. Scagnelli*, W. F. Clark+*,
+School of Engineering, University of Vermont, Burlington, VT,
*IBM Systems and Technology Group, Essex, Junction, VT

Abstract: Statistical phase noise analysis and measurements are presented for a population of RF CMOS VCOs. The measured mean values for phase noise at 1kHz and 1MHz offset are -46 dBc/Hz and -130 dBc/Hz respectively. A large variation from the mean (3dBc/Hz) is observed for the close-in phase noise. This is attributed to the upconverted transistor 1/f noise and its statistical nature. Simulations with two versions of statistical 1/f noise models are compared to measurements.

RM03D-4 14:20
Novel Pseudo-Drain (PD) RF Power Cell in 0.13μm CMOS Technology

S.Y. Huang, C.C. Hung, T.L. Lee, V. Liang, UMC, Inc., Taiwan

Abstract: This paper proposes a cost-effective RF power cell manufactured in an advanced 0.13μm CMOS technology. Without adding additional masks, cost, and process, the power performance can be improved just by using the standard N-well and shallow-trench-isolation processes to form a higher resistive region. This "Pseudo-Drain" structure increases the breakdown voltage to more than 4.3V and is higher than the value of 2.5V of the standard 0.13μm core-MOS transistor.

RM03D-5 14:40
Characterization and Modeling of Asymmetric LDD MOSFET for 65nm CMOS RF Power Amplifier Design

Kai-Yi Huang, Po-Chih Wang, Yuh-Sheng Jean, Ta-Hsun Yeh, Ying-Hsi Lin, Realtek Semiconductor Corp., Hsin-Chu, Taiwan, 300, ROC

Abstract: This study demonstrates an RF active device based on Asymmetric Lightly Doped Drain MOSFET structure. It is suitable to be used in RF PA design for SoC in advance 65nm and below technology. The manufacturing of A-LDD MOSFET is compatible with standard CMOS process and no extra mask required. A RF macro model of A-LDD MOSFET is proposed by combining a bias dependent series resistance sub-circuit with BSIM4 MOS model. Besides, a cascode PA composed of A-LDD device is designed and simulated.

Monday June 16, 2008
15:30
GWCC– Room A411
Session RM04A: Wireless Systems

Chair: Glenn Chang, MaxLinear
Co-Chair: Natalino Camilleri, Alien Technology

RM04A-1 15:30
A 5.8GHz Low-IF Mult-Data Rate GFSK Transceiver with Carrier Recovery and Integrated 21dBm Power Amplifier

C. Quek, S. Farahvash, W. Roberts, M. Romney, D. Walker, C. Otten, R. Wei, D. Schwan, M. Mostafa[1], D. Haab, J. Liu[2], H. Liem[3], R. Koupal[4], RFMD, [1]Beceem Communications, [2]Marvell Semiconductor Inc., [3]Sigma Designs Inc., [4]Scintera Networks Inc.

Abstract: A highly integrated 5.8GHz transceiver capable of supporting multiple data rates has been designed in 0.18μm SiGe BiCMOS for digital cordless phones and streaming audio applications. It includes a clock data recovery circuit (CDR). The transmitter with an integrated power amplifier consumes 185mA achieving an output power of 20.5dBm and the receiver consumes 65mA achieving a sensitivity of -103.5dBm and -101.5dBm at 1.536Mbps and 2.048Mbps respectively. The active area is 7.3mm^2.

RM04A-2 15:50
An Ultra Low Power 130nm CMOS Direct Conversion Transceiver for IEEE802.15.4

C. Bernier, F. Hameau, G. Billiot, E. de Foucauld, S. Robinet, J. Durupt, F. Dehmas, E. Mercier, P. Vincent, L. Ouvry, D. Lattard, M. Gary, C. Bour, J. Prouvée, S. Dumas, CEA-LETI, MINATEC, Grenoble, France

Abstract: A fully integrated 2.4GHz transceiver based on the IEEE802.15.4 specification has been designed using a 130nm CMOS technology. Concurrent system and design optimizations were required to reach an energy efficiency of 21.5nJ/bit in RX mode and 32.5nJ/bit in TX modes, respectively, at a data rate of 250kbit/s. The circuit includes a -5dBm transmitter, a -81dBm sensitivity receiver, an integer N PLL with 5MHz reference, a dual I/Q 3-bit ADC at 4MS/s, an analog RSSI with 8-bit ADC at 8kS/s.

RM04A-3 16:10

A Compact and Power Efficient Local Oscillator Generation and Distribution System for Complex Multi Radio Systems

Reza Roufoogaran*, Tom (Qiang) Li*, Adedayo Ojo**, Shelley Cheng***, C. Paul Lee**, Sajeevan Mahadeva*, Prashant Shetter***, Arya Behzad**, *Broadcom Corporation, Irvine, CA, **Broadcom Corporation, San Diego, CA, ***Broadcom Corporation, Sunnyvale, CA

Abstract: A 65nm, 0.53mm^2, CMOS multi-radio-frequency local oscillator generation and distribution system, utilizes single phase routings, a single VCO and smaller Q inductors (compensated by a negative R stage) to reduce area, quadrature coupling, and power consumption. The LO amplitude, IQ imbalances and current consumption are adjusted dynamically by an automatic control loop in order to maintain optimum performance. This work results in 60% area and 50% power savings relative to prior implementations

RM04A-4 16:30

A 900-MHz RFID System with TAG-Antenna Magnetically-Coupled to the Die

A. Finocchiaro*, G. Ferla*, G. Girlando*, F. Carrara**, G. Palmisano**, *STMicroelectronics, Catania, Italy, **University of Catania, Catania, Italy

Abstract: An innovative UHF-RFID system employing a magnetic coupling between the die of a TAG and its external antenna is presented. The proposed solution avoids the physical connection between die-antenna, thus improving TAG feasibility while reducing assembling and testing costs. This solution permits to perform wireless on wafer TAG testing.

RM04A-5 16:50

A 2mW 400MHz RF Transceiver SoC in 0.18μm CMOS Technology for Wireless Medical Applications

M.R. Nezhad-Ahmadi*, G. Weale*, A. El-Agha*, D. Griesdorf*, G. Tumbush**, A.Hollinger***,M.Matthey***,H.Meiners***, S. Asgaran*, *AMI Semiconductor, Waterloo, ON, Canada, **AMI Semiconductor, Colorado, ***AMI Semiconductor, Marin, Switzerland

Abstract: A 2mW 400MHz 128kbps-FSK RF transceiver was implemented in a 0.18μm CMOS technology for wireless medical applications. The transceiver was directly matched to a non-50ohm miniaturized dipole antenna. The receiver sensitivity of -93dBm (BER=10^{-3}) was measured for 128Kbps data rate.The transceiver architecture has the ability of selection of image band in receive mode and transmitting in the image band in transmit mode. The whole transceiver occupies a die area of less than 2.6mm^2.

Monday June 16, 2008
15:30
GWCC– Room A405
Session RM04B: Advanced Frequency Synthesizer Design

Chair: Bertan Bakkaloglu, Arizona State University
Co-Chair: Sanjay Raman, Virginia Tech/DARPA

RM04B-1 15:30
(INVITED) Analysis and Modeling of Noise Folding and Spurious Emission in Wideband ΔΣ; Fractional-N Synthesizers

Waleed Khalil*, Hiva Hedayati**, Bertan Bakkaloglu**
and Sayfe Kiaei**, Intel Corporation*, Arizona State University**

Abstract: Fractional-N synthesizers are subject to generation of undesired spurious energy due to both linear and nonlinear processes. In this paper an accurate model for modeling the non-linear, time-varying nature of the phase frequency detector (PFD), charge pump and frequency divider is presented. A behavioral model is also used to show that the more detrimental near-integer in-band spurs can be generated by cross-coupling between the synthesizer's various building blocks.

RM04B-2 15:50
A 40GHz Fractional-N Frequency Synthesizer in 0.13μm CMOS

Chao-Ching Hung, Ding-Shiuan Shen and Shen-Iuan Liu, Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taiwan, R. O. C.

Abstract: A 40GHz fractional-N frequency synthesizer with a divide-by-64/64.5/65/65.5 fractional multi-modulus divider (MMD) is presented in a 0.13μm CMOS technology. This fractional MMD provides a half division step of a conventional integer MMD. The measured fractional spur is below -50dB. The measured phase noise is -75.3dBc/Hz and -93.24dBc/Hz at 1MHz and 3MHz offset, respectively. The die area is 1.34 x 1.26 mm^2 and the power dissipation is 105mW from the supply of 1.5V.

RM04B-3 16:10

A 0.13μm CMOS Σ–Δ Frequency Synthesizer with an Area Optimizing LPF, Fast AFC Time, and a Wideband VCO for WCDMA/GSM/GPRS Applications

Kun-Seok Lee, Hwayeal Yu, Hyung Ki Ahn, Hyoung-Seok Oh, Dongjin Keum, and Byeong-Ha Park, Samsung Electronics, Korea

Abstract: This paper presents a fully integrated fractional-N frequency synthesizer with an area optimizing LPF, a fast AFC Time, and a wideband on-chip LC VCO for WCDMA/GSM /GPRS/EDEG transceivers. The LPF employs a staked structure of MIM and MOS capacitors to economize the area. A fast AFC time is realized by using the high frequency prescaler output signal as a reference clock determining the AFC frequency resolution. To suppress the **Σ–Δ** noise boosting, phase switching type prescaler is used.

RM04B-4 16:30

A Fully Integrated 1.175-to-2GHz Frequency Synthesizer with Constant Bandwidth for DVB-T Applications

L. Lu, L. Yuan, H. Min and Z. Tang, ASIC & System State Key Laboratory, Fudan University, China

Abstract: A fully integrated 1.175 to 2GHz differentially tuned frequency synthesizer aimed for DVB-T tuners is implemented in 0.18μm CMOS. Techniques are proposed to make the loop bandwidth constant across the whole output frequency range to maintain phase noptimization and loop stability. It exhibits in-band phase noise of -97.6dBc/Hz at 10kHz offset and integrated phase error of 0.63° from 100Hz to 10MHz. The chip draws 10mA from a 1.8V supply while occupying 2.6mm^2 die area.

RM04B-5 16:50

A Digitally Calibrated 64.3-66.2GHz Phase-Locked Loop

Kun-Hung Tsai, Jia-Hao Wu, and Shen-Iuan Liu, Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taiwan, R. O. C.

Abstract: In this paper, a 64.3-66.2GHz digitally-calibrated phase-locked loop (PLL) is presented in 0.13μm CMOS technology. A digital calibration circuit is used to align the center operation frequency between the VCO and the divider. At 64.3GHz, the measured noise at 1MHz offset is 84.1dBc/Hz. The PLL consumes 72mW without output buffers from 1.2V supply.

Monday June 16, 2008
15:30
GWCC– Room A406-7
Session RM04C: RF Switches and Switchable Components

Chair: Joe Staudinger, Freescale, Inc
Co-Chair: Noriharu Suematsu, Mitsubishi Electrics

RM04C-1 15:30
(INVITED) An Ultra-Low Insertion Loss T/R Switch Fully Integrated With 802.11b/g/n Transceiver in 90nm CMOS

A.A.Kidwai, *C.T.Fu, R.Sadhwani, Chu Chi D, J.C.Jensen, S.Taylor, Intel Corporation, Hillsboro, OR, *National Chiao-Tung University, Hsinchu, Taiwan

Abstract: An Ultra Low Insertion loss T/R switch fully integrated with 802.11b/g/n direct conversion transceiver front end in 90nm CMOS. The receiver achieves 3.6dB NF at 2.4GHz. The T/R switch P1dB is approx 31dBm. The T/R switch has been designed and tested and has 0.3dB insertion loss in the transmit mode and adds 0.1dB of NF in the receive mode while occupying 0.02mm^2 of the die area.

RM04C-2 15:50
A 5-GHz, 30-dBm, 0.9-dB Insertion Loss Single-Pole Double-Throw T/R Switch in 90nm CMOS

C.-T. Fu* **, S. S. Taylor*, C.-N. Kuo**, * Intel Corporation, Hillsboro, Oregon, ** National Chiao-Tung University, Hsinchu, 300, Taiwan

Abstract: A 5GHz, 30-dBm CMOS T/R switch implemented in 90nm CMOS is reported. A body isolation technique is employed and optimized for power handling capability. Inductors are employed with the transistor switches for parallel resonance to improve isolation. Thick oxide NMOS transistors are used for the switching transistors and placed inside the inductors to reduce the active chip area to approximately 0.2mm^2. 0.9-dB insertion loss for both TX and RX modes is achieved with a 5-V control voltage.

RM04C-3 16:10
5-6 GHz SPDT Switchable Balun Using CMOS Transistors

B-W. Min, G. M. Rebeiz*, University of Michigan at Ann Arbor,
*University of California at San Diego

Abstract: This paper presents a switchable transformer balun using CMOS switches. The top four metal layers of a CMOS process are used for the transformer. The secondary inductor is symmetrically wound, and the CMOS transistors are placed at the center-taps for the switching operation. The measured insertion loss of the switchable balun is 1.6-1.7 dB at 5-6 GHz with excellent input/output match, and the P1dB is 12 dBm. To our knowledge, this is the first implementation of a switchable transformer balun.

RM04C-4 16:30
A Stage-Bypass SOI-CMOS Switch for Multi-Mode Multi-Band Applications

A. Scuderi, C.D. Presti*, F. Carrara*, B. Rauber**, G. Palmisano*,
STMicroelectronics, Catania, Italy, *University of Catania, Italy,
**STMicroelectronics, Crolles, France

Abstract: A double-pole double-throw SOI CMOS switch is presented, which can be exploited to bypass a power stage in a radio transmitter with the aim of improving efficiency in applications requiring transmit power control. The switch is designed through transistors stacking. It is able to manage up to a 35 dBm input power with less than 0.35 dB insertion loss from 500 MHz through 3 GHz. Series-shunt topology allows a better than 40 dB isolation to be obtained in high-power mode with excellent linearity.

RM04C-5 16:50
High Power GaN HEMT Microwave Switches for X-band and Wideband Applications

A. Bettidi, A. Cetronio, M. De Dominicis*, G. Giolo*, C. Lanzieri,
A. Manna*, M. Peroni, C. Proietti, P. Romanini, SELEX Sistemi Integrati
SpA, *Elettronica SpA, Italy

Abstract: The design, fabrication and test of X-Band and 6-18 GHz wideband high power SPDT MMIC switches in GaN technology are presented. Said switches have demonstrated state-of-the-art performance and RF fabrication yields better than 65%. In particular the X-Band switch has an on-state power handling capability of better than 37dBm at the 1dB insertion loss compression point and the wideband switch shows a insertion loss compression of 1dB for input power higher than 34.3 dBm in the overall bandwidth.

Monday June 16, 2008
15:30
GWCC– Room A404
Session RM04D: CMOS Transceiver Front-ends

Chair: Georg Boeck, University of Technology, Berlin
Co-Chair: Walid Ali-Ahmad, Mediatek Singapore Pte Ltd

RM04D-1, 15:30
A CMOS Code-Modulated Path-Sharing Multi-Antenna Receiver Front-End for Spatial Multiplexing, Spatial Diversity and Beamforming

F. Tzeng, A. Jahanaian, P. Heydari, University of California, Irvine

Abstract: Design of novel 5GHz multi-antenna RF front-end, which is capable of performing spatial multiplexing, spatial diversity, and beamforming. The use of a unique code-modulation scheme at the RF stages of the signal paths enables linear combination of all mutually orthogonal code-modulated received signals. The combined signal is then fed to a single RF/baseband/ADC chain, resulting in a significant reduction of power consumption and area, as well as mitigating the issue of LO routing/distribution.

RM04D-2 15:50
A High Performance 2-GHz Direct-Conversion Front End with Single-Ended RF input in 0.13μm CMOS

Y.Feng*, G.Takemura**, S.Kawaguchi**, P.Kinget*, *Columbia University, New York,, **Toshiba Corporation Semiconductor Company, Yokohama, Japan

Abstract: This paper describes a 2.1-GHz CMOS front-end with a single-ended low noise amplifier (LNA) and a double balanced, current-driven passive mixer. The LNA features an on-chip transformer load to perform single-ended to differential conversion. Implemented in a 0.13μm CMOS process, it achieves 30 dB conversion gain, a low noise figure of 3.1 dB, a 40 kHz 1/f noise corner, an in-band IIP3 of -12 dBm and IIP2 better than 39 dBm, while consuming only 12 mW from a 1.5V power supply.

RMO4D-3 16:10

A 6-to-18 GHz Tunable Concurrent Dual-Band Receiver Front End for Scalable Phased-Arrays in 0.13μm CMOS

Y. Wang, S. Jeon, A. Babakhani, and A. Hajimiri, California Institute of Technology, Pasadena, CA

Abstract: This paper presents a study and design of tunable concurrent dual-band receiver. Different system architectures and building blocks have been compared and analyzed. A tunable concurrent dual-band receiver front end has then been designed and characterized. It operates across a tri-tave 6-18GHz bandwidth with a nominal 17-25dB conversion gain, worst-case -15dBm IIP3, and worst-case -24.5dBm ICP1dB.

RMO4D-4 16:30

A Rapid Interference Detector for Ultra Wideband Radio Systems in 0.13μm CMOS

Tien-Ling Hsieh, Peter Kinget*, Ranjit Gharpurey, University of Texas at Austin, TX, 78712, *Columbia University, NY

Abstract: A broadband low-power down-converter that can rapidly scan the UWB spectrum within several tens of nano-seconds to detect large interferers, is presented. The detector employs cascaded image-reject stages, each consisting of harmonic-rejection mixers, and decomposes the spectrum into 16 equal sub-bands. The LO path uses a single HF input with integer dividers. The IC is in 0.13μm CMOS. It requires 17mA in the signal path and 24mA for the LO path, from a 1.2V VDD, while spanning 1.75 to 8.75GHz.

RMO4D-5 16:50

Integrated Time Division Multiplexing Front-End Circuit for Multi-Antenna RF Receivers

G. Krishnamurthy, K. G. Gard, North Carolina State University

Abstract: A fully integrated receiver front-end circuit for a 4:1 time division multiplexing of RF signals from an antenna array is introduced. The switching necessary for multiplexing is implemented as an array of low noise amplifiers operating at 2.4 GHz with selectable outputs. The circuit includes on-chip input and output matching networks. A digital controller for rotating through the amplifier inputs was also incorporated. The multiplexer design was fabricated in a 0.18μm RF-CMOS process.

Tuesday June 17, 2008
8:00
GWCC– Room A311
Session RTU1A: Silicon Millimeter-Wave 2

Chair: Carlos E. Saavedra, Queen's University, Canada
Co-Chair: Brian Floyd, IBM

RTU1A-1 8:00
(INVITED) mm-Wave Silicon ICs: An Opportunities For Holistic Design

Ali Hajimiri, California Institute of Technology, Pasadena, CA

Abstract: Millimeter-waves integrated circuits offer a unique opportunity for a holistic design approach encompassing RF, analog, and digital codesign, as well as radiation and electromagnetics. The ability to deal with the complete system from the digital circuitry to on chip antennas and everything in between offers unparalleled opportunities for completely new architectures and topologies, previously impossible due the partitioning of various blocks in conventional design.

RTU1A-2 8:20
A 24 GHz 4-Channel Phased-Array Receiver in 0.13 μm CMOS

Tiku Yu, Gabriel M. Rebeiz, University of California, San Diego

Abstract: An integrated 24 GHz 4-channel phased-array receiver front-end is implemented in 0.13μm CMOS. An All-RF architecture is adopted and results in low power consumption and very small chip area. Each phased-array channel has a measured gain of 15 dB for a 2.5 GHz bandwidth, a NF of 6.5 dB, and an input P1dB of -25 dBm. The measured 16 phase states exhibit < 0.5 dB rms gain error and < 3 degrees rms phase error at 21-24.5 GHz. The entire array consumes 120 mW and occupies an area of 2.11 x 1.43mm^2.

RTU1A-3 8:40
A 24-GHz Full-360 Degrees CMOS Reflection-Type Phase Shifter MMIC with Low Loss-Variation

Jen-Chieh Wu, Chia-Chan Chang, Sheng-Fuh Chang, and Ting-Yueh Chin, Department of Electrical Engineering, Department of Communications Engineering, Center for Telecommunication Research, National Chung Cheng University, Chia-Yi, 621, Taiwan

Abstract: A 24-GHz bi-directional CMOS reflection-type phase shifter (RTPS) with full 360° phase tuning range and minimal insertion-loss variation is presented. Two circuit enhancement techniques are employed: the broadside-coupled transformer-based hybrid and the π-type resonated varactor load. The implemented 0.18μm CMOS RTPS demonstrates a measured phase shift range of 360° with small insertion-loss variation of ±1.2 dB at 24 GHz. The chip is 0.33mm^2 in area and it consumes zero DC power.

RTU1A-4 9:00
A High-Linearity, LC-Tuned, 24-GHz T/R Switch in 90-nm CMOS

Piljae Park, Dong Hun Shin, John J. Pekarik*, Mark Rodwell and C. Patrick Yue, High-Speed Silicon Lab, University of California, Santa Barbara, CA 93106, *IBM Microelectronics, Essex Junction, VT

Abstract: We have presented the design of a 24-GHz SPDT T/R switch that achieves the highest linearity (28.7dBm of P_{-1}dB) among CMOS switches for mm-wave applications. The switch utilizes a single 1.2-V digital control signal to select Rx/Tx mode and to set trce/drain bias of the switch devices. The design focuses on the techniques to increase the power handling capability in the transmit (Tx) mode. The prototype switch is well suited for integration with multi-channel transceiver.

RTU1A-5 9:20
A 24 GHz 3.3 dB NF Low Noise Amplifier Based Upon Slow Wave Transmission Lines and the 0.18μm CMOS Technology

A. Sayag*, S. Levin**, D. Regev**, D. Zfira**, S. Shapira**, D. Goren*** and D. Ritter*, *Department of Electrical Engineering, Technion, Haifa, Israel, **Towere Semiconductors Inc., Midgal Maemek, Israel, ***IBM Haifa Research Laboratories, Haifa, Israel

Abstract: A 24 GHz low noise amplifier using standard 0.18μm digital CMOS technology is presented. Matching networks were based upon slow wave transmissions lines. Peak gain of 12.8 dB at 24 GHz and in-band minimum noise figure less than 4 dB were obtained at power consumption of 8 mW. These record results demonstrate the usefulness of the slow wave transmission line approach. A compact model of slow wave transmission lines is briefly described as well.

Tuesday June 17, 2008
8:00
GWCC– Room A312
Session RTU1B: Digital Enabled VCOs

Chair: Tian-Wei Huang, National Taiwan University
Co-Chair: Adrian Maxim, Silicon Labs

RTU1B-1 8:00
A Self-Calibrated LC Quadrature VCO in a Current-Limited Region

S. Byun, K.-W. Kim*, D.-H. Lee*, J. Laskar*, C. S. Kim, ETRI, South Korea, *Georgia Institute of Technology

Abstract: This paper presents a self-calibrated LC quadrature VCO in a current-limited region. Our steady-state phasor analysis shows that phase and amplitude errors of an LC QVCO in a current-limited region are linearly related to each other. Based on this linear relationship, we propose a self-calibration technique which uses a low speed amplitude error detector instead of a conventional high speed phase detector. As a prototype, a 2.7GHz self-calibrated LC QVCO was implemented in a 0.18μm CMOS process.

RTU1B-2 8:20
VCO Gain Calibration Technique for GSM/EDGE Polar Modulated Transmitter

H. K. Ahn, K.-S. Lee, H. Yu, H.-S. Oh, D. Keum, B.-H. Park, Samsung Electronics, Korea

Abstract: This paper describes a VCO gain calibration technique for the two-point modulation scheme using delta-sigma frequency synthesizer. The proposed technique enables PLL-based phase modulator to have wide bandwidth with good signal quality. A fully integrated GSM/EDGE polar modulated transmitter, implemented in a 0.13μm CMOS process, is presented to show the feasibility of the calibration technique. After the calibration, it shows a margin of 8dB to the spectrum mask at 400kHz offset with EVM of 2%.

RTU1B-3 8:40
A Low-Noise VCO with a Constant Kvco For GSM/GPRS/EDGE Applications

T. Y. Lin, T. Y. Yu, L. W. Ke, G. K. Deng, MediaTek Inc. No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300, R.O.C.

Abstract: A low-noise LC-tank VCO with a constant KVCO for GSM/GPRS/EDGE applications is presented. The proposed compensation technique helps to minimize the KVCO variation within the operation frequency of interest. the measured KVCO is 29MHz/V with a± tuning range for a single sub-band and the overall KVCO variation is 2.5% when the compensation technique is enabled. Based on this low-noise VCO, the achieved DCT phase noise is -165dBc/Hz at a 20MHz frequency offset from a 915MHz carrier.

RTU1B-4 9:00
A Transfer-Curve-Folded DCO in 0.13μm CMOS

Jing-Hong Conan Zhan, RF Division, MediaTek, HsinChu, Taiwan

Abstract: A DCO which achieves fine frequency resolution, provides interface controls for all-digital PLLs, and has a folded transfer curve to avoid frequency discontinuity is presented. The DCO occupies 520μm x 780μm, uses 20mA current and operates from 3.2GHz to 4.0GHz. Its phase noise at 400kHz, 3MHz and 20MHz are 117.3, -135.9 and -153.3dBc/Hz, respectively. Its frequency coverage range and the phase noise satisfy requirements for GSM/GPRS/ EDGE applications.

RTU1B-5 9:20
A Ring VCO with Wide and Linear Tuning Characteristics for a Cognitive Radio System

J.Choi, K.Lim, J.Laskar, Georgia Electronic Design Center, Georgia Institute of Technology

Abstract: This paper presents a novel voltage-controlled ring oscillator for a Cognitive Radio System. In order to obtain a linear frequency-voltage characteristic over a wide tuning range while maintaining good phase noise performance, a transmission gate was adopted in a saturated-type ring oscillator. The resistance tuning capability of the transmission gate was then theoretically and experimentally analyzed.

Tuesday June 17, 2008
8:00
GWCC– Room A315-316
Session RTU1C: Supply Modulators for Power Amplifiers

Chair: Noriharu Suematsu, Mitsubishi Electrics
Co-Chair: Freek van Straten, NXP

RTU1C-1 8:00
A 50MHz Bandwidth Multi-Mode PA Supply Modulator for GSM, EDGE and UMTS Application

P.G. Blanken*, R. Karadi**, H.J. Bergveld**, *Philips Research Laboratories, **NXP Semiconductors (Research), Netherlands

Abstract: This paper describes the design and measurement results of a supply modulator for a PA for GSM, EDGE and UMTS application. The modulator combines a high-bandwidth class-AB linear regulator with an efficient DC/DC converter in a master-slave configuration. The DC/DC converter is current-mode controlled and has been designed to operate at switching frequencies between 1MHz and 25MHz. A damped dual-inductor LCR filter was inserted in the output branch of the DC/DC converter for ripple suppression.

RTU1C-2 8:20
An Envelope Tracking Power Amplifier Using An Adaptive Biased Envelope Amplifier for WCDMA Handsets

K. Takahashi, S. Yamanouchi, T. Hirayama, and K. Kunihiro, NEC Corporation

Abstract: An envelope tracking power amplifier (ET-PA) using a self-oscillation pulse-width-modulation circuit with an adaptive bias technique is presented. Since this approach enables the envelope amplifier to change the output power without degrading the signal resolution, the developed ET-PA shows a low adjacent channel leakage power ratio (ACPR) of less than -38 dBc in a wide output power range from 10 to 27 dBm. The ET-PA shows 45.4% overall efficiency at peak output power of 28 dBm.

RTU1C-3 8:40

A 3x3mm^2 Embedded-Wafer-Level Packaged WCDMA GaAs HBT Power Amplifier Module with Integrated Si DC Power Management IC

Gary Hau, Shih Hsu, Yutaka Aoki*, Takeshi Wakabayashi*, Naoki Furuhata**, Yukinobu Mikado**, ANADIGICS, Inc.., Casio Computer Co., LTD., Japan.*, IBIDEN Co., Ltd., Japan. **

Abstract: A 3x3mm^2 WCDMA PA module integrated with GaAs PA and Si BiCMOS DC power management IC is presented. The PA collector voltage is adaptively optimized through the DC-DC converter in the Si IC for reducing PA current consumption under backoff operation. A novel embedded-wafer-level-package (EWLP) technology was developed to achieve the module miniaturization. At 16dBm and 24dBm Pout, the current consumptions of the PAM are reduced from 162mA and 370mA, to 65mA and 237mA, over conventional design.

RTU1C-4 9:00

Integration of a Cellular Handset Power Amplifier and A DC/DC Converter in a Silicon-On-Insulator (SOI) Technology

A. Tombak, R. J. Baeten, J. D. Jorgenson, D. C. Dening, RFMD Inc., Corporate R&D, 7628 Thorndike Rd., Greensboro, NC

Abstract: A DC/DC buck converter was integrated with a cellular handset power amplifier (PA) in a Silicon-On-Insulator (SOI) technology. The technology was designed to allow integration of high-performance reliable RF power devices with the front-end. The power devices uses an LDMOS-based MOS device, called Integrated Power MOS (IPMOS). A 3-stage power amplifier was designed for GSM850/900 and DCS/PCS bands. The PA achieved typical power added efficiencies (PAE) greater than 60%.

RTU1C-5 9:20

Supply Modulators for RF Polar Transmitters

J. N. Kitchen, C. Chu*, S. Kiaei*, B. Bakkaloglu*, Ubidyne, Inc., *Arizona State University

Abstract: This paper summarizes the advantages of PA linearization via polar modulation and illustrates the necessity for high-performance supply modulators in polar transmitters. Two potential modulator solutions are introduced; both having between 4MHz and 20MHz occupied RF bandwidth and more than 65dB SFDR. These modulators process envelope information for 1625kb/s 8PSK and CDMA IS95 applications in polar PA architectures.

Tuesday June 17, 2008
8:00
GWCC– Room A314
Session RTU1D: Advanced Frequency Generation Techniques

Chair: Domine Leenaerts, NXP
Co-Chair: Ting-Ping Liu, Winbond Electronics (Shanghai)

RTU1D-1 8:00
A Low Noise Programmable Clock Multiplier Based on A Pulse Injection-Locked Oscillator with a Highly-Digital Tuning Loop

B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, Massachusetts Institute of Technology

Abstract: This paper introduces a pulse injection-locked oscillator that provides low jitter clock multiplication of a clean input reference clock. A mostly-digital feedback circuit provides continuous tuning of the oscillator such that its natural frequency is locked to the injected frequency. The prototype uses a 50 MHz reference input to generate a 3.2 GHz output with integrated phase noise, reference spur, and estimated deterministic jitter of 270 fs rms, - 60 dBc, and 310 fs (pk-pk), respectively.

RTU1D-2 8:20
A 1.6-to-3.2/4.8 GHz Dual-Modulus Injection-Locked Frequency Multiplier in 0.18μm Digital CMOS

L. Zhang, D. Karasiewicz, B. Cifctioglu and H. Wu, Laboratory for Advanced Integrated Circuits and Systems, Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY

Abstract: We propose a variable-modulus injection-locked frequency multiplier for better harmonic suppression using low-Q on-chip inductors in digital CMOS. A prototype dual-modulus frequency doubler/tripler with 1.6GHz input implemented in 0.18μm CMOS is demonstrated. At 5% locking range, the doubler mode achieves fundamental suppression of 42dB with 2.2mW power consumption; while the tripler mode achieves 40dB suppression at the fundamental and 32dB at the second harmonic, consuming 3.7mW.

RTU1D-3 8:40

Sub-mW Multi-GHz CMOS Dual-Modulus Prescalers Based on Programmable Injection-Locked Frequency Dividers

X. P. Yu, J. Zhou*, X. L. Yan, W. M. Lim**, M. A. Do**, Zhejiang University, *Shanghai Jiao Tong University, **Nanyan Technological University, China and Singapore

Abstract: Dual-modulus prescalers based on programmable Injection-Locked Frequency Dividers are presented. With a multi-phase injection, variable division ratios are obtained by switching different # of input signals. Implemented in 0.18μm CMOS process, the dual-modulus prescaler achieves an operating range of 1.8-6GHz with 0.22mW measured power consumption from a 1V supply. Based on the same architecture, a 0.15mW 5GHz 2/3 dual-modulus prescaler and a 0.29mW 5.5GHz 8/9 prescaler is demonstrated.

RTU1D-4 9:00

A 50-to-62GHz Wide-Locking-Range CMOS Injection-Locked Frequency Divider With Transformer Feedback

Y.-H. Wong, W.-H. Lin, J.-H. Tsai, T.-W. Huang, Dept. of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan, 106, R.O.C.

Abstract: A 50-to-62GHz injection-locked frequency divider (ILFD) with transformer feedback technique is designed in 0.13-micron CMOS technology for wide locking range. The measurement results show that the free-running frequency is 55.3 GHz and the total locking range is 12GHz (>20%) at the input power level of 0dBm while consuming 10.8 mW from a 0.9V power supply. The phase noise of the divider is -124.93dBc/Hz at 1MHz offset from the carrier.

RTU1D-5 9:20

Fully Integrated Frequency and Phase Generation for a 6-18GHz Wideband Phased-Array Receiver in CMOS

F. Bohn, H. Wang, A. Natarajan, S. Jeon, A. Hajimiri, California Institute of Technology, Pasadena, CA

Abstract: Fully integrated frequency-phase generators for a 6-18GHz wide-band phased-array receiver element are presented that generate 5-7GHz and 9-12GHz first LO signals with less than -95dBc/Hz phase noise at 100kHz offset. Second LO signals with digitally controllable four-quadrant phase- and amplitude spread with better than 2.7° resolution are generated and allow removal of systematic reference clock skew as well as accurate selection of the received signal phase.

Tuesday June 17, 2008
8:00
GWCC– Room A313
Session RTU1E: On-chip Microwave Passive Components

Chair: Bob Stengel, Motorola Labs
Co-Chair: Louis Liu, Northrop Grumman

RTU1E-1 8:00
Broadband Variable Passive Delay Elements Based on an Inductance Multiplication Technique

E. Adabi, A. M. Niknejad, University of California at Berkeley

Abstract: A new technique for making broadband and variable passive delay elements is described. By introducing a variable inductance structure and using it along with available varactors, synthesized transmission lines could be implemented with variable delay while maintaining a constant Z over the line bandwidth. By exploiting the effect of mutual inductance, delay values can be tuned beyond $\sqrt{LC}$ a single unit cell and two unit cells cascaded were implemented in 90nm digital CMOS process.

RTU1E-2 8:20
Wideband Mixed Lumped-distributed-element 90° and 180° Power Splitters on Silicon Substrate for Millimeter-wave Applications

A. Chen(1,2), H.-B. Liang(3), Y. Baeyens(1), J. Lin(2), Y.-K. Chen(1). Y.-S. Lin(3), (1) Alcatel-Lucent/Bell Laboratories, Murray Hill, NJ, (2) University of Florida, Gainesville, FL, (3) National Chi Nan, Univeristy, Puli, Taiwan

Abstract: This paper presents two millimeter-wave lumped-distributed 90° and 180° power splitters fabricated in the back-end-of-the-line (BEOL) of a 0.18 μm SiGe BiCMOS technology. The 180° and 90° power splitters based on mixed lumped-distributed-element three-port Wilkinson power divider with phase shifters at the outputs are shown to achieve an amplitude balance of better than 0.05 dB and 0.21 dB, respectively, at 77 GHz.

RTU1E-3 8:40
A Compact 5GHz Q-enhanced Standing-Wave Resonator-based Filter in 0.13μm CMOS

Dan Shi, Michael P. Flynn, University of Michigan, Ann Arbor, MI

Abstract: A fully-integrated 5GHz bandpass filter with 0dB IL and 3dB bandwidth of 9.5% (1dB bandwidth of 6%) is reported. The filter employs novel on-chip capacitively-loaded, transmission-line standing-wave resonators and Q-enhancement circuits. A prototype 5GHz on-chip filter, implemented in 0.13μm CMOS, dissipates 2.88mW from a 1.2V supply, and occupies a die area of .03mm^2.

RTU1E-4 9:00
3D Group-Cross Symmetrical Inductor: A New Inductor Architecture improving Self-Resonance Frequency and Q Factor

F. Gianesello[1], D. Gloria[2], C. Raynaud[1,2], P. Touret[1,2] and B. Rauber[1], [1]STMicroelectronics, FTM, TPS Lab, 850 avenue Jean Monnet, 38926 Crolles, 2CEA Leti, avenue des martyrs, 38000 Grenoble

Abstract: During past years, High Resistivity SOI CMOS technology has emerged as a promising one for the integration of RF applications. In this trend, 3D symmetrical spiral inductor (3DSI) has been proposed on SOI to lower the amount of area consumed by inductor while offering comparable performance than equivalent bulk technology. This paper presents a novel 3D inductor architecture, 3D group-cross symmetrical spiral inductor, which has higher self-resonance frequency and quality factor than 3DSI.

RTU1E-5 9:20
A Derived Physically Expressive Circuit Model for Integrated Passives in RFIC

K. Yang*, H. Hu*, K. L. Wu*, and W. Y. Yin**, * Department of Electronic Engineering, The Chinese University of Hong Kong, Hong Kong, ** Center for Microwave and RF Technologies, Shanghai Jiao Tong University, Shanghai, China

Abstract: A systematic derived circuit model for integrated passives in RFICs is presented. This generic model represents clear physical meaning and can be easily plugged into the RFIC design flow. As demonstration examples, the physically meaningful circuit models of a section of coplanar waveguide (CPW) and a spiral inductor fabricated using 0.18μm CMOS process are derived. Excellent agreement of the Q performance and the frequency responses of the derived circuit can be observed from 0.45 GHz to 10 GHz.

Tuesday June 17, 2008
13:20
GWCC– Room A407
Session RTU3A: Complex Integration Challenges: Characterization and Modeling

Chair: Francis Rotella, Peregrine Semiconductor
Co-Chair: Yuhua Cheng, Peking University

RTU3A-1 13:20
(INVITED) ESD-RFIC Co-Design Methodology

*Xiaokang Guan, *Xin Wang, *Lin Lin, *Guang Chen, *Albert Wang, **Hainan Liu, **Yumei Zhou, ***Hongyi Chen and ****Lee Yang and Bin Zhao, *University of California, Riverside, **Institute of Microelectronics, CAS, **Tsinghua Univ, **** SMIC, China and Freescale Semiconductor

Abstract: RF ESD protection circuitry design emerges as a big challenge to RF IC design, where the main problem is associated with performance degradation of RF IC due to ESD-induced parasitics. It has been difficult to incorporate the ESD impacts into RF IC design due to lack of proper co-design approach and ESD device models. This paper presents a new ESD-RFIC co-design methodology, including RF ESD design optimization and characterization, as well as RF I/O re-matching techniques.

RTU3A-2 13:40
Electromagnetic and Thermal Co-Analysis for Distributed Co-design and Co-simulation of Chip, Package and Board

S.Wane* and A. Kuo**, *:NXP-Semiconductors, Campus EffiScience, Caen, 14000,France , **:Apache-Optimal Design Solutions, 2645 Zanker Road , San Jose (CA)

Abstract: This paper discusses Electromagnetic (EM) and Thermal Co-Analysis for chip, package and board co-design and co-simulation. The limitation of classical divide-and-conquer approaches based on cascading techniques are investigated in reference to global methodologies where Chip, Package and Board are simulated using one single model methodology. Cascade and single model methodologies are applied to a real-world NXP-Semiconductors System-in-Package carrier products,

RTU3A-3 14:00
Study of the Different Coupling Mechanisms Between a 4 GHz PPA and a 5-7 GHz LC-VCO

S. Bronckers[1,2], G. Vandersteen[1,2], L. De Locht[2], G. Van der Plas[1], Y. Rolain[2), (1)] IMEC, Belgium - [2)]ELEC, Vrije Universiteit Brussel, Belgium

Abstract: The coupling of the transmitted RF signal of the Power Amplifier (PA) into the sensitive Voltage Controlled Oscillator (VCO) of a transceiver can cause failure of the RFIC. It is not obvious for the designer to identify which coupling mechanism can be held responsible for the degradation of the VCO. Thus it remains an open problem to decide which appropriate counter-measure should be taken. Different experiments are carried out on a 0.13μm CMOS 4GHz PPA and a 5-7GHz LC-VCO to gain insight.

RTU3A-4 14:20
A Simple and Complete Circuit Model for the Coupling Between Symmetrical Spiral Inductors in Silicon RF-ICs

F. Vecchi*, M. Repossi**, A. Mazzanti***, P. Arcioni*, F. Svelto*, * Università degli Studi di Pavia, Italy, ** STMicroelectronics, Italy, *** Università di Modena e Reggio Emilia, Italy

Abstract: Modern RFICs have achieved an impressively integration level, making coupling effects among different sections of the circuit a potential limit to their functionality. This paper presents a physical equivalent circuit for the accurate wideband modeling of coupling between spiral inductors in CMOS technology. The model proves to be very accurate up to frequencies well above the inductor self-resonance. A simple approximate expression useful for the quick estimate of cross-talk is also introduced.

RTU3A-5 14:40
Isolation Enhancement in Integrated Circuits Using Dummy Metal Fill

Steven G. Gaskill, Vikas S. Shilimkar, Andreas Weisshaar, Oregon State University

Abstract: Metal fill patterning in modern IC processes is often viewed as parasitics to be minimized. Here, we use metal fills to improve isolation. The improved isolation comes at the cost of increased capacitive loading. This loading-isolation tradeoff is analyzed for various grounding strategies. It is found to be best to ground first inner metal-fill. The effect of finite ground impedance is also analyzed. A ground impedance path of less than 500Ω is shown to give sufficient grounding up to 10GHz.

Tuesday June 17, 2008
13:20
GWCC– Room A406
Session RTU3B: UWB LNA's

Chair: Danilo Manstretta, University of Pavia
Co-Chair: Kirk Ashby, Microtune, Inc.

RTU3B-1 13:20
A 90-nm CMOS Two-Stage Low-Noise Amplifier for 3-5-GHz Ultra-Wideband Radio

Giuseppina Sapone and Giuseppe Palmisano, Università di Catania, Facoltà di Ingegneria, DIEES, Catania, Italy

Abstract: An LNA for 3-5-GHz UWB applications is presented. The circuit was fabricated in a 90-nm CMOS process. It consists of a complementary PMOS / NMOS pair, which provides wideband input matching, while the second stage adopts a transformer-loaded cascode topology. The LNA achieves a power gain of 13.5 dB and a 3.1-to-5.9-GHz 3-dB gain bandwidth, while it features a noise figure of 2.8 dB. Measurements reveal excellent input matching in the 3.1-to-10.6 GHz band. The LNA draws 4.5mA at a 1.2-V supply.

RTU3B-2 13:40
A 1.0 V, 2.5 mW, Transformer Noise-Canceling UWB CMOS LNA

T. Kihara, T. Matsuoka, and K. Taniguchi, Graduate School of Engineering, Osaka University, Osaka, Japan

Abstract: A 1.0 V, 2.5mW, transformer noise-canceling UWB CMOS LNA is presented. A transformer, composed of an input inductor and shunt peaking inductor, partly cancels the noise from a common-gate MOSFET. The combination of the transformer with an output series inductor provides wideband input impedance matching. The LNA, implemented with 90-nm digital CMOS technology, occupies 0.10mm^2 and achieves S11<-10 dB, NF<3.4 dB, and S21>7.8 dB over 3.1-10.6 GHz.

RTU3B-3 14:00
A 90-nm CMOS LNA for MB-OFDM UWB in QFN Package

W .K. Wong, M. A. Arasu, W. K. Chan*, Institute of Microelectronics, *Wipro techno centre, Singapore

Abstract: In this work, the design of a single ended low-noise amplifier (LNA) dedicated for MB-OFDM Band Group-1 ultra-wide-band (UWB) band is described. It achieves a flat gain from 2 to 5GHz of 17dB while drawing a current of 15.9mA from a 1.2V supply. The circuit has been implemented in 90-nm CMOS technology and features a minimum noise figure (NF) of 2.5dB over the frequency range as well we an input referred third order intermodulation (IIP3) of -8dBm.

RTU3B-4 14:20
A 2.5-dB NF 3.1-10.6-GHz CMOS UWB LNA with Small Group-Delay-Variation

H. Y. Hang, Y. S. Ln, and C. C. Chen, Department of EE, National Chi Nan University, Taiwan

Abstract: A 3.1-10.6-GHz UWB LNA with excellent phase linearity property using standard 0.13μm CMOS technology is reported. To achieve high and flat gain and small group-delay-variation at the same time, the inductive peaking technique is adopted in the output stage for bandwidth enhancement. The UWB LNA dissipates 10.68 mW power and achieves S_{11} of -17.5- -33.6 dB, S_{22} of -14.4- -16.3 dB, and S21 of 7.92±0.23 dB over the 3.1-10.6 GHz band of interest. Excellent NF of 2.5 dB is achieved at 2.5 GHz.

RTU3B-5 14:40
A RF CMOS Amplifier with Optimized Gain, Noise, Linearity and Return Losses for UWB Applications

G. D. Nguyen, K. Cimino, M. Feng, University of Illinois at Urbana-Champaign

Abstract: Trade-off between noise figure (NF) and input return loss (S_{11}) imposes a fundamental limitation on the design of LNA for UWB applications. A graph-based approach using Smith chart to achieve optimum values for both NF and S_{11} over the desired bandwidth is presented. The proposed method and device optimization techniques are systematically incorporated to enhance the overall LNA performance in terms of gain, noise, linearity and power consumption.

Tuesday June 17, 2008
13:20
GWCC– Room A315-316
Session RTU3C: WLAN and Broadband Power Amplifiers

Chair: Freek van Straten, NXP
Co-Chair: David Ngo, RFMD

RTU3C-1 13:20
A 27dBm, SiGe-BiCMOS Transmitter With 62% PAE and Operation Class Control for Large-Bandwidth Polar Modulation

M.A.T. Sanduleanu, R.P. Aditham*, Philips Research Einhoven,
*NXP Semiconductors, The Netherlands

Abstract: This paper presents a SiGe BiCMOS transmitter for large bandwidth Polar Modulation and PWM signals. For flexibility, the transmitter presented in the paper has an externally controllable class of operation. Fabricated in a SiGe BiCMOS process (QUBIC4G), the measured saturated output power of the transmitter is 27dBm and the measured PAE is 62%. It features an IMD3 of -30dBc up to 25dBm peak envelope power and fulfills the spectral mask for WLAN 802.11.a signals.

RTU3C-2 13:40
A Fully Integrated 2x2 Power Amplifier for Dual Band MIMO 802.11n WLAN Application using SiGe HBT Technology

H.H.Liao, H.Jiang*, P.Shanjani, A.Behzad, Broadcom Corporation,
*San Francisco State University

Abstract: A fully monolithic 2x2 (2x a-band, 2x g-band) power amplifier based upon SiGe HBT process is developed for the dual band MIMO 802.11n WLAN system. In order to achieve desirable performances for the 5GHz band and high integration level, a special Through-Wafer-Via(TWV) process on Si wafer was developed and utilized. In this work, both a-band and g-band PAs show above 17dBm linear power output for -28dB EVM and more than 18dBm for -25dB EVM with 14% efficiency for a- and 19% efficiency for g-band.

RTU3C-3 14:00

A Decade Bandwidth, Low Voltage, Medium Power Class B Push-Pull Si/SiGe HBT Power Amplifier Employing Through Wafer Vias

T. S. Wooten, L. E. Larson, University of California at San Diego, Center for Wireless Communications

Abstract: We report a 0.5-5 GHz, 2V Class B push-pull power amplifier in a through-wafer via Si/SiGe HBT process. The amplifier utilized a small, low loss, broadband balun and a coupled spiral inductor transformer. Power added efficiencies greater than 40% from 1 GHz to 4 GHz and greater than 30% from 0.5 to 5 GHz have been achieved. Small signal gain of greater than 13dB and maximum output power of 22 dBm were realized from 0.5 GHz to 4 GHz with a 2 V supply voltage.

RTU3C-4 14:20

A X-Band CMOS Power Amplifier with On-Chip Transmission Line Transformers

B.-H. Ku, S.-H. Baek and S. Hong, School of Electrical Engineering and Computer Science, KAIST, Daejeon, 305-701, Korea

Abstract: A X-band CMOS power amplifier (PA) has been fabricated using a 0.18-um CMOS technology. On-chip transmission line transformers are used as matching elements for output, input, and inter-stage matching. The power amplifier provides the saturated output power of 23.5 dBm and 1-dB gain-compressed output power (P_{1dB}) is 21 dBm at 8.5 GHz with 3.3 V supply. The measured PAE is 19% at 8.5 GHz. Among the reported X/Ku band CMOS power amplifiers, this amplifier has the largest output power.

RTU3C-5 14:40

A Broadband Low Cost GaN-on-Silicon MMIC Amplifier

Bernard Geller, Allen Hanson, Apurva Chaudhari, Andrew Edwards and Isik C. Kizilyalli, Nitronex Corporation, Durham, NC, 27703

Abstract: The design and performance of a 0.1 to 5 GHz distributed medium power amplifier is described. The circuit is realized using a low-cost GaN-on-silicon MMIC technology featuring 0.5μm gate length GaN HFETs on a 150μm thick high resistivity silicon substrate. The circuit was designed using a non-linear FET model and standard passive component models. The first pass circuit demonstrated a saturated output power of 2W and a maximum efficiency of greater than 30% at 1 GHz.

Tuesday June 17, 2008
15:30
GWCC– Room A406
Session RTU4B: Voltage Controlled Oscillators

Chair: Jing-Hong Chen, Analog Device
Co-Chair: Stephen Dow, ON Semiconductor

RTU4B-1 15:30
A Temperature-Compensated Low-Noise Digitally-Controlled Crystal Oscillator for Multi-Standard Applications

Ming-Da Tsai, Chih-Wei Yeh, Yi-Hsien Cho, Ling-Wei Ke, Pei-Wei Chen, Guang-Kaai Dehng, MediaTek Inc. No. 1, Dusing Rd. 1, Hsinchu Science Park, Hsinchu, Taiwan 300, R.O.C.

Abstract: This paper presents an integrated 26-MHz DCXO with temperature compensation function for multi-standard cellular applications, that achieves a phase noise of -154 and -159 dBc/Hz at 10 kHz and 100 kHz offset, respectively. The frequency instability over temperature is compensated by built-in temperature sensor and compensating capacitor. The frequency instability from -10 to 55° C is about ±1 ppm.

RTU4B-2 15:50
A BiCMOS Voltage Controlled Oscillator and Frequency Doubler for K-Band Applications

Tino Copani, Bertan Bakkaloglu, Sayfe Kiaei, Connection One, Department of Electrical Engineering, Arizona State University

Abstract: A mm-wave voltage controlled oscillator and frequency doubler for 18GHz applications are presented. A 9.5-GHz voltage controlled oscillator is implemented by using a double LC-tank resonator to improve loaded Q at high frequencies. Inductive coupling is exploited to design a 18GHz frequency doubler which improves harmonic spur rejection and immunity to supply noise. The circuits are implemented in a 100-GHz ft SiGe BiCMOS process and achieve a FOM of -183dBc/Hz at 19GHz.

RTU4B-3 16:10

A Novel Compact Complementary Colpitts Differential CMOS VCO with Low Phase-Noise Performance

Chien-Cheng Wei, Yi-Tzu Yang, and Hsien-Chin Chiu, Department of Electronic Engineering, Chang Gung University, Taoyuan, Taiwan, Republic of China

Abstract: A low phase-noise Ka-band CMOS voltage controlled oscillator with compact size is proposed in this paper. The CMOS VCO core adopts a new complementary Colpitts structure in a 0.18μm CMOS technology to achieve the differential operation and better phase noise performance, as well as work at much higher frequency. The VCO operates from 29.8 to 30 GHz with 200MHz tuning range. The measured phase-noise at 1-MHz offset is -109 dBc/Hz at 30 GHz and 105.5 dBc/Hz at 29.8 GHz.

RTU4B-4 16:30

A Low-Voltage High-Frequency CMOS LC-VCO Using a Transformer Feedback

Chih-Hsiang Chang and Ching-Yuan Yang, Department of Electrical Engineering, National Chung Hsing University, 250, Kuo-Kuang Road, Taichung, Taiwan

Abstract: The paper describes a 0.18-μm CMOS 8.5-GHz LC-tank VCO using a technique of reducing parasitic capacitances. Compared to the traditional crossed coupled method with more parasitic capacitances, in this work a symmetry transformer introduced by a transformer on feedback currents from the active components is employed to reduce parasitic capacitances in the VCO. It can easily arrive at the requirement for high-frequency operation with the tuning range of 8.32 to 8.75 GHz (5%) at 0.7 V supply.

RTU4B-5 16:50

Current Reuse Cross-Coupling CMOS VCO Using the Center-tapped Transformer in LC Tank for Digitally Controlled Oscillator

Youngjae Lee,Seokbong Hyun,Cheonsoo Kim, RF/Analog SoC Design Team, ETRI, Korea

Abstract: A current reuse cross-coupling transformer-based VCO with low phase noise and low power consumption was implemented in 0.13μm CMOS. The oscillation frequency was tuned from 4.6GHz to 6GHz (26% tuning range) using two different-sized varactor that adjusted fine and coarse tuning. The measured phase noise at 5.0GHz was -124dBc/Hz (1MHz offset) and maximum output power level was -5.5dBm. The 0.4mmx0.3mm core consumes very low power of 1.8mW for 1.2V and FOM has -196.2dB.

Tuesday June 17, 2008
15:30
GWCC– Room A315-316
Session RTU4C: Advances in silicon RFIC Devices

Chair: Eli Reese, TriQuint
Co-Chair: Waleed Khalil, Intel

RTU4C-1 15:30
Effect of Technology Scaling on RF Performance of the Transistors Fabricated by Standard CMOS Technology

Han-Su Kim, Chulho Chung, Joohyun Jeong, Seung-Jae Jung, Jinsung Lim, JinHyoun Joe, Jaehoon Park, HyunWoo Lee, Gwangdoo Jo, Kangwook Park, Jedon Kim, Hansu Oh, and Jong Shik Yoon, Samsung Electronics, System LSI Division

Abstract: Cut-off frequency of 300 GHz is demonstrated for transistors with a gate length of 35 nm fabricated by 45 nm standard CMOS technology. Current gain and noise is improved with scaling down technology. Power gain increase saturates at 45 nm as technology advances. Such saturation in power gain is attributed to rapid increase in gds. Additional efforts are required to reduce gds for continuous improvement in power gain with the scaling. V_{th} optimization can be one of options to achieve better g_{ds}.

RTU4C-2 15:50
Process Dependence of 0.11μm RF CMOS on High Resistivity substrate for System on Chip (SOC) Application

T. Ohguro, K. Kojima, N. Momo, H. S. Momose, Y. Toyoshima, Toshiba Corporation, Semiconductor Company, Center for Semiconductor Research and Development, Japan

Abstract: The high resistivity Si substrate is attractive for analog/RF circuits. The high resistivity substrate, however has dependence of the resistivity on sinter process such as 400C, degrades leakage current between nweels, snap-back voltage in latch-up behavior and RF noise. In this paper, the optimum processes are discussed and new model for Si substrate resistivity dependence of RF noise is proposed.

RTU4C-3 16:10

Improved RF-Performance of Sub-Micron CMOS Transistors by Asymmetrically Fingered Device Layout

C. Weyers, D. Kehrer*, J. Kunze, P. Mayr, D. Siprak**, M. Tiebout**, J. Hausner** and U. Langmann, Ruhr-Universität Bochum, *Qimonda AG, **Infineon Technologies AG, Germany

Abstract: Novel MOS-transistor layouts for RF applications are presented. These improvements allow for increased device currents and reduced parasitic wiring capacitances simultaneously. Ring oscillators fabricated in a 65nm digital CMOS technology are used for verification. An increase of 14% in oscillation frequency compared to classical multi-finger layouts corroborates the improvement by the modifications.

RTU4C-4 16:30

Effects of Forward Body Biasing on the High Frequency Noise in Deep Submicron NMOSFETs

Hao Su, Hong Wang, Tao Xu, Rong Zeng, Microelectronic Centre, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore

Abstract: In this paper, the impact of forward body biasing on the high frequency noise in deep sub-micrometer NMOSFETs is presented. Experimental results show that high frequency noise increased with the body bias V_b, and has positive dependence on the substrate bias. Possible mechanism behind increase in RF noise of MOSFET under forward body bias is studied. Increase of NF_{min} and R_n with increase in V_b appears as great concern for application of forward body bias scheme in low noise circuit design.

RTU4C-5 16:50

On-chip Calibration of RF Detectors by DC Stimuli

R.Ramzan, J.Dabrowski, Linkoping Univetsity, Sweden

Abstract: In the nanometer regime,circuits exhibit wide parameter variability. On-chip Design for Testability (DfT) features also suffer from parameter variability. Therefore, RF calibration of all on-chip test structures is mandatory. In this paper, Artificial Neural Networks are employed as multivariate regression technique to architect a general RF calibration scheme using DC- instead of RF stimuli. This relaxes the routing requirements on a chip for GHz signals along with the reduction in test time.

Tuesday June 17, 2008
14:00
GWCC– Room A3
Session RTUIFR: Interactive Forum

Chair: Yann Deval, University of Bordeaux, IMS Lab
Co-Chair: Tina Quach, Freescale Inc.

RTUIF-01
An RFIC Within a Direct Open-Loop Polar Multimode Transmitter for UMTS/EDGE/GSM

S. Osman, W. Lee, E. McCune, S. Hirano*, M. Maeda*, K. Ishida*, Panasonic Emerging Advanced RF Laboratory (PEARL), ,*Network Development Center (NDC), Matsushita Electric Industrial , Co.,Ltd., Japan

Abstract: An RFIC within a direct polar multimode transmitter that supports UMTS, GSM, and EDGE is shown in 0.18μm CMOS. Design details, and chip-set system application are explained. The chip architecture applies phase accurate FLL two-point modulator with ΔΣ back control for AM-PM corrected wideband phase modulation to an LC VCO, and AM-AM corrected envelope drive of multi-stage saturated PA. IC measurement results and chip-set system performance are presented.

RTUIF-02
A GSM/EDGE Transmitter in 0.13-μm CMOS Using Offset Phase Locked Loop and Direct Conversion Architecture

S. F. Chen, Y. B. Lee, Bosen Tzeng, C. C. Tang, Charles Chiu, Rickey, Yu, Ovid Lin, L. W. Ke, C. P. Wu, C. W. Yeh, P. Y. Chen, G. K. Dehng, MediaTek Inc.

Abstract: A GSM/EDGE transmitter implemented in 0.13-μm CMOS using offset phase locked loop and direct conversion architecture is presented. The transmitter consists of a DCT, an OPLL with a TXVCO, a fractional-N synthesizer with a RFVCO and LDO regulators. Transmitter delivers 5dBm output power with 1% rms phase error and the modulation spectrum at 400kHz offset is better than -63dBc in GSM mode. In EDGE mode, it has 5dBm output power with 0.5dB gain step per bit.

RTUIF-03

A Low Spurious 400M-6GHz SiGe-MMIC Direct Conversion Transceiver using $2f_{LO}$ LO Switching Configuration for Cognitive Radio

K. Tsutsumi, F. Onoma, J. Koide, M. Uesugi, N. Suematsu, H. Harada*, Mitsubishi Electric Corp., *National Institute of Information and Communications Technology, Japan

Abstract: A low spurious SiGe-MMIC direct conversion transceiver using $2f_{LO}$ LO switching configuration for cognitive radio is described. By applying proposed LO configuration to the transceiver, Tx spurious is lowered compared to the conventional configuration. The direct conversion transceiver MMIC using $2f_{LO}$ LO switching configuration is fabricated in 0.18μm SiGe-BiCMOS process. Measured results show a high modulation accuracy over 400M-6GHz, and low Tx spurious characteristics.

RTUIF-04

A Direct Conversion 4.9GHz to 5.925GHz OFDM Receiver with Matched Non-Integer Quadrature LO

Nitin Madan, Amit Burstein, Joshua Park*, Kerry Phillips, Jeffrey Feigin, Skyworks Solutions Inc., *Sitrix Inc.

Abstract: A direct conversion 4.9GHz to 5.925GHz OFDM Receiver IC with Non-Integer Matched Quadrature LO that supports channel bandwidths from 1 MHz to 28 MHz is manufactured on Jazz μm BiCMOS process. This chip has a noise figure less than 6dB and Input Pf greater than -14 dBm at maximum gain. The I/Q gain mismatch is less than 0.15dB and phase error is less than 3degree without any calibration during manufacturing or feedback from baseband

RTUIF-05

A 12-mW 500-Mb/s 1.8μm CMOS Pulsed UWB Transceiver Suitable for Sub-meter Short-range Wireless Communication

Mamoru Sasaki, Hiroshima University, Hiroshima, Japan

Abstract: This paper describes a 500-Mb/s 12-mW pulsed UWB transceiver in 1.8-μm CMOS technology for sub-meter short-range wireless communication. The transceiver employs two functional blocks for reducing power dissipation: one is an on-chip transformer-basedF pulse power converter and another is an asynchronous RF-baseband direct demodulator. The prototype chip with printed dipole antenna can operate at a bit-error rate of 10-3 or less on 40-cm distance, while dissipating less than 24μW/Mb/s.

RTUIF-06

UWB Antenna Diplexer with Mode Conversion Using High Quality Passive and Active Technology

M. Gamal El Din*, Koen Mertens**, Bernd Geck* and H. Eul*,*Institute of Radiofrequency and Microwave Engineering Hanover, University, Appelstraße 9A, 30167 Hanover, Germany, **Infineon, Technologies Austria AG, Siemensstrasse 2, 9500 Villach, Austria.

Abstract: This paper presents an UWB antenna diplexer chip fabricated using high quality passive and active Si-Cu (P7MI) technology. This antenna diplexer has three functions, the main function is filtering for two band groups, the second function is matching between two impedance levels and the third function is differential to single ended mode conversion. This chip together with Multichip packaging module technique enables a dual band group WiMedia UWB radio on full silicon RFIC.Chip size 1.65x1.6mm^2

RTUIF-08

A 0.13μm CMOS 4-Channel UWB Timed Array Transmitter Chipset with sub-200ps Switches and All-Digital Timing Circuitry

Z. Safarian, T-S.Chu, H. Hashemi, University of Southern California

Abstract: A 4-channel ultra wideband timed array transmitter chipset is reported in 0.13μm CMOS technology that is suitable for radar and imaging applications. It consists of an all-digital timing control and impulse generation circuitry chip and a set of UWB forming switches. The proposed UWB timed array architecture eliminates the need for area and power hungry true time delay circuitry that would have been otherwise needed for beam-forming.

RTUIF-09
A Tunable Bandpass BAW-Filter Architecture Using Negative Capacitance Circuitry

C. Tilhac, S. Razafimandimby, A. Cathelin, S. Bila*, V. Madrangeas*, D. Belot, STMicroelectronics, Crolles, France, *XLIM Laboratory, University of Limoges, France

Abstract: This paper demonstrates the functionality of a WCDMA tunable BAW filter with negative capacitors which in term of silicon area becomes interesting contrary to previous papers with inductors. With this new architecture and good parameters for the negative capacitance we are able to respect the WCDMA specifications and to compensate BAW process variations that are ±1% on the filter center frequency. The circuit consists of a flip-chip assembly of a BAW SMR and STM BiCMOS 0.25μm chip.

RTUIF-10
A 71-76 GHz CMOS Variable Gain Amplifier Using Current Steering Technique

Che-Chung Kuo, Zuo-Min Tsai, Jeng-Han Tsai, Huei Wang, The Graduate Institute of Communication Engineering of National Taiwan University

Abstract: A 71-76 GHz high dynamic range CMOS RF variable gain amplifier (VGA) is presented. Variable gain is achieved using two current-steering trans-conductance stages, which provide high linearity with relatively low power consumption. The circuit is fabricated in a MS/RF 90-nm CMOS technology. This VGA achieves a 14-dB maximum gain, a 30-dB gain controlled range. To the author's knowledge, this VGA demonstrates the highest operation frequency among the reported CMOS VGAs.

RTUIF-11

Design and Analysis of a High-Performance Cascode Bipolar Low Noise Amplifier With Shunt Feedback Capacitor

Byoungjoong Kang, Sung-Gi Yang, Jinhyuck Yu, Wooseung Choo, Byeong-Ha Park, SAMSUNG ELECTRONICS Co., Ltd, Korea

Abstract: In this paper, a cascode bipolar low noise amplifier (LNA) employing shunt feedback capacitor is presented, for which the linearity and the noise figure (NF) can be optimized by reducing transistor size and degeneration inductance. We also show that the second-order interaction, which affects the third-order nonlinearity, becomes insensitive to low-frequency input termination as the DC current increases. Finally, the method of removing the low-frequency trap is presented.

RTUIF-12

A 2.2dB NF, 5-6GHz Direct Conversion Multi-Standard RF Receiver Front-End in 90nm CMOS

Brent R. Carlton, Jon S. Duster, Stewart S. Taylor, and Jing-Hong, Conan Zhan*, Communication Circuits Lab, Intel, Hillsboro, Oregon; *RF Division, MediaTek, HsinChu, Taiwan

Abstract: A multi-standard direct conversion receiver achieves 2.2dB NF @ 6GHz and 15kHz flicker noise corner with -30dBm in-band input p1dB. The 3dB RF bandwidth is 4.6-6.5GHz, power dissipation is 56mW from 1.3V and active die area is less than 1.2 mm^2 including the input matching network. Three gain steps of 6dB are provided with a maximum gain of 39dB and -18 dBm iIP3.

RTUIF-13

A 1.2-V Low LO-Power 3-5 GHz Broadband CMOS Folded-Switching Mixer for UWB Receiver

H.Y. Wang, K.F. Wei, J.S. Lin and H.R. Chuang, Institute of Computer and Communication Engineering, Department of Electrical Engineering, National Cheng Kung University, Tainan,Taiwan

Abstract: A 1.2-V broadband down-conversion mixer for ultra-wideband (UWB) system applications is presented. The mixer is fabricated in the 0.18μm 1P6M standard CMOS process. To achieve low dc power consumption for UWB applications, the LC folded-switching aph is utilized to reduce supply voltage as well as dc power consumption. A CMOS inverter with current-reuse technology is used in the transconductance stage. The transconductance stage and the switching stage are ac-coupled with capacitors.

RTUIF-14
Scalable Statistical Measurement and Estimation of a mm-Wave CML Static Divider Sensitivity in 65nm SOI CMOS

Daeik D. Kim, Choongyeun Cho, Jonghae Kim, IBM Semiconductor Research and Development Center, Hopewell Junction, NY

Abstract: A CML static divider operates up to 82.4GHz with 90% yield for 0dBm input is statistically measured and estimated. The proposed method of statistical measurement enables reliable sensitivity curve estimation by 55% of standard variation, based on the analytic model, simulations, and scalable DC and RF measurements for the first time. A 300mm full wafer is scanned for the validation.

RTUIF-15
An On-Chip Dipole Antenna for Millimeter-Wave Transmitters

P. H. Park, S. S. Wang, and T. Y. Chan*, Stanford University, Stanford, CA, *Chung Ching University, Taiwan, ROC

Abstract: This paper presents an on-chip dipole antenna that radiates power directly from the die at millimeter-wave frequencies. To improve the transmission efficiency, a rectangular silicon "lens" is attached on top of the chip. This increases the ant the upward direction by 8-13 dB, while suppressing backside radiation. A 28-GHz prototype CMOS transmitter has been demonstrated by integrating this antenna with a standing-wave oscillator.

RTUIF-16
A 24-GHz CMOS Butler Matrix MMIC for Multi-Beam Smart Antenna Systems

Ting-Yueh Chin, Sheng-Fuh Chang, Chia-Chan Chang and Jen-Chieh Wu, Department of Electrical Engineering, Department of Communications Engineering, Center for Telecommunication Research, National Chung Cheng University, Chia-Yi, 621, Tawain

Abstract: A 24-GHz CMOS Butler Matrix MMIC is presented, in which the multi-layer structure of CMOS process is utilized to realize the bulky Butler matrix in silicon. The implemented MMIC only occupies an area of 0.41 mm^2. The experimental results show that the insertion losses are 2.2±0.6 dB and the phase errors are within 6° from 23 to 25 GHz. By feeding the measured signals to an antenna array, four orthgonal beams are generated at -49, -15°, 15°, and 49°, respectively, within 0.3° direction error.

RTUIF-17
170-GHz Transceiver with On-Chip Antennas in SiGe Technology

E. Laskin, K.W. Tang, K.H.K Yau, P. Chevalier*, A. Chantre*, B. Sautreuil*, S.P. Voinigescu Edward S. Rogers Sr. Dept. of ECE, University of Toronto, Toronto, OM M5S 3G4, Canada, * STMicroelectronics, 850 rue Jean Monnet, F-38926, Crolles, France

Abstract: A single-chip transceiver with on-die TX and RX antennas, 165GHz oscillator and divider is reported in a SiGe HBT process with fT/fMAX of 275GHz/340GHz. This marks the highest frequency transceiver in silicon and the highest level of functional integration on a single die above 100GHz in any semiconductor technology. The gain peaks at -5dB at 170GHz and the transmit power is -5dBm when measured at the transceiver pads. Both degrade by 25dB when measured on the transceiver with on-die antennas.

RTUIF-18
60 GHz Transmitter Circuits in 65nm CMOS

Alberto Valdes-Garcia, Scott Reynolds, and Jean-Oliver Plouchart, IBM, T. J. Watson Research Center, Yorktown Heights, NY

Abstract: Fundamental building blocks for a 60GHz transmitter front- end in 65nm CMOS are presented. A single-stage, single-ended, power amplifier operates from a 1.2V supply; at 62GHz, peak power gain of 4.5dB, output 1dB CP of 6dBm, saturated power of 9dBm, and peak power added efficiency of 8.5% are measured. A double-balanced, Gilbert-based, up-conversion mixer employs a 1.5V supply; with LO of 50GHz and IF of 10GHz, 6.5dB of conversion loss and output 1dB compression point of -6.5dBm are measured.

RTUIF-19
A 40 GHz, Broadband, Highly Linear Amplifier, Employing T-coil Bandwidth Extension Technique

Hammad M. Cheema, Reza Mahmoudi, M.A.T. Sanduleanu*, Arthur van Roermund, Department of Electrical Engineering, Mixed-Signal Microelectronics Group, Eindhoven University of Technology, The Netherlands, *Philips Research Eindhoven, The Netherlands

Abstract: This paper presents a broadband,highly linear amplifier suitable for multi-standard mm-wave applications such as car radar,LMDS and satellite return channel.It can also be utilized as an efficient output buffer for measurements of mm-wave circuit components.It exhibits a 3-dB bandwidth of 40 GHz with a pass-band gain of 6 dB. The presented amplifier is highly linear with an IP3 of +18 dBm. It has been implemented in a bulk 90nm CMOS LP(low power) technology and consumes 3.3 mW from a 1.2V supply

RTUIF-20,
A 44.5 GHz Differentially Tuned VCO in 65nm Bulk CMOS with 8% Tuning Range

H.M. Cheema, R. Mahmoudi, A.H.M.van Roermund, M.A.T. Sanduleanu*, Department of Electrical Engineering, Eindhoven University of Technology, *Philips Research, Eindhoven, The Netherlands

Abstract: This paper presents a low power, low phase noise mm-wave voltage controlled oscillator. The VCO can be tuned from 41 to 44.5 GHz (8% tuning range) and utilizes a differential tuning mechanism based on varactors and fixed MIM capacitors. Fabricated in a bulk CMOS 65nm technology, it consumes 3.6 mW and exhibits a phase noise of -106 dBc/Hz at 1 MHz offset from a 41.2 GHz carrier. The resulting FOM is -192.7 dBc/Hz, which is the best reported value for VCOs operating above 40 GHz.

RTUIF-21
Colpitts VCOs For Low-phase Noise and Low-power Applications With Transformer-coupled Tank

E. van der Heijden, A. Farrugia**, R. Breunisse*, C.S. Vaucher, R. Pijper, NXP Semiconductors Research, Eindhoven, The Netherlands, *NXP Semiconductors, Nijmegen, The Netherlands, **Philips Research, Eindhoven, The Netherlands

Abstract: This paper presents two transformer-coupled tank VCOs, implemented in a 0.25μm SiGe:C BiCMOS technology. The VCOs have different impedance-levels of the LC-tank and the active circuit, showing a trade-off between low phase noise and low power. The VCOs include a 2.7 V supply regulator and the VCO cores dissipate 11 and 4.5 mA respectively. The measured tuning range for both VCOs is from 16.8 to 17.6 GHz and the phase noise is <-90 dBc/Hz@100 kHz from the carrier for the complete tuning range.

RTUIF-22
An 11.5% Frequency Tuning, -184 dBc/Hz Noise FOM 54 GHz VCO

S. Bozzola*, D. Guermandi**, A. Mazzanti***, F. Svelto*, *Università degli Studi di Pavia, **STMicroelectronics, ***Università di Modena e Reggio Emilia, Italy

Abstract: This work presents a robust, low area, spectral pure 65nm VCO for mm-wave applications. The varactor, an inversion mode MOS, takes advantage of the minimum feature provided by the technology to optimize capacitance tuning range and Q. The inductor is a 1 turn spiral. A combination of digital and analog tuning is chosen to lower VCO gain. Prototypes show the following measured results: 11.5% frequency tuning range around 54GHz. Noise FOM is -184 dBc/Hz. Power consumption is 7.2 mW.

RTUIF-23
Frequency Dividers with Enhanced Locking Range
Kun-Hung Tsai, Jia-Hao Wu, and Shen-Iuan Liu, Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taiwan, R. O. C.

Abstract: The locking range of the CML divide-by-two divider with the inductive shunt peaking is analyzed. The dividers using the locking-range-enhanced techniques have been realized in 0.13μm CMOS process. Experimental results show that the locking raoposed divider is improved 30.8% and 62.5% by adopting the current-reused and the gm-boosted technique, respectively. When both techniques are adopted, the locking range is 101.67% larger than the conventional on at the same power consumption.

RTUIF-24
A 3μW, 400 MHz Divide-by-5 Injection-Locked Frequency Divider with 56% Lock Range in 90nm CMOS
Julie R. Hu, Brian P. Otis, University of Washington

Abstract: An ultra-low power injection locked frequency divider (ILFD) is presented and demonstrated. Based on a 5-stage single ended ring oscillator, the ILFD achieves a lock range of 56% at a division ratio of 5 in the medical implant communications service (MICS) and the 433MHz ISM frequency bands. The ILFD is implemented in a 90nm CMOS process. It consumes 3μW of power from a 1.0V supply and 100μm^2 of area. The circuit achieves a frequency divider figure-of-merit of 134 GHz/mW.

RTUIF-25
A 5GHz CMOS PLL with Low K_{VCO} and Extended Fine-Tuning Range
Stephen P. Bruss and Richard R. Spencer, University of California Davis

Abstract: A 5GHz dual-path integer-N PLL uses an *LC* VCO and softly switched capacitors in the integral path to extend the fine-tuning range while keeping K_{VCO} low. The loop BW is 80kHz, the reference spur level is <-70dBc with a 1MHz reference frequency and total loop filter capacitance of only 37pF. The measured phase noise is -73dBc/Hz and -114dBc/Hz at 10kHz and 1MHz offsets, respectively. This 0.23mm^2 PLL is fabricated in a 90nm standard digital CMOS process and consumes 10mW from a 1.2V supply.

RTUIF-26

A 0.13μm CMOS 90 dB Variable Gain Pre-power Amplifier using Robust Linear-in-dB Attenuator, Y. Araki, T. Hashimoto, S. Otaka, Corporate R&D Center, Toshiba Corporation, Japan

Abstract: A 0.13um CMOS pre-power amplifier with 90dB gain range is fabricated. The pre-power amplifier consists of 4 variable attenuators and 3 fixed gain amplifiers, where the proposed attenuator suppresses the attenuation variation due to V_{th} variation. The pre-power amplifier outputs +4dBm with 75mW and -80dBm with 65mW. The ACPR is -48dBc and the EVM is less than 1.0% at Pout = +4dBm. The attenuation variation of less than $\pm$5dB is achieved.

RTUIF-27

A 600MHz CMOS OFDM LINC Transmitter with a 7 Bit Digital Phase Modulator

K. Kim, S. Byun*, K. Lim, C-H. Lee**, J. Laskar, Georgia Institute of Technology, Atlanta, GA, 30332, USA,, *ETRI, Daejeon, 305-350, South Korea,, **Samsung RFIC Design Center at Georgia Tech., Atlanta, GA

Abstract: This paper presents a new architecture for a LINC transmitter adopting a digital phase modulator (DPM). The DPM uses a 7 bit digital input to directly modulate the RF phase of each path, thus simplifying gain/phase mismatch compensation. Furthermore, this feature needs only one set of test signals for gain and phase mismatch detection. The implemented LINC transmitter IC consumes 140mA from a 1.9V supply and transmits a 6MHz bandwidth 64-QAM OFDM signal in the UHF TV band.

RTUIF-28

A Low Insertion Loss, High Linearity, T/R Switch in 65 nm Bulk CMOS for WLAN 802.11g Applications

Yiping Han,Keith Carter*,Lawrence E. Larson, Arya Behzad*, University of California at San Diego,*Broadcom

Abstract: A transmit-receiver (T/R) switch is fabricated in a 65 nm CMOS process for WLAN 802.11g applications. By floating the triple well device, the switch achieves low insertion loss, high power handling capability and good linearity simultaneously. In the transmit mode, the switch features 0.8 dB insertion loss, 29 dBm output P1dB and less than 0.2dB EVM degradation at 24 dBm output power level. In the re-ceive mode, it exhibits 1.6 dB insertion loss and 28dB isolation at 2.45GHz.

RTUIF-29

A New Highly-Scalable Equivalent Circuit Model For On-chip Symmetrical Transformer With Accurate Substrate Modeling

Chuan Wang, Huailin Liao, Chen Li, Xiong Yongzhong*, Ru Huang, Institute of Microelectronics, Peking University, Beijing 100871, China, *Institute of Microelectronics, Singapore

Abstract: A new equivalent circuit for on-chip symmetrical transformers is presented with all the model elements driven from fabrication specifications.Two coupled transformer loops are developed for each coil to calculate the parameters of skin effect,proximity effect and reflective effect of substrate eddy current respectively. Model accuracy is demonstrated by comparing simulated and measured S-parameters,coils inductance,coupling coefficient,and maximum available gain over a wide geometry configuration

RTUIF-30

Nonlinear Behavioral Modelling of Oscillators in VHDL-AMS using Artificial Neural Networks

M. Kraemer, D. Dragomirescu, R. Plana, LAAS-CNRS, University of Toulouse, 7 Avenue de Colonel Roche, 31077 Toulouse cedex 4, France

Abstract: An approach to behavioral modeling of microwave oscillators is described. The presented model takes into account start-up, steady state behavior and phase noise. To describe the nonlinearities, an Artificial Neural Network (ANN) is employed. The dynamic behavior of the oscillator is described in VHDL-AMS. As opposed to input-output models of microwave devices, this paper presents a self sustaining oscillation, which starts from a small injected excitation (noise) and ends in a stable limit cycle.

PANEL SESSIONS

Monday, June 16, 2008
12:00 - 13:15 • Room A412

MILLIMETER-WAVE IC: IS SILICON WINNING? IS GAAS STILL ALIVE?

Organizers: **Chinchun Meng,** National Chiao Tung University

Moderator: **Huei Wang,** National Taiwan University

Panel: **Young-Kai Chen,** Bell Labs Alcatel-Lucent
Bryan Floyd, IBM
Ali Hajimiri, California Institute of Technology
Joy Laskar, Georgia Institute of Technology
Chinchun Meng, National Chiao Tung University
Sorin Voinigescu, University of Toronto
Herbert Zirath, Chalmers University of Technology

Sponsor: **RFIC**

Abstract: Fully integrated 60 GHz MMICs were successfully built by PHEMT/ MHEMT technologies while advanced CMOS and SiGe HBT technologies have also shown good promise on 60 GHz MMICs. GaAs technology was not fairly invested at the beginning of RFIC revolution even though it is known to have better intrinsic properties. Thus, the panel will examine which technology will be the winner at the millimeter-wave regime and whether GaAs can come back at the microwave regime.

Tuesday, June 17, 2008
12:00 - 13:15 • Room A305

COGNITIVE RADIO FOR OPEN ACCESS AND WHITE SPACE

Organizer: **Kyutae Lim**, Georgia Institute of Technology

Panel: **Dr. Fred Martin**, Motorola Inc.
Dr. Kursat Kimyacioglu, Philips USA
Dr. Stewart S. Taylor, Intel
Dr. Kihong Kim, Samsung Electro-Mechanics
Dr. Mathew Sherman, General Vice Chair of IEE Standard Association, BAE Systems

Sponsors: **IMS** and **RFIC**

Abstract: The UHF band, which is recognized as the best spectrum for mobile communication has been used for broadcasting service over 50 years. From early 2009, Analog TV services will be completely replaced by Digital TV service in many of country including North America, Europe, Asia and Australia. In USA, the FCC is aggressively moving forward to maximize the usage of last greatest spectrum for wireless communication.

As a first step, FCC is auctioning 100 MHz band in 700MHz which is being emptied after DTV spectrum transition. Especially one chunk of spectrum is designated as "Open Access," which means that user can access this frequency by any device and software, which has not been allowed since most of the carriers controlled the device and accessibility of the frequency band. After the spectrum auction, FCC is making another important decision of granting for secondary user to access locally unused the DTV spectrum, so called "White Space." Together with "Open Access" and "White Space," consumers will enjoy uncharted wireless communication services, which has improved connectivity, data throughout with fraction of cost. This panel session will explore the scenario of new wireless communication services in the future and discuss the technical challenges to enable such communication services. Panelist includes expertise of network architecture, MAC PHY layer, Policy and RF/Analog.

Wednesday, June 18, 2008
12:00 - 13:15 • Room A305

WIRELESS MEDICAL TECHNOLOGY

Organizer/ Moderator: **Mark J. Phelps, Ph.D.**

Panel:
Mark Allen, Ph.D., Senior Vice Provost, Georgia Tech & CTO, CardioMems
Leonardo Estevez, Ph.D., Technology Strategy, Wireless Terminal Business Unit, Texas Instruments
Shelley Hartman, MBA, CEO, LifeSync Corporation
William Pierce, CEO, Foresight Medical Technology
Marshall Stanton, MD, VP Remote Disease Management, Medtronic
Max Stachura, MD, Georgia Research Alliance, Telemedicine
Robert Schmidt, CEO, Cleveland Medical Devices

Sponsor: **IMS**

Wednesday, June 18, 2008
12:00 - 13:15 • Room A302

THE RISE OF SYSTEM AND SERVICE ENGINEERING

Chairs/ Moderators:
Professor Barry Spielman, Washington University
Professor Michael Steer, North Carolina State
Professor Rolf Jansen, Aachen University

Panel:
Dr. Gerald M. Borsuk, Assoc. Director of Research for Systems, Naval Research Laboratory
Professor Robert Jackson, University of Massachusetts Amherst
Professor Linda Katehi, Provost, University of Illinois Urbana Champaign
Dr. Charles F. Krumm, Cosemi Technologies, Inc., Chief Operation Offi cer
Dr, Rick Martin, Director, Advanced Global Strike Systems, Boeing – St. Louis, MO
Dr. David M. McQuiddy, Texas Instruments, Raytheon, TriQuint
Professor Christopher Snowden, University of Surrey

Sponsor: **MTT-6 Microwave and Millimeter-Wave Integrated Circuits**

Thursday, June 19, 2008
12:00 - 13:15 • Room A305

AUTOMOTIVE RADAR: AN OPPORTUNITY AND A CHALLENGE FOR RF AND MICROWAVE ENGINEERS (IMS PANEL)

Chairs/ Moderator: **Ashok Bindra,** Penton Media

Panel: **John Irza,** The MathWorks
Jean-Pierre Lanteri, Tyco M/A-COM
Dr. Johann-Friedrich Luy, Daimler
Dr. Colin Warwick, Agilent Technologies

Sponsors: **MTT-9** and **MTT-16**

WORKSHOPS AND SHORT COURSES

Workshops and Tutorials are offered on Sunday, Monday and Friday of Microwave Week. They are distinguished by the following features:

- Advanced Level Workshops (designated as WSA, WSB, etc.) present the state of the art to specialists who are already experienced in the topic area.
- Tutorial Level Workshops (designated as TSB, RSC, etc.) are targeted towards educating attendees in new areas of microwave technology, reviewing material that is primarily a revision of previously published information.

All Workshops and Tutorials will be held at the Georgia World Congress Center. Specific room assignments will be announced at check-in.

RFIC SPONSORED SUNDAY WORKSHOPS AND SHORT COURSES

WSA – 08:00-17:00
High Data Rate 60GHz Radio Link Applications & Design

Topics & Speakers:

1- Millimeter Wave Terrestrial Gigabit Class Radio Technology, Lockie Douglas, Gigabeam
2- Design and Layout of Single-Chip 77-96GHz Receivers and Transceivers, Sean Nicolson PhD, University of Toronto
3- A Transceiver for 60GHz High Data Rate Wireless Transmission, Prof. Joy Laskar, Georgia Tech
4- A CMOS mmW approach for 60GHz Transceiver - Francesco Svelto, Pavia
5- 60 GHz RF Transceiver Circuits and System Integration Based on Commercial pHEMT and mHEMT Technologies, Prof. Herbert Zirath, Chalmers University
6- SiGe Power Amplifiers for 60 GHz Communication Systems, Prof. Georg Boeck, Berlin University of Technology
7- Broadband Millimeter Wave Communication, System Design Concepts and Trials, Wilhelm Keusgen PhD, Heinrich-Hertz-Institut Berlin
8- Adaptive Digital Predistortion of Nonlinear Power Amplifiers Using Signal Dependent Reduced Order Memory Correction, Neil Braithwaite PhD, Powerwave technologies

Organizers: **Mr. Didier Belot,** ST Microelectronics
Prof. Jean-Baptiste Begueret, University of Bordeaux
Prof. Georg Boeck, TU, Berlin
Prof. Eric Kerherve, University of Bordeaux

Sponsors: **RFIC**

Workshop Abstract: The presentations in this workshop will cover different aspects of 60GHz radio links. The morning session will open with a discussion of the applications of 60GHz radios followed by an overview of the main challenges of mmW integration. Then, several speakers will present example solutions in both CMOS and SiGe technologies.

WSB – 08:00-17:00
Advances in Circuit Design for Wideband Millimeter Wave Applications

Topics & Speakers:

1- Millimetre Wave Systems: Existing and Up-coming Applications, Dr. Dietmar Köther, IMST, RF Test Center

2- System Level Aspects, Baseband Architectures, Modulation and Standardization of 60 GHz Wireless Communication, Dr. André Bourdoux, IMEC

3- Millimeter Wave Design in Bulk-CMOS and CMOS-SOI, Dr. Andreia Cathelin, STMicroelectronics, FTM/Central CAD & Design Solutions

4- S-Parameters Measurements and Small Signal Modeling of sub 65nm Silicon MOSFETs up to 220 GHz, Nicolas Waldhoff, IEMN

5- Circuit Design Challenges for High-Power mmWave and THz Applications, Prof. Ullrich Pfeiffer, University of Siegen, Institute of High-Frequency and Quantum Electronics

6- 80-160 GHz CMOS and SiGe BiCMOS Building Block Design, Prof. Sorin Voinigescu, University of Toronto

7- Nonlinear Millimeter-Wave Modelling of Electron Devices in the Presence of Low-Frequency Dispersive Effects, Dr. Antonio Raffo, University of Ferrara

8- Highly Integrated MMICs Based on III-V Technologies for Millimeterwave/THz Applications, Prof. Herbert Zirath, Chalmers University of Technology, Department of Microtechnology and Nanoscience

Organizers: **Prof. Dominique Schreurs, K.U.Leuven,** Div. ESAT-TELEMIC
Prof. Patrick Reynaert, K.U.Leuven, Div. ESAT-MICAS

Sponsors: **MTT-1, MTT-6, MTT-20, MTT-23, RFIC**

Workshop Abstract: Wireless and mobile telecommunication applications in the lower microwave frequency range have become commonplace. To be able to offer higher data rates to the demanding market, research is gradually focusing towards millimeter wave frequencies. The advantage of millimeter waves is that they are capable of providing wide (in the absolute sense) bandwidth for very high-speed wireless access. Next, millimeter wave networks are becoming viable due to cost reduction in semiconductor devices. This workshop aims at informing the attendees about the recent developments in this area. The workshop includes overview talks on emerging wideband millimeter wave applications. Recent advances in circuit design using various device technologies will be covered in great detail. As these progresses are intrinsically connected with developments in modelling and measurement techniques, those aspects are addressed as well. Ample time will be foreseen to allow interactions between attendees and speakers.

WSD – 08:00-17:00
RF SoC Interaction With Peripherals and the Demand for Attention to Coupling Effects in Early Design Phases

Topics & Speakers:

1- Cross coupling in Baseband-Radio SoCs, Dr. Dietolf Seippel, Infineon Technologies
2- Parasitic-aware Design Methodology for Wireless SoC, Dr. Robert A. Mullen, Cadence
3- Post-Silicon and Pre-Silicon Techniques for Mitigating the Effects of Interference in Wireless SoCs, Oren Eliezer, Texas Instruments
4- Advanced EM simulation technology for RF SoC modeling, Dr. Jan Vanhese, Agilent
5- Noise Coupling in RF and mixed-signal Circuits: Modeling and Experimental Validation, Dr. Geert van der Plas, IMEC
6- Electrical Signal Integrity Analysis in Mixed-Signal and RF ICs, Dr. Francois Clement, S.A. CWS
7- RF SoC coupling effects and interaction with peripherals: needs to be dealt with in the early design phases!, Dr. Jan Niehof, NXP Semiconductors
8- Isolation Issues in Multi Chip Radio Modules for Cellular Applications: On Chip, Module-Chip and in Module, Jyoti Mondal, Freescale Semiconductor

Organizers: **Dr. Jan Niehof,** NXP Semiconductors
Oren Eytan Eliezer, Texas Instruments
Sponsors: **RFIC**

Workshop Abstract: This workshop will focus on the key requirements to address physical design issues in the early design phases of complex RF SoC design. The workshop will be divided into two sessions. The morning session will focus on the required specifications related to the SoC physical design, including tool and flow requirements. Recognized companies and partnerships active in the semiconductor industry will give these presentations and explain their needs through actual examples. In the afternoon session, EDA vendors will give presentations to react on the customer requirements. They will present the future direction and CAD/EDA roadmaps to address these issues.

WSE – 08:00-12:00
Advanced PLL Architectures for Embedded SoC Applications

Topics & Speakers:

1- Digital Clock and Data Recovery for Software-Programmable Links, Jafar Savoj, Rambus Inc
2- Why Moore's law and scaling work for mm-wave CMOS Synthesizers:, Dr. Sorin Voinigescu, University of Toronto
3- Understanding Digital Quantization in Delta-Sigma and Related Fractional-N PLLs, Dr. Sudhakar Pamarti, UCLA
4- Digital Implementation Techniques for Fractional-N Frequency Synthesizers, Dr. Michael Perott, MIT
5- All-digital PLL Architectures for Fully-integrated Receiver SoCs, Dr. Francesco Svelto, University of Pavia

Organizers: **Dr. Bertan Bakkaloglu,** Arizona State University
Prof. Sayfe Kiaei, Arizona State University
Sponsors: **RFIC**

Workshop Abstract: The ongoing migration of RF systems towards single-chip mixed-signal receiver/transceiver SoCs pushed towards a more digital-friendly implementation of the RF frequency synthesizers. The speed of modern CMOS technologies and advances in digital signal processing have enabled the evolution of PLL clock synthesis and clock and data recovery (CDR) circuits from analog to digital architectures. Digital solutions benefit from reduction of area and power consumption with device scaling, and facilitate porting of circuits across process nodes. Such designs achieve much lower power consumption, higher levels of integration, and improved immunity to supply and substrate noise compared to their analog counterparts. This workshop discusses state of the art approaches to digital intensive PLLs for SoC applications.

WSG – 13:00-17:00
Analog-Digital Co-Design Techniques for Nanometer CMOS Transceiver SoC Integration

Topics & Speakers:

1 - Correcting Nanometer CMOS RF Circuit Impairments – Prof. Bram Nauta (University of Twente)
2 - Circuit Design Techniques for Ultra-low Voltage RF Receiver - Prof. Peter Kinget (Columbia University)
3 - Analog-assisted digital and digitally-enhanced analog techniques for mixed signal SoC transceivers - Prof. John Long (University of Delft)
4 - Digital signal processing techniques for linearity and efficiency enhancement of Envelope Tracking, EER, and Doherty amplifiers. - Prof. Larry Larson (UC San Diego)
5 - Designing CMOS wireless system-on-a-chip for WLAN - Dr. David Su (Atheros)
6 - Advantages of SoC for cellular RF transceiver design - Dr. Andre Hanke (Infineon)

Organizers: **Dr. Bogdan Staszewski,** Texas Instruments
Prof. Yann Deval, IMS, University of Bordeaux
Dr. Adrian Maxim, Siicon Laboratories

Sponsors: **RFIC**

Workshop Abstract: The nanometer CMOS processes bring devices with high fT, enabling the SoC integration of multi-GHz RF communication systems. This gave a tremendous cost, area and power saving when compared with traditional bipolar or BiCMOS solutions. However, the higher noise, larger mismatches and wider process variations of nanometer FETs require extensive digital calibration to compete with traditional analog solutions. This workshop addresses advanced analog-digital co-design techniques which trade the higher speed and larger digital gate density of nanometer CMOS processes for relaxed analog front-end specifications. First, the ways to correct the nanometer CMOS device impairments and the very low-voltage circuit design challenges are presented. Then, new mixed-signal and all-digital approaches to implement traditional analog functions are investigated. Final presentations show how the analog-digital co-design techniques are applied to the major wireless applications: cellular, WLAN and broadcast.

WSI – 08:00-12:00
Adaptive Low-Power Front-Ends for Wireless Communication Systems

Topics & Speakers:

1- Low-power Reconfigurable Transmitter Architectures, Prof. Lawrence Larson, UC San Diego
2- CMOS power amplifiers for mobile terminals, Prof. Patrick Reynaert, KU Leuven
3- Leveraging VCO-based Quantization to Achieve Low Power, Wideband A/D Conversion for Multi-Standard RF Front-ends, Prof. Mike Perrott, MIT
4- Low-power Receivers Concepts: An Industrial Example, Dr. Robert B. Staszewski, Texas Instruments
5- Integrated Power Management Circuits for Wireless Applications, Prof. Hoi Lee, University of Texas

Organizers: **Dr. Gernot Hueber,** DICE GmbH
Dr. Robert Bogdan Staszewski, Texas Instruments
Prof. Stefan Heinen, Infineon Technologies

Sponsors: **RFIC**

Workshop Abstract: Current and future mobile terminals are becoming increasingly complex because they have to deal with a variety of frequency bands and communication standards. Achieving multi-band/multi-mode functionality poses a unique challenge on the RF-transceiver design due to limitations in terms of frequency agile RF components that meet the demanding cellular performance criteria, at costs that are attractive for mass market applications. The focus of this workshop will be on novel transceiver concepts for low power multimode/multi-band cellular systems from the antenna to baseband. Approaches include novel architectures, highly-configurable analog circuitry, digitally-assisted analog modules and the integration of digital signal processing into the traditionally purely analog front-end. However, the utilization of digital signal processing capabilities is in line with the ongoing trend towards SoCs in minimum-featuresized CMOS.

WSJ – 13:00-17:00
Advancements in Power Amplifiers and Transmitters for Mobile Wireless Products

Topics & Speakers:

1- Market Trends and Key Design Challenges for Mobile Cellular & WiMax Transmitters, Dr. Ken Weller, Skyworks Solutions
2- Overview, Transmitter Linearization and Efficiency Enhancement Techniques, Gord Rabjohn, SiGe Semiconductor
3- Application of Adaptive Digital Predistortion for EDGE, W CDMA, and LTE Mobile Transmitters, Dr. George Norris, Freescale Semiconductor
4- Advancements in Power Amplifiers for Polar Modulation Architectures, Wayne Kennan, RFMD
5- Power Amplifier Architectures for 3G Handsets: Balanced vs. Single-ended Structure, Dr. Gary Zhang, Skyworks Solutions
6-Switched Doherty PAs for 3G, Thomas Apel, Triquint Semiconductor
7- Improvements in Power Amplifier Performance via Adaptive Antenna Matching Techniques, Andre Van Bezooijen, NXP Semiconductor

Organizers: **Joseph Staudinger,** Freescale Semiconductor
Dr. Natalino Camilleri, Alien Technology
Sponsors: **RFIC, IMS**

Workshop Abstract: Advancements in wireless transmitters continue to focus on improving efficiency while maintaining acceptable levels of linearity. Emerging high speed data centric services result in RF signals which are particularly challenging to amplify in a handset environment. The large dynamic range and high instantaneous bandwidths are difficult to linearly amplify, especially in very low cost small footprint packaging. Additionally, multi-mode and multi-band operation further extends the operational performance space of the underlying power amplifier. Current efforts focus on both the overall transmitter architecture as well as the underlying power amplifier circuit. Several presentations focus on the application of adaptive digital pre-distortion linearization techniques supporting 2.5G, 3G, and LTE signal formats. Subsequent presentations examine innovative circuit techniques employed to improve the underlying amplifier.

WSK – 08:00-12:00
Advances in High Power Devices and PA Architectures for Wireless Infrastructure

Topics & Speakers:

1- Trends in High Power and Efficiency Amplifiers for Infrastructure,Dr. John Wood, Freescale Semiconductors Inc., Phoenix AZ, USA
2- Recent Advances in LDMOS Technology, Dr. Wayne Burger, Freescale Semiconductors Inc., Phoenix AZ, USA
3- Improvement of GaN HEMT for High Efficiency PA Technique, Dr. Toshi Kikkawa, Fujitsu Laboratories Ltd, Japan
4- Applying GaN HEMT Amplifiers to High Efficiency Techniques, Dr. David Runton, RF Micro Devices, Phoenix AZ, USA
5- Recent Advances on Doherty Amplifiers, Dr. J. Gajadharsing, NXP Semiconductors Inc., Nijmegen, The Netherlands
6- Digital Envelope Tracking and Load Modulation Technique for Efficiency and Linearity, Dr. Yuanxun Ethan Wang, UCLA, Electrical Engineering Department, LA, USA

Organizers: **Dr. Edmar Camargo,** RF Micro Devices Scotts Valley, CA, USA
Dr. Carlo Poledrelli, NXP Semiconductors, Nijmegen, The Netherlands

Sponsors: **MTT-5, MTT-7, MTT-20, RFIC**

Workshop Abstract: The market requirements on PA technology, has been increasingly demanding in terms of power, efficiency and linearity. This workshop will address these issues on the status of device technology, including LDMOS and GaN in the first part. In the second their application on PA, targeting high efficiency or high linearity will be discussed. The amplifier techniques such as Envelope Tracking and Switched Mode will be covered and a special emphasis will be dedicated to the Doherty configuration combined with Digital Pre-distortion. The workshop subjects will be covered by academic and international industry specialists detailing their developments and solutions.

WSL – 08:00-17:00
On-Chip Calibration, Compensation, and Filtering Techniques for Wireless SoC

Topics & Speakers:

1- IIP2 and DC offset calibration techniques in 3G transceivers, Dr. Krzysztof Dufrene, DICE Danube Integrated Circuit Engineering GmbH
2- Accurate tuning and calibration of Fractional-N frequency synthesizers, Waleed Khalil, Robert Santucci, and Dmitry Petrov, Intel Corp.
3- Calibration Techniques for Wireless SoCs, Arya Behzad, Broadcom Corp.
4- Digital Hardware and Software Based Mechanisms for Calibration and Compensation in Wireless SoCs, Oren Eliezer, Texas Instruments
5- Compensation of radio impairments for low cost wireless transceiver design, Steve Cicarrelli, Qualcomm
6- Calibration, Compensation, and On-chip Filtering techniques used in 3G transceivers, Jonathan Strange, Mediatek Wireless, UK
7- Digital Calibration Techniques for Cellular Receivers, Abdellatif Bellaouar, Sherif Embabi, and Hamid Safiri, Sirific Wireless
8- Digital Calibration Techniques for Cellular Transmitters, Abdellatif Bellaouar, Sherif Embabi, and Hamid Safiri, Sirific Wireless

Organizers: **Dr. Walid Ali-Ahmad,** MediaTek, Singapore
Sponsors: **RFIC**

Workshop Abstract: As wireless SoCs are being targeted for multi-standard and multi-band applications, the demand is still for excellent radio performance and minimum number of off-chip components. In addition, higher quality modulation techniques are being used in these systems to deliver higher data rates in a cellular environment. Hence, there is more weight being put on developing RF front-ends which are as good as ideal! Furthermore, there is currently a big emphasis on eliminating the undesirable large number of external RF SAW filters in multi-band operation. In order to achieve all these new requirements, on-chip correction techniques are needed that complement the on-chip radio circuitry and benefit from state-of-the-art CMOS processes currently available for wireless SoCs. This workshop will review on-chip calibration techniques for RF and BB impairments compensation, plus on-chip filtering circuitry to relax front-end linearity requirements and minimize the need for off-chip filters.

WSM – 08:00-12:00
Advanced CMOS Based Systems for Biomedical Applications

Topics & Speakers:

1- Ultra Low Power Wireless for Body Sensor Networks, Mr. Alan Wong, Toumaz Technologies
2- Clinical Prosthetic Devices for Glaucoma, Epilepsy, and Traumatic Brain Injury Repair, Dr. Pedro Irazoqui, Purdue University
3- Mixed-signal data mining on microphone array hearing aids, Dr. Shantanu Chakrabartty, Michigan State University
4- CMOS ICs for Biomedical Spectroscopy, Dr. Arjang Hassibi, University of Texas at Austin
5- Wireless Power and Data Telemetry for Bioelectronics Systems, Dr. Wentai Liu, UC Santa Cruz

Organizers: **Dr. Sudipto Chakraborty,** Texas Instruments
Dr. Shekar Rao, Texas Instruments
Sponsors: **RFIC**

Workshop Abstract: CMOS integration has impacted numerous diverse disciplines in the recent years. Biomedical technology is a rapidly emerging area and low power, miniaturized solutions have attracted great deal of interest. Such systems are usually perceived by integration of diverse building blocks such as sensors, power management, telemetry and analog processing, to name a few. In this workshop, we will explore the applications of Silicon based technologies in various areas of biomedical technology developments.

WSN – 13:00-17:00
Low-Voltage RF Design in 45nm and Beyond

Topics & Speakers:

1- Radio-Frequency Receiver Design in 45nm Digital CMOS Technology, Dr. Christopher D. Hull, Intel Corp.
2- Transmitters in 45nm and Beyond : Whither Linear, Dr. Earl McCune, Panasonic
3- Challenges in Low Voltage Frequency Synthesizer Design, Prof. Sudhakar Pamarti, UCLA
4- A/D Converter Design in 45nm and Beyond, Prof. Boris Murmann, Stanford University

Organizers: **Dr. Stewart S. Taylor,** Intel Corp.
Dr. Jacques C. Rudell, Intel Corp.
Sponsors: **RFIC**

Workshop Abstract: Architecture and circuit refinements/evolution have postponed the pain of low-voltage design. With most 45nm processes using a 1V supply, radical new thinking is required to realize high performance front-end transceivers in current and future silicon CMOS technologies. Although the intrinsic speed of the device (ft) has now reached well into the 100GHz region, new challenges with respect to low gain (gm*Ro), higher 1/f noise, extreme mismatch conditions, and low supply voltages will require a new design paradigm. This half day workshop will focus on some of the key challenges associated with realizing robust circuits in 45nm processes and beyond. The first speaker will focus on receiver architectures and circuits for nanometer technologies while the second speaker will give a similar presentation on transmitter design. The third presentation will focus on synthesizers and finally, the fourth presentation will focus on data converters.

TSB – 13:00-17:00
Noise In Linear Circuits

Topics & Speakers:

1- Physical Sources of Noise, Marian Pospieszalski, NRAO.
2- Noise Analysis of Linear Networks, Luciano Boglione, UMass-Lowell.
3- Noise Measurement, Luciano Boglione, UMass-Lowell.
4- Noise Models of Solid State Devices'', Marian Pospieszalski, NRAO
5- Low Noise Amplifiers, Luciano Boglione, UMass-Lowell.
6- Miscellaneous Topics, Marian Pospieszalski, NRAO.

Organizers: **Dr. Luciano Boglione,** University of Massachusetts-Lowell, Engineering Technology
Marian Pospieszalski, NRAO

Sponsors: **MTT-14, MTT-23, RFIC**

Workshop Abstract: The workshop will address both theoretical and specific technical concepts encountered in the analysis, measurement and design of linear noisy circuits. Although the material to be presented can be found in many published books and papers, it is usually broadly scattered and not necessarily presented in orderly sequence. This workshop will focus on tutorial exposition of some key physical and network theoretic ideas as applied to practical models, circuits and measurement methods. It is therefore addressed to those interested in developing a good understanding of noise in microwave devices and circuits, especially to those practitioners entering the field. The subjects to be covered are as follows: Physical sources of noise, Noise analysis of linear networks, Noise measurement, Noise models of solid-state devices, Low-noise amplifiers, and miscellaneous topics associated with noise in linear circuits.

WORKSHOPS

OTHER SUNDAY WORKSHOPS

Number	Time	Description
WSC	13:00-17:00	Recent Advances in GaN HEMT Performance, Modeling, Linearity and Design Techniques
WSF	08:00-17:00	Medical Applications of RF and Microwaves
WSH	08:00-17:00	Measurements for Wireless System-Level Evaluation
TSC	08:00-12:00	Advances in CAD Techniques for EM Modeling and Design Optimization

MONDAY WORKSHOPS

Number	Time	Description
WMA	08:00-17:00	Highly Efficient Linear Power Transmitters for Wireless Applications based on Switching Mode Amplifiers
WMB	08:00-17:00	Enabling Technologies for Wireless Transceivers Beyond-3G
WMC	08:00-17:00	Challenges in Model-based HPA Design
WMD	08:00-17:00	Millimeter-Wave Power Amplifier Technology: Power, Linearity and Efficiency
WME	08:00-17:00	CMOS/SiGe-based Systems for mm-Wave Commercial Applications
WMF	08:00-12:00	Design and implementation techniques for multiband filters and practical points of view.
WMG	13:00-17:00	Miniaturization Techniques of RF and Microwave Filters
WMH	08:00-17:00	Advances in Reconfigurable Microwave Technologies for Wireless Communication and Radar Sensing
WMI	08:00-12:00	High Speed Signal Integrity Workshop with Emphasis on Jitter
WMJ	08:00-12:00	3D Metamaterials: Theory, Structures, Techniques, and Devices
WMK	08:00-17:00	High-speed electronic technologies for > 100-G communications
WML	13:00-17:00	Progress in Microwave Ferrite Materials and Applications
WMM	13:00-17:00	Printed RF Electronics, RFID's and Wireless Sensors: State and Challenges
WMN	08:00-17:00	Applications and Misapplications of Measurement Uncertainty
TMA	08:00-12:00	RF Design Components of Magnetic Resonance Imaging
TMB	13:00-17:00	Demystifying Microwave Signal Integrity - High Speed Design & Measurement

FRIDAY WORKSHOPS

Number	Time	Description
WFA	08:00-17:00	Unification of Time Domain Methods in Computational Electromagnetics
WFB	08:00-17:00	System in Package Technologies and Trends
WFC	08:00-17:00	Progress in Local and Global Positioning in Europe
WFD	08:00-17:00	Computational Multi-Physics Techniques for the Analysis & Design of Electromagnetic Micro/Nano-Devices
TFA	08:00-12:00	Spectrum Policy for the Microwave Engineer: Getting Technology from the Lab to the Marketplace

ADVANCE REGISTRATION - see center registration form

Advance registration and instructions for completing registration form.

ADVANCE REGISTRATION

Please follow these instructions for completing the Advance Registration Form on the Center Insert. Advance Registration rates are valid until the deadlines shown on the form and are approximately 30% lower than the on-site fees shown on Page 93. Registration is required for all attendees, including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the breakfasts, workshops, technical sessions, and Exhibition Hall. This form is not used for the guest tour registration, which is described elsewhere in this Program Book. Each registrant must submit a separate form with payment. Registration by telephone is available for handicap, special needs, or information; please call 1-781-769-9750.

① METHODS OF REGISTRATION

Individuals can register online, by FAX, or by mail. Those registering by mail should send their form in early enough to ensure the application is received by the deadline; otherwise on-site fees will be charged. If the registration is sent by FAX, do not send it by mail. Additional items can be added on site after advance registration.

② PERSONAL INFORMATION

For phone numbers outside the U.S., please include a country code. If you would like to receive information by email from the IEEE, MTTS, or microwave companies, mark the appropriate boxes. An optional complimentary badge for one guest allows access to the Hospitality Suite, Plenary Session, and Exhibition Hall but does not allow access to Technical Sessions and Workshops.

③ MEMBERSHIP

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check-in at the conference. Registrants who do not have a current IEEE membership card at check-in will be charged the nonmember rates. If you are not a member and wish to take advantage of the member rates, call 1-800-678-IEEE or visit www.ieee.org/services/join prior to registering.

④ SYMPOSIA

Microwave Week hosts three symposia: the International Microwave Symposium (IMS), the RFIC Symposium, and the ARFTG Conference. Select the conferences you wish to attend. Students, retirees, and IEEE Life Members receive a discount on registration fees. To qualify as a student, a registrant must be either an IEEE Student Member or a full-time student carrying a course load of at least nine credit hours.

- IMS Technical sessions are held on Tuesday, Wednesday, and Thursday. Registration includes continental breakfast, admission to the exhibits, abstract books, and a CD-ROM.
- RFIC technical sessions are held on Monday and Tuesday. Registration includes continental breakfast, admission to the RFIC, Reception and exhibits, a digest, and a CD-ROM
- ARFTG technical sessions are held on Friday. Registration includes breakfast, lunch, a CD-ROM, and admission to the ARRFTG exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE members.
- Microwave Week hosts the largest exhibition of its kind with over 400 companies. Exhibit-only registration is available onsite for $20.15

⑤ EXTRA CD-ROMS AND DIGESTS

Additional CD-ROMS (IMS, RFIC and ARFTG) and digests (RFIC only) are available for purchase and pickup at the conference. After the Symposium, digests (RFIC only) and CD-ROMS (IMS, RFIC and ARFTG) will be available for purchase from IEEE.

⑥ AWARDS BANQUET

The MTT-S Awards Banquet will be held on Wednesday from 19:30 to 22:00 at the Omni Hotel in the Grand Ballroom. The evening will include fine dining, an awards presentation, and entertainment. Major Society awards will be presented.

⑦ BOXED LUNCHES

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the Panel Sessions or Exhibition Hall during lunchtime. It is encouraged to purchase boxed lunches in advance, as on-site pricing will be higher. Refunds are NOT available since these lunches are ordered in advance.

⑧ WORKSHOPS

The workshop fee includes a CD-ROM and speaker's notes for that workshop. Full day workshops and morning workshops include a continental breakfast, boxed lunch and a morning refreshment break. Afternoon workshops include a boxed lunch and an afternoon refreshment break. The All-Workshop CD-ROM fee includes material for all workshops on one CD-ROM but does not include admission to any workshops.

⑨ REMITTANCE

Individual remittance must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on a U.S. bank, traveler's check, international money order, or credit card (VISA, MasterCard or American Express only). Personal checks must be encoded at the bottom with the bank, account, and check number. Bank drafts, wire transfers, cash, and purchase orders are UNACCEPTABLE and will be returned. Please make checks and money orders payable to "IEEE/MTT-S". Written requests for refunds will be honored if received by May 9, 2008.

ON-SITE REGISTRATION

ADVANCE REGISTRATION

On-site registration for all Microwave Week events will be available at the Georgia World Conference Center. Registration hours are:

Saturday, June 14	14:00 - 18:00
Sunday, June 15	07:00 - 18:00
Monday, June 16	07:00 - 17:00
Tuesday, June 17	07:00 - 17:00
Wednesday, June 18	07:00 - 17:00
Thursday, June 19	07:00 - 15:00
Friday, June 20	07:00 - 09:00

EXHIBIT ONLY REGISTRATION

Exhibit-only registration is available on-site for $20.

GUEST TOUR REGISTRATION

Registration for guest tours will be available in Georgia World Congress Center lobby. Please refer to the Guest Tour Program section of this Program Book for further details and tour descriptions.

PRESS REGISTRATION

Credentialed press representatives are welcome to register without cost, receiving access to technical sessions and exhibits. Digests are not included. The Press Room is located in GWCC Building A Room 412A on Tuesday through Thursday.

ARFTG REGISTRATION

Late on-site ARFTG Registration will be available at the Omni Hotel on Friday from 07:00 to 11:00. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

ON-SITE REGISTRATION (continued)

REGISTRATION FEES

	Member	Non-Member
IMS Sessions	$515 ($80)	$770 ($160)
IMS Sessions (no CD-ROM)	$440	$650
Single-day Registration	$270	$375
RFIC Sessions	$260	$390
RFIC Reception Only	$65	$85
ARFTG Sessions	$270	$415
IMS and ARFTG CD ROM	$75	$145
RFIC Digest	$75	$145
RFIC CD ROM	$75	$145
Box Lunches (per day)	$25	$25
Awards Banquet	$95	$95
Workshops (full day)	$200	$300
Workshops (half day)	$150	$225
All Workshops CD ROM	$240	$350
ARFTG Conference Compendium CD ROM		
ARFTG Workshop Compendium CD ROM	$75	$110
Exhibition Only Pass	$20	$20

*Student, retiree and IEEE Life Member prices are shown in parenthesis.

REFUND POLICY

Written requests received by May 5, 2008 will be honored. **Refund requests postmarked after this date and on-site refunds will be granted ONLY if an event is cancelled.** This policy applies to registrations for the symposium sessions, workshops, digests, extra CD-ROMS, awards banquet and boxed lunches. Please state the pre-registrant's name and provide a mailing address for the refund check. If registration was paid by credit card, the refund will be made through an account credit. Account number must be provided if the initial registration was done on-line. Address your requests to:

MTT-S Registration
685 Canton Street
Norwood, MA USA 02062-2608

SOCIAL EVENTS

Sunday, 15 June 2008
RFIC RECEPTION — 19:00-21:00
Georgia World Congress Center, Room A412ab

Immediately following the RFIC Plenary Session is the RFIC Reception to be held in adjacent room 412ab at the Georgia World Congress Center. This social event is a key component of the RFIC Symposium, providing an opportunity to connect with old friends, make new acquaintances, and catch up on the wireless industry. Admittance is included with RFIC Symposium registration. Additional tickets can also be purchased separately at registration.

Monday, 16 June 2008
IMS 2008 RECEPTION — 18:00-20:00
Omni Hotel, Grand Ballroom

All Microwave Week attendees and exhibitors are invited to attend a reception hosted by IMS 2008 in the Grand Ballroom of the Omni Hotel.

Tuesday, 17 June 2008
WOMEN IN MICROWAVES RECEPTION — 18:00-20:00
Omni Hotel, International Ballroom A

STUDENT RECEPTION — 9:00-21:00
Omni Hotel, International Ballroom D

JOE TAYLOR RUMP SESSION RECEPTION — 18:30-20:00
Georgia World Congress Center, A411

A reception will be held for all attendees of the Joe Taylor Rump Session prior to the presentation.

HAM RADIO SOCIAL — 20:00-22:00
Georgia World Congress Center, A412ab

Radio amateurs attending the IEEE MTT-S International Microwave Symposium (IMS 2008) in Atlanta are invited to the Ham Radio Social. It follows the talk by Joe Taylor K1JT on "The Discovery of Gravity Waves Amidst the Noise," which leads into the WSJT software for weak-signal amateur communication. The organizers are Fritz Raab W1FR and Al Katz K2UYH.

Wednesday, 18 June 2008
INDUSTRY HOSTED COCKTAIL RECEPTION — 18:00-20:00
Omni Hotel, International Ballroom

Symposium Exhibitors will host a cocktail reception. Complimentary beverage tickets will be included in the registration packages.

MTT-S AWARDS BANQUET — 19:30-22:00
Omni Hotel, Grand Ballroom

The MTT-S Awards Banquet includes a fine dinner, awards presentation, and entertainment. Major society will be presented. Tickets can be purchased at the time of registration.

Thursday, 19 June 2008
MTT-S STUDENT AWARDS LUNCHEON — 12:00-14:00
Omni Hotel, International Ballroom F

All students are invited to attend the luncheon, which recognizes recipients of the IMS 2008 Student Paper Awards, MTT-S Graduate Fellowships, MTT-S Undergraduate Scholarships, the Student High-Efficiency Power Amplifier Competition Prize, and the Student Low Power Consumption FM Radio Receiver Design Competition.

MTT-S GRADUATES OF THE LAST DECADE
(GOLD) RECEPTION — 17:30-19:00
STATS Food Play Sports Bar

The IEEE MTT GOLD Committee invites all MTT GOLD members to a reception at the STATS Food Play Sports Bar which is conveniently located in downtown Atlanta across from the Georgia World Congress Center. This will be an excellent opportunity not only to relax and entertain, but also to interact and network with other GOLD members. If you require more information regarding GOLD or the reception, please feel free to stop by the GOLD Pavillion located in Hall A3 of the exhibition hall.

HOSPITALITY SUITE and RECREATIONAL ACTIVITIES

HOSPITALITY SUITE: OMNI HOTEL - PECAN ROOM (LEVEL M3)

We are pleased to offer a hospitality suite in the Omni Hotel for the families of our technical attendees to relax and enjoy in between experiencing everything that Atlanta, GA has to offer. The suite will be open Sunday, 15 June through Friday 20 June from 07:00 to 12:00 and will offer a light breakfast, grab-and-go snacks, and guest tour information.

Please note that guest badges are required for entry into the Hospitality Suite.

RECREATIONAL ACTIVITIES:

While you are in Atlanta we hope that you can enjoy the all that the city has to offer. From the sleek modern sky scrapers, to the quaint southern charm, we have a variety of activities planned for you and your guests to enjoy all aspects of life in and around Atlanta.

We have partnered with Atlanta Arrangements, Inc, the premier destination management company in Atlanta. They will handle all aspects of the activity registration and on-site logistics of each event. Please visit their website, http://www.atlantaarrange.com/ims/, to preregister for each activity and to see the most up-to-date information regarding the tours. Atlanta Arrangements may also be reached at 1-800-883-3866 or aai@atlantaarrange.com.

We strongly recommend that you secure your space on your favorite tours as soon as possible! However, there will be an on-site sign-up desk available in the Building A Level 4 Lobby near the IMS 2008 main registration area. Come enjoy southern hospitality at its best. See you in the Big Peach!

Sunday, 15 June 2008 HALF DAY TOUR OPTION
13:00-18:00 - ATLANTA'S FAMOUS FIRSTS

Introducing the world's favorite soft drink and the first cable television network on earth, both of whom proudly call Atlanta home. As part of the Cable News Network, CNN and Headline News have their home in the heart of downtown Atlanta. Today, you will catch a glimpse of the fast-paced excitement of a 24-hour news broadcast in the making with a tour of Inside CNN Atlanta. You'll view the newsroom, the cameras and lights, and all the other behind-the-scenes places and things the viewing public never sees. The World of Coke is a new and expanded attraction where you can explore the complete story - past, present and future - of the world's best-known brand. There's something for visitors of all ages to enjoy, from a thrilling 4D cinematic experience, to the largest collection of Coke memorabilia ever assembled,

ADULT: $36.00 per person **CHILD** (5-12 yrs)**:** $32.00 per person

Price includes guides, tour of CNN and coke, and entrance fee.

PLEASE NOTE: Children under the age of 6 are not allowed to tour CNN.

Monday, 16 June 2008 HALF DAY TOUR OPTION
09:00-12:00 - GEORGIA'S STONE MOUNTAIN

Come explore Stone Mountain Park, a 3,200 acre world where excitement's carved in stone. Georgia's Stone Mountain, known as the eighth wonder of the world, amazes millions of people and was formed approximately 300 million years ago. The giant granite rock rises 1,683 feet above sea level and covers 583 acres of rolling plateau. The largest bas-relief sculpture in the world, the Confederate Memorial Carving, depicts three heroes of the Civil War-Confederate President Jefferson Davis and Generals Robert E. Lee and Thomas J. "Stonewall" Jackson. The three-acre carved surface is larger than a soccer field!

COST: $40.00 per person. *Price includes luxury motorcoach transportation, guides, choice of two attractions, parking, and entrance fees.*

Monday, 16 June 2008 **FULL DAY TOUR OPTION**
10:00-15:00 **- WILD ATLANTA!**

Begin your day on an urban safari to the magical land of Zoo Atlanta. From the zebras and giraffes of the Ketambe bush to the gorillas and orangutans of the Ford African Rain Forest, the zoo's exotic residents will provide the perfect backdrop for this wild day. Zoo Atlanta is committed to studying giant pandas, to help them to survive and avoid extinction. You may experience rare up-close viewing opportunities in the Asian Forest Exhibit and Conservation Center. Everybody seems to love giant pandas! Following their visit to the zoo, guests will get to visit the Georgia Aquarium. Guests can explore all of the Aquarium's fascinating exhibits where they will be amazed at every turn! This world-class entertainment attraction features more than 100,000 animals from over 500 species. The Aquarium itself holds over eight million gallons of fresh and marine water! The exterior of the Georgia Aquarium building has been designed to look like a giant ship breaking through a wave. As guests enter the huge atrium inside the building, they will be led into the facility by "a wall of fish" guiding them inside. At the aquarium, guests will also be able to enjoy lunch on their own at the food court.

ADULT: $70.00 per person **CHILD:** (3 - 11 yrs)**:** $62.00 per person
Price includes luxury motorcoach transportation, guides, and admission fees.

Tuesday, 17 June 2008 **HALF DAY TOUR OPTION**
13:00-17:00 **- A TASTE OF THE PEACH**

Relax as your experienced guide acquaints you with the city's history—from its fiery past to its exciting future. Catch a glimpse of Peachtree Center, Georgia's gold-domed State Capitol, the Georgia World Congress Center, the Georgia Dome, Philips Arena, Centennial Olympic Park, CNN Center, Martin Luther King, Jr. Historic District and much, much more. Then it's off toward revitalized Midtown, home of the world headquarters of the Coca-Cola Company, the ever-expanding campus of Georgia Institute of Technology and the newly constructed Atlantic Station, with a live, work and play environment.

COST: $31.00 per person. *Price includes luxury motorcoach transportation, guides, self guided tour of MLK Center, tour of cyclorama and entrance fees.*

Tuesday, 17 June 2008 **FULL DAY TOUR OPTION**
09:30-15:30 **– COVINGTON'S MANSIONS AND MAGNOLIAS**

Be carried away to ages past; back to the time of mansions and magnolias. Go east to the town of Covington, where you will tour beautiful historic homes. These fine homes have been beautifully maintained and are decorated in keeping with the styles of their era. All are private homes, with the owners serving as your guide at each. Lunch will be served at the Blue Willow Inn, a charming restaurant house in a turn of the century Greek Revival mansion. Here you can help yourself to the all-you-can-eat Southern buffet.

COST: $72.00 per person. *Price includes luxury motorcoach Transportation, guides, tour of 3 homes, lunch at the Blue Willow Inn, and entrance fees.*

Wednesday, 18 June 2008 **HALF DAY TOUR OPTION**
09:00-13:00 **- ATLANTA'S FAMOUS FIRSTS**

ADULT: $36.00 per person **CHILD** (5-12 yrs)**:** $32.00 per person
Price includes guides, tour of CNN and Coke and entrance fees.

Wednesday, 18 June 2008 **HALF DAY TOUR OPTION**
10:00-15:00 **- MOMMY AND ME**

This tour is the perfect way to explore the city of Atlanta with your kids! Bond with other parents and their children as you experience two of Atlanta's most popular attractions for children, Imagine It and the Georgia Aquarium. Begin your day with face painting at the hotel! A face painter will be on-site to draw your kids' favorite pictures on their faces to get them ready for their day of fun! Then your guests will walk from the hotel to Imagine It, the Children's Museum that is just across Centennial Olympic Park. The mission of Imagine It! The Children's Museum of Atlanta is to create environments and activities where young children experience the power of imagination and the pure delight of learning with each other and with grown-ups. As a group your kids are sure to make new friends and interact with one another during this fun learning experience! Following Imagine It! your guests will head to the Georgia Aquarium. Here at the Aquarium your guests can enjoy lunch on their own at the food court! On the way back to the hotel, be sure to stop by the fountains in Centennial Olympic Park to cool off before heading back to the hotel! This fun-filled day is sure to be a great bonding experience for the children and their parents.

ADULT: $60.00 per person **CHILD** (3 – 11 yrs)**:** $55.00 per person
Price includes guides, face painter, and admission fees.

Wednesday, 18 June 2008 **FULL DAY TOUR OPTION**
09:30-16:00 **- THE GOOD LIFE IN HISTORIC BUCKHEAD**

Buckhead is Atlanta's premier residential and shopping district. Tour Georgia's elegant Governor's Mansion, a stunning example of Classical Revival architecture. This 1968 mansion, the home of Georgia's Chief Executive and his family, is filled with an extensive collection of Federal period furniture and Aubusson carpets. Afterward, visit the Atlanta History Center with its regal Swan House, quaint Tullie Smith House, and the Atlanta History Museum with the recently opened Centennial Olympic Games Exhibit. Enjoy a truly Southern lunch at the Swan Coach House, the former garage and servant quarters for the Swan House. Following their visit to the Atlanta History Center, guests will continue with a visit to the Carter Presidential Library.

COST: *$94.00 per person. Price includes luxury motorcoach transportation, tour of Governor's Mansion, Tour of the History Center, Tullie Smith and The Swan House, lunch, and entrance fees.*

Thursday, 19 June 2008 **HALF DAY TOUR OPTION**
13:00-17:00 **- CULTURAL MIDTOWN**

Start your day with a visit to the glorious Atlanta Botanical Gardens, a showcase of the most beautiful and unusual flora in our region, located on a 60-acre site in Midtown's Piedmont Park. Take a quiet stroll through the massive hardwood forest or the lovely vegetable, rose or Japanese gardens. Then feast your senses at the magnificent Dorothy Fuqua Conservatory. Under the glittering glass dome live some of the world's most exotic and glorious plants. Next, enjoy a spectacular visit to one of Atlanta's favorite attractions, Margaret Mitchell's "Dump". This is the home she lived in with her husband while writing the world famous book Gone With the Wind in 1926. You will also have the opportunity to visit a museum at the Margaret Mitchell House. The museum exhibits Herb Bridges collection of Gone With The Wind movie memorabilia and opened on December 15, 1999, the 60th anniversary of Gone With The Wind's premiere. Bridges is considered the world's foremost authority on Gone With The Wind and this is the largest memorabilia collection.

COST: $52.00 per person. *Price includes luxury motorcoach, guides, self guided tours of High museum and the Margaret Mitchell House, and entrance fees.*

Thursday, 19 June 2008 **HALF DAY TOUR OPTION**
09:00-14:00 **- SHOP TILL YOU DROP**

Enjoy a day full of shopping as your motorcoach takes you to elegant Buckhead. Phipps Plaza - named a "Southern Best" in "Southern Living" magazine's Readers' Choice Awards - is anchored by Nordstrom, Parisian, and Sak's Fifth Avenue. Atlanta's premier upscale shopping center, Phipps Plaza is home to more than 100 specialty stores, 4 restaurants, including the newly opened Twist serving creative satays, tapas, and wraps, and a 14-screen AMC theatre. Across the way from Phipps Plaza is Lenox Square. Lenox Square is anchored by Neiman Marcus, Macy's and Bloomingdale's. Guests are treated to unique specialty retailers such as BCBG, Burberry, Brooks Brothers, Cartier, Louis Vuitton, Hermes, Ferragamo, Ralph Lauren, St. John's Knits and Versace Jeans Couture. Experience fine dining at the new Clubhouse, Brasserie Le Coze or Prime. You are also invited to enjoy a meal at one of five casual eateries, or even a quick bite at one of a wide selection of specialty food shops at the Market Food Court.

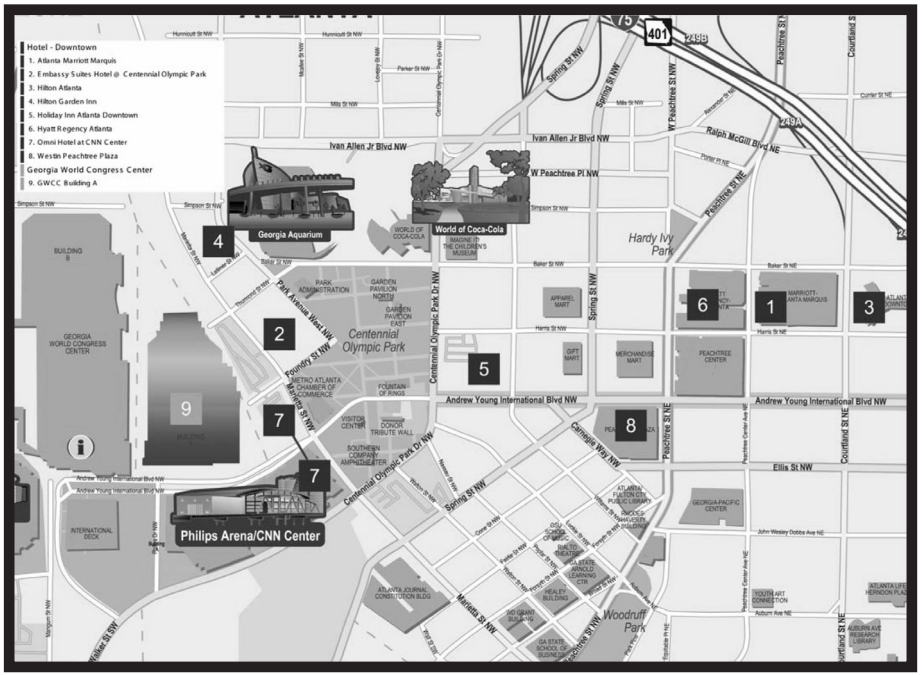
COST: $24.00 per person. *Price includes luxury motorcoach transportation.*

Thursday, 19 June 2008 **HALF DAY TOUR OPTION**
14:30-18:30 **- OUTLET SHOPPING**

Spend a great afternoon shopping at the North Georgia Premium Outlets, located in Dawsonville, north of Atlanta. Discover 140 outlet stores offering the area's finest collection of designer fashions and leading brand names, all at everyday savings of 25% to 65%. You will find a wide assortment of specialty shops such as Anne Klein, BCBG Max Azria, Donna Karan, Gap Outlet, Polo Ralph Lauren, Crate & Barrel Outlet, Royal Doulton, Williams - Sonoma Furniture and Outlet and many more. Your motorcoach/minibus will bring you to the outlets where you can spend a whole afternoon finding great deals. If you need a break, you can enjoy lunch on your own at the Main Street Eatery.

COST: $28.00 per person. *Price includes luxury motorcoach transportation.*

NOTES:



RFIC Attendee Hotels

1. Atlanta Marriott Marquis
2. Embassy Suites
3. Hilton Atlanta
4. Hilton Garden Inn
5. Holiday Inn Atlanta Downtown
6. Hyatt Regency Atlanta
7. Omni Hotel at CNN Center – Headquarters Hotel
8. Westin Peachtree Plaza
9. Georgia World Congress Center

IEEE
468 Walden Trail
Waxhaw, NC 28173

2008 RFIC Symposium
Atlanta, Georgia
June 15-17, 2008

PROGRAM