2025 IEEE Radio Frequency Integrated Circuits Symposium

RFIC

San Francisco, California, USA
15–17 June 2025

IEEE

PROGRAM

Moscone Convention Center

Sponsored by

IEEE Microwave Theory and Technology Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society

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IEEE MICROWAVE THEORY & TECHNOLOGY SOCIETY

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RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 15 June 2025
Moscone Center

Enjoy an entertaining and relaxing evening with your RFIC colleagues and friends at the special Sunday night RFIC events.

17:30–19:00, Plenary Session, Esplanade Ballroom: The evening begins with a warm welcome by the General Chair and the TPC Chair, the Student Paper Awards, the Industry Paper Awards, and the Tina Quach Service Award ceremony followed by two plenary speakers: Dr. John Smee, Qualcomm, Senior Vice President of Engineering, and Maryam Rofougaran, Movandi, CEO and Co-founder.

19:00–21:00, RFIC Symposium Reception and Showcase, Rooms 301–304: Food and drinks will be provided while you connect with colleagues, friends, make new acquaintances, and catch up on the latest developments in the field. The Symposium Showcase will feature our industry and student paper awards finalists and the Systems & Applications Forum. The selected authors will present their innovative work in electronic poster format or show a live demonstration.

Your admittance is included with the RFIC Symposium registration and the Super-pass registration. Those who cannot attend the rest of RFIC but don't want to miss the event can purchase Sunday-night-only tickets. Please see https://rfic-ieee.org/ for more details.

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RFIC Symposium Schedule (14–17 June 2025)

Event	Location	Sat 14 June	Sun 15 June	Mon 16 June	Tue 17 June
Registration	South Lobby	08:00–17:00	07:00–18:00		
Speakers' Breakfast	301–304 (Sun) 303–304 (Mon, Tue)		07:00–08:00		
Workshops	Rooms 201, 203–208, 210, 211, 215, 305/309, 306–308, 310–312		08:00–11:50 13:30–17:20		
Workshops Lunch	301–304		11:40–13:00		
Technical Lecture	Rooms 212–214		12:00–13:20		
Plenary Session	Esplanade Ballroom		17:30–19:00		
Reception and Symposium Showcase	Rooms 301–304		19:00–21:00		
Technical Sessions	Rooms 203, 205, 207			08:00–09:40 10:10–11:50 13:30–15:10 15:40–17:20	
Panel Sessions	Room 301			12:00–13:30	
Student-Industry-Academia RFIChat	Room 301				17:30–19:00

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Welcome Message from Chairs

IEEE RFIC Symposium (RFIC) is the premier event for cutting-edge innovation and technical excellence dedicated to showcasing the latest breakthroughs and research findings across various domains related to Radio Frequency (RF), millimeter-wave (mm-Wave), and wireless Integrated Circuits (ICs). RFIC 2025 is held at the Moscone Center, in San Francisco, CA, right in the heart of Silicon Valley from Sunday morning, 15 June, through Tuesday night, 17 June

We thank you for participating on behalf of the RFIC Executive and Steering Committees.

RFIC 2025 introduces several additions to its program, reflecting its commitment to innovation and inclusivity, to drive progress in RFIC design while shaping the next generation of engineers. The new RFIC Integrated Systems and Applications category welcomes presentations on complete systems. The introduction of the Industry Track bridges academia and practice, inviting professionals to share proven techniques, lessons learned, and impactful RFIC designs.

The technical sessions will span all the topics of the community such as highly integrated wireless systems-on-chip, power amplifiers and front-end circuits or oscillators, frequency synthesizers, device modeling, packaging, and testing technologies. Some emerging topics are now well confirmed such as AI and machine learning applied to RF circuits, D-band circuits, wireline, optical, quantum computing, and sensing circuits. System-level innovations will also be presented with imaging, satellite communications, and biomedical applications.

RFIC 2025 begins with 12 workshops and a technical lecture covering advanced RFIC design, communications, and emerging challenges. Topics include frequency synthesizer techniques, low-power RFIC architectures, and advanced power amplifiers. Communications discussions will focus on 5.5G and 6G phased array systems, self-interference cancellation, and RFICs for LEO satellite broadband. Emerging challenges include quantum computing RF design and SiP/3DHI for mm-wave phased arrays. The Technical Lecture delivered by world-renowned Dr. Shahriar Shahramian, Bell Laboratories, Nokia, will present an 80-minute discussion on the art of metrology, from measurement techniques to pitfalls.

The RFIC Plenary Session will conclude the day with conference highlights, the presentation of the Student and Industry Best Paper Awards, and two plenary talks. In his talk "RFIC in the Age of 6G: Challenges, Innovations, and Future Directions", Dr. John Smee (Senior Vice President of Engineering at Qualcomm), will provide an overview of advancements in RFICs needed to meet the demands of 6G, such as new spectrum integration, enhanced power efficiency, and enabling innovations like ambient IoT, RF sensing, and full duplex communications. In her talk "Next-Gen RFICs: Redefining Data Centers and Wireless Networks for the AI Era", Maryam Rofougaran (Movandi, CEO and Co-founder), will discuss the role of RFICs in data center interconnections, highlighting innovations in mm-wave and sub-THz RFICs for sustainable, scalable, and high-performance connectivity.

The RFIC Reception will follow with highlights from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC 2025 Sponsors. You can enjoy close-up discussions with authors demonstrating their work in a lab-like environment.

RFIC 2025 will offer panel sessions during the lunch breaks. Monday's lunchtime panel, titled "Low-Earth-Orbit (LEO) Satellite Broadband: Revolutionizing Communication or Just Adding Space Debris?" will open the debate on global connectivity challenges or high costs and limited accessibility. Tuesday's lunchtime panel, organized jointly with IMS 2025 and titled "RFIC Innovation: Has the Field Stalled or Are Researchers Losing Their Way?" will discuss a questionable maturing field of RFIC design shifting towards AI-driven heterogeneous integration or challenges posed by funding limitations and publication-focused research culture stifling true innovation.

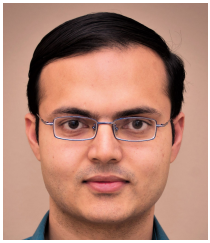
Finally, RFIC 2025 proposes a farewell event called Student-Industry-Academia RFIChat where the next generation of engineers made of students and young professionals can meet, interact, and learn about technology trends and future career opportunities from industry experts

We welcome you all to the 2025 RFIC Symposium in San Francisco, CA.

François Rivet
General Chair
University of Bordeaux

Mohyee Mikhemar
TPC Chair
Broadcom

Amin Arbabian
TPC Co-Chair
Stanford University



Bodhisatwa Sadhu
TPC Co-Chair
IBM T.J. Watson Research Center

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RFIC 2025 Schedule

Moscone Center

Saturday, 14 June 2025

08:00–17:00 Registration — South Lobby

Sunday, 15 June 2025

07:00–18:00 Registration — South Lobby
07:00–08:00 Speakers' Breakfast — 301–304
08:00–11:50 Workshops — 201, 203–208, 210, 211, 215, 305/309, 306–308, 310–312
11:40–13:00 Workshops Lunch — 301–304
12:00–13:20 Technical Lecture — 212–214: *The Art of Metrology — Measurement Techniques & Pitfalls*
13:00–17:20 Workshops — 201, 203–208, 210, 211, 215, 305/309, 306–308, 310–312
17:30–19:00 RFIC Plenary — Esplanade Ballroom
19:00–21:00 Welcoming Reception Featuring Symposium Showcase — 301–304

Monday, 16 June 2025

07:00–18:00 Registration — South Lobby
07:00–08:00 Speakers' Breakfast — 303–304
08:00–09:20 RMo1A — 203: *Digital Transmitters and Power Amplifiers*
08:00–09:20 RMo1B — 205: *Reconfigurable Phased Arrays for Satellite Communication*
08:00–09:20 RMo1C — 207: *mm-Wave Circuit Advances in Industry*
09:40–10:10 Coffee Break — 2nd Floor Meeting Room Foyer
10:10–11:50 RMo2A — 203: *High Performance Power Amplifiers and Front-End Modules*
10:10–11:30 RMo2B — 205:
Advances in VCO Design at Microwave, mm-Wave, and Sub-THz Frequencies
10:10–11:50 RMo2C — 207: *mm-Wave Building Blocks and Components*
12:00–13:30 RFIC Panel Session — 301: *Low-Earth-Orbit (LEO) Satellite Broadband: Revolutionizing Communication or Just Adding Space Debris?*
13:30–14:50 RMo3A — 203: *Advanced Frequency Generation in Sub-10nm CMOS and SiGe BiCMOS*
13:30–14:50 RMo3B — 205: *mm-Wave Transmitter and Receiver Front-Ends*
13:30–15:10 RMo3C — 207: *High Speed and Domain Specific Data Converters*
15:10–15:40 Coffee Break — 2nd Floor Meeting Room Foyer
15:40–17:20 RMo4A — 203: *Transmitters Beyond 100GHz*
15:40–17:20 RMo4B — 205: *Design Techniques of RF/mm-Wave Low-Noise Amplifiers (LNAs) and Frontend Modules (FEMs)*
15:40–17:20 RMo4C — 207: *Unleashing Energy Efficiency and High Linearity in IoT RFICs*

Tuesday, 17 June 2025

07:00–18:00 Registration — South Lobby
07:00–08:00 Speakers' Breakfast — 303–304
08:00–09:40 RTu1A —203: *mm-Wave Power Amplifiers and Transmitters*
08:00–09:40 RTu1B —205: *High-Performance RF Oscillators*
08:00–09:40 RTu1C —207: *Pushing RFIC Boundaries with Out-of-the-Box Innovation*
09:40–10:10 Coffee Break — Exhibit Hall
10:10–11:50 RTu2A —203: *Design Techniques for High Performance SiGe PAs*
10:10–11:30 RTu2B —205: *mm-Wave and Sub-THz Radar SoCs and Sensing Techniques*
10:10–11:50 RTu2C —207:
Heterogeneous Integration for RF/mm-Wave Applications and Measurement Techniques
12:00–13:30 RFIC/IMS Joint Panel Session — 301:
RFIC Innovation: Has the Field Stalled or Are Researchers Losing Their Way?
13:30–15:10 RTu3A —203: *PLLs and Frequency Multipliers*
13:30–15:10 RTu3B —205: *D-Band Circuits and Systems for Sensing and Communications*
13:30–15:10 RTu3C —207: *High-Speed Circuits and Systems for Photonic and Quantum Applications*
15:10–15:40 Coffee Break — Exhibit Hall
15:40–17:20 RTu4A —203: *Circuit Techniques for Radar and Phased Array*
15:40–17:20 RTu4B —205: *Circuit Blocks for D-Band Integrated Systems*
15:40–17:20 RTu4C —207: *Innovations in Low-Power, High-Performance Receiver Front-Ends*
17:30–19:00 Student-Industry-Academia RFIChat — 301:
Battle of the Bands: Matching Career Path to Frequency of Interest

RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 15 June 2025
Moscone Center

17:30–19:00
RFIC Plenary
Esplanade Ballroom
Chair: François Rivet, University of Bordeaux
Co-Chair: Mohyee Mikhemar, Broadcom

17:20	Doors opening and musical welcome
17:30	Welcome Message from General Chair and TPC Chair Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
18:00	RFIC in the Age of 6G: Challenges, Innovations, and Future Direction John Smee, Qualcomm
18:30	Next-Gen RFICs: Redefining Data Centers and Wireless Networks for the AI Era Maryam Rofougaran, Movandi

19:00–21:00
RFIC Welcoming Reception Featuring Symposium Showcase
Rooms 301–304

The RFIC Interactive Reception highlights the Student Paper Awards finalists, the Industry Paper Awards finalists, and the Systems & Applications Forum in an engaging social and technical evening event with food and drinks. Authors of these showcase papers will present their innovative work, summarized in poster format. Some showcase papers will also offer live demonstrations. This event is supported by the RFIC Symposium corporate sponsors.

Do not miss the RFIC Reception!

RFIC Plenary Speaker 1

Dr. John Smee
Senior Vice President of Engineering
Qualcomm

RFIC in the Age of 6G: Challenges, Innovations, and Future Directions

Abstract: In the upcoming era of 6G, RFICs are set to undergo transformative advancements to meet the demands of next-generation wireless communications. As on-device AI expands to more connected compute applications, the wireless data transfer requirements and number of connected edge devices will keep increasing. This talk will explore the incredible opportunities for RF development, including integrating new spectrum bands like the upper mid-band (6–15 GHz) with the wide range of existing FDD and TDD frequency bands for cellular systems. These advancements will enable innovative solutions in network infrastructure and devices, with a focus on improving the coverage and power efficiency for next-generation wireless systems. We will also delve into the latest innovations and future directions of RF technology, emphasizing its critical role in achieving the ambitious use cases envisioned for 6G such as ambient IoT, RF sensing, and full duplex communications. Join us as we highlight the bright future for RFICs and their pivotal role in the 6G revolution.

About Dr. John Smee

John Smee is Senior Vice President of Engineering and Global Head of Wireless Research at Qualcomm. He oversees all 5G/6G and Wi-Fi R&D projects including systems design, standards contributions, and advanced radio, hardware, and software research testbeds and technology trials with industry partners. He joined Qualcomm in 2000, holds over 200 U.S. Patents, and has focused on the innovation and commercial launches of wireless communications across 5G NR, 4G LTE, 3G CDMA, and IEEE 802.11. He also leads Qualcomm's companywide academic collaboration program across AI, augmented/virtual reality, automotive, IOT, security, semiconductor, and wireless. John was chosen to participate in the National Academy of Engineering Frontiers of Engineering program and served on the National Academy of Medicine Committee on Emerging Science, Technology, and Innovation. He received his Ph.D. in electrical engineering from Princeton University and also holds an M.A. from Princeton and an M.Sc. and B.Sc. from Queen's University.

RFIC Plenary Speaker 2

Maryam Rofougaran
CEO and Co-Founder
Movandi

Next-Gen RFICs: Redefining Data Centers and Wireless Networks for the AI Era

Abstract: As data demands surge across wireless networks and data centers — driven by AI growth — high-frequency RFICs are becoming vital to the future of both wireless and wireline connectivity. Operating in the millimeter-wave (mmWave) and sub-Terahertz (THz) frequencies, future RFICs unlock unprecedented data rates, enabling high-speed and low-latency links — both wirelessly to consumers as well as within data centers between GPUs. With new higher modulation techniques, sub-THz RFICs reduce latency and power usage, paving the way for sustainable, scalable data center interconnect architectures. Innovations in RF process nodes enable higher maximum frequencies and lower power consumption, optimizing RFICs' efficiency and performance. This presentation will explore the transformative role of RFICs across applications such as next-generation radars, sensors, 5G/6G networks, and satellite communications, with a focus on their pivotal role in data center interconnections.

About Maryam Rofougaran

Maryam Rofougaran is CEO and Co-founder of Movandi, a leader in RF and millimeter wave semiconductor and technology commercializing multi-gigabit millimeter wave networks. Movandi is breaking through the coverage and network challenges of millimeter wave networks. Their BeamXR active repeater and system solutions solve today's real-world 5G deployment challenges — by increasing 5G coverage and capacity, while reducing infrastructure costs by more than 50%, accelerating large-scale 5G commercialization. Before founding Movandi, Maryam was Senior Vice President of Radios at Broadcom Corporations and was instrumental in starting and building the wireless business at Broadcom and in growing it to annual revenue of more than $3 billion. Her first start-up Innovent System was acquired by Broadcom Corporations in 2000 and was the entrance of Broadcom into the wireless market. She is an Inventor and co-inventor on more than 300 U.S. patents. Maryam has a BS and MS in Electrical Engineering from UCLA. She was part of the team at UCLA that made RFCMOS and SOCs a reality. Maryam has been a member of various councils including CNBC CEO council and GSA CEO council.

The Student Paper Awards Finalists

Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

The RFIC Student Paper Award aims to encourage student submissions and give finalists the opportunity to promote their research during the reception following the plenary session. This year's finalists, listed below, were nominated by the RFIC Technical Program Committee. A panel of judges from the committee selected the top three papers through a thorough review and discussion process. All finalists receive complimentary registration to the RFIC Symposium. The winners will be announced during the RFIC Plenary Session on 15 June 2025 and will each receive a plaque.

A 19GHz Circular Polarized 256-Element CMOS Phased-Array Transmitter with 11W Average Power Consumption for LEO Satellite Terminal
[1]Science Tokyo, Japan, [2]Axelspace, Japan
Xiaolin Wang[1], Dongwon You[1], Xi Fu[1], Takeshi Ota[1], Michihiro Ide[1], Sena Kato[1], Jill Mayeda[1], Makoto Higaki[2], Jumpei Sudo[2], Hiroshi Takizawa[2], Masashi Shirakura[2], Takashi Tomura[1], Hiroyuki Sakai[1], Kazuaki Kunihiro[1], Kenichi Okada[1], Atsushi Shirane[1]
RMo1B-1 8:00

A 60-GHz Area-Efficient Coupled Standing-Wave-Oscillators LO Distribution Network for a 240-GHz 2-D Phased-Array
[1]National Taiwan University, Taiwan, [2]University of California, Berkeley, USA
Ying-Han You[1], Pin-Yu Lin[1], Sih-Ying Chen[1], Wei-Yu Lin[2], Jun-Chau Chien[2]
RMo2B-1 10:10

A 40GS/s 8bit Time-Interleaved Time-Domain ADC Featuring SFDR-Enhanced Sample-and-Hold Circuit and Power-Efficient Adaptive Pulse Generator in 28nm CMOS
[1]Xidian University, China, [2]Tsinghua University, China
Chenghao Zhang[1], Maliang Liu[1], Yuan Chang[1], Yihang Yang[1], Yintang Yang[1], Yong Chen[2]
RMo3C-1 13:30

An Ultra-Compact Switchless Bidirectional PA-LNA with 8-Shaped Transformer-Based Inter-Stage Matching Networks for W-Band Applications
SCUT, China
Lingtao Jiang, Lihong Chen, Xianfeng Que, Quan Xue, Yanjie Wang
RMo4B-4 16:40

Topology-Optimized Nonintuitive Multilayered mm-Wave Power Amplifiers
University of Southern California, USA
Vinay Chenna, Hossein Hashemi
RTu2A-1 10:10

3D-Millimeter Wave Integrated Circuit (3D-mmWIC): A Gold-Free 3D-Integration Platform for Scaled RF GaN-on-Si Dielets with Intel 16 Si CMOS
[1]MIT, USA, [2]Georgia Tech, USA, [3]AFRL, USA, [4]Universität der Bundeswehr München, Germany
Pradyot Yadav[1], Jinchen Wang[1], Danish A. Baig[2], Juan Pastrana-Gonzalez[3], John Niroula[1], Patrick Darmawi-Isakandar[1], Ulrich L. Rohde[4], Ahmad Islam[3], Muhannad Bakir[2], Ruonan Han[1], Tomás Palacios[1]
RTu2C-4 11:10

A 28–38GHz Digitally-Assisted Frequency Tripler with Background Calibration in 55nm SiGe BiCMOS

[1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy

D. Lodi Rizzini[1], F. Tesolin[1], M. Rossoni[1], B. Nanino[1], P. Granata[1], R. Moleri[1], A. Mazzanti[2], A.L. Lacaita[1], S.M. Dartizio[1], S. Levantino[1]

RTu3A-3 14:10

A Terahertz FMCW Radar with 169-GHz Synthetic Bandwidth and Reconfigurable Polarization in 40-nm CMOS

[1]SCUT, China, [2]CAS, China, [3]UTS, Australia

Aguan Hong[1], Xiang Yi[1], Yanjun Wang[1], Jianmin Hu[2], Zhantao He[1], Guohao He[1], Yang Yang[3], Jiexin Lai[3], Hongli He[1], Lina Su[1], Zhenyu Deng[2], Jingting Xie[2], Shaqi Yang[2], Hongkun Zhou[2], Lingeng Zheng[2], Sicheng He[1], Pei Qin[1], Haoshen Zhu[1]

RTu3B-2 13:50

A Fully Integrated 263-GHz Retro-Backscatter Circuit with 105°/82° Reading Angle and 12-dB Conversion Loss

MIT, USA

Mingran Jia, Jinchen Wang, Jaehong Jung, Xibi Chen, Eunseok Lee, Anantha P. Chandrakasan, Ruonan Han

RTu3B-4 14:30

A 19.4-fs$_{RMS}$ Jitter 0.1-to-44GHz Cryo-CMOS Fractional-N CP-PLL Featuring Automatic Bleed Calibration for Quantum Computing

[1]Xidian University, China, [2]Tsinghua University, China

Jinhai Xiao[1], Yong Chen[2], Ningyi Zhang[1], Rui Liu[1], Yuhao Zhang[1], Peng Luo[1], Maliang Liu[1], Yintang Yang[1], Xiaohua Ma[1], Yue Hao[1]

RTu3C-1 13:30

A 15/30/60-GHz 1TX/4RX Radar Chipset Achieving 6° Angular Resolution Using Frequency Dimension for Virtual Aperture Expansion

[1]UESTC, China, [2]University of Macau, China

Ruilin Liao[1], Haoran Wang[1], Jingzhi Zhang[1], Wei-Han Yu[2], Yue Song[1], Hongyang An[1], Huihua Liu[1], Kai Kang[1]

RTu4A-1 15:40

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

The Industry Paper Awards Finalists

Chair: Patrick Reynaert, KU Leuven

The RFIC Industry Paper Awards highlights outstanding industry papers. The six finalists are listed below. These papers received nominations from the TPC sub-committees and godparents in a doubleblind review. From these six papers, a two-stage review process was conducted by a committee of TPC judges to identify the top 3 papers that have the highest impact on the field of RFIC. These 3 winners will be announced at the RFIC Plenary Session in San Francisco where each winner will receive a plaque in recognition for their outstanding contribution.

D-Band Radio-on-Glass Modules for Spectrally-Efficient FD & FDD Multi-Kilometer Wireless Backhaul Links
Nokia Bell Labs, USA
Shahriar Shahramian, Michael J. Holyoak, Mustafa Sayginer, Mike Zierdt, Chris Adams, Muhammad Waleed Mansha, Joe Weiner, Ayush Rai, Ismail Kartam, Yves Baeyens
RMo1C-4 9:00

A High Power SOI-CMOS WI-FI 6 Front-End Module with Reconfigurable Class-J Power Amplifier
CEA-Leti, France
Pascal Reynier, Ayssar Serhan, Alexandre Giry
RMo2A-4 11:10

A 13.5 to 23GHz Compact PLL Based on a 0.006mm² Transformer-Based Dual-Resonator Tuned LC VCO in 5nm CMOS
IBM, USA
Armagan Dascurcu, Bodhisatwa Sadhu, Herschel Ainspan, Gary Kurtzman, John Borkenhagen, Zheng Xu, Jim Strom
RMo3A-1 13:30

A 16–22GHz Fractional-N PLL in 8nm FinFET with 68 fs_{rms} Jitter
[1]Samsung, USA, [2]Samsung, Korea
Wanghua Wu[1], Zhiyu Chen[1], Kyumin Kwon[1], Suoping Hu[1], Pak-Kim Lau[1], Changhun Song[1], Ali Binaie[1], Santosh Kumpatla[1], Juyeop Kim[1], Jeiyoung Lee[2], Chih-Wei Yao[1], Sangwon Son[1], Joonhoi Hur[1]
RMo3A-2 13:50

A 210–320GHz Power-Combining Distributed Frequency Doubler with Tuned Pre-Amplification in 0.13μm SiGe BiCMOS
Nokia Bell Labs, USA
Akshay Visweswaran, Yves Baeyens, Mustafa Sayginer, Hernan Castro, Ayush Rai, Shahriar Shahramian
RMo3A-3 14:10

Enabling Fast Steering of Arbitrary Beams with Phased Arrays
IBM, USA
Arun Paidimarri, Bodhisatwa Sadhu, Mark Yeck, Alberto Valdes-Garcia
RTu1C-2 8:20

Industry Paper Contest Eligibility: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must present the paper at the symposium.

Sunday, 15 June 2025 **17:30–18:00** **Esplanade Ballroom**

RFIC Reception and Symposium Showcase Featuring Systems & Applications Forum and Best Student/Industry Paper Showcase

Systems & Applications Forum Chair: Xiang Gao, Zhejiang University
Student Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center
Industry Chair: Patrick Reynaert, KU Leuven

Join us immediately following the plenary session for the RFIC Reception and Symposium Showcase, supported by the RFIC Symposium's corporate sponsors. This event blends social and technical interactions, featuring food, drinks, and a showcase of RFIC innovation. The reception will spotlight the Student and Industry Paper Award finalists, and Systems and Applications via large electronic posters and live demonstrations. It offers attendees an engaging preview of cutting-edge research. This is a unique opportunity to network, to get a taste of innovative research, and have an early look at select papers scheduled for presentation over the following two days. The list of participating authors and demos was current as of 10 May 2025.

Student Paper Awards Finalists' Showcase/Demonstrations

A 19GHz Circular Polarized 256-Element CMOS Phased-Array Transmitter with 11W Average Power Consumption for LEO Satellite Terminal
[1]Science Tokyo, Japan, [2]Axelspace, Japan
Xiaolin Wang[1], Dongwon You[1], Xi Fu[1], Takeshi Ota[1], Michihiro Ide[1], Sena Kato[1], Jill Mayeda[1], Makoto Higaki[2], Jumpei Sudo[2], Hiroshi Takizawa[2], Masashi Shirakura[2], Takashi Tomura[1], Hiroyuki Sakai[1], Kazuaki Kunihiro[1], Kenichi Okada[1], Atsushi Shirane[1]
RMo1B-1 8:00

A 60-GHz Area-Efficient Coupled Standing-Wave-Oscillators LO Distribution Network for a 240-GHz 2-D Phased-Array
[1]National Taiwan University, Taiwan, [2]University of California, Berkeley, USA
Ying-Han You[1], Pin-Yu Lin[1], Sih-Ying Chen[1], Wei-Yu Lin[2], Jun-Chau Chien[2]
RMo2B-1 10:10

A 40GS/s 8bit Time-Interleaved Time-Domain ADC Featuring SFDR-Enhanced Sample-and-Hold Circuit and Power-Efficient Adaptive Pulse Generator in 28nm CMOS
[1]Xidian University, China, [2]Tsinghua University, China
Chenghao Zhang[1], Maliang Liu[1], Yuan Chang[1], Yihang Yang[1], Yintang Yang[1], Yong Chen[2]
RMo3C-1 13:30

DEMO *An Ultra-Compact Switchless Bidirectional PA-LNA with 8-Shaped Transformer-Based Inter-Stage Matching Networks for W-Band Applications*
SCUT, China
Lingtao Jiang, Lihong Chen, Xianfeng Que, Quan Xue, Yanjie Wang
RMo4B-4 16:40

Topology-Optimized Nonintuitive Multilayered mm-Wave Power Amplifiers
University of Southern California, USA
Vinay Chenna, Hossein Hashemi
RTu2A-1 10:10

Sunday, 15 June 2025 **19:00–21:00** **Rooms 301–304**

3D-Millimeter Wave Integrated Circuit (3D-mmWIC): A Gold-Free 3D-Integration Platform for Scaled RF GaN-on-Si Dielets with Intel 16 Si CMOS

[1]MIT, USA, [2]Georgia Tech, USA, [3]AFRL, USA, [4]Universität der Bundeswehr München, Germany

Pradyot Yadav[1], Jinchen Wang[1], Danish A. Baig[2], Juan Pastrana-Gonzalez[3], John Niroula[1], Patrick Darmawi-Isakandar[1], Ulrich L. Rohde[4], Ahmad Islam[3], Muhannad Bakir[2], Ruonan Han[1], Tomás Palacios[1]

RTu2C-4 11:10

A 28–38GHz Digitally-Assisted Frequency Tripler with Background Calibration in 55nm SiGe BiCMOS

[1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy

D. Lodi Rizzini[1], F. Tesolin[1], M. Rossoni[1], B. Nanino[1], P. Granata[1], R. Moleri[1], A. Mazzanti[2], A.L. Lacaita[1], S.M. Dartizio[1], S. Levantino[1]

RTu3A-3 14:10

DEMO

A Terahertz FMCW Radar with 169-GHz Synthetic Bandwidth and Reconfigurable Polarization in 40-nm CMOS

[1]SCUT, China, [2]CAS, China, [3]UTS, Australia

Aguan Hong[1], Xiang Yi[1], Yanjun Wang[1], Jianmin Hu[2], Zhantao He[1], Guohao He[1], Yang Yang[3], Jiexin Lai[3], Hongli He[1], Lina Su[1], Zhenyu Deng[2], Jingting Xie[2], Shaqi Yang[2], Hongkun Zhou[2], Lingeng Zheng[2], Sicheng He[1], Pei Qin[1], Haoshen Zhu[1]

RTu3B-2 13:50

A Fully Integrated 263-GHz Retro-Backscatter Circuit with 105°/82° Reading Angle and 12-dB Conversion Loss

MIT, USA

Mingran Jia, Jinchen Wang, Jaehong Jung, Xibi Chen, Eunseok Lee, Anantha P. Chandrakasan, Ruonan Han

RTu3B-4 14:30

A 19.4-fs$_{RMS}$ Jitter 0.1-to-44GHz Cryo-CMOS Fractional-N CP-PLL Featuring Automatic Bleed Calibration for Quantum Computing

[1]Xidian University, China, [2]Tsinghua University, China

Jinhai Xiao[1], Yong Chen[2], Ningyi Zhang[1], Rui Liu[1], Yuhao Zhang[1], Peng Luo[1], Maliang Liu[1], Yintang Yang[1], Xiaohua Ma[1], Yue Hao[1]

RTu3C-1 13:30

A 15/30/60-GHz 1TX/4RX Radar Chipset Achieving 6° Angular Resolution Using Frequency Dimension for Virtual Aperture Expansion

[1]UESTC, China, [2]University of Macau, China

Ruilin Liao[1], Haoran Wang[1], Jingzhi Zhang[1], Wei-Han Yu[2], Yue Song[1], Hongyang An[1], Huihua Liu[1], Kai Kang[1]

RTu4A-1 15:40

Industry Paper Awards Finalists' Showcase/Demonstrations

DEMO *D-Band Radio-on-Glass Modules for Spectrally-Efficient FD & FDD Multi-Kilometer Wireless Backhaul Links*
Nokia Bell Labs, USA
Shahriar Shahramian, Michael J. Holyoak, Mustafa Sayginer, Mike Zierdt, Chris Adams, Muhammad Waleed Mansha, Joe Weiner, Ayush Rai, Ismail Kartam, Yves Baeyens
RMo1C-4 9:00

DEMO *A High Power SOI-CMOS WI-FI 6 Front-End Module with Reconfigurable Class-J Power Amplifier*
CEA-Leti, France
Pascal Reynier, Ayssar Serhan, Alexandre Giry
RMo2A-4 11:10

DEMO *A 210–320GHz Power-Combining Distributed Frequency Doubler with Tuned Pre-Amplification in 0.13μm SiGe BiCMOS*
Nokia Bell Labs, USA
Akshay Visweswaran, Yves Baeyens, Mustafa Sayginer, Hernan Castro, Ayush Rai, Shahriar Shahramian
RMo3A-3 14:10

Systems & Applications Forum Showcase/Demonstrations

DEMO *A Fully Integrated Optimal Modulation Bits-to-RF Digital Transmitter Using Time-Interleaved Multi-Subharmonic-Switching DPA*
[1]Boston University, USA, [2]MIT, USA, [3]Northeastern University, USA
Timur Zirtiloglu[1], Arman Tan[1], Basak Ozaydin[2], Ken Duffy[3], Muriel Medard[2], Rabia Tugce Yazicigil[1]
RMo1A-5 9:00

DEMO *An Ultra-Compact and Broadband C-X-Band Wilkinson Power Divider/Combiner Using a Folded Two-Section Mechanism in 65-nm Bulk CMOS Technology*
Beijing Institute of Technology, China
Jiazhi Ying, Zhiqiang Zhao, Yikun Wang, Kaiqiang Zhu, Houjun Sun
RMo2C-5 11:30

DEMO *Fully-Integrated Autonomous K-Band Complex Permittivity Sensor in 22nm FDSOI for Biomedical Body Parameter Monitoring Applications*
Technische Universität Braunschweig, Germany
Adilet Dossanov, Moritz Weißbrich, Alexander Meyer, Liubov Bakhchova, Finn-Niclas Stapelfeldt, Guillermo Payá-Vayá, Vadim Issakov
RTu1C-5 9:20

RFIC Panel Session

Monday, 16 June 2025
12:00–13:30
Room 301

Panel Sessions Chair: Vito Giannini, Uhnder

Low-Earth-Orbit (LEO) Satellite Broadband: Revolutionizing Communication or Just Adding Space Debris?

Panel Organizers and Moderators:
Salvatore Finocchiaro, *Qorvo*
Travis Forbes, *Sandia National Laboratories*

Panelists: **Kenichi Okada**, *Science Tokyo*
Ryan Jennings, *Qorvo*
John Cowles, *Analog Devices*
Adrian Tang, *NASA JPL*
Will Craven, *Maxar Space Infrastructure*

Abstract: Large corporations are investing billions of dollars building thousands of LEO satellites to offer broadband internet services to rural and under-developed areas. In addition, many countries are jumping onto this wagon to secure their own access to the internet as part of a national security policy. On the other hand, the high satellite launch cost, hardware cost, and high monthly subscription fees do not seem to fit the objective of providing broadband access to the general earth population, many of whom are living in poverty. Come join the panel and find out if this is expensive space junk or a revolution in broadband internet access.

RFIC/IMS Joint Panel Session

Tuesday, 17 June 2025
12:00–13:30
Room 301

Panel Sessions Chairs
RFIC: Vito Giannini, Uhnder
IMS: Alfred Riddle, Quanergy Solutions
Austin Chen, Peraso

RFIC Innovation: Has the Field Stalled or Are Researchers Losing Their Way?

Panel Organizers and Moderators:
Subhanshu Gupta, *Washington State University*
Pierluigi Nuzzo, *University of California, Berkeley*
Oren Eliezer, *Samsung*

Panelists: **Naveen Yanduru**, *Axiro*
Lawrence Kushner, *Raytheon Technologies*
Andreia Cathelin, *STMicroelectronics*
Oleh Krutko, *imec*
Ali Niknejad, *University of California, Berkeley*
Dev Shenoy, *Office of the Under Secretary of Defense for Research & Engineering*

Abstract: The past few years have arguably seen a decrease in transformational or disruptive discoveries reported in radio-frequency integrated circuits (RFIC) papers and publications. Does this indicate that RFIC design has reached its maturity, or does it instead suggest a shift of innovations in emerging areas across the boundary of RFIC design, such as the heterogeneous integration of silicon, antennas, and processors using advanced packaging? If so, what should our community look for in publications and what would be considered "publishable work"? Are universities and research institutions addressing the most compelling challenges? And what has been the role of the funding agencies in promoting fundamental research? Our panel of experts, with the audience's participation, will attempt to answer these questions and diagnose the trends seen in RFIC publications and in the field in general.

Student-Industry-Academia RFIChat

Tuesday, 17 June 2025
17:30–19:00
Room **301**

Student Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

Battle of the Bands: Matching Career Path to Frequency of Interest

Moderators:
Emily Naviasky, *IBM T.J. Watson Research Center*
Debopriyo Chowdhury, *Broadcom*

Panelists: **Kimia Ansari**, *Danger Devices*
Jon Comeau, *Otava*
Mark Rodwell, *University of California, Santa Barbara*
Kevin Tien, *IBM T.J. Watson Research Center*
Dean White, *Qorvo*
Rabia Yazicigil Kirby, *Boston University*

Abstract: Experts in different wireless bands battle it out to discuss which frequency bands have the most promise. Which band will have the most jobs and investment in the coming years? Which will have the most interesting research? And what lessons have they learned about how to switch bands if they decide they want to try something new? We'll look at not just 5G and radar but up to THz and optical bands and down to lower frequency bands more relevant for biology and sensing.

RFIC Technical Lecture

Sunday, 15 June 2025
12:00–13:20
Rooms **212–214**

Chair: Steven Turner, BAE Systems

The Art of Metrology – Measurement Techniques & Pitfalls

Speaker: **Shahriar Shahramian**, *Director, Nokia Bell Labs*

Abstract: Advancements in instrumentation and metrology over the past decade have been extraordinary, blurring the boundaries between measurement domains. We rely on these tools as windows into reality, yet the increasing complexity of measurement setups, abstraction of instrument functions, and limited user experience (often) result in erroneous characterizations. Faulty measurements not only risk reputational damage within the scientific community but can also lead to costly failures, potentially causing millions of dollars in losses during productization. This lecture celebrates the ingenuity of modern test equipment while also highlighting their limitations and the challenges of accurate DUT characterization.

About Dr Shahriar Shahramian

Shahriar Shahramian (SM '06) received his Ph.D. degree from University of Toronto in 2010 where he focused on the design of mm-wave data converters and transceivers. Shahriar has been with the Bell Laboratories – Nokia since 2009 and is currently the Lab Leader (Director) of the RFIC & Packaging Research Lab. His research focus includes the design of mm-wave wireless and wireline integrated circuits and systems. Shahriar is a Bell Labs Fellow and leads the design and architecture of several state-of-the-art ASICs for optical coherent and wireless backhaul products. Shahriar has served as the chair mm-Wave & THz subcommittee of IEEE BCICTS & mm-Wave SoCs at IEEE RFIC and member of the technical program committee IEEE ISSCC. He has also served as the guest Editor of the IEEE Journal of Solid-State Circuits (JSSC).

Shahriar has been the recipient of Ontario Graduate Scholarship, University of Toronto Fellowship, and the best paper award at the CSICS Symposium in 2005, 2015 and RFIC Symposium in 2015, 2020, 2022 and ISSCC in 2018. Shahriar is also the recipient of the IEEE MTT Young Engineer Award in 2020. He holds an Adjunct Associate Professor position at Columbia University, has received several teaching awards and is the founder and host of The Signal Path educational video series. Shahriar has also presented short courses and workshops at the IEEE CSICS, BCTM, BCICTS, RFIC/IMS and ISSCC conferences.

Monday, 16 June 2025
8:00–9:20
Room 203
Session RMo1A: Digital Transmitters and Power Amplifiers

Chair: Andreia Cathelin, STMicroelectronics, France
Co-Chair: Xun Luo, UESTC, China

RMo1A-1 8:00

A 71–86GHz 1024QAM Direct-Carrier Phase-Modulating Transmitter with Digital-to-Phase Converters and Constant-Envelope Phasors

Jia Zhou[1], Chao-Jen Tien[1], Christopher Chen[1], Jieqiong Du[1], Jhih-Wei Chen[1], Arhison Bharathan[1], Adrian J. Tang[2], Sai-Wang Tam[3], Mau-Chung Frank Chang[1]; [1]University of California, Los Angeles, USA, [2]Jet Propulsion Laboratory, USA, [3]NXP Semiconductors, USA

Abstract: This paper presents a 71–86GHz 1024QAM Direct-Carrier Phase-Modulating Transmitter (DCPM-TX), solely by using 9-bit digital-to-phase converters based on digitally-controlled artificial dielectric (DiCAD) transmission lines, and constant-envelope phasor combiners. The prototype DCPM-TX delivers 20Gbps at 1024QAM and 25Gbps at 256QAM across 71–86GHz with peak P_{out} over 16dBm while consuming 340mW DC power and 0.675mm^2 core Si area.

RMo1A-2 8:20

A 50–64GHz 21.4dBm, 20.6% SE Intrinsically Linear Digital Cartesian Transmitter with 6.5° System AM-PM Distortion Using Impedance-Compensated RFDAC in 40-nm CMOS

Deshan Tang, Bingzheng Yang, Xun Luo; UESTC, China

Abstract: This paper presents a 50–64GHz intrinsically linear and efficient digital Cartesian transmitter (TX). Such TX mainly consists of an impedance-compensated Cartesian RFDAC, a 4-to-1 linear power combining PA, an IQ generator, and baseband digital circuits. The low power impedance-compensated RFDAC can achieve constant source impedance for high linearity. The power combining PA provides high output power with high efficiency. Asymmetrical interstage matching network between RFDAC and PA can cancel the LO leakage of the RFDAC. The proposed digital Cartesian TX is implemented in conventional 40-nm CMOS technology. The TX demonstrates a peak output power of 21.4dBm and a peak SE of 20.6%. The AM-PM distortion is 6.5°. The INL is less than 0.1 and the DNL is between +1 LSB to -1 LSB. The TX supports 8Gb/s 16-QAM modulated signals and 3Gb/s 64-QAM modulated signals at 60GHz.

RMo1A-4 8:40

An 802.15.4/4z-Compliant UWB All-Digital Transmitter with Hybrid FIR Filtering Achieving 47dBr Sidelobe Suppression

Ziying Huang, Wei Deng, Haikun Jia, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents an IEEE 802.15.4/4z-compliant UWB all-digital transmitter that incorporates hybrid FIR filtering. The reconfigurable and compact hybrid filter consists of a polyphase digital FIR filter and a transformer-combined FIR filter. With the proposed filter, the transmitter achieves 47 dBr sidelobe suppression without any off-chip filters, fully complying with worldwide power spectral density regulations. An on-chip parallel-combining transformer is implemented, which realizes FIR summation while also accomplishing load modulation, thereby enhancing power back-off (PBO) efficiency. Fabricated in 28nm CMOS technology, the transmitter achieves 14.6 dBm peak output power with power added efficiencies (PAEs) of 29% and 25% for 0-dB/6-dB PBOs at 6.5 GHz.

RMo1A-5 9:00

A Fully Integrated Optimal Modulation Bits-to-RF Digital Transmitter Using Time-Interleaved Multi-Subharmonic-Switching DPA

Timur Zirtiloglu[1], Arman Tan[1], Basak Ozaydin[2], Ken Duffy[3], Muriel Medard[2], Rabia Tugce Yazicigil[1]; [1]Boston University, USA, [2]MIT, USA, [3]Northeastern University, USA

Abstract: A fully integrated bits-to-RF transmitter featuring deep power back-off (PBO) enhancements is demonstrated, incorporating a time-interleaved multi-subharmonic-switching digital power amplifier (DPA) and a harmonic-rejection digital-to-phase converter (DPC). This architecture also employs a non-uniform Optimal Modulation (OM) constellation to enhance the transmission error rate. The system implemented in 65 nm CMOS achieves 58.1% peak power-added efficiency (PAE) and 52% peak system efficiency (SE) with 22.7 dBm peak output power, using 2.6 and 1.3 V VDDs. Dynamic measurements of a 64-point OM constellation achieved 23.1% PAE and 19.4% SE at 16.9 dBm average output power, while maintaining an EVM of -29.9 dB at 1.5 GHz carrier frequency. Compared to standard QAM, the proposed OM scheme reduces the bit error rate (BER) by 2.4× and the symbol error rate (SER) by 4.5×, demonstrating its suitability for high-efficiency and reliable signal transmission.

Monday, 16 June 2025
8:00–9:20
Room 205
Session RMo1B:
Reconfigurable Phased Arrays for Satellite Communication
Chair: Kostas Doris, NXP Semiconductors, The Netherlands
Co-Chair: Aarno Pärssinen, University of Oulu, Finland

RMo1B-1 8:00
A 19GHz Circular Polarized 256-Element CMOS Phased-Array Transmitter with 11W Average Power Consumption for LEO Satellite Terminal

Xiaolin Wang[1], Dongwon You[1], Xi Fu[1], Takeshi Ota[1], Michihiro Ide[1], Sena Kato[1], Jill Mayeda[1], Makoto Higaki[2], Jumpei Sudo[2], Hiroshi Takizawa[2], Masashi Shirakura[2], Takashi Tomura[1], Hiroyuki Sakai[1], Kazuaki Kunihiro[1], Kenichi Okada[1], Atsushi Shirane[1]; [1]Science Tokyo, Japan, [2]Axelspace, Japan

Abstract: This article presents a 256-element CMOS active phased-array TX that works at 19GHz for LEO satellite applications. This work proposed a new structure for circular polarization (CP) wave generation that features low power consumption and enables dual-CP waves to be emitted in two directions. Besides, in the measurement, this work proposed a baseband CP cross-polarization interference cancellation technique implemented on an arbitrary waveform generator (AWG), which can improve the dual-CP signal's signal-to-noise ratio (SNR) for 10dB in the error vector magnitude (EVM) measurement. The proposed structure's power consumption is 11W at 56 dBm average output power, which is 29.5% lower than the state-of-the-art. And it consumes 18W at 62 dBm maximum EIRP. The beam steering ability of this work can achieve ±65° with a side lobe level > 10 dB.

RMo1B-2 8:20
A Ka-Band 64-Element 4-Beam Polarization-Reconfigurable Phased Array Based on 65-nm CMOS Tx RFICs for SATCOM

Zixian Ma[1], Xinhong Xie[1], Huiyan Gao[2], Bing Lan[1], Nayu Li[3], Haotian Chen[1], Chunyi Song[3], Zhiwei Xu[1]; [1]Zhejiang University, China, [2]Georgia Tech, USA, [3]Donghai Laboratory, China

Abstract: This paper presents a 27.5–31.5 GHz single-aperture-integrated low-profile 64-element 4-beam phased array, which incorporates 16 Ka-band 8-element 4-beam transmitter front-end ICs in 65-nm CMOS. An 18-layer hybrid-laminated printed circuit board is utilized to enable a high-density design. A slot-fed dual-polarized patch antenna array with decoupling structures is designed to enable polarization (Pol) diversity within a simple geometry. Four sets of onboard 1:16 Wilkinson power dividing networks are realized for high-isolation multi-beam forming. Moreover, cross-Pol cancellation can be achieved by using auxiliary beams. Simulation and measurement results show that the proposed multibeam array can generate four independent beams scanning up to ±60° in the elevation plane. Larger than 50-dBm EIRP at P_{sat} across the frequency band is demonstrated and 4 such arrays can be assembled into a 256-element multibeam system for better scanning and EIRP performance.

RMo1B-3 8:40

An 18-to-50GHz 2-Element Phased-Array CMOS Transceiver with Dual-Resonator T/R Switch with Three-Port Reconfigurable Network and Embedded Tunable Image Rejection Filter

Junlong Gong, Wei Deng, Fuyuan Zhao, Haikun Jia, Weiqi Zheng, Linjun Gu, Shulin Yao, Dongfang Li, Hongliang Wu, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents a 2-element multi-band phased-array transceiver covering FR2-NTN n510/n511/n512 bands and 5G FR2 n257/n258/n259/n260/n261/n262 bands in 65-nm CMOS. Thanks to the proposed dual-resonator T/R switch with three-port reconfigurable network (TP-FRN), the transceiver can operate with two modes and achieves 18-to-50 GHz coverage. The measured peak OP1dB is 16.7 dBm with 27.3 dB S21 at 28 GHz in TX mode and the minimum noise figure (NF) is 7.1 dB with 35 dB S21 and -35.3 dBm IP1dB at 22 GHz in RX mode. Benefiting from the notch filter based tunable image rejection filter, an image-rejection ratio (IMRR) of 28.2-to-64.7 dBc can be achieved for the full path (TX-to-RX). Utilizing the bidirectional mixer (Bi-Mixer) to reduce the power consumption and complexity of the LO phase-shifting based system. Each element front-end (FE) consumes DC power 244 mW from 1 V and 2 V in TX and 53 mW in RX, and the corresponding chip total power consumption is 434 mW and 337 mW. The full path link performance is validated with 400M 64-QAM signals and achieve EVM results better than -25 dB.

RMo1B-5 9:00

An 18–32-GHz Reconfigurable Multi-Beam Phased-Array Transceiver in 65-nm CMOS for Wideband Wireless Communications

Nayu Li[1], Botao Yang[2], Yiwei Liu[2], Zixian Ma[2], Xinhong Xie[2], Huiyan Gao[3], Shaogang Wang[2], Hang Lu[2], Bing Lan[2], Na Yan[4], Qun Jane Gu[3], Chunyi Song[1], Zhiwei Xu[1]; [1]Donghai Laboratory, China, [2]Zhejiang University, China, [3]Georgia Tech, USA, [4]Fudan University, China

Abstract: This paper presents an 18–32-GHz eight-element phased array transceiver (TRX) with four simultaneously reconfigurable beams. It employs a triple-coupled transformer (TCT) embedded T/R switch topology with 2nd harmonic trapping technique to boost power and noise performances of the T/R front ends. A millimeter-wave field-programmable beamforming network (BFN) is proposed to support the bidirectional multi-beam aggregation and regulation. The chip was fabricated in 65-nm CMOS and occupies a 22.88-mm^2 area. It achieves 56% fractional bandwidth, <5.7-dB receive noise figure (NF) at 18–32 GHz, and 18.3/18.8-dBm transmit peak 1-dB gain compression point (P_{1dB})/ saturated output power (P_{sat}). It demonstrates a state-of-the-art number of reconfigurable beams in millimeter-wave RF-beamforming phased array TRXs with decent noise and power performances.

Monday, 16 June 2025
8:00–9:20
Room 207
Session RMo1C: mm-Wave Circuit Advances in Industry
Chair: Travis Forbes, Sandia National Laboratories, USA
Co-Chair: Justin Wu, Amlogic, Taiwan

RMo1C-1 8:00
A 35–65GHz Quadrature-Balanced N-Path Filter with a 0.1–0.9GHz Tunable Bandwidth

S. Yamashita, Y. Tsukui, Y. Kawamura, K. Mori, A. Hirai; Mitsubishi Electric, Japan

Abstract: In this work, we present a 35–65GHz quadrature-balanced N-path filter with a tunable bandwidth of 0.1–0.9 GHz, to realize a flexible direct digital RF modulator in terms of frequency, bandwidth, and modulation in the millimeter-wave band. The proposed filter includes transformer-based balanced quadrature hybrid couplers at the input and output, and core circuits composed of four paths. The filter achieves high-frequency operation by driving four-phases RF signals with 50% duty cycle clock signals. Additionally, it achieves a wide tunable bandwidth using a baseband amplifier that can control its cutoff frequency. The filter, which implemented in a 45-nm CMOS SOI technology, operated from 35 to 65 GHz. It achieved an insertion loss of < 8.7 dB, a return loss of < 10.3 dB, and a noise figure of < 25.7 dB. Moreover, it realized a tunable bandwidth from 0.1 to 0.9 GHz with a power consumption of 10.4–11.8mW and a chip size of 0.96 mm^2. The filter achieved an EVM of -41.5 dB and -32.0 dB for narrowband signals (20 Msps, 1024-QAM) and wideband (800 Msps, 64-QAM) signals, respectively.

RMo1C-2 8:20
A 60GHz Fully Integrated Low-IF CMOS Radar Transceiver with -6dBm IP1dB and -14 to 5dBm Power Control for Ultra-Short-Range Applications

Byeong-Taek Moon[1], Kyunghwan Kim[1], Jaeyeon Jeong[1], Goeun Baek[1], Doyoon Kim[1], Hongkie Lim[1], Junseong Kim[1], Minseob Lee[1], Seungyoon Jung[1], Kyungwoo Yoo[1], Taewoo Yu[1], Taeyeon Kim[1], Sungjoo Kim[1], Yoonki Lee[1], Woncheol Lee[1], Oren Eliezer[2], Hyun-Chul Park[1], Chan-Hong Park[1]; [1]Samsung, Korea, [2]Samsung, USA

Abstract: This work presents a 60 GHz fully integrated low-intermediate frequency (IF) transceiver (TRX) for ultra-short-range frequency-modulated continuous-wave (FMCW) radars, fabricated in a 28-nm FD-SOI CMOS process. This radar TRX includes a front-end, an analog baseband (ABB), a chirp generator, and loopback test circuits. It offers a wide transmitter output power dynamic range from -14 to 5 dBm to optimize the receiver SNR for various scenarios of interest. Additionally, it provides an input 1 dB compression point of -6 dBm to handle strong spillover signals through a high-pass filter-first ABB, and a noise figure of 16.6 dB at 115 kHz IF. The chirp generator based on a two-point modulation demonstrates high linearity of 164 kHz (0.0027%) at a chirp bandwidth of 6 GHz. The compact design occupies a core area of 2.5 mm^2 and consumes DC power of 147 mW, making it suitable for mobile device-based solutions.

RMo1C-3 8:40

A CMOS-Enabled Heterogeneously-Integrated InP HEMT W-Band LNA with 2.8-dB Noise Figure at 7.7-dB Gain and 4.5 mW P_{DC}

Justin J. Kim, Alex Dinkelacker, Nicholas Vong, Michael D. Hodge, Matthew H. Tom, Bennett C. Coy, Mark R. Soler, Christopher Maxey, Florian Herrault, James F. Buckwalter; PseudolithIC, USA

Abstract: We report the integration of an Indium Phosphide (InP) high-electron mobility transistor (HEMT) into an RF CMOS wafer for a W-band (60–90 GHz) low-noise amplifier (LNA). One- and two-stage differential LNAs include CMOS circuits that support RF power detection and temperature sensing. Prototype LNAs are implemented on both a silicon interposer and a 130-nm RF CMOS process for performance comparison. The 1-stage LNA demonstrates a maximum gain of 12.6 dB and the wideband 2-stage LNA has a peak gain of 15.1 dB. The minimum noise figure of the heterogeneous InP-CMOS LNA is 2.8 dB at 7.7-dB gain while consuming 4.5 mW, outperforming CMOS LNAs in W-band.

RMo1C-4 9:00

D-Band Radio-on-Glass Modules for Spectrally-Efficient FD & FDD Multi-Kilometer Wireless Backhaul Links

Shahriar Shahramian, Michael J. Holyoak, Mustafa Sayginer, Mike Zierdt, Chris Adams, Muhammad Waleed Mansha, Joe Weiner, Ayush Rai, Ismail Kartam, Yves Baeyens; Nokia Bell Labs, USA

Abstract: This paper presents a modular, spectrally-efficient D-Band backhaul communication system for full-duplex and frequency-division duplex deployment. The RF modules leverage three highly-integrated D-Band RFICs. The transmitter, receiver & power amplifier chipsets are flip-chipped onto a glass platform for compact and low-loss integration. The transmitter module achieves a saturated output power of 18 dBm and OIP3 of 28 dBm, while the receiver module features a noise figure of 8 dB and an IIP3 of -12 dBm. The point-to-point link is capable of bi-directional data rates above 2×32 Gb/s with 256-QAM modulation at distances reaching 200 meters and supports multi-kilometer wireless links with 16-QAM at 4 GBaud/s.

Monday, 16 June 2025
10:10–11:50
Room 203
Session RMo2A:
High Performance Power Amplifiers and Front-End Modules
Chair: Debopriyo Chowdhury, Broadcom, USA
Co-Chair: Rocco Tam, NXP Semiconductors, USA

RMo2A-1 10:10
A 13-GHz Single Chip Front-End Module with 42% TX PAE and 2.2-dB RX Noise Figure in 0.15-μm E/D-Mode GaAs pHEMT Technology for 6G Wireless Communications

Jungsik Kim, Kyung Pil Jung, Seung Hun Kim, Sungjae Oh, Seong-Kyun Kim, Dongjin Jung, Dae Young Lee; Samsung, Korea

Abstract: This paper presents a novel single-chip RF front-end module (FEM) designed using a 0.15-μm GaAs E/D-mode pHEMT process for 6G upper mid-band applications. The integration of both enhancement-mode (E-mode) and depletion-mode (D-mode) pHEMTs on a single die enables the design to leverage the complementary strengths of these device types. The E-mode pHEMT, with its high gain and low loss, is utilized in the low-noise amplifier (LNA) and the TX/RX SPDT switch, ensuring minimal insertion loss and enhanced noise performance. The D-mode pHEMT, characterized by low gate leakage and high linearity, is employed in the power amplifier (PA) to maximize output power and efficiency. At the design center frequency of 13 GHz, in TX mode, the FEM achieves a gain of 16.9 dB, a P_{sat} of 27.4 dBm, and a PAE of 42%. In RX mode, the FEM achieves a noise figure (NF) of 2.4 dB and a gain of 16.9 dB.

RMo2A-2 10:30
A 13-GHz Harmonic Tuned Asymmetric Doherty Power Amplifier with Compact and Precise Matching Network for 6G Application

Seung Hun Kim, Kyung Pil Jung, Sungjae Oh, Jungsik Kim, Seong-Kyun Kim, Dongjin Jung, Dongki Kim, Dae Young Lee; Samsung, Korea

Abstract: This paper presents a 13-GHz 2-stage asymmetric Doherty power amplifier (DPA) with improved power back-off (PBO) efficiency for 6G application. In order to achieve the improved efficiency and precise impedance matching, the second harmonics are directly terminated and the transistor core is re-modeled along with a routing line. A modified power divider and asymmetric input/output matching networks are designed for 8 dB PBO. The designed PA is implemented in a GaAs pHEMT process with a compact chip size of 3.64×2.34 mm^2. From continuous wave measurement, the PA achieves a maximum output power of 27.6 dBm with a peak and a back-off power-added efficiency (PAE) of 43.0% and 28.3% at 13.2 GHz. From applying a 100 MHz 64-QAM 5G NR signal, the PA shows an average power of 19.6 dBm with a PAE of 28.2% and an ACLR of -44.5 dBc by using DPD.

RMo2A-3 10:50

A Ku-Band 2-Stage Differential Doherty Power Amplifier with Compact Asymmetric Doherty Combiner Based on Virtual Stub in 0.15-μm GaAs pHEMT

Sungjae Oh, Seung Hun Kim, Kyung Pil Jung, Jungsik Kim, Hyeong Jin Kim, Seong-Kyun Kim, Dongjin Jung, Dongki Kim, Dae Young Lee; Samsung, Korea

Abstract: This paper presents Ku-band two-stage symmetric Doherty power amplifier (DPA) that utilizes a virtual stub-based combiner architecture. The new combiner design converts virtual stubs into a differential combiner and allows a carrier amplifier to operate at impedance values more than twice as high as R_{opt} under low power conditions. Therefore, the DPA achieves peak efficiency at back-off power of greater than 6 dB. The fabricated DPA with 0.15-μm GaAs pHEMT delivers a P_{sat} of 28.1–28.7 dBm, linear gain of 13.2–15.7 dB, peak PAE of 39.8–44.0%, and 6 dB back-off PAE of 31.5–36.0% within the frequency bandwidth from 12.4 to 14.0 GHz. The designed DPA also achieves a PAE_{avg} of 27.8–33.1% and adjacent channel leakage power ratio (ACLR) of -25.5{–}{-24.3} dBc at P_{avg} of 20.8–21.3 dBm for a 5G NR signal with 100 MHz bandwidth and PAPR of 7.5 dB peak to average power ratio.

RMo2A-4 11:10

A High Power SOI-CMOS WI-FI 6 Front-End Module with Reconfigurable Class-J Power Amplifier

Pascal Reynier, Ayssar Serhan, Alexandre Giry; CEA-Leti, France

Abstract: This paper presents the design and experimental characterization of a high-power monolithic SOI-CMOS Front End-Module (FEM) supporting Wi-Fi 6 signals over the 5.1 to 5.9GHz frequency band. The FEM includes an SP3T antenna switch, a power amplifier (PA), a low noise amplifier (LNA) with bypass mode, and a digital controller. The LNA achieves 14dB of power gain with less than 2.1dB of noise figure (NF) with 25mW of power consumption. The reconfigurable differential Class-J PA delivers 32dBm of saturated output power (P_{sat}) with 34% of peak PAE. Without DPD, the reconfigurable PA achieves state-of-the art performance with 20/18dBm of linear output power (P_{out}) for an EVM of -34/-37.5dB with 80MHz MCS9/MCS11 signals.

RMo2A-5 11:30

An Ultra-Compact, >17dBm P_{OUT}, >30% PAE, Single Transformer-Based Doherty PA in 28-nm CMOS FD-SOI for 5G FR2 UE AiP Products

Han-Woong Choi, Jongwon Yun, Jaeyeon Jeong, Iljin Lee, Geonho Park, Youngsub Kim, Hongmin Choi, Hyun-Chul Park, Chan-Hong Park; Samsung, Korea

Abstract: An ultra-compact Doherty power amplifier (PA), designed to operate across the n257, n258, and n261 bands for 5G FR2 user equipment (UE) with antenna-in-package (AiP) integration, is implemented in 28-nm CMOS FD-SOI technology. It is optimized for mobile applications, featuring a single amplifier-like footprint that enhances both efficiency and integration, and utilizes a staggered inter-stage matching network to compensate for the gain imbalance caused by the hybrid coupler. It also employs an adaptive bias circuit with a modified operational amplifier to enable wideband operation and achieve high efficiency in power back-off regions. The design is compact, relying solely on lumped components for implementation. The fabricated Doherty PA demonstrates output power above 17 dBm and power-added efficiency (PAE) of 30% when tested with 5G DFT-s QPSK modulation signals.

Monday, 16 June 2025
10:10–11:30
Room 205
Session RMo2B: Advances in VCO Design at Microwave, mm-Wave, and Sub-THz Frequencies
Chair: Alexandre Siligaris, CEA-Leti, France
Co-Chair: Hamidreza Aghasi, University of California, Irvine, USA

RMo2B-1 10:10
A 60-GHz Area-Efficient Coupled Standing-Wave-Oscillators LO Distribution Network for a 240-GHz 2-D Phased-Array

Ying-Han You[1], Pin-Yu Lin[1], Sih-Ying Chen[1], Wei-Yu Lin[2], Jun-Chau Chien[2]; [1]National Taiwan University, Taiwan, [2]University of California, Berkeley, USA

Abstract: This paper presents a 60-GHz LO distribution network for a 240-GHz 2-D phased-array transceiver in TSMC 28-nm CMOS technology. The network couples multiple half-wavelength standing-wave oscillators (C-SWOs) through single-sided transmission-line coupling with layout optimized for area efficiency and unit-element symmetry. The 4×2 array prototype shows the desired synchronicity from the measured phase noise improvement as well as the observation of the injection-pulling spectrum. The tolerance of array to element mismatches are quantified and the phase skews at 0.33~3.28° between pairs of SWOs are measured. Per element power consumption is 15 mW.

RMo2B-2 10:30
A Compact 190GHz Push-Push Colpitts VCO in 130-nm BiCMOS with 3.5%-DC-to-RF Efficiency and 3.9-dBm Peak Output Power

Hanlin Yang[1], Hao He[1], Jianbo Huang[1], Yi Liu[2], Zhou Shu[1], Howard Cam Luong[2], Kevin Chai[3], Yongxin Guo[4]; [1]NUS, Singapore, [2]HKUST, China, [3]A*STAR, Singapore, [4]CityUHK, China

Abstract: A compact high-DC-to-RF-efficiency push-push Colpitts voltage-controlled oscillator (VCO) operating at 190 GHz is proposed. By introducing a second-harmonic quarter-wavelength open-circuited transmission line (QOTL) at the base of the bipolar junction transistor (BJT), more RF power is delivered to the load, and both output power and DC-to-RF efficiency are enhanced. Fabricated in a 130-nm SiGe BiCMOS process, the VCO prototype driving a 50-Ω load without additional buffer measures a frequency range from 185.3 GHz to 192.4 GHz while achieving 3.9-dBm peak output power and 3.5% DC-to-RF efficiency and occupying a core area of 180×185 μm^2.

RMo2B-3 10:50

An Image-Reused Phase-Tuning mm-Wave QVCO with a FoM_T of -204 dBc/Hz

Yue Zhu[1], Yuri Lu[1], Chunqi Shi[1], Leilei Huang[1], Hao Deng[2], Jinghong Chen[2], Runxi Zhang[1]; [1]East China Normal University, China, [2]University of Houston, USA

Abstract: This paper presents an image-reused phase tuning technique (IPTT) for millimeter-wave (mm-wave) quadrature voltage-controlled oscillators (QVCOs). The phase shifter addresses the -45°–45° phase rotation limitation, extending it to 135°–225°. This enhancement extends the QVCO tuning range without deteriorating phase noise. To facilitate the expanded phase tuning range, a transformer-based fourth-order resonator providing bimodal impedance is employed in the proposed QVCO. The bimodal impedance ensures intra-band monotonicity and inter-band continuity, optimizing the overall tuning range. Mismatch mitigation and PLL integration of the proposed QVCO are also discussed. A prototype QVCO, operating from 31.6 to 49.2 GHz, is fabricated in a 40-nm CMOS process. Measurement results show that the QVCO consumes 10 mW of power and achieves a tuning range of 44% and phase noise of -129 dBc/Hz at 10-MHz offset. This leads to a figure of merit (FoM_T) of -204 dBc/Hz at a 10-MHz offset.

RMo2B-4 11:10

A 580-μW 13.8–16.2-GHz Series-Tank-Assisted Transformer-Based Oscillator Achieving -188 dBc/Hz FoM and 50MHz/V Supply Pushing

Sayan Kumar, Sumit Dash, Robert Bogdan Staszewski, Teerachot Siriburanon; University College Dublin, Ireland

Abstract: This paper proposes a sub-mW LC-oscillator operating from 13.8 to 16.2 GHz. The proposed oscillator employs a self-biased inverter-based complementary G_m-cell with series capacitors that shield the main tank from the supply-dependent capacitance of the G_m-cell devices. This reduces the sensitivity to voltage supply variations. Additionally, the series capacitors form an auxiliary series tank along with the main parallel LC tank. As a result, it forms a complex tank with an enhanced voltage swing, thereby lowering phase noise (PN). Fabricated in 28nm CMOS, the proposed oscillator achieves -121 dBc/Hz at 10MHz offset from a 14 GHz carrier frequency. This results in an FoM of -188 dBc/Hz. The proposed oscillator exhibits a low supply pushing of 50 MHz/V and a flicker noise corner <400 kHz across the tuning range (TR). The proposed work achieves a record-low power consumption of 580 μW in the >10 GHz category.

Monday, 16 June 2025
10:10–11:50
Room 207
Session RMo2C: mm-Wave Building Blocks and Components
Chair: Mohamed Elkhouly, Broadcom, USA
Co-Chair: Giuseppe Gramegna, imec, Belgium

RMo2C-1 10:10
A 28–40GHz 6-Bit Variable Gain Phase Shifter with <0.4°/<0.31dB PS RMS Phase/Gain Errors and 31.5-dB Gain Tuning Range

Tao Zhang, Haohui Chen, Depeng Sun, Lisheng Chen, Ruixue Ding, Shubin Liu, Zhangming Zhu; Xidian University, China

Abstract: This paper presents a 28–40 GHz 6-bit variable gain phase shifter (VGPS) with 31.5-dB tuning range and low RMS phase/gain errors in 65-nm CMOS for millimeter-wave (mm-Wave) applications. A novel VGPS architecture based on switchless cascode variable gain amplifiers (VGAs) and a gain/quadrant-control IQ generator is proposed. To minimize device parasitics and input/output (I/O) impedance variations across different phase states, a switchless cascode VGA structure is employed to weight the I and Q signals, achieving low RMS phase/gain errors with 5 mW power consumption. In addition, cascode current-canceling (CCC) VGAs are integrated and co-designed with IQ generator, providing a 31.5-dB gain tuning range and wideband balanced IQ signals. Fabricated in 65-nm CMOS process, the proposed VGPS occupies a core chip area of 0.57 mm^2. Measurements show the VGPS achieves 6-bit phase control with -0.3 dB peak gain, <0.4° RMS phase error, and <0.31 dB RMS gain error across 28–40 GHz. It also provides 6-bit 31.5 dB gain control with <0.35 dB RMS gain error across 28–40 GHz. Furthermore, the measured average input 1-dB gain compression point (IP_{1dB}) is >-1.1 dBm.

RMo2C-2 10:30
A V-Band Transmitter Front-End IC for Phased-Array FMCW Radar with Impedance-Invariant Variable-Gain Phase Shifter

Mingyu Lee[1], Subin Lim[1], Euijin Oh[1], Goo-Han Ko[2], Si-Keuk Ryu[2], Eun-Taek Sung[3], Donghyun Baek[2], Jong-Ryul Yang[4], Seungchan Lee[1], Jinseok Park[1]; [1]Chonnam National University, Korea, [2]Chung-Ang University, Korea, [3]ETRI, Korea, [4]Konkuk University, Korea

Abstract: This paper presents a V-band transmitter front-end (TXFE) IC for phased-array frequency-modulated continuous wave (FMCW) radar, which includes a variable-gain phase shifter and medium-output power amplifier (PA). For accurate phase and gain control, the phase shifter employs an impedance-invariant technique by combining two vectors which one is always 90° ahead than the other. Therefore, variation of the current flowing each I and Q amplifier in vector generator are compensated during phase and gain control. The PA comprises four stages with three cascode pre-amplifiers featuring cross-coupled capacitors. The proposed TXFE IC was fabricated in 65-nm bulk CMOS process with a core size of 0.81 mm^2. The measured RMS phase error of 6-bit phase resolution was 2.15°, and the RMS gain error of 5-bit gain states for a 16-dB dynamic range was 0.43 dB at 58.5 GHz. The measured peak gain and P_{sat} were 28 dB and 11.9 dBm, respectively, at 58.5 GHz and 60 GHz.

RMo2C-3 10:50

A Compact 25–32GHz Frequency Doubler with up to 32% Efficiency and >39 dBc Harmonic Rejection in 22nm FDSOI

Mohammed Helal, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: A frequency doubler with state-of-the-art power efficiency, high harmonic rejection, and a compact footprint is presented. The doubler utilizes a push-push architecture with a three-coil transformer load that creates a notch response, rejecting the 4th harmonic. This enables pushing the doubler to higher output power, enhancing its efficiency. The doubler incorporates an input balun for fundamental suppression, thus exhibiting high rejection to all undesired harmonics. The design is implemented in 22nm FDSOI with a core area of 0.054 mm^2. The doubler achieves a measured output power of 4–6 dBm at an output frequency of 25–32 GHz with an input power of 8 dBm. The measured 1st and 4th harmonic rejection ratios are greater than 42 and 39 dBc, respectively. The measured DC power is 11–15 mW, yielding an efficiency of 17–32%. To the authors' knowledge, this is the highest reported efficiency for a frequency doubler implemented in a CMOS technology.

RMo2C-4 11:10

A 24–31GHz Compact Low-Power Complex Impedance Sensor for Beamforming Transmitters in 22nm FD-SOI

Xuepu Wu[1], Yang Zhang[1], Giovanni Mangraviti[1], Rana ElKashlan[1], Dries Peumans[2], Piet Wambacq[1]; [1]imec, Belgium, [2]Vrije Universiteit Brussel, Belgium

Abstract: We present a complex impedance sensor to measure the impedance variations at the output of a (phased-array) transmitter (TX) operating around 28GHz. Based on complex voltage sensing of the output balun in a transmitter, the envelope detectors and injection-locked ring oscillators (ILRO) split the amplitude and phase sensing of voltages for computing the complex impedance. With a bandwidth spanning from 24GHz to 31GHz and an input power dynamic range of 7dB, this circuit can sense reflection coefficients up to 0.74 with a maximum magnitude error of 0.14 and a maximum phase error of 12.8°. It consumes 8mW of power and occupies only 0.0043mm^2.

RMo2C-5 11:30

An Ultra-Compact and Broadband C-X-Band Wilkinson Power Divider/ Combiner Using a Folded Two-Section Mechanism in 65-nm Bulk CMOS Technology

Jiazhi Ying, Zhiqiang Zhao, Yikun Wang, Kaiqiang Zhu, Houjun Sun; Beijing Institute of Technology, China

Abstract: This paper presents an ultra-compact and broadband C-X-band Wilkinson power divider/ combiner comprised of two power combining 1:4 units, respectively for IF and LO frequency. To overcome the isolation bandwidth constraints, two sections of $\lambda/4$ transmission lines are employed and innovatively realized within one inductor footprint by using a magnetic coupling self-canceling technique. A novel shielding topology is adopted to achieve IF/LO isolation enhancement and amplitude/phase uniformity simultaneously. The prototype is implemented with core sizes of 0.069/0.059 mm^2 for IF/LO networks, respectively. Measurement results show insertion loss within 3.2/3.4 dB, isolation greater than 24.9/26.0 dB across IF (6–10 GHz)/LO (8–12 GHz) frequency range, and over 60-dB isolation between IF and LO crossover branches. To the best of our knowledge, this design achieves the most compact normalized core size, competitive fractional isolation bandwidth, and the highest branch isolation among the published works.

Monday, 16 June 2025
13:30–14:50
Room 203
Session RMo3A: Advanced Frequency Generation in Sub-10nm CMOS and SiGe BiCMOS

Chair: Bichoy Bahr, Texas Instruments, USA
Co-Chair: Steven Turner, BAE Systems, USA

RMo3A-1 13:30

A 13.5 to 23GHz Compact PLL Based on a 0.006mm² Transformer-Based Dual-Resonator Tuned LC VCO in 5nm CMOS

Armagan Dascurcu, Bodhisatwa Sadhu, Herschel Ainspan, Gary Kurtzman, John Borkenhagen, Zheng Xu, Jim Strom; IBM, USA

Abstract: A transformer-based, dual-resonator tuning technique is introduced to enable a wide frequency tuning range LC VCO while occupying a compact area. The VCO, implemented in 5nm CMOS, overcomes the inductor area constraints imposed by tight bump pitches in scaled CMOS. The VCO is integrated into an integer-N PLL with a measured tuning range of 52% (13.5 to 23 GHz) and an RMS jitter of <260fs (f_0/1667–50GHz). The VCO's compact area of 0.006mm² is the smallest among LC VCOs with a comparable tuning range.

RMo3A-2 13:50

A 16–22GHz Fractional-N PLL in 8nm FinFET with 68 fs_{rms} Jitter

Wanghua Wu[1], Zhiyu Chen[1], Kyumin Kwon[1], Suoping Hu[1], Pak-Kim Lau[1], Changhun Song[1], Ali Binaie[1], Santosh Kumpatla[1], Juyeop Kim[1], Jeiyoung Lee[2], Chih-Wei Yao[1], Sangwon Son[1], Joonhoi Hur[1]; [1]Samsung, USA, [2]Samsung, Korea

Abstract: We present a 16–22 GHz low-jitter fractional-N PLL for 5G mm-wave mobile application. It features an integrated low-cost crystal oscillator (XO) reference at 153.6 MHz and a reconfigurable 19-GHz quad-core VCO and achieves 68-fs rms jitter in fractional-N mode, integrated from 10 kHz to 10 MHz. To minimize inband phase noise (PN), a 153.6-MHz on-chip XO followed by a frequency doubler is employed. The XO achieves -160 dBc/Hz at 1-MHz frequency offset and consumes 4.5 mW. Using a doubler not only reduces the PN amplification of the phase detector and the feedback divider, but also suppresses the PLL inband PN due to the flicker noise of the reference clock buffer. The reconfigurable multi-core VCO occupies the same footprint as a conventional quad-core oscillator and can be programmed to single-core, dual-core, and quad-core three modes to trade off power consumption for PN. Implemented in 8-nm FinFET, the PLL occupies 0.38 mm² and achieves an rms jitter of 120 fs at 18 GHz while consuming 16 mW at single-core VCO mode. Its rms jitter reduces to 88 fs and 68 fs at dual-core and quad-core VCO modes, respectively.

RMo3A-3 14:10

A 210–320GHz Power-Combining Distributed Frequency Doubler with Tuned Pre-Amplification in 0.13μm SiGe BiCMOS

Akshay Visweswaran, Yves Baeyens, Mustafa Sayginer, Hernan Castro, Ayush Rai, Shahriar Shahramian; Nokia Bell Labs, USA

Abstract: The paper presents the theory and design of a broadband distributed frequency doubler operating across 210–320GHz. We introduce power combining within the distributed structure, with two sets of distributed doublers driving a common transmission-line load. Passband characteristics over the desired frequency range are introduced with stagger-tuned narrowband pre-amplifier stages employed in each unit cell of the 15-stage doubler, which extends flat output power beyond fT. The 3V prototype in 0.13μm SiGe BiCMOS (f_T/f_{MAX} 300/450GHz) delivers 3.6dBm power at 300GHz to a 50Ω load, with a conversion gain of 13.6dB. It is the highest reported output power at 300GHz for Silicon and InP-HBT based frequency multipliers.

RMo3A-4 14:30

Design Technology Co-Optimization for RF/mmWave Circuits with Circuit Under Inductor (CUI) in FinFET CMOS Technologies

Hsieh-Hung Hsieh[1], Wei-Ling Chang[1], Kai-Chun Chang[1], Wen-Sheng Chen[1], Yen-Jen Chen[1], Tzu-Jin Yeh[1], Shenggao Li[2], Shih-Hsien Yang[1], Hua-Chou Tseng[1], Cho-Ying Lu[1], Hwa-Yu Yang[1], Guo-Wei Huang[3]; [1]TSMC, Taiwan, [2]TSMC, USA, [3]NARLabs-TSRI, Taiwan

Abstract: This paper presents an approach, circuit under inductor (CUI), to reduce chip area as a solution for design technology co-optimization (DTCO) in sub-10-GHz RF and millimeter-wave (mmWave) applications. With the use of CUI and dual ultra-thick metal (DUTM) scheme as well as design guidelines, a smaller footprint can be obtained for a 2.4-GHz LC-VCO in 6-nm CMOS and a 28-GHz PA in 16-nm CMOS while the RF performance is less impacted compared to the reference case. For the 2.4-GHz LC-VCO with the CUI, the measured phase noise at a 1-MHz offset and tuning range are -117.3 dBc/Hz and 21%, respectively. As for the 28-GHz PA with the CUI, the P_{sat} of 19.7 dBm and the peak PAE of 38.1% are achieved. The measured results successfully manifest the feasibility of the proposed CUI.

Monday, 16 June 2025
13:30–14:50
Room 205
Session RMo3B: mm-Wave Transmitter and Receiver Front-Ends
Chair: Swaminathan Sankaran, Texas Instruments, USA
Co-Chair: Shahriar Shahramian, Nokia Bell Labs, USA

RMo3B-1 13:30
A 15–50GHz LNA with 2.4dB NF and 25.4±1.4dB Gain in 0.15μm GaAs pHEMT Process

Nengyuan Zhong[1], Yao Li[1], Shiwei Hu[1], Chenhao Gao[1], Xiang Wang[2], Yanjie Wang[1]; [1]SCUT, China, [2]NJUST, China

Abstract: A four-stage ultra-wideband 15–50 GHz LNA in 0.15 μm GaAs pHEMT process is presented in this paper. A RLC feedback with a virtual ground capacitance (RLC & VGC) topology used in current-reuse structure is proposed, which enables flexible adjustment of both low- and high-frequency gain. Moreover, a RC parallel circuit and LR series circuit are exploited to improve gain flatness. Several bandwidth extension techniques are employed to expand the bandwidth up to 50 GHz. A prototype of a four-stage common-source (CS) LNA with the proposed techniques is designed and fabricated in a 0.15 μm GaAs pHEMT process. Measurement results show a noise figure (NF) of 2.4 dB, a gain exceed 24 dB with the gain flatness of ±1.4 dB. Due to the utilization of the self-biasing technology, the chip consumes a DC power of 168 mW with a single DC supply of +4V. The amplifier achieves good linearity, with an output 1 dB compression point (OP_{1dB}) of 13.4 dBm and a third-order intercept point (OIP3) of 23 dBm.

RMo3B-2 13:50
Design of 22.6–29.5/30.4–43.5GHz Dual-Band Low Power LNA with 2.6–3.8dB NF for Millimeter-Wave 5G Applications in 28-nm CMOS

Haitao Lin[1], Li Gao[1], Xinyang Liu[2], Xiu Yin Zhang[1]; [1]SCUT, China, [2]Sanechips Technology, China

Abstract: This paper presents a reconfigurable dual-band low power low noise amplifier (LNA) for 5G millimeter-wave (mm-Wave) applications. In the proposed LNA, a two-stage amplifier is designed with wideband input matching network. Compact switchable triple coupled transformer (STCT) is applied to the interstage matching network. The STCT can adjust the transmission poles by tuning the coupling of inductors to achieve reconfigurable operating bands. Additionally, the STCT generates a transmission zero in the low band mode, resulting in a high image rejection ratio. Fabricated in TSMC 28-nm CMOS process, the proposed LNA occupies a compact core size of only 0.09 mm^2. The measured results show that the low band has a peak gain of 19.7 dB with a 3 dB bandwidth of 22.6–29.5 GHz and the high band has a peak gain of 19.2 dB with a 3 dB bandwidth of 30.4–43.5 GHz. The LNA achieves a minimum NF of 2.6/2.9 dB, and IP1dB of -18.7/-18.3 dBm in the low/high band mode. The total DC power consumption is only 10 mW.

RMo3B-3 14:10

A 50–68GHz IF Absorptive Receiver with 8-GHz IF-Bandwidth Supporting 16-Channel Carrier-Aggregation and 12Gbps-64QAM Modulation for 5G NR FR2-2 Application

Aoran Han, Qingxian Li, Jie Zhou, Xun Luo; UESTC, China

Abstract: This paper presents a 50–68 GHz IF absorptive receiver. The intermodulation interference caused by IF signal reflection to the mixer is mitigated through absorptive IF amplifier, enabling a wideband and flattened IF bandwidth. The wideband optimal noise performance and input matching of the LNA are achieved using a defectively-coupled transformer. Verified in a conventional 40-nm bulk CMOS technology, the proposed receiver demonstrates a 26.2 dB conversion gain and a gain tuning range of 13 dB with an 8 GHz IF bandwidth. I/Q calibration-free operation is achieved with 5-dB BW, with an image rejection ratio (IRR) ranging from 28 to 60.5dB. Benefited from the IF absorption technique, the proposed RX supports 4Gbps-256QAM modulation, 9.6Gbps-64QAM 16-channel and 12Gbps-64QAM 8-channel carrier aggregation, which is attractive for 5G NR FR2-2 applications.

RMo3B-4 14:30

A 22-to-50GHz Bi-Directional Beamforming CMOS Front-End with Distributed Impedance Reshaping Technique for 5G NR FR2 Applications

Weiqi Zheng, Wei Deng, Junlong Gong, Haikun Jia, Dongze Li, Hongliang Wu, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents an ultra-wideband beamforming front-end in 65nm CMOS for n257/n258/n259/n260/n261/n262 5G FR2 applications. Multiple impedance reshaping techniques are introduced to enable a continuous ultra-wideband design. To address the challenges of broadband matching and the losses introduced by matching elements, an implicit distributed inductor matching method is proposed to compress the impedance trace for low-noise amplifier (LNA) input matching. A bidirectional synergized transformer-based reflection-type phase shifter (STB-RTPS) is demonstrated, achieving broadband phase shifting. Over the frequency band of 22.1–49.8 GHz, the RX front-end achieves a measured RX noise figure (NF) of 5.2–6.3 dB. In TX mode, over the bandwidth of 22.8–49.3 GHz, the design achieves a saturated output power of 18.61 dBm and an output 1dB compression point of 16.76 dBm. Both TX and RX offer 6-bit phase control and 4-bit amplitude control, achieving an in-band EVM of < -26 dB for 400 Msym/s 64QAM wireless communication.

Monday, 16 June 2025
13:30–15:10
Room 207
Session RMo3C: High Speed and Domain Specific Data Converters
Chair: Emily Naviasky, IBM T.J. Watson Research Center, USA
Co-Chair: Antoine Frappé, Université de Lille, France

RMo3C-1 13:30
A 40GS/s 8bit Time-Interleaved Time-Domain ADC Featuring SFDR-Enhanced Sample-and-Hold Circuit and Power-Efficient Adaptive Pulse Generator in 28nm CMOS

Chenghao Zhang[1], Maliang Liu[1], Yuan Chang[1], Yihang Yang[1], Yintang Yang[1], Yong Chen[2]; [1]Xidian University, China, [2]Tsinghua University, China

Abstract: This paper reports a 40 GS/s 8b Time-Interleaved (TI) time-domain gated-ring-oscillator analog-to-digital converter (GRO-ADC). The smallest interleaving number of 32 is achieved with a single 8-bit GRO-ADC operating at 1.25 GS/s in 28 nm CMOS, leading to a low routing and front-end complexity between recently published works. An adaptive-working pulse generator eliminates the previous topology's unnecessary pulse and minimizes the pulse generation power. The sampling front-end employs a linearity-enhanced boosted switch that supports short-time and high input voltage sampling, as well as a switched class-AB output buffer for low-power driving and nonlinear coupling suppression at high input frequency. Also, the multi-channel interleaved architecture also frees the GRO-ADC from single-channel calibration and reduces the sub-ADC design complexity. The TI GRO-ADC prototype is fabricated in a 28 nm CMOS process with an active area of 0.015 mm^2. Under a maximum input swing of 0.8-V_{ppd}, it scores a measured peak SNDR of 40.3 dB and SFDR of 56 dB, respectively, at the conversion rate of 40 GS/s, along with the Walden figures of merit (FoMw) of 41.6 fJ/conversion step.

RMo3C-2 13:50
A 12-Bit 6-GS/s Time-Interleaved SAR ADC with On-Chip Mismatch Calibration in 28nm CMOS Technology

Sebastian Linnhoff[1], Frowin Buballa[1], Michael Reinhold[2], Rene Spanl[2], Erik Sippel[3], Friedel Gerfers[1]; [1]Technische Universität Berlin, Germany, [2]Robert Bosch, Germany, [3]FAU Erlangen-Nürnberg, Germany

Abstract: This article presents a wideband 12 bit 6 GS/s time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC) implemented in a 28nm CMOS technology addressing FMCW based radar, as well as instrumentation applications demanding excellent ADC linearity. The proposed ADC makes use of a wideband front-end featuring two subsequent ranks of pseudo-differential push-pull input buffers to distribute the input signal to 19 12 bit 375 MS/s SAR-ADC lanes. Each SAR-ADC lane takes advantage of a sub-2 radix split CDAC with a 9% overrange, a distributed sample switch implemented as an isolating T-switch and a fully loop-unrolled comparator architecture. Furthermore, the ADC system features an on-chip digital calibration engine to correct inter-channel mismatch effects such as gain, offset and sample-phase

mismatch. Measurement results reveal an SNDR and SFDR of 50 dB and 62.8 dBc respectively for a $1V_{ppd}$ single tone sine wave input signal across the entire 3 GHz Nyquist-band with an HD3 of 72.7 dBc at Nyquist. The complete ADC system draws 2.5W from four power supplies (1V, 1.8V, 2.5V and -1.3V), resulting in a Schreier Figure-of-Merit (FoM_s) of 145/141 dB for low and high-frequency inputs respectively.

RMo3C-3 14:10

Mostly Digital, Calibration-Free, Band-Pass Delta-Sigma Modulator Using Dual Time-Interleaved Noise-Shaping SAR ADCs

Matt Kinsinger, Anoop Bengaluru, Jia-Ching Chuang, Sumukh Bhanushali, Arindam Sanyal; Arizona State University, USA

Abstract: This work presents a highly digital, band-pass delta-sigma modulator (BPDSM) using dual, time-interleaved (TI) noise-shaping successive approximation register (NS-SAR) analog-to-digital converters (ADCs). Use of TI, low-pass DSM shifts digitization from intermediate frequency (IF) to baseband, and increases energy-efficiency as well as relaxes the realization of a sharp noise-transfer function (NTF). However, time-interleaving results in spurs that appear as images in the signal band and necessitates mismatch calibration. The proposed technique uses dual BPDSMs operating at different IFs to deterministically push all interleaving spurs out of the signal band without any calibration. Third-harmonic spurs fall out of band if the IF BW is less than Fs/10. A prototype test-chip fabricated in 65nm uses dual 4× TI BPDSMs and achieves 66.7dB SNDR in 2MHz bandwidth at 20MHz IF while consuming 1.36mW.

RMo3C-4 14:30

Circuits-Informed Machine Learning Technique for Blind Open-Loop Digital Calibration of SAR ADC

Sumukh Bhanushali[1], Debnath Maiti[1], Phaneendra Bikkina[2], Esko Mikkola[2], Arindam Sanyal[1]; [1]Arizona State University, USA, [2]Alphacore, USA

Abstract: This work presents a supervised machine-learning (ML) approach for blind digital calibration of SAR ADCs without requiring prior knowledge of errors. A 2-layer neural network learns the difference between outputs of a high-speed ADC and a low-speed, reference ADC when their sampling instants align and uses this knowledge to estimate and subtract errors in high-speed ADC at the back-end. The proposed ML-calibration improves SFDR of a 28nm, 12-bit, 84MHz ADC by >38dB while consuming 25.8fJ/conversion-step.

RMo3C-5 14:50

A 17mW 8-Element 2-Beam Hybrid Slepian Beamforming Receiver with SAR-ADC-Based Charge-Domain Multiply and Accumulation

Zhengqi Xu[1], Zhiyuan Zhao[1], Michael A. Laun[1], Coleman DeLude[2], Justin Romberg[2], Michael P. Flynn[1]; [1]University of Michigan, USA, [2]Georgia Tech, USA

Abstract: True-time-delay (TTD) beamformers are very desirable for wideband wireless communication but existing approaches suffer from high hardware costs especially for large-scale arrays. In this work, a hybrid Slepian beamforming receive architecture reduces the power and area costs for TTD implementations. The approach reduces the number of ADCs and delays for TTD but retains the digital-delay advantage of digital beamforming. The proposed architecture employs charge-domain complex multiply and accumulate (MAC) inside SAR ADCs. The beamformer supports eight IF inputs and two simultaneous baseband outputs. Fabricated in 28 nm CMOS, the prototype consumes only 17 mW and occupies 0.035 mm^2. The measured error vector magnitudes (EVMs) are better than -30 dB for quadrature amplitude modulation (QAM)-16 and QAM-256.

Monday, 16 June 2025
15:40–17:20
Room 203
Session RMo4A: Transmitters Beyond 100GHz
Chair: Aritra Banerjee, University of Illinois at Chicago, USA
Co-Chair: Andrea Mazzanti, Università di Pavia, Italy

RMo4A-1 15:40
A D-Band Direct-Modulation 64-QAM Transmitter with On-Chip Digital Calibration in 16nm FinFET Technology

Runzhou Chen[1], Hao-Yu Chien[1], Chao-Jen Tien[1], Hong-Shen Chen[2], Hsieh-Hung Hsieh[2], Tzu-Jin Yeh[2], Mau-Chung Frank Chang[1]; [1]University of California, Los Angeles, USA, [2]TSMC, Taiwan

Abstract: This paper presents a D-band direct-digital transmitter that employs RF-DACs to perform modulation in the RF domain. It achieves 64-QAM with a maximum data rate of 48 Gb/s and an EVM of -23.8 dB. Meanwhile, a switch-based variable gain amplifier (VGA) and a digitally controlled artificial dielectric (DiCAD) are implemented on each of the I/Q paths to achieve refined on-chip amplitude and phase calibration. The transmitter is manufactured in 16nm FinFET technology with an integrated frequency octupler and a power amplifier. The transmitter has a 3-dB bandwidth of 129–146 GHz, a P_{sat} of 12.2 dBm, and a total DC power consumption of 235 mW.

RMo4A-2 16:00
A 110 to 122-GHz Four-Channel Oversampling Digital-to-Phase Transmitter for Scalable, Energy-Efficient Arrays

Justin J. Kim[1], Alex Dinkelacker[1], Jeff Shih-Chieh Chien[2], James F. Buckwalter[1]; [1]University of California, Santa Barbara, USA, [2]Samsung, USA

Abstract: An oversampling digital-to-phase (ODP) transmitter (TX) is proposed based on scaling independent channels consisting of a multiplier chain (XN), two-bit quadrature phase shifter (PS), and a power amplifier (PA). Each channel operates under constant envelope conditions for maximum power efficiency. Direct digital modulation is applied to the RF carrier of each channel. The prototype array, fabricated in a 22-nm FD-SOI CMOS technology, consists of four channels operating over a 3-dB bandwidth from 110 to 122 GHz. The CMOS chip is flip-chip mounted onto a Low-Temperature Co-fired Ceramic (LTCC) interposer with integrated Vivaldi antennas and wire-bonded to a PCB. The 4-element array exhibits a measured peak effective isotropic radiated power (EIRP) of 26.6 dBm with ±25° scanning range. With just two bits of phase control per channel, the proposed array is able to achieve 8-PSK modulation at 1.5 Gbps, 1 dB power back off, and 12.3% EVM. Despite no explicit amplitude modulation, 8-APSK modulation is achieved at 150 Mbps, 3-dB power back off, and 12.8% EVM. The proposed direct modulation scheme is a scalable millimeter-wave (mm-wave) TX architecture for digital modulation and beamsteering.

RMo4A-3 16:20

A 45Gb/s D-Band Hybrid Star-QAM-OOK Transmitter Using a Quad-Harmonic Modulator with Constant Impedance Balanced Architecture in 90nm SiGe BiCMOS

Haoling Li, Najme Ebrahimi; Northeastern University, USA

Abstract: This work presents a D-band reconfigurable Quadrature Second Harmonic modulator. The proposed modulator features a quadrature frequency doubler with integrated shunt switches at the common-emitter node, and with balanced switching mechanism inspired by photonic interferometer, enabling reconfigurable 4-APSK (Star QAM) and OOK modulation. The design maintains a nearly constant input and output impedance across all modulation states, minimizing Error Vector Magnitude (EVM) variation over the bandwidth and enabling robust performance for next-generation short-range high-speed connectivity. Developed using a 90 nm SiGe BiCMOS process and heterogeneously integrated with a fused silica antenna, the modulator achieves a data rate of up to 45 Gb/s with EVM better than -19 dB and less than ± 1.6 dB variation across a 20% bandwidth spanning 132 GHz to 158 GHz. The chip occupies an area of 1.1 mm×1.75 mm, consumes an average P_{DC} of 100 mW, and delivers -3.6 dBm P_{sat} with a spectral efficiency of 3.3 pJ/bit.

RMo4A-4 16:40

A 200-GHz Phased Array Transmitter with Element-Level Scanning Antenna for ±45° Scanning Range with 0.71λ_0 Antenna Pitch

Si-Yuan Tang, Peigen Zhou, Rui Zhou, Rui Zhang, Zongxiang Wang, Dawei Tang, Long Wang, Xiaoyue Xia, Wentao Zhu, Jirui Li, Jinben Li, Pinpin Yan, Hao Gao, Jixin Chen, Wei Hong; Southeast University, China

Abstract: This paper presents a compact 200 GHz SiGe-based two-channel phased array with an on-chip integrated multiplier-by-6 driver chain. Each channel is composed of an on-chip element-level scanning antenna (ELSA), two frequency doublers, two driver amplifiers (DA), two 6-bit phase shifters (PS), and two 5-bit variable gain amplifiers (VGA). By switching the state of the two PSs in a channel, the radiation pattern of the ELSA could be flexibly controlled. Therefore, even if ELSAs are integrated in a large-pitch phased array, the wide scanning range could be ensured by switching its radiation pattern for simultaneous main lobe enhancement and grating lobe suppression. The measured peak output power of the frequency doubler is 5.6 dBm, with a 3-dB bandwidth from 184 to 213 GHz. At 0.71 λ_0 channel spacing, the two-channel phased array demonstrates a measured EIRP of 13.5 dBm, while a wide scanning range of ±45° is obtained.

RMo4A-5 17:00

A 270-to-300GHz Amplifier-Last Transmitter with 6.7dBm Peak Output Power Using 130nm SiGe Process

Peigen Zhou, Jixin Chen, Zuojun Wang, Jiayang Yu, Zhe Chen, Hao Gao, Wei Hong; Southeast University, China

Abstract: This paper presents an amplifier-last transmitter (TX), operating from 270-to-300 GHz, in a 130 nm SiGe BiCMOS process. The TX is composed of a 250 GHz multiplier-by-6 local oscillator (LO) chain, an-isolation-enhanced fundamental mixer, and a four-stage g_m-boosting power amplifier (PA). The measured peak output power of the LO chain is 7.8 dBm at 250 GHz. The TX achieves a measured peak P_{sat} of 6.7 dBm at 278 GHz and 282 GHz, and delivers a measured maximum OP_{1dB} of 5 dBm at 280 GHz with 3 dB bandwidth larger than 26 GHz. The measured LO leakage and image signal rejection are better than 21.7 dBc and 34.1 dBc respectively. For the first time, the silicon-based PA is integrated with 300 GHz TX, and the TX achieves the highest P_{sat} and OP_{1dB} compared to other state-of-the-arts >250 GHz silicon-based TX.

Monday, 16 June 2025
15:40–17:20
Room 205
Session RMo4B: Design Techniques of RF/mm-Wave Low-Noise Amplifiers (LNAs) and Front-End Modules (FEMs)
Chair: Hsieh-Hung Hsieh, TSMC, Taiwan
Co-Chair: Ying Chen, Samsung, USA

RMo4B-1 15:40
A 23–40GHz Compact LNA with Dual-Path Noise-Cancelling Technology Enabled by a Quad-Coil Coupled Transformer

Yongchun Li, Taotao Xu, Pei Qin, Quan Xue, Wenquan Che; SCUT, China

Abstract: This paper presents a 23–40 GHz low-noise amplifier (LNA) that employs dual-path noise-cancelling technology. The proposed noise-cancelling method, implemented through a quad-coil coupled transformer network, significantly reduces the circuit noise while maintaining a compact layout. To enhance the gain and stability of the circuit, a common-source stage with single-ended neutralization is incorporated after the noise-cancelling stage. Fabricated using TSMC 65-nm CMOS process, the LNA achieves a maximum gain (S_{21}) of 15.7 dB, a minimum noise figure (NF) of 2.79 dB, and occupies a chip area of 0.089 mm^2. The amplifier operates at a supply voltage of 0.6 V, consuming 14 mW of power.

RMo4B-2 16:00
A 3.23dB Average NF and 2.32dB Minimum NF V-/E-Band Common-Gate/Common-Source Joint-Feeding LNA with Three-Line Coupler Input Matching for Simultaneous Noise/Power Matching

Boce Lin, Niccoló Villaggi, Tzu-yuan Huang, Hua Wang; ETH Zürich, Switzerland

Abstract: The proposed and implemented V/E-band low noise amplifier (LNA) in 22nm CMOS FDSOI covering 3dB bandwidth of 60.6 to 74.4GHz. It achieves a measured average noise figure (NF) of 3.23dB averaged over the 3dB bandwidth and over 5 samples. Moreover, it records a measured averaged minimum NF of 2.32dB at 65GHz over 5 samples. It utilizes a three-line coupler to provide wide-band simultaneous noise and power matching and trans-conductance (gm) boost. This LNA design provides a compact chip area with moderate power consumption and extremely low NF, which together can support the future backhaul system and fixed wireless networks of 5G and beyond-5G communication.

RMo4B-3 16:20

A 22-nm CMOS 3.5–7.2GHz Wideband FEM with a Balanced-Power-Combining DPA and a Dual-Resonant Input Matching LNA

Kangjie Zhao[1], Can Liu[1], Linfeng Zou[1], Kai Liu[1], Yuan Xu[1], Xinyi Jiang[1], Ruilai Xu[1], Wangdong Xie[1], Yang Zhou[1], Hao Deng[2], Leilei Huang[1], Chunqi Shi[1], Lei Chen[3], Jinghong Chen[2], Runxi Zhang[1]; [1]East China Normal University, China, [2]University of Houston, USA, [3]SUEP, China

Abstract: This paper presents a 3.5–7.2 GHz wideband front-end module (FEM) implemented in 22-nm CMOS technology. The FEM consists of a digital power amplifier (DPA) and a low noise amplifier (LNA). The DPA utilizes a 4-way balanced-power-combining (BPC) network with electrical coupling compensation to minimize broadband amplitude modulation (AM) and phase modulation (PM) mismatches among the four sub-arrays. To improve efficiency and linearity, an AM-PM distortion-canceling power cell is developed. The LNA employs a dual-resonant input matching (DRIM) approach to achieve wideband input impedance and noise matching. The DPA achieves a peak output power of 30.08 dBm with a drain efficiency of 43.31% at 6 GHz. For a 40 MHz 256-QAM signal, the average output power (P_{avg}) is 19.09, 21.07 and 17.18 dBm at 4.5, 6, and 7.2 GHz, respectively, with average drain efficiency (DE_{avg}) of 20.39%, 20.6% and 18.5%. For a 20 MHz 1024-QAM signal, the P_{avg} is 16.7, 18.25 and 17.55 dBm at 4.5, 6 and 7.2 GHz with DE_{avg} of 18.22%, 18.41% and 16.53%, respectively. The LNA achieves a peak S21 of 18.8 dB at 6 GHz, with the noise figure (NF) of 1.7 dB and S11 and S22 below -10 dB across the 3.5–7.2 GHz range.

RMo4B-4 16:40

An Ultra-Compact Switchless Bidirectional PA-LNA with 8-Shaped Transformer-Based Inter-Stage Matching Networks for W-Band Applications

Lingtao Jiang, Lihong Chen, Xianfeng Que, Quan Xue, Yanjie Wang; SCUT, China

Abstract: This paper presents an ultra-compact wideband bidirectional switchless PA-LNA for W-band wireless applications. The proposed PA-LNA adopts a single-signal-path topology, integrating highly efficient 8-shaped transformers and tri-coil baluns to minimize electromagnetic cross-coupling, reduce insertion loss, and enhance linearity in a compact size. The PA-LNA prototype is fabricated in 40nm CMOS LP process. It achieves a 3-dB bandwidth from 79 GHz to 92 GHz, a saturated output power (P_{sat}) of 13.7 dBm, an output 1-dB compression point (OP1dB) of 8.7 dBm, and a maximum power-added efficiency (PAE) of 9.5% in PA mode. In LNA mode, it exhibits a 3-dB bandwidth from 86 GHz to 98 GHz and a minimum noise figure (NF) of 8.2 dB, all within a compact core area of only 0.1 mm^2.

RMo4B-5 17:00

A 24–30GHz GaN-on-SiC T/R Front-End Module with 37.1-dBm Output Power and 34.4% PAE

Cheng-Jie Hu, Hui-Yang Li, Jin-Xu Xu, Run-Feng Chen, Jun-Ming Zhu, Xiu Yin Zhang; SCUT, China

Abstract: This paper presents a 24–30 GHz transmit-receive (T/R) front-end module (FEM) on a 150-nm GaN-on-SiC HEMT process. The transmitting chain is constructed by two fully symmetrical push-pull power amplifier (PA) with a balun as the power distributing network. The waveform engineering technique is used in the impedance matching for high efficiency. The second harmonic is controlled by exploiting the inherent isolation of the balun's center-tap point which helps to optimize the second harmonic impedance without affecting the fundamental response. The receiving chain consists of a three-stage low-noise amplifier (LNA) with a gain of over 20 dB and wideband noise matching across the operation bandwidth. A high-order stacked-transistor single-pole double-throw (SPDT) switch is designed with a low insertion loss of 0.75 dB and an IP_{1dB} of 44 dBm, ensuring no gain compression in transmitting mode. In measurement, the proposed FEM operating across 24–30 GHz demonstrates a peak P_{sat} of 37.1 dBm and peak power added efficiency (PAE) of 34.4% in the Tx mode. An EVM of 5.54% and an average output power of 30.1 dBm with a 64-QAM modulated input signal of 100 MHz bandwidth at 26 GHz are realized. In the Rx mode, the front-end demonstrates an NF of less than 3.1 dB with a gain of 20–21.3 dB. The FEM chip area is 3.6×2.7 mm^2.

Monday, 16 June 2025
15:40–17:20
Room 207
Session RMo4C:
Unleashing Energy Efficiency and High Linearity in IoT RFICs

Chair: Yao-Hong Liu, imec, The Netherlands
Co-Chair: Pierluigi Nuzzo, University of California, Berkeley, USA

RMo4C-1 15:40

A Single-Side-Band Frequency Translated 64-QAM Backscatter Communication IC with Phase-Rotation Time-Variant Reflector and LUT-Based Digital Predistortion

Shuangfeng Kong, Fengjun Chen, Zhiqiang Huang; HKUST Guangzhou, China

Abstract: This paper presents a backscatter communication integrated circuit (IC) that supports single-sideband (SSB) frequency translation by using a fully-integrated phase-rotation time-variant reflector. It also supports high-order modulation schemes via a high-resolution tunable RLC network and lookup table (LUT)-based digital predistortion. The proposed backscatter communication IC supports B/QPSK and 16/64-QAM modulation, achieving an EVM of 7.51% at the maximum data rate of 18 Mb/s for 64-QAM modulation, while consuming only 20.97 μW. This design is fabricated in a 40-nm CMOS process with a core area of 0.17 mm^2.

RMo4C-2 16:00

A 742μW -94.5dBm Sensitivity 5G-NR Wake-Up Receiver

Siyu Wang, David D. Wentzloff; University of Michigan, USA

Abstract: This work presents a wake-up receiver (WUR) compliant with the draft 5G low-power wake-up signal (LP-WUS) specification. The 5G LP-WUS uses multi-carrier (MC) OOK modulation which enables a PLL-less, single-phase direct conversion architecture that significantly reduces power consumption compared to a conventional cellular receiver. The WUR employs a current-reuse LNTA for a high sensitivity under a low power budget. A current-mode RF front-end with an enhanced baseband TIA is implemented for blocker-tolerance. Fabricated in 65-nm CMOS, the WUR consumes 742 μW active power and achieves a -94.5 dBm sensitivity and -63.5 dB out-of-band (OOB) signal-to-interference ratio (SIR).

RMo4C-3 16:20

A Harmonic-Suppressing Gain-Boosted N-Path Receiver with Clock Bootstrapping for IoT Applications

Soroush Araei, Mohammad Barzgari, Haibo Yang, Negar Reiskarimian; MIT, USA

Abstract: This article presents a compact harmonic-suppressing gain-boosted N-path receiver for Internet of Things (IoT) applications. It features a passive harmonic rejection extension within the feedback path of an amplifier for early suppression of harmonic blockers and a pipeline down-mixer achieving over 3× passive gain. In addition, a low-power, scalable clock-boosting technique is introduced to enable operation under a low-voltage power supply. The prototype receiver (RX),

implemented in 22-nm fully depleted silicon-on-insulator (FD-SOI) technology, occupies 0.048 mm^2. Consuming only 1.27–5.48 mW, it operates across 0.25–3 GHz and achieves blocker 1-dB compression point (B1dB) of -3/-2 dBm at the $3^{rd}/5^{th}$ harmonics, respectively. Furthermore, local oscillator (LO) leakage at the antenna port demonstrates superior performance compared to state-of-the-art designs, with worst-case -73 dBm across the entire frequency range.

RMo4C-4 16:40

A 1.9–4GHz Receiver with Enhanced In-Band and Out-of-Band Linearity Using Double Sampling and Time-Domain Processing

Sreeni Poolakkal[1], Dipan Kar[1], Arpit Rao[1], Daniel Mazidi[1], Praveen Venkatachala[2], Subhanshu Gupta[1]; [1]Washington State University, USA, [2]Skyworks Solutions, USA

Abstract: This paper presents an energy-efficient wireless receiver (RX) with enhanced in-band and out-of-band linearity. Conventional RX architectures are limited in gain, sensitivity, and linearity arising from supply dependence (V_{DD}) leading to significant performance degradation when processing multiple signals of varying strengths. Both the trans-impedance amplifier (TIA) and the voltage amplifiers in conventional RXs especially in advanced technology nodes induce distortion and clipping in dynamic environments comprising of multiple moving sources that alter signal strength. This work investigates scaling-friendly time-domain signal processing replacing supply-dependent amplifiers with a double-sampled VCO-based voltage-to-time converters (VTC) followed by a time to digital converter (TDC) for digital readout. We enhance the VTC in-band linearity by a preceding double sampler and overall receiver out-of-band linearity using a two-stage filtering technique including a time-domain filter implemented using switched-capacitor-based voltage feedback. The proposed RX achieves a compression point of -6dBm, an in-band IIP3 of +4dBm, and an out-of-band (OOB) IIP3 of +10dBm, while consuming only 18mW.

RMo4C-5 17:00

A 5.75mW Fully-Integrated Galvanic Isolator for Gate Drivers with Asynchronous 66.7/66.7Mb/s Full-Duplex Communication

Lucrezia Navarin[1], Karl Norling[2], Marco Parenzan[2], Alexander Uran[2], Stefano Ruzzu[2], Krithika Rathinam[2], Andrea Neviani[1], Andrea Bevilacqua[1]; [1]Università di Padova, Italy, [2]Infineon Technologies, Austria

Abstract: This work presents a low power fully-integrated galvanic isolator for gate drivers featuring asynchronous full-duplex communication. The proposed design uses ASK and LSK modulation schemes to achieve symmetric 66.7/66.7 Mb/s throughput, using a compact 2.2mm^2 chip area. Full-duplex communication is ensured in a completely asynchronous scenario, enabling event-driven bidirectional data transfer through gate drivers. The prototype fabricated in a 0.13μm HV CMOS technology consumes 5.75mW from the 1.5V supply. The propagation delay at the maximum data rate is below 20 ns.

Tuesday, 17 June 2025
8:00–9:40
Room 203
Session RTu1A: mm-Wave Power Amplifiers and Transmitters
Chair: Song Hu, Apple, USA
Co-Chair: Hyun-Chul Park, Samsung Electronics, Korea

RTu1A-1 8:00
A 10 to 40GHz Stacked Push-Pull Class-B Power Amplifier in 45-nm CMOS SOI with 20.4dBm P_{SAT} and Continuously Supporting 72Gb/s 64-QAM and 10Gb/s 1024-QAM Signals

Saleh Hassanzadehyamchi[1], Hadi Bameri[1], Ali M. Niknejad[2], Omeed Momeni[1]; [1]University of California, Davis, USA, [2]University of California, Berkeley, USA

Abstract: This paper presents a broadband, high-efficiency stacked push-pull class-B power amplifier in 45-nm CMOS SOI that has a peak P_{SAT} of 20.4dBm and a maximum power-added efficiency of 40.2%. Harmonic superposition of the drain-source current waveforms in a push-pull topology is utilized to enhance bandwidth (BW) and linearity while maintaining the same efficiency level as a regular Class-B PA. Equivalent circuits of tapered transmission lines, along with a low quality-factor inductive-resistive matching are used for broadband input and output matching of the PA. The PA achieves a very flat P_{sat} with a record 1-dB BW of 30 GHz (120%) over 10 to 40 GHz. The PA has a peak small-signal gain of 13.8 dB with a 3-dB BW from 11.5 to 44.9 GHz. Furthermore, based on modulation tests, the proposed PA supports 10 Gb/s 1024-QAM and 6–72 Gb/s 64-QAM modulated signals. The DC power consumption is 182mW, and the chip dimensions are 0.92mm×2.1 mm.

RTu1A-2 8:20
A Wideband Dual-Mode Power Amplifier with Slotline-Based Series-Parallel Combiner in 28-nm Bulk CMOS Technology

Gunwoo Park, Sanggeun Jeon; Korea University, Korea

Abstract: This paper presents a wideband dual-mode power amplifier (PA) implemented in a 28-nm bulk CMOS technology. The PA features a reconfigurable differential 4/8-way power combiner, utilizing a slotline-based series-parallel combiner (SSPC) and shunt switches, which supports two operation modes: high-power mode (HPM) and low-power mode (LPM). In HPM, the PA achieves a 3-dB bandwidth of 27.9 GHz, with saturated output power (P_{sat}) of 18–19.3 dBm, 1-dB compression power (OP_{1dB}) of 13.2–15.1 dBm, and maximum power-added efficiency (PAE_{max}) of 20.4–28.0% over the frequency range of 45–70 GHz. In LPM, the 3-dB bandwidth is 30.8 GHz, with P_{sat} of 13.6–14.3 dBm, OP_{1dB} of 9.2–10.3 dBm, and PAE_{max} of 12.5–17.1%. At 60 GHz, measurements using a 64-QAM, 12-Gb/s signal demonstrate an rms error vector magnitude (EVM) of -25.3 dB, an average PAE (PAE_{avg}) of 5.1%, and an average output power (P_{avg}) of 10.7 dBm in HPM, and -27.3 dB, 2.9%, and 5.3 dBm, respectively, in LPM.

RTu1A-3 8:40

A K-Band Process-Corner Robust Balanced Power Amplifier Utilizing Current-Mode Adaptive Biasing Network in 65-nm CMOS

Jiankai Zhao, Haikun Jia, Qiuyu Peng, Wei Deng, Zhan Gao, Xiaochuan Duo, Zhihua Wang, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents an adaptive biased K-band balanced power amplifier robust to process corner variations and featuring high modulation data rate with enhanced PAE at power back-off level. The proposed architecture, utilizing current-mode adaptive biasing network (ABN) with adjustable weight and a true power detector, offers a significant improvement in AM-AM distortion over process corner variation, from 5.6dB to 1.7dB, compared with conventional voltage-mode ABN. Fabricated in 65-nm CMOS technology, the measured OP1dB variation of the PA over multi-chips is only 0.5dB. With improved ABN bandwidth, the PA achieves a 4.8Gbps data rates when 256-QAM modulation is applied.

RTu1A-4 9:00

A D-Band Guanella Transformer Based Stacked Doherty Power Amplifier with Adaptive Bias Network in 250-nm InP DHBT

Senne Gielen[1], Berke Gungor[2], Yang Zhang[1], Mark Ingels[1], Patrick Reynaert[2]; [1]imec, Belgium, [2]KU Leuven, Belgium

Abstract: This paper presents a compact D-band Doherty power amplifier (PA) in 250-nm InP DHBT. The power amplifier core consists of a stacked common-emitter and common-base pair and utilizes an integrated 1:4 Guanella transformer for interstage matching. A power detector as well as an adaptive bias network are also implemented to boost the linearity and efficiency of the amplifier. The PA achieves a small-signal gain of 17.8 dB and a small-signal bandwidth of 14.7 GHz. In continuous-wave measurements, the power amplifier has a saturated output power of 20.3 dBm. The amplifier achieves a maximum power-added efficiency (PAE) of 21.4% and 11.5% with 6-dB power backoff. The performance of the amplifier is verified with modulated measurements up to 24 Gb/s.

RTu1A-5 9:20

A 23.6–30.0GHz Phased-Array Transmitter with Wide-Angle-Scanning Load-Compensation Technique Achieving OTA-Tested 2.9dB Array-Gain Enhancement and 1.2dB EVM Improvement

Mengqian Geng, Yiming Yu, Bohan Sun, Riqi Wang, Huihua Liu, Yunqiu Wu, Chenxi Zhao, Kai Kang; UESTC, China

Abstract: In this paper, a wideband phased-array transmitter (TX) featuring a wide-angle-scanning load-compensation technique is demonstrated. This technique aims to compensate for antenna-load impedance variation of large-scale phased-array systems during beam scanning. It is implemented by a Doherty PA integrated with two digitally controlled phase-shifting cells positioned in both the main and auxiliary paths of the PA. Based on calculated beam-angle-dependent antenna-load impedances, the technique can adjust the phase and amplitude difference between the main and auxiliary paths of the PAs, thereby enabling the main-path PA to always operate with a consistent antenna load. The proposed phased-array TX is fabricated in a 65nm CMOS process. The measurement results show that the TX achieves a 3-dB gain bandwidth of 6.4 GHz, ranging from 23.6 to 30 GHz. It has an output 1-dB compression point (OP_{1dB}) of 15.7 dBm and a saturated output power of 19.9 dBm. Thanks to the load compensation scheme, the PA attains 2.8 dB gain enhancement and 4.1 dB OP_{1dB} improvement within a full-span 4:1 VSWR circle. A prototype 4-element phased-array TX is designed based on the chip. With the proposed technique, the over-the-air (OTA)-tested array gain and EVM are respectively improved by 2.9 dB at a beam angle (θ_0) of -20° and 1.2dB at -30° θ_0, compared with that without enabling the method.

Tuesday, 17 June 2025
8:00–9:40
Room 205
Session RTu1B: High-Performance RF Oscillators
Chair: Hanli Liu, Zhejiang University, China
Co-Chair: Teerachot Siriburanon, University College Dublin, Ireland

RTu1B-1 8:00
An Inverse Class-F VCO with Reduced Third Harmonic Detriment Using a High Fundamental and Second Harmonic Q-Factor Resonator Achieving a 198.9dBc/Hz Peak FoM

Yue Wu, Yatao Peng, Fengen Yuan, Jiawei Li, Jun Yin, Rui P. Martins, Pui In Mak; University of Macau, China

Abstract: This paper presents a novel topology to design the inverse-class-F voltage-controlled oscillator (VCO). The proposed architecture employs a distributed dual-mode resonator (DMR) as the LC tank to replace the transformer (xfmr)-based tank in the conventional class-F^{-1} VCOs. The proposed DMR can achieve high Q-factors at both the fundamental and 2nd harmonic frequencies by avoiding magnetic flux cancellation that is inevitable for the xfmr-based counterpart. Using this DMR to construct a class-F^{-1} VCO, the ratio of 2nd harmonic to fundamental components in the output oscillation is considerably large. This results in a sufficiently wide duration of impulse sensitivity function (ISF)~0 within the output waveform period to suppress noise to PN conversion without introducing excessive drain to gate gain. In the class-F^{-1} VCOs, the misaligned third harmonics in the oscillating signal deteriorates the ISF. Thanks to the DMR's dual high-Q characteristics, the proposed VCO considerably reduces the detrimental 3rd harmonic components, further optimizing PN. The fabricated VCO prototype demonstrates a frequency tuning range (FTR) from 9.37 GHz to 10.86 GHz, with a best-in-class phase noise (PN) of -143 dBc/Hz at a 10 MHz offset, corresponding to a peak figure of merit (FoM) of 198.9 dBc/Hz.

RTu1B-2 8:20
A 4.21-to-15.18GHz Pure Magnetic-Coupling and Fully Symmetrical Quad-Core Quad-Mode VCO Achieving 220.5dBc/Hz $FoM_{TA@10MHz}$

Shijin Huang, Pei Qin, Haoshen Zhu, Xiang Yi, Wenjie Feng, Wenquan Che, Quan Xue; SCUT, China

Abstract: This work proposes a wide frequency tuning range (FTR) and low phase noise (PN) quad-core quad-mode voltage-controlled oscillator (VCO) which features pure magnetic-coupling technique and fully symmetrical topology. The proposed centrosymmetric transformer, which integrates four coupled inductors and an embedded switched inductor, enables quad-mode operation through pure magnetic coupling without causing any FTR degradation due to extra electrical coupling. Furthermore, the fully symmetrical inductive, capacitive, and active elements, as well as the routing layout, minimize mismatches among the VCO cores and effectively synchronize each

core, optimizing phase noise in quad-core operation. The proposed quad-core quad-mode VCO achieves an FTR of 113.2% (4.21 to 15.18 GHz), a PN of -141.4 dBc/Hz at a 10 MHz offset from 4.28 GHz, a peak FoM_T of 211.6 dBc/Hz and a peak FoM_{TA} of 220.5 dBc/Hz at a 10 MHz offset.

RTu1B-3 8:40

7.8-to-10.7GHz Reliable-Mode-Switching Series Resonance Oscillator with Bidirectional Inductive-Mode-Pulling Achieving -156.5dBc/Hz Phase Noise and 199.2dBc/Hz FoM_T at 10MHz Offset in 40-nm CMOS

Qiao Leng, Yiyang Shu, Yu Wang, Xun Luo; UESTC, China

Abstract: This paper proposes a reliable-mode-switching series resonance oscillator with bidirectional inductive-mode-pulling to achieve ultra-low phase noise and wide tuning range, simultaneously. The connection of mode switches are designed to avoid large parasitic capacitance and voltage swing. The bidirectional inductive-pulling transformer is introduced to expand the frequency range of both even and odd modes without reliability risk. Meanwhile, the balanced-slope NMOS inverter is introduced to minimize the common mode ripple and ensure the virtual ground for mode switching. Prototyped in a 40-nm CMOS process, the measured VCO exhibits merits of 31.6% FTR from 7.8 to 10.7 GHz, -156.5dBc/Hz phase noise, and 199.2dBc/Hz FoM_T at 10MHz offset.

RTu1B-4 9:00

A Compact VCO Using Coupling-Canceling Common-Mode Resonance Expansion Achieving 120–155kHz 1/f³ Corner and 0.27dB FoM Variation Without Harmonic Tuning

Xiangjian Kong[1], Kai Xu[2], Hao Lian[1], Fa Dai[1], Chunbing Guo[1]; [1]GDUT, China, [2]King's College London, UK

Abstract: This paper presents a voltage-controlled oscillator (VCO) with low flicker phase noise corner, leveraging a coupling-canceling (CC) common-mode (CM) resonance expansion technique. The design features a tail 8-shaped inductor coupled with the drain inductor to create a high-order CM resonance, enhancing the CM resonance expansion. To achieve a high and wideband CM impedance within a compact layout, staggered tap inductors are employed to mitigate the CM coupling effect, effectively addressing the notch issue in transformer-based wideband networks. Consequently, both the drain and source of the MOSFET benefit from wideband CM resonance. The proposed VCO achieves a low 120 kHz 1/f³ phase noise corner while consuming only 6 mW at 8.45 GHz. It is fabricated in a 65-nm CMOS process and occupies a core area of 0.115 mm^2. The measured phase noise at a 1 MHz offset frequency is -121.64 dBc/Hz, yielding a peak Figure-of-Merit (FoM) of 192.25 dBc/Hz. The FoM variation at 1 MHz offset is below 0.27 dB, and the 1/f³ corner remains below 155 kHz across the entire tuning range, without requiring manual CM tuning.

RTu1B-5 9:20

A Multi-Tap-Transformer Based Quad-Core Dual-Mode VCO Achieving 213.1dBc/Hz $FoM_{TA@100kHz}$ and Wideband $1/f^3$ Noise Suppression

Yuhui Li, Pei Qin, Haoshen Zhu, Xiang Yi, Wenjie Feng, Wenquan Che, Quan Xue; SCUT, China

Abstract: This work proposes a multi-tap transformer-based quad-core dual-mode voltage-controlled oscillator (VCO) with wideband $1/f^3$ noise suppression. The design integrates enhanced electromagnetic (E-M) mixed-coupling and harmonic-free-like techniques, achieving a high drain-to-gate voltage gain and generating a non-shaping balanced impulse sensitivity function (ISF). This approach effectively mitigates both thermal and flicker noise in the VCO across a wide bandwidth. Furthermore, a wide frequency tuning range (FTR) is realized by employing two identical orthogonally stacked dual-core multi-tap transformer VCOs combined with mode switches that define two distinct resonant modes. The proposed VCO demonstrates an impressive FTR of 62.8% (4.54–8.7 GHz), phase noise (PN) of -103.2 dBc/Hz and -146.9 dBc/Hz at 100 kHz and 10 MHz offsets from a 4.8 GHz carrier, and a $1/f^3$ PN corner frequency spanning 70 to 250 kHz. Additionally, it achieves a peak figure of merit with tuning (FoM_{TA}) of 213.1 dBc/Hz and 216.5 dBc/Hz at 100 kHz and 10 MHz offsets, respectively.

Tuesday, 17 June 2025
8:00–9:40
Room 207
Session RTu1C:
Pushing RFIC Boundaries with Out-of-the-Box Innovation
Chair: Aly Ismail, Apple, USA
Co-Chair: Jin Zhou, MediaTek, USA

RTu1C-1 8:00
An Ultra Low Power Analog/Mixed-Signal Processor for a Smart RF Signal Classification System in the ISM Band

N. Pekcokguler[1], C. Dehollain[2], A. Burg[2], P. Courouve[3], D. Morche[3]; [1]Analog Devices, Germany, [2]EPFL, Switzerland, [3]CEA-Leti, France

Abstract: In this work, we propose an ultra-low power highly configurable analog/mixed-signal (AMS) processor as part of a smart RF signal detection and recognition system focusing on the ISM band. The analog feature extraction approach reduces power consumption and data rate through smart feature selection. The implemented highly configurable analog circuit enables detection and recognition of various signal types across a large variety of spectrum conditions. The proposed system achieves state-of-the-art accuracy with sub-mW power consumption.

RTu1C-2 8:20
Enabling Fast Steering of Arbitrary Beams with Phased Arrays

Arun Paidimarri, Bodhisatwa Sadhu, Mark Yeck, Alberto Valdes-Garcia; IBM, USA

Abstract: Phased array-based systems must support the formation of beams with precise lobes and nulls in specific locations to operate effectively in complex environments with multiple users, objects, and interferers. Additionally, the ability to steer these non-conventional beam configurations rapidly is highly desirable. Current methods for fast beam steering are either constrained by the limited memory capacity of RF front-ends or restricted to fast steering of beams with sinc-shaped patterns. In this work, we introduce an approach for enabling the rapid steering of arbitrary beams every 200ns. Our method involves defining a desired beam shape in the broadside direction and steering it through a transformation process. Measurements of spatial and temporal variations of beamforming gain using a 16×16 element phased array at 28 GHz validate the effectiveness of this technique. The measured beam shapes include (1) a beam with a null 26° to the left of the main lobe (2) a multi-armed beam with three lobes at -18°, 0° and +28° and (3) a 40°-wide flat-topped beam.

RTu1C-3 8:40

An 8-Lane 58Gb/s/Lane 0.66pJ/bit Modulator Driver Electrical-IC for a 3-D Integrated Silicon Photonic Transmitter in 22nm FD-SOI Process

Laszlo Szilagyi[1], Bartek J. Pawlak[2], Luc Pauwels[3], Pieter Bex[3], Chiara Marchese[3], Guy Lepage[3], Yoojin Ban[3], Dimitrios Velenis[3], Nikos Argyris[4], Dimitrios Kalavrouziotis[4], Konstantinos Tokas[4], Paraskevas Bakopoulos[4]; [1]GlobalFoundries, Germany, [2]GlobalFoundries, Belgium, [3]imec, Belgium, [4]NVIDIA, Greece

Abstract: A modulator driver circuit for electro-absorption modulators (EAMs) is designed in 22 nm FD-SOI technology as part of the electrical integrated circuit (EIC) of a 3D-integrated 8-lane silicon photonic (SiPh) transmitter. The high driving voltage EAMs require, exceeding the breakdown voltage of the process is achieved by using stacked switches within the floating substrates of the SOI process. The high bitrate signal is delivered via level-shifters and pre-amplifiers to the high-voltage output stage. Limiting amplifiers and inductive peaking techniques are employed to increase the data rate (DR). Die level measurements show 1.87 V_{pp} voltage swing with a 2 V supply at 58 Gb/s where the transmission is still error-free (BER< 10^{-12}). Optical measurements on the 3-D-hybrid integrated EIC with a photonic IC (PIC) show 50 Gb/s/lane signal output. As a result of the implemented switching output stage, the overall EIC energy efficiency for the 8 lanes is as low as 0.66 pJ/bit for 58Gb/s and 0.76 pJ/bit for 50 Gb/s.

RTu1C-4 9:00

A 6.5 to 9GHz IEEE 802.15.4/4z Compatible IR-UWB SoC Capable of Handling -22dBm WiFi-5 or -24 to -17dBm LTE Blocker Levels

Babak Vakili-Amini[1], Maxime Vignasse[1], Syed Enam[1], Amit Sarkar[1], Jaydeep Dalwadi[1], Javier Velandia[2], Mahdi Bagheri[1], Sebastien Darfeuille[2], Yi-Wen Chen[1], Melina Apostolidou[3], Jan van Sinderen[3], Henrik Jensen[1], Rozi Roufoogaran[1]; [1]NXP Semiconductors, USA, [2]NXP Semiconductors, Austria, [3]NXP Semiconductors, The Netherlands

Abstract: This work presents a single-die IEEE 802.15.4/4z compliant impulse-radio ultra-wideband SoC chip that supports single-sided & double-sided two-way ranging, time difference of arrival (TDoA) & phase difference of arrival (PDoA) ranging and IR-UWB radar. The transceiver includes two stand-alone receiver (Rx) chains and one combined transmit & receive (TRx) chain, which can interface with four antennas to improve diversity. The maximum transmit peak power is 15 dBm or higher across the UWB bands from 6.5 to 9 GHz (Ch5 to Ch12). The Rx sensitivity is -96.6 to -95.7 dBm (6.81 Mb/s and <1% PER) and -103 to -101 dBm (850 kb/s and <1% PER) across the UWB channels. Receivers show 3 dB de-sense for WiFi-5 blocker levels of -22 dBm or LTE blocker levels of -24 to -17 dBm. The chip is fabricated in 28 nm CMOS technology with a radio size of 4.47 mm^2.

RTu1C-5 9:20

Fully-Integrated Autonomous K-Band Complex Permittivity Sensor in 22nm FDSOI for Biomedical Body Parameter Monitoring Applications

Adilet Dossanov, Moritz Weißbrich, Alexander Meyer, Liubov Bakhchova, Finn-Niclas Stapelfeldt, Guillermo Payá-Vayá, Vadim Issakov; Technische Universität Braunschweig, Germany

Abstract: This work presents a fully integrated low-power system-on-chip (SoC) for autonomous body monitoring applications in 22nm FDSOI CMOS technology. The proposed SoC comprises a K-band complex permittivity sensor, a 10-bit successive approximation register (SAR) analog to digital converter (ADC), an ultra-low-power (ULP) NanoController as a programmable Finite-State Machine (FSM), an integrated ULP voltage/current reference circuit, and low-drop-out (LDO) voltage regulators as a power management unit. The functionality of the dielectric sensor has been validated and calibrated using isopropanol, ethanol, and methanol solutions as material-under-test (MUT). The complete SoC occupies a chip area of 2mm^2, has an average power consumption of 14.3μW during a 10-minute measurement cycle.

Tuesday, 17 June 2025
10:10–11:50
Room 203
Session RTu2A: Design Techniques for High Performance SiGe PAs
Chair: Tolga Dinc, Texas Instruments, USA
Co-Chair: Shintaro Shinjo, Mitsubishi Electric, Japan

RTu2A-1 10:10
Topology-Optimized Nonintuitive Multilayered mm-Wave Power Amplifiers
Vinay Chenna, Hossein Hashemi; University of Southern California, USA

Abstract: Algorithmic inverse design and optimization of multistage power-combined power amplifiers (PA) with nonintuitive layout geometries is presented. The computationally-efficient iterative algorithms determine the geometry of multi-layered metal structures as well as the size and bias of transistors with minimal human intervention. Fabricated W-Band SiGe HBT PA prototypes with nonintuitive multilayered layouts generated using this approach experimentally achieve > 30% peak power added efficiency (PAE) at peak P_{SAT} > 17.3 dBm while occupying < 0.08 mm^2.

RTu2A-2 10:30
31.7 and 36.7dBm Ka-Band SiGe BiCMOS Power Amplifiers Using Resonated Amplifier Cores and Optimized Power Combining
Alexander Haag[1], Ahmet Çağrı Ulusoy[2]; [1]milli IC, Germany, [2]KIT, Germany

Abstract: This paper presents 31.7dBm and 36.7 dBm (4.7 W) K_a-band power amplifiers (PAs) in a 130nm silicon germanium (SiGe) BiCMOS technology operating from a 3.5V supply. High peak power-added efficiency (PAE) of 37% and 28% is achieved, respectively. This high output power and efficiency is enabled by refining a PA core design method for large device parallelization and optimized multi stage Wilkinson combiners. The PAs feature a single stage 4-to-1 and two stage 16-way power combiner with a simulated combining loss of only 0.64 and 1.3 dB, respectively. For a 400MBd 64-QAM signal at an EVM_{RMS} of -25 dB, the smaller PA delivers an average output power of 24.7dBm with an average PAE of 10.6%, while the larger version achieves 29.2dBm at 7.1%.

RTu2A-3 10:50
A SiGe Common-Collector-Common-Base Linear Power Amplifier with 17–28-GHz P_{1dB} 3-dB Bandwidth and Enhanced Large-Signal Stability
Tsung-Ching Tsai, Ahmet Çağrı Ulusoy; KIT, Germany

Abstract: This paper presents a broadband SiGe common-collector-common-base (CC-CB) two-stage linear PA with enhanced large-signal stability. Through driving-point admittance analysis, the conventional SiGe cascode PA topology, equipped with a common-emitter device, is shown to be prone to large-signal instability, rendering it unsuitable for broadband PA designs. To address this, the adoption of a CC stage is explained in detail. In addition, a stacked distributed balun is proposed for broadband output matching, accounting for the constraints of limited substrate resistivity. The proposed PA achieves a P_{sat} of 19.3 to 23.3dBm, with a PAE_{sat} of 10.4 to 28.6% over 17 to 30GHz. The

P_{1dB} 3-dB bandwidth ranges from 17 to 28GHz, with a PAE_{1dB} of 11.0 to 22.1%. The PA supports 400-MBd 32-APSK/64-QAM signals. For 64-QAM signals, it achieves 14.7–18.9dBm/6.0–15.7% P_{avg}/PAE at an EVM_{rms} level of -25dB, from 18 to 28GHz.

RTu2A-4 11:10

A Linear Q-Band Balanced Power Amplifier in a 130nm SiGe BiCMOS Technology Using Two-Tone Load-Pull Optimization

Alexander Haag[1], Ahmet Çağrı Ulusoy[2]; [1]milli IC, Germany, [2]KIT, Germany

Abstract: This paper presents a Q-band power amplifier (PA) in a 130nm silicon germanium (SiGe) BiCMOS technology envisioned for future satellite communication (SatCom) applications. To optimize linear efficiency a two-tone load-pull technique is used. As a metric for linearity the third order intermodulation distortion (IMD3) is used with a target value of -25 dBc. Leveraging this technique, the PA achieves a saturated output power of 24.2 dBm and a peak power-added efficiency (PAE) of 33% at 40 GHz. The PAE at IMD3 = -25 dBc is measured to be 15%, and 13.2% for a 400 MBd 64-QAM signal for an EVM_{rms} of -25.3 dB. A balanced architecture is used for good input and output return loss response.

RTu2A-5 11:30

A 5/6GHz Compact, Dual-Band, and Highly Linear Wi-Fi 6E SiGe HBT Power Amplifier Using Q-Modulated Switched Capacitor Interstage Matching Network and Optimized Output Stage

Yoongoo Kang, Hanjung Lee, Inchan Ju; Ajou University, Korea

Abstract: This Work presents a compact, highly linear SiGe HBT power amplifier (PA) for Wi-Fi 6E application. To cover the entire 5/6GHz band, a Q modulated switched capacitor interstage matching network, a broadband transformer balun, and an optimized output stage layout are co-designed With these circuit design techniques, the proposed PA maintains similar small/large signal performance at 5/6 GHz band. The two-stage PA is fabricated in 0.35-μm SiGe HBT Bi-CMOS technology, with its chip DIE size of 0.73 mm^2. Measured small signal gains are 27.0/27.0 dB at 5/6GHz band, with gain variation less than 0.12dB at any 80MHz channel bandwidth (BW). Linear output power (P_{AVG}) is 18.2/18.7/18.1/18.3/17.9/17.9 dBm (EVM=-32 dB) at 5250/5570/5850/6025/6585/6985 MHz under an 802.11ac MCS9 VHT80 signal. The SiGe PA also supports 802.11ax MCS11 VHT160 signal with P_{AVG} of 7.1 dBm, at EVM = -38 dB.

Tuesday, 17 June 2025
10:10–11:30
Room 205
Session RTu2B:
mm-Wave and Sub-THz Radar SoCs and Sensing Techniques
Chair: Yahya Tousi, University of Minnesota, USA
Co-Chair: Oren Eliezer, Samsung, USA

RTu2B-1 10:10
A 4.6mW 232GHz Autodyne Complementary Self-Injection-Locked Radar for Micrometer-Level Displacement Sensing and Imaging

Sidharth Thomas, Wei Sun, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: This paper presents a novel complementary self-injection-locked (CSIL) radar architecture for low-power, high-accuracy THz phase sensing. The CSIL radar employs a self-injection mechanism within a coupled oscillator system, where a portion of the transmitted signal reflects off the target and is reinjected into the radar. This self-injection process induces an amplitude imbalance between the oscillators as a function of the target distance. By measuring this amplitude imbalance, the system can estimate relative displacements within an unambiguous range of $\lambda/4$. Unlike conventional phase-sensing radars, CSIL eliminates the need for complex, power-hungry frequency synthesis. It also operates in autodyne mode and is inherently immune to self-interference. The proposed radar is fabricated using the TSMC 65nm process. Operating at 232 GHz, it achieves a static range accuracy of 20 μm while consuming only 4.6 mW of DC power. Imaging measurements are also presented, highlighting the potential of CSIL in low-power 3D imaging.

RTu2B-2 10:30
400-GHz Concurrent Transceiver Imaging Pixel with Improved Noise Performance and Increased Injection Locking Range

Goutham Murugesan[1], Muhammad Awais[1], Sarfraz Shariff[1], Yukun Zhu[1], Pranith Reddy Byreddy[1], Frank Zhang[1], Wooyeol Choi[2], Kenneth K. O[1]; [1]University of Texas at Dallas, USA, [2]Seoul National University, Korea

Abstract: A 400-GHz concurrent transceiver imaging pixel integrating an injection locking circuitry, VCO, SHM, TIA, and patch antenna within a $(\lambda/2)^2$ area and fabricated in the GF 22-nm FDSOI CMOS process achieves a measured locking range of 8.5 GHz by injection locking through the drain resonator of the VCO. The transmitter delivers a measured peak EIRP of -14.8 dBm and the receiver exhibits a minimum DSB NF of 33 dB. The system consumes 63.2 mW of DC power at 0.8-V V_{DD}. This design has ~5.5 dB lower DSB NF and 9.5× higher locking range compared to the state-of-art $(\lambda/2)^2$ pixels operating at ~400 GHz.

RTu2B-4 10:50

A 140GHz FMCW Radar with 22dB Wideband RF-Domain Multipath Self-Interference Cancellation in 28nm CMOS

Yikuan Chen, Hesham Beshary, Ethan Chou, Meng Wei, Nima Baniasadi, Ali M. Niknejad; University of California, Berkeley, USA

Abstract: This paper presents a D-band CMOS FMCW radar with active self-interference (SI) cancellation in the RF domain. The proposed scheme first uses a transmitter (TX) IQ-mixer to ensure coherent sampling of the SI beat signal and simplify the SI parameter estimation. Then, it replicates the multipath SI using another IQ-mixer and cancels the SI before the LNA. This scheme enhances the radar's dynamic range and the ability to discern sub-meter short range targets. The chip was fabricated in a 28nm CMOS process, and the measurements demonstrate 22 dB wideband SI cancellation for a 10-GHz wide FMCW chirp and up to 44.7 dB narrowband SI cancellation.

RTu2B-5 11:10

An E-Band Phase-Modulated Bistatic Radar with 10mW/Channel Fast-Time Baseband Processing

Wen Zhou, Yahya Tousi; University of Minnesota, USA

Abstract: This work presents a bi-static phase-modulated pulse radar based on analog processing of the fast-time radar signal compatible with communication systems. Based on the proposed scheme we implement an SoC with four parallel processing units consuming 10mW/channel with the quadrature receiver enabling phase-insensitive detection of multiple targets. The 60GHz radar chip is fabricated in 65nm TSMC with a total area of 1.6mm^2. We calibrate and characterize the radar in both monostatic and full bistatic modes. The system demonstrates -90dBm multi-target detection sensitivity and a 7.3cm rms range precision across the full measurement range. This work features the first bi-static E-band module featuring analog fast-time processing for energy efficient and scalable radar sensing.

Tuesday, 17 June 2025
10:10–11:50
Room 207
Session RTu2C: Heterogeneous Integration for RF/mm-Wave Applications and Measurement Techniques
Chair: Duane Howard, Astranis Space Technologies, USA
Co-Chair: Florian Voineau, STMicroelectronics, France

RTu2C-1 10:10
A 3D Heterogeneously Integrated Power Amplifier Module Using BiCMOS and RF SOI CMOS Technologies for 5G Applications

Antoine Le Ravallec, Sébastien Sadlo, David Gaidioz, Christophe Arricastres, Romain Coffy, Frédéric Paillardet, Olivier Noblanc; STMicroelectronics, France

Abstract: This paper presents the first full 3D heterogeneously integrated (HI) power amplifier (PA) module for 5G sub-6 GHz applications, using 130-nm BiCMOS and 130-nm RF Silicon-on-insulator (SOI) CMOS technologies. The cost-effective 3D power amplifier module contains a BiCMOS driver flip-chip on an RF SOI power stage including LDMOS transistors with its analog supply control, inside a 4×4mm^2 QFN package. The 3D power module exhibits a power gain of 38 dB. The maximum PAE is 32% and the maximum measured output power is 35.3 dBm at 3.4 GHz. The core size of the 3D module is 3.6mm^2.

RTu2C-2 10:30
Heterogeneous Integration of a 0.15μm GaN Circulator and a 45nm RF SOI Voltage-Boosted Clock Generation IC

Nishant Patil, Armagan Dascurcu, Nusrat Jahan, Harish Krishnaswamy; Columbia University, USA

Abstract: Advanced CMOS nodes suffer from low linearity due to limited breakdown voltages, while III-V semiconductors offer limited BEOL and integration capability, making it challenging to design complex circuits. Heterogeneous integration of III-V MMICs with CMOS ICs enables the use of the "best junction for the function" to achieve superior dynamic range, but requires tight integration of the ICs with controlled interconnects. This paper presents the first demonstration of a heterogeneously integrated GaN LPTV switched-transmission-line circulator with a CMOS clock generation IC that benefits from the high integration capability of CMOS and superior switch characteristics of GaN. Measurements show 2.5dB DC transmission loss and >17dB isolation across DC–3.35GHz. It provides 11.8dBm IP1dB and 23.9dBm IIP3 thanks to voltage-boosting stacked clock drivers used in CMOS SOI IC. The circulator-clock-chip combo requires only a single-phase external clock at 2.49GHz instead of complex off-the-shelf multi-phase clocks, making it easy to integrate into system-level applications.

RTu2C-3 10:50

Heterogeneously-Integrated Amplifier-on-Glass with Embedded Gallium Nitride (GaN) Dielet for mmWave Applications

Xingchen Li[1], Pradyot Yadav[2], Tomás Palacios[2], Madhavan Swaminathan[1]; [1]Georgia Tech, USA, [2]MIT, USA

Abstract: This work presents the first demonstration of a heterogeneously integrated millimeter-wave (mmWave) amplifier-on-glass with embedded Gallium Nitride (GaN) high-electron-mobility transistors (HEMT) dielet. With the embedded GaN dielet in the prepared glass cavity, redistribution layers (RDL) on the glass package serve as the back-end-of-lines (BEOL) of the circuit and interconnections to other integrated components. In this work, the effects of embedding on GaN performance are studied and a single-stage mmWave amplifier is designed. The amplifier fabrication is enabled by the in-house process capabilities from GaN HEMT preparation to package BEOL build-up. The realized GaN amplifier-on-glass shows >7 dB gain with a bandwidth of 27.35–34.63 GHz. This work offers a self-packaged, cost-effective solution for future GaN-based, heterogeneously integrated mmWave systems.

RTu2C-4 11:10

3D-Millimeter Wave Integrated Circuit (3D-mmWIC): A Gold-Free 3D-Integration Platform for Scaled RF GaN-on-Si Dielets with Intel 16 Si CMOS

Pradyot Yadav[1], Jinchen Wang[1], Danish A. Baig[2], Juan Pastrana-Gonzalez[3], John Niroula[1], Patrick Darmawi-Isakandar[1], Ulrich L. Rohde[4], Ahmad Islam[3], Muhannad Bakir[2], Ruonan Han[1], Tomás Palacios[1]; [1]MIT, USA, [2]Georgia Tech, USA, [3]AFRL, USA, [4]Universität der Bundeswehr München, Germany

Abstract: This paper presents a gold-free 3D millimeter wave integrated circuit (3D-mmWIC). Highly scaled GaN-on-Si front-end-of-line (FEOL) RF dielets are integrated with Intel 16 Si CMOS using Cu-Cu thermocompression bonding (TCB), solder-free 3D heterogeneous integration (3DHI). To demonstrate this process, two different 3D-mmWIC amplifiers targeting the 5G NR FR2 band are fabricated utilizing multiple dielets. The first amplifier implements a conjugate matching of the dielets, achieving a maximum small-signal gain of 4.8 dB and a 3 dB bandwidth of 26–30 GHz. The second amplifier implements additional cross-neutralization capacitance to achieve a maximum small-signal gain of 6.2 dB and a 3 dB bandwidth of 26–32 GHz. Both 3D-mmWICs are extremely compact with a total chip area of 0.49 mm^2.

RTu2C-5 11:30

Determination of the Thermal Noise Parameters of FD-SOI MOSFET Through Hybrid Noise Matrix

B. Dormieu, J. Azevedo Gonçalves, C. Belem Gonçalves, P. Scheer, F. Paolini, G. Gouget;
STMicroelectronics, France

Abstract: A powerful formalism for determining thermal noise parameters, referred to as the NFYs method, is described for MOSFET transistors. This method leverages hybrid two-port network theory and common assumptions about the transistor's noise sources. It requires only the measurement of the noise figure at a single source admittance and the S-parameters, eliminating the need for equivalent circuit theory or the traditional and complex multi-impedance setup. After detailing the mathematical development of the method, its results are compared to those of two previous methods to demonstrate its efficiency and validity.

Tuesday, 17 June 2025
13:30–15:10
Room 203
Session RTu3A: PLLs and Frequency Multipliers
Chair: Ahmed Elkholy, Broadcom, USA
Co-Chair: Jingzhi Zhang, UESTC, China

RTu3A-1 13:30
A 116–132GHz -193.6dBc/Hz-FoM$_T$ -252.8dB-FoM$_J$ Frequency Synthesizer Using a 114fs-Jitter 60-GHz Double-Sampling PLL with Magnetic Parabolic Tuning and Injection-Locked Frequency Doubler

Zhiyu Liu, Howard Cam Luong; HKUST, China

Abstract: A wide-tuning-range (TR) low-phase-noise (PN) D-band frequency synthesizer cascades a mm-Wave double-sampling PLL (DSPLL) with a D-band differential-output injection-locked frequency doubler (ILFM×2). DSPLL consists of a dual-band VCO (DBVCO) with magnetic parabolic tuning and split primary coils, an injection-locked frequency divider (ILFD), and a superior double-sampling phase detector (DSPD) enabling a dual-path loop filter. ILFM×2 features differential outputs, self-oscillation current boosting, and center-tap injection. Fabricated in a 28-nm CMOS, the synthesizer measures TR of 12.9% from 116 to 132G, PN@1M normalized to 120G of -92.9~-106.1dBc/Hz, jitter (1k–100M) of 35.1–145.3fs, FoM$_T$@1M of -180.6~-193.6dBc/Hz, and FoM$_J$ of -240.3~-252.8dB.

RTu3A-2 13:50
A 324-to-360-GHz -6-dBm Output Power THz Phase-Locked Loop in 40-nm CMOS

Wei-Tang Tseng[1], Te-Yen Chiu[2], Chun Wang[2], Chun-Hsing Li[1]; [1]National Taiwan University, Taiwan, [2]National Tsing Hua University, Taiwan

Abstract: A 340-GHz THz phase-locked loop (PLL) composed of an 85-GHz integer-N charge-pump PLL (CPPLL) and a 340-GHz frequency quadrupler (FQ) is proposed for THz communication applications. The FQ utilizes an optimal harmonic impedance matching technique to provide high conversion gain and output power. Given the targeted 340-GHz output frequency, this FQ enables the CPPLL to operate at a lower frequency of 85 GHz, significantly improving the THz PLL's phase noise (PN) and frequency tuning range. Implemented in a 40-nm CMOS technology without ultra-thick metal layers, the proposed THz PLL can be locked from 324 to 360 GHz. It achieves an output power of -6 dBm, a reference spur of -35.5 dBc, a PN of -87.4 dBc/Hz at the 1-MHz offset, and an RMS jitter of 145 fs integrating over 10 kHz to 100 MHz at 340 GHz. The THz PLL exhibits the highest figure of merit beyond 300 GHz.

RTu3A-3 14:10

A 28–38GHz Digitally-Assisted Frequency Tripler with Background Calibration in 55nm SiGe BiCMOS

D. Lodi Rizzini[1], F. Tesolin[1], M. Rossoni[1], B. Nanino[1], P. Granata[1], R. Moleri[1], A. Mazzanti[2], A.L. Lacaita[1], S.M. Dartizio[1], S. Levantino[1]; [1]Politecnico di Milano, Italy, [2]Università di Pavia, Italy

Abstract: This work presents a 28-to-38 GHz frequency tripler in 55-nm SiGe BiCMOS technology. An on-chip background calibration technique maximizes the output power, improving the fundamental harmonic rejection over wide input-frequency and input-power variations. The implemented tripler, which occupies an area of 0.4 mm^2 and dissipates a power of 54 mW, achieves more than 40-dB fundamental harmonic rejection across a 3-dB bandwidth of 10.2 GHz (30.3%) and over 13 dB of input-power variation.

RTu3A-4 14:30

A 35.2–51.4GHz Frequency-Tracking Injection-Locked Frequency Tripler Achieving >28.5dBc Harmonic Rejection Ratios, -7.3dBm Output Power, and 4.3dB Output Power Variation

Zixi Jing, Yi Liu, Howard Cam Luong; HKUST, China

Abstract: This paper presents a frequency-tracking injection-locked frequency tripler (ILFT) featuring wide locking range (LR), high harmonic rejection ratios (HRRs), high output magnitude, and low output magnitude variations. The proposed ILFT utilizes a single-ended injection combined with an amplitude detection method to enhance frequency tracking bandwidth. A dual-core topology is also implemented to improve even harmonic rejection and to provide differential output signals. Fabricated in a 28-nm CMOS process, the ILFT measures an LR of 37.5% from 35.2 to 51.4GHz while achieving an output power of -7.3dBm with power variation of 4.3dB and HRR_1 and HRR_2 of 45.2–52dBc and 28.5–46.5dBc, respectively. The total power consumption of the dual-core frequency-tracking ILFT is 11.6mW.

RTu3A-5 14:50

A High-Conversion-Gain Compact W-Band Distributed Doubler with Second Harmonic Positive Feedback Using Cross-Coupled Capacitor

Dongho Yoo, Byung-Wook Min; Yonsei University, Korea

Abstract: This paper presents a compact and high conversion gain (CG) W-band differential distributed doubler. The proposed two-stage distributed doubler consists of two push-push frequency doublers (PPFDs), utilizing a compact in-phase and quadrature-phase generator with a 90° electrical length of transmission lines. Furthermore, cross-coupled capacitors are connected from the output of the PPFD to the input of the other PPFD, forming a second harmonic positive feedback (SHPF) and enhancing the CG at $2f_0$. Comparing the measurement results of the distributed doublers with and without the SHPF, 6-dB improvement in CG, resulting in a peak CG of 0.1 dB. The doubler achieves a 3-dB bandwidth of 13.9 GHz, which is from 74.8 to 88.7 GHz. The saturated output power is 6.7 dBm with a 35-mW DC power consumption. The fundamental rejection ratio is >36 dBc and the core size is only 0.05 mm^2.

Tuesday, 17 June 2025
13:30–15:10
Room 205
Session RTu3B:
D-Band Circuits and Systems for Sensing and Communications
Chair: Vadim Issakov, Technische Universität Braunschweig, Germany
Co-Chair: Zeshan Ahmad, Coherent, USA

RTu3B-1 13:30
A Low-Power D-Band Radar Transceiver with TL-MCR Matching Technique and Output Phase Shifting

Zesen Chen[1], Likang Du[1], Nayu Li[2], Qun Jane Gu[3], Chunyi Song[1], Zhiwei Xu[1]; [1]Zhejiang University, China, [2]Donghai Laboratory, China, [3]Georgia Tech, USA

Abstract: This paper proposes a D-band frequency-modulated continuous-wave (FMCW) radar transceiver with two transmitters (TX) and two receivers (RX) fabricated in 28nm CMOS. Transmission-line magnetic-coupled resonator (TL-MCR) matching technique in local-oscillator (LO) distributor enhances the gain and reduces power consumption. D-band phase shifters are integrated into transmitters to support precise output phase shifting. The transceiver achieves a 7.6dB noise figure, 67dB conversion gain (CG), 13.3dB output saturation power and 14.3% drain efficiency with 360° phase shifting. Power consumption per one transmitter and one receiver operation is 285mW.

RTu3B-2 13:50
A Terahertz FMCW Radar with 169-GHz Synthetic Bandwidth and Reconfigurable Polarization in 40-nm CMOS

Aguan Hong[1], Xiang Yi[1], Yanjun Wang[1], Jianmin Hu[2], Zhantao He[1], Guohao He[1], Yang Yang[3], Jiexin Lai[3], Hongli He[1], Lina Su[1], Zhenyu Deng[2], Jingting Xie[2], Shaqi Yang[2], Hongkun Zhou[2], Lingeng Zheng[2], Sicheng He[1], Pei Qin[1], Haoshen Zhu[1]; [1]SCUT, China, [2]CAS, China, [3]UTS, Australia

Abstract: The ultra-high-precision wireless sensing capability is in high demanded, but current radars face bandwidth and cost problems. This paper presents a terahertz (THz) ultra-broadband FMCW radar using a sparse synthetic bandwidth architecture. Using a 40-nm CMOS technology, a dual-band sparse SBR prototype with substrate-coupling antenna and reconfigurable polarization is proposed, capable of achieving 141~310GHz synthetic operating frequencies (i.e. 169 GHz/74.9% synthetic bandwidth) and 1.0 mm range resolution.

RTu3B-3 14:10

A 108-to-141.8GHz 27.1%-Tuning-Range Synthesizer Employing a Dual-Reference-FTL Sub-Sampling PLL and 3rd-Harmonic-Enhancement Class-F VCO and Injection-Locked Frequency Tripler

Khoi T. Phan, Howard Cam Luong; HKUST, China

Abstract: A sub-THz frequency synthesizer employs a cascade of a sub-sampling PLL featuring a frequency-tracking loop with dual co-prime sub-sampling factors for an infinite lock-in range, a 3rd harmonic-amplitude-enhancement class-F VCO, a harmonic-rejection-enhancement class-F ILFT, and a feed-forward locking-range enhancement. The proposed synthesizer measures 27.1% frequency tuning range from 108 GHz to 141.8 GHz with maximum output power of -22dBm, -3dB bandwidth of 25GHz while consuming 38mW.

RTu3B-4 14:30

A Fully Integrated 263-GHz Retro-Backscatter Circuit with 105°/82° Reading Angle and 12-dB Conversion Loss

Mingran Jia, Jinchen Wang, Jaehong Jung, Xibi Chen, Eunseok Lee, Anantha P. Chandrakasan, Ruonan Han; MIT, USA

Abstract: This paper presents the first fully integrated on-chip sub-THz retro-backscatter CMOS circuit, operating at 263 GHz. Using the Van Atta reflector principle and a signal swapping and mode-conversion electromagnetic structure, the design achieves retro-directive operation with a 3-dB angle availability of 105°/82°. Fabricated in an Intel-16 CMOS process, the prototype demonstrates BPSK modulation over an input power range of -7 dBm to -13.9 dBm at 263 GHz, exhibiting a measured conversion loss of 12 dB and capability of Mbps-level data rate at 5-cm reader-to-chip distance. These findings validate a low-cost, low-power, wide-angle THz retro-backscatter solution, improving the performance and practicality of ultra-miniaturized tag applications.

RTu3B-5 14:50

A 127-to-156GHz 64QAM/256QAM Zero-IF CMOS Transceiver Chipset Achieving 42dB IRR and 17.8dBm Output Power

Ziyuan Guo, Wei Deng, Weiqi Zheng, Xinyu Jiang, Haikun Jia, Fuyuan Zhao, Hongliang Wu, Baoyong Chi; Tsinghua University, China

Abstract: To address the demand for D-band applications requiring massive access with high modulation orders for users, a DC-coupled zero-IF(ZIF) transceiver chipset is proposed in this paper. To enhance the image rejection ratio (IRR), the transceiver adopts a wideband load-impedance robust stack coupler. To improve linearity, a biasing-free transconductance compensation mixer and an 8-way power combining power amplifier (PA) based on an enhanced magnetic coupling cavity with transmission line (EMCC-TL) are proposed. Measurement results show that the system achieves a maximum IRR of 47dB and an output power of 17.8dBm. Additionally, the transmitter(TX) and receiver(RX) achieve data rates of 6Gbps for 64QAM and 1.6Gbps for 256QAM with a 2GHz variable gain amplifier (VGA) operating bandwidth.

Tuesday, 17 June 2025
13:30–15:10
Room 207
Session RTu3C: High-Speed Circuits and Systems for Photonic and Quantum Applications
Chair: Sushil Subramanian, Intel, USA
Co-Chair: Bahar Jalali Farahani, Cisco, USA

RTu3C-1 13:30
A 19.4-fs_{RMS} Jitter 0.1-to-44GHz Cryo-CMOS Fractional-N CP-PLL Featuring Automatic Bleed Calibration for Quantum Computing

Jinhai Xiao[1], Yong Chen[2], Ningyi Zhang[1], Rui Liu[1], Yuhao Zhang[1], Peng Luo[1], Maliang Liu[1], Yintang Yang[1], Xiaohua Ma[1], Yue Hao[1]; [1]Xidian University, China, [2]Tsinghua University, China

Abstract: This paper presents the first cryogenic fractional-N charge-pump phase-locked loop (CP-PLL) operating at 4K, which can provide ultra-low-jitter clocks for data converters and precisely matched pump sources for the parametric amplifiers in superconducting quantum computers, thereby enhancing the accuracy of qubit control and the purity of the readout signal. Realized in a 28-nm CMOS, the CP-PLL prototype demonstrates stable operation across an ultra-wide temperature range from 4 K to 300 K, with an ultra-low jitter of 19.4 fs and a reference level of below -71 dBc, while offering a wide output frequency range from 0.1 to 44 GHz. Through the implementation of automatic bleed calibration, integer boundary spurs are further suppressed by an additional 40 dBc.

RTu3C-2 13:50
A Low-Power High-Dynamic-Range Analog Correlator Based on Parametric Multiplication and Integration

Amirhossein Aalipour Hafshejani, Yuanxun Ethan Wang; University of California, Los Angeles, USA

Abstract: This paper presents an analog correlator for radar and communication applications. The proposed correlator leverages a parametric mixer as the RF multiplier core, enabling a high dynamic-range while being low-power due to its fully passive architecture. Fabricated using 22-nm CMOS FDSOI technology, the prototype achieves a measured hardware dynamic range of 55 dB and supports a template symbol rate of 1 GSym/s with a scalable integration time. Additionally, the correlator unit can be extended into a multi-tap correlator network, delivering a computing efficiency of 300 TOPS/W. Comprehensive time- and frequency-domain characterization of the chip prototype demonstrates its effectiveness in applications such as time-of-arrival estimation and signal detection.

RTu3C-3 14:10

A 204GS/s 1-to-2 Analog Demultiplexer in 22nm FDSOI CMOS

Truman Jian, Rafid A. Khan, Ashley Rivera, Danylo Tkachenko, Sorin P. Voinigescu; University of Toronto, Canada

Abstract: A 204GS/s 1-to-2 analog demultiplexer (ADEMUX) is reported with a measured bandwidth of 60 GHz and a hold-mode isolation > 20 dB up to 67 GHz. It operates with rail-to-rail sampling clock signals up to at least 102 GHz, the highest in CMOS. A SFDR of 32 dB was measured for 11GHz, 600mV$_{ppd}$ sinusoidal inputs sampled with a 64GHz clock. Large signal operation was demonstrated by demultiplexing a 92GBaud (184Gb/s) PAM-4 input into two 46Baud PAM-4 output streams sampled on opposite phases of the 46GHz clock signal. The data path of the ADEMUX consumes 48 mW from 0.8 V, while the power consumption of the clock amplifier is 109 mW from 0.8V and 1.2V supplies.

RTu3C-4 14:30

A 224-Gb/s PAM-4 Linear Distributed Driver for Silicon-Photonic Modulators in SiGe BiCMOS

Han Liu[1], Ruogu Deng[2], Zizheng Dong[1], Guike Li[1], Jian Liu[1], Nanjian Wu[1], Wim F. Cops[3], Tao Chen[3], Liyuan Liu[1], Nan Qi[1]; [1]CAS, China, [2]UCAS, China, [3]Shenzhen Sibroad Microelectronics, China

Abstract: A 224-Gb/s PAM-4 linear distributed driver for silicon-photonic (SiPh) Mach-Zehnder modulators (MZM) is presented in 180-nm SiGe BiCMOS. Equalization is integrated to enhance high-frequency components, compensating for SiPh MZM roll-off and interconnect loss. The driver employs a distributed amplifier structure with BJT-based drive cells. Within each cell, a capacitive-division topology minimizes the effect of BJT's input resistance. The artificial transmission line (ATL) of the amplifier features an m-derived termination for improved port impedance matching. A trimming shield technique in the layout design addresses non-idealities, such as high-frequency peaking and reflections. Experimental results demonstrate a typical bandwidth of 65 GHz with >9-dB maximum equalization capability. Eye diagrams for NRZ/PAM-4 modulation schemes and various bit rates are measured with a maximum output swing of 3.917 V$_{ppd}$. Error-free performance up to 224 Gb/s PAM-4 is confirmed through bathtub-curve tests.

RTu3C-5 14:50

A ±1V-DC to 20-GHz Front-End Chipset with 1.5-Vpp AC and 0.5-to-1V DC Outputs for Direct Sampling Real-Time Oscilloscopes

Zhaowu Wang[1], Xinyan Li[1], Chi Zhang[1], Xiaochen Tang[1], Ronglin Chen[1], Ze Yu[1], Ruilin Liao[1], Zhenyu Wang[1], Yicheng Wang[1], Xinyi Jiang[1], Yiming Xu[1], Zhiyu Wang[2], Shengchuan Chen[2], Kai Kang[1], Yue Zhang[2], Yong Wang[1]; [1]UESTC, China, [2]Jiujin Technology, China

Abstract: This paper presents a 20 GHz DC-coupled RF front-end chipset for direct sampling digital real-time oscilloscopes. The chipset consists of four chips: a DC canceling amplifier (DCCA), a distributed active balun (DAB), an equalizer, and a dual differential output variable gain amplifier (DDO-VGA). The DCCA cancels the input DC voltage with a range of ±1V. The DAB achieves single-ended to differential conversion in a wideband starting from DC. The DDO-VGA has two well balanced differential outputs with output DC adjustment. All four chips are DC-coupled and the DC voltages in inter-stages are shifted to 0 V. This chipset is prototyped with a 0.10-μm GaAs pHEMT technology. The measurements of the front-end show a 4.5-to-6.5dB noise figure, 23-dB gain tuning range, and <1-dB/V gain variation across ±1V input DC over DC-to-20 GHz bandwidth.

Tuesday, 17 June 2025
15:40–17:20
Room 203
Session RTu4A: Circuit Techniques for Radar and Phased Array
Chair: Roxann Broughton-Blanchard, Analog Devices, USA
Co-Chair: Chun-Huat Heng, National University of Singapore, Singapore

RTu4A-1 15:40
A 15/30/60-GHz 1TX/4RX Radar Chipset Achieving 6° Angular Resolution Using Frequency Dimension for Virtual Aperture Expansion

Ruilin Liao[1], Haoran Wang[1], Jingzhi Zhang[1], Wei-Han Yu[2], Yue Song[1], Hongyang An[1], Huihua Liu[1], Kai Kang[1]; [1]UESTC, China, [2]University of Macau, China

Abstract: The angular resolution of a millimeter-wave frequency-modulated continuous-wave (FMCW) radar can be significantly improved by stimulating antenna arrays with multiple frequencies, thus diversifying electrical distances under a fixed physical distance across antenna elements to expand the virtual aperture. With three different stimulating frequencies, the radar array that includes N transmitters (TX) and N receivers (RX) can form a virtual array of N^6 elements in addition to the multiple-input and multiple-output (MIMO) operation, which creates only N^2 virtual elements. As a proof-of-concept, we demonstrate a single-channel TX chip and a dual-channel RX chip in 65-nm CMOS technology. The chips can operate at 15, 30, and 60 GHz with >23% bandwidth. The TX has 11.8, 10.1, and 12.0 dBm output power, while the RX has 9.8, 12.6, and 12.4 dB noise figure and -0.7, 1.5, and -0.2 dBm out-of-band (OOB) input 1-dB compression point (IP1dB), measured at 15, 30, and 60 GHz respectively. In the system demonstration, we use 1 TX chip and 2 RX chips to form a 1 TX and 4 RX demonstration board. The over-the-air (OTA) demonstration shows a 6° angular resolution, which is improved by 4× compared to the conventional 1 TX and 4 RX radar system.

RTu4A-2 16:00
An 8-Element 800MHz BW 0.083mm²/element Scalable Current-Mode True-Time-Delay Analog Combiner for Low SWaP-C Antenna Arrays

Ajinkya Kharalkar[1], Paavan Gouniyal[1], Sumit Khalapure[1], Shubham Jain[1], Rajesh Zele[1], Sreeni Poolakkal[2], Soumen Mohapatra[2], Subhanshu Gupta[2]; [1]IIT Bombay, India, [2]Washington State University, USA

Abstract: This paper presents a scalable current-mode true time delay (CMTTD) analog baseband combiner for large antenna arrays. The proposed combiner uses current-mode signal addition and alleviates the scalability-bandwidth trade-off in the state-of-the-art (SOTA) switched-capacitor-based combiners. An improved current-mode sample-and-hold (CSH) cell using a replica branch is proposed for wideband operation. A constant-slope-based phase interpolator (PI) generates programmable clock phases for signals from different antenna elements. The CMTTD IC is prototyped in 65nm CMOS technology and supports 8 antenna elements with up to 800MHz signal bandwidth. The combiner achieves a measured delay resolution of 4.59ps, signal-to-noise-and-distortion

(SINAD) ratio of 41.1dB, and 37.3dB at signal frequencies of 200MHz and 800MHz respectively, and EVM of -20.35dB for 16QAM signal at 1.652 Gb/s data rate. The IC occupies an active area of 0.083 mm^2 per antenna element while consuming 7.5mW DC power per antenna element from a 1V supply.

RTu4A-3 16:20

A Compact, 17.8TOPS/W, 2Gbps Programmable Analog Matched Filter and Coherent Accumulator for 79GHz PMCW Radar

Hongzhe Jiang, Chuhan Xue, Jingyi Huang, Peter R. Kinget; Columbia University, USA

Abstract: We present an analog matched filter (MF) and coherent accumulator for 79GHz phase modulated continuous wave (PMCW) radar. The MF uses a current-switching-based architecture, eliminating the high-speed front-end ADC while operating up to 2Gbps with a programmable sequence length up to 768. The coherent accumulator combines accumulation and digitization with a single-slope-ADC-based structure. The prototype has an area 2.57mm^2 while consuming 202.4mW. The MF achieves a power efficiency of 17.8 TOPS/W and an area efficiency of 0.00063mm^2/len. The coherent accumulator supports 88 range bins resulting in a 7.5cm resolution.

RTu4A-4 16:40

A 28-nm 9-mm High-Resolution Multi-Mode IR-UWB Radar SoC with 16-GS/s Equivalent-Time Sampling for Non-Contact Detection of Human Vital Signs

Peng Luo[1], Yong Chen[2], Yuyang Liu[1], Ruan Jiang[1], Jinhai Xiao[1], Maliang Liu[1], Yintang Yang[1], Xiaohua Ma[1], Yue Hao[1]; [1]Xidian University, China, [2]Tsinghua University, China

Abstract: This paper presents a 9-mm high-resolution multi-mode impulse radio ultra-wideband (IR-UWB) radar system on chip (SoC) for the non-contact detection of human vital signs. It incorporates a radio-frequency front-end transceiver, a 4-GS/s 8-channel time-interleaved analog-to-digital converter, a 4-phase clock generator, and a digital part. The proposed all-digital transmitter has two operation modes, namely, a voltage control delay line (VCDL) mode and a modulated pulse mode. For alignment in the equivalent time sampling (ETS) mode, an on-chip IR-UWB state machine is devised to control the IR-UWB SoC operation. The IR-UWB chip is prototyped in a 28-nm CMOS process. A clear walk pathway of up to 3.75 m is measured in the VCDL mode. A maximum detection range of 10 m is tested in the 1-bit modulated pulse mode and a range of up to 12 m is measured under the 5-bit barker code modulated pulse mode. Clear breath detection is executed in the ETS mode at a detection distance of 2.5 m. The total area of the chip is 1.08×1.125 mm^2.

RTu4A-5 17:00

A Fully-Integrated Doppler-Assisted FMCW Radar with Low Hertz Range Noise Figure for Indoor Localization and Vital Sign Sensing

Yuqin Zhang[1], Zitong Zhang[1], Zhiluo Zhang[1], Zhenyu Zhang[1], Yue Zhu[1], Ruilai Xu[1], Ying Liu[1], Shixiang Ding[1], Jikun Wang[1], Kaige Wang[1], Dalin Li[1], Peng Wang[1], Guangsheng Chen[1], Hao Deng[2], Leilei Huang[1], Chunqi Shi[1], Jinghong Chen[2], Runxi Zhang[1]; [1]East China Normal University, China, [2]University of Houston, USA

Abstract: This paper presents a Doppler-assisted frequency modulated continuous wave (FMCW) radar that leverages the benefits of FMCW's range resolution and Doppler's sensitivity for indoor applications. The Doppler mode reuses circuit blocks in the FMCW mode to reduce power consumption and area overhead. Low-frequency noise contributions from the receiver circuits are analyzed and an "RF+LO+BB" combined noise figure (NF) optimization scheme is proposed to minimize the low-frequency noise. The radar employs a nested phase-locked loop frequency synthesizer with low phase noise and incorporates an optimized ΔT_{step} selection technique to improve chirp linearity. Designed in a 55-nm CMOS technology, the radar achieves NFs of 32 dB and 12 dB at 10 Hz and 1 kHz, respectively, and a chirp linearity of 0.0039% over a 3.52 GHz chirp bandwidth (BW), leading to a range resolution of 4.7 cm. The radar occupies an area of 12.7 mm^2, and consumes 220 mA of current in the FMCW mode and 160 mA in the Doppler mode under a power supply of 3.3 V.

Tuesday, 17 June 2025
15:40–17:20
Room 205
Session RTu4B: Circuit Blocks for D-Band Integrated Systems
Chair: Muhammad Waleed Mansha, Nokia Bell Labs, USA
Co-Chair: Kenichi Okada, Science Tokyo, Japan

RTu4B-1 15:40
110-to-140GHz Frequency Tripler with 13% Efficiency, 7.2dBm Psat Using Adaptive Biasing and 3rd Harmonic Boosting in 22nm FDSOI

Victor Lasserre, Sarah Koop-Brinkmann, Christian Ziegler, Finn-Niclas Stapelfeldt, Vadim Issakov; Technische Universität Braunschweig, Germany

Abstract: This paper presents a high-efficiency D-band frequency tripler in 22nm FDSOI CMOS. The operation point is chosen using drain current Taylor series derivation to boost the 3rd harmonic (H3) adaptively. The tripler core transitions for increasing input power (P_{in}) from compressive to expansive behavior thanks to the proposed biasing scheme. At low P_{in} of -10dBm the tripler achieves a peak conversion gain of 11 dB thanks to step-up balun and capacitive over-neutralization. Yet, at high P_{in} of 4 dBm, the 5th-order nonlinearity boosts 3rd-harmonic and enables achieving 13% peak efficiency and Psat of 7.2 dBm.

RTu4B-2 16:00
A 126–137GHz Regenerative Frequency Shifter in 22nm FDSOI

Victor Lasserre[1], Finn-Niclas Stapelfeldt[1], Sarah Koop-Brinkmann[1], M. Dimić[2], F. Padovan[2], Vadim Issakov[1]; [1]Technische Universität Braunschweig, Germany, [2]Infineon Technologies, Austria

Abstract: This paper presents the concept of a regenerative D-band frequency shifter. The circuit can be viewed as an extension of the Miller fractional frequency generator. Yet, as opposed to the second-order Miller modulator, we propose an architecture based on two mixers. By careful choice of the bandpass filter networks, providing sufficient loop gain, and enforcing loop phase conditions for the wanted spur, one can suppress the unwanted spurs and support the loop oscillation at the desired frequency. The output signal is only present when an input is applied. The main spur at the output f_{OUT} follows the input frequency f_{IN} as $f_{OUT} = f_{IN} + f_{OFFSET}$. To verify the proposed concept we present an integrated circuit realized in 22nm FDSOI CMOS. Among the different applications of this circuit, we find a low-power alternative to a fractional multiplier for generating narrowband carrier frequencies in the LO chain. For example, for an input frequency of 80 GHz, the circuit yields an output at 140 GHz, resulting in an effective fractional multiplication ratio of 7/4. The proposed circuit consumes 81mW from a single 0.8V supply and operates over an output frequency range of 126–137 GHz. A peak output power of 4.9dBm is measured at 127 GHz. The spur suppression is above 29 dB. To the best of authors' knowledge, this is the first dynamic frequency shifter in D-band.

RTu4B-3 16:20

A 200GHz Quasi-Circulator with a Widely Tunable Termination for >30dB Isolation and 8.3dB SNR Degradation in a 22nm FD SOI Process

Hyunwoo Seo, Omeed Momeni; University of California, Davis, USA

Abstract: This paper presents a quasi-circulator design optimized for sub-THz applications, operating at 200 GHz and fabricated using 22-nm FD SOI technology. The proposed design features a coupled Coplanar Waveguide (CPWG) and novel tunable terminations, achieving a wide impedance tuning range to address antenna mismatches up to -15 dB. Measurement results demonstrate a TX-to-RX isolation of >30 dB at 200 GHz with over a 7.2-GHz bandwidth and insertion losses of 5 dB and 3.2 dB for TX-to-ANT and ANT-to-RX paths, respectively. This compact, low-power design achieves minimal IL at 200 GHz, offering a robust solution for high-frequency systems.

RTu4B-4 16:40

An Ultra-Compact and Wideband D-Band Power Amplifier in 28nm CMOS with Area-Efficient Coupled Line-Based Matching Network

Hyo-Ryeong Jeon[1], Hokeun Lee[1], Sang-Gug Lee[1], Kyung-Sik Choi[2]; [1]KAIST, Korea, [2]Yonsei University, Korea

Abstract: This paper presents an ultra-compact and wideband D-band power amplifier (PA) utilizing area-efficient coupled line (CPL)-based matching networks. The design overcomes the size limitation in the signal propagation direction by employing CPL-based matching networks and shunt capacitors, enhancing bandwidth while achieving a compact form factor. Implemented in a CMOS 28nm process, the proposed 3-stage PA achieves a 3-dB bandwidth of 45.1 GHz with a peak gain of 12.2 dB, an OP1dB of 7.6 dBm, and a power-added efficiency (PAEmax) of 10.2%. With a core area of only 0.24×0.065 mm^2, the PA achieves the highest OP1dB per unit area among D-band PAs based on CMOS bulk process, making it a leading candidate for 2-D scalable D-band beamforming transmitter arrays.

RTu4B-5 17:00

A 110-to-203-GHz 18.3-dBm Broadband Power Amplifier Using Modified Three-Conductor Baluns in 130-nm SiGe BiCMOS

Shuyang Li[1], Shouqing Fu[1], Xin Liu[2], Quanqin Liao[3], Huibo Wu[1], Shunhua Hu[1], Wenhua Chen[1]; [1]Tsinghua University, China, [2]Xidian University, China, [3]Wuhan University, China

Abstract: This paper presents a broadband high-power sub-terahertz (sub-THz) power amplifier (PA). By integrating the traditional three-conductor (TC) balun with coupled lines (CP lines), a modified TC balun is proposed for broadband low-loss power combining without significantly increasing the chip area. A pair of these baluns is further connected through a T-junction to form a four-way hybrid power combiner. Based on this combiner, a three-stage four-way PA has been fabricated in a 130-nm SiGe BiCMOS technology. The PA achieves a maximum small-signal gain of 25.2 dB and a 3-dB small-signal bandwidth of 65 GHz from 110 to 175 GHz. It shows a peak saturation output power (P_{SAT}) of 18.3dBm and delivers more than 15.3-dBm P_{SAT} from 110 to 203 GHz within a small core area of 0.17mm^2.

Tuesday, 17 June 2025
15:40–17:20
Room 207
Session RTu4C:
Innovations in Low-Power, High-Performance Receiver Front-Ends
Chair: Marcus Granger-Jones, Qorvo, USA
Co-Chair: Andrea Bevilacqua, Università di Padova, Italy

RTu4C-1 15:40
A 2.4GHz 676μW Receiver Front-End with Passive Analog FIR Filtering Embedded in Down-Converter Achieving >60dB Blocker Rejection
Wenjing Zhang, Chao Chen, Yu Guo, Yan Zhao, Wenhan Yang; Southeast University, China
Abstract: This paper presents a 2.4GHz low-power receiver front-end that embeds passive analog finite impulse response (AFIR) filtering within the down-converter stage to enhance out-of-band blocker rejection. Distinct from conventional passive down-converters, the down-converted current is periodically conducted according to the FIR sequence and weight coefficients in each step, achieving analog FIR filtering after integration and sampling. The weight coefficients for each step-phase are precisely implemented by periodically time-varying passive switch arrays. The chip prototype, fabricated in a 28-nm process, occupies an active area of 0.24mm^2. It attains a stop-band rejection exceeding 60dB, with a transition band only four times the signal bandwidth. Owing to the passive AFIR introducing an out-of-band rejection characteristic without additional current consumption, the total power consumption of the proposed front-end is only 676μW at a supply voltage of 0.65V.

RTu4C-2 16:00
10-to-30-GHz Blocker-Tolerant Mixer-First Receivers with 40-dB/Decade Transition-Band Roll-Off and Maximum 61.7-dB LO-to-RF Isolation
Kai Li, Shaoquan Wang, Keping Wang; Tianjin University, China
Abstract: This paper presents two RF-to-Millimeter-Wave blocker-tolerant mixer-first receivers. A feedforward path with phase compensation is designed parallel to the main path to cancel the out-of-band (OOB) blocker. It can break the trade-off between mixer switch size and OOB rejection, thereby simultaneously achieving high transition-band roll-off and excellent LO-to-RF isolation. In addition, a balanced input network is employed to achieve broadband input matching. LC tanks are introduced into the second design to further improve the OOB rejection. Fabricated in a 130 nm SOI CMOS process, the proposed receivers achieve a transition-band roll-off of 40 dB/decade and OOB rejection of 25–55 dB in the frequency range of 10–30 GHz. It also achieves a maximum LO-to-RF isolation of 61.7 dB at 11 GHz.

RTu4C-3 16:20

An 11.5mW 12.3–14.5GHz Passive Mixer-First Receiver Front End Achieving 4.2dB NF and -5dBm B1dB

Alain H. Antón, Jamie C. Ye, Sanaz Sadeghi, Alyosha C. Molnar; Cornell University, USA

Abstract: This work presents a low power, high dynamic range passive mixer-first receiver for the proposed 6G FR3 band. The proposed architecture achieves high performance at low power by directly driving the mixers with harmonically enhanced (HE) waveforms generated by a class F^{-1} quadrature oscillator. Additionally, an overlap suppression front-end (FE) network is implemented that enables a wide range of mixer biases for optimal performance resulting in a more robust design to process and voltage variations. The 12.3–14.5GHz prototype is implemented in a FinFet process exhibiting a 4.2dB noise figure (NF), -5dBm Blocker 1dB (B1dB) compression point, and 7.3dBm out-of-band (OOB) third-order input intercept point (IIP3) with a total power consumption of 11.5mW while occupying 0.28mm^2.

RTu4C-4 16:40

A 4.2dB NF and 39dB Passive Gain Ultra-Low Power Receiver Front-End with an RF-IF Dual-Stage Capacitive Stacking Technique

Jin Jin, Zhepu Xu, Haipeng Bai, Bowei Xiao, Wen Wu, Tongde Huang; NJUST, China

Abstract: This paper introduces a novel RF-IF dual-stage capacitive stacking technique for ultra-low-power 2.4 GHz receiver front-ends. The gain of the proposed front-end is fully composed of the passive components (i.e., transformer and the switched-capacitor (SC) network), hence has good linearity. Furthermore, an unbalanced topology is adopted in the RF-SC section for gain and noise optimization. Fabricated in 22 nm CMOS, this work achieves 11.1 dBm OOB-IIP_3, 4.2 dB noise figure, and 39 dB passive gain while consuming 360 μW power.

RTu4C-5 17:00

A 0.2–6GHz 65nm CMOS Active-Feedback LNA with Threefold Balun-Error Correction and Implicit Post-Distortion Technique

Benqing Guo; CUIT, China

Abstract: We propose a wideband low-noise amplifier (LNA) with balun-error correction and linearity enhancement. Towards active feedback LNA in double CS stages, a threefold correction of voltage ratio preset, differential current balancer (DCB), and high-frequency RC compensation is applied to lower balun error across the passband. A linearization structure without penalty of add-on parasitic and noise is proposed herein. The active feedback path is reused as post-linearization to tap and cancel distortion of input CS stages at the LNA outputs. The distortion of the active load is regulated by tuning the output CM level via a CMFB block, to compensate for the residual distortion offset. A CM-DM noise conversion through asymmetry of output resistance is suppressed by the OTA filtering. Measurement results show that within the bandwidth of 0.2–6 GHz, the LNA prototype implemented in standard 65 nm CMOS technology, achieves a gain of 19.5 dB, a noise figure (NF) of 2.8 dB. Across the passband, gain and phase errors are within 0.5 dB and 1° while the average IIP3 reaches 2.5 dBm. The proposed circuit consumes 14.7 mW and occupies core area of 0.095 mm^2.

WORKSHOPS

Workshops are offered on Sunday, Monday and Friday at the Moscone Convention Center. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

WSC (Half-Day): Sunday 08:00–11:50
AI/ML for Next-Generation Microwave Design and Modeling: From Devices to Systems

Sponsor: **IMS/RFIC**

Organizers: **Kamal Samanta**, *AWMT*
Caglar Ozdag, *IBM Research*

Abstract: As the world rapidly embraces Artificial Intelligence (AI) and Machine Learning (ML) across various industries, the key question arises: how can we best leverage AI/ML to transform our own field? This workshop addresses this critical question by highlighting cutting-edge research from industry and academia experts who are using AI to transform microwave design. With new techniques emerging at an unprecedented pace, the workshop will shine a light on their revolutionary potential in RF and microwave engineering. The focus is on how AI is streamlining design processes, optimising results and enhancing productivity, ultimately helping engineers to navigate increasingly complex challenges in ways that were previously not possible. Our six distinguished speakers, all pioneers in their respective areas, will present a comprehensive view of AI's role in advancing the entire spectrum of microwave engineering, including topics such as device modeling (including GaN PA), component synthesis (together with inductor, transformer and other passives), circuit (including RFIC and MMICs) and system design, performance optimisation (like PA linearisation) and electronic design automation (EDA) covering RF to THz frequencies. Attendees will gain valuable insights into how AI/ML is reshaping the future of microwave engineering, providing the tools and perspectives needed to stay ahead and empowering innovation and realisation of advanced devices to highly integrated modules/systems, enabling applications for 5G, 6G and beyond.

Speakers:

1. "State-of-the-Art Microwave Device Modeling Enabled by Artificial Intelligence and Machine Learning", **Jianjun Xu**, *Keysight Technologies*
2. "Physics-Informed Machine Learning-Based Digital Predistortion of RF Power Amplifiers", **Tao Yu**, *Analog Devices*
3. "AI/ML Techniques Supporting the Design Automation of RF/mm-Wave Devices and Circuits", **Fábio Passos**, *Instituto Superior Técnico*
4. "AI-Enabled Discovery of New RF/mm-Wave Architectures and Synthesis of End-to-End RFICs", **Kaushik Sengupta**, *Princeton University*
5. "AI-Based Algorithms in Analog Circuit Topology Generation and Beyond", **Xin Zhang**, *IBM*
6. "AI/ML for Microwave Modeling and Optimization", **Qi-Jun Zhang**, *Carleton University*

WSA (Full-Day): Sunday 08:00–17:20
Frequency Synthesizer Design – From Fundamentals to Advanced Techniques

Sponsor: **RFIC**

Organizers: **Wanghua Wu**, *Samsung*
Ahmed Elkholy, *Broadcom*
Teerachot Siriburanon, *University College Dublin*
Salvatore Finocchiaro, *Qorvo*

Abstract: Frequency synthesizers are among the most critical blocks in wireless, wireline, and digital clocking applications. This workshop will cover both the fundamentals and the latest advances in frequency synthesis circuits and systems to efficiently generate LO signals with low phase noise, low spurious tones, and large modulation bandwidth. Prior-art techniques will be discussed in-depth, such as energy-efficient reference clocks, ultra-low phase noise voltage-controlled oscillators, digital PLL fundamentals, modern low-jitter fractional-N PLLs using both LC-oscillators and ring-oscillators. Special attention will also be given to pulling and spur mitigation techniques and PLL-based chirp generators for FMCW radar applications.

Speakers:

1. "Reference Oscillator Architectures and Design Considerations", **Danielle Griffith**, *Texas Instruments*
2. "Beyond All-Digital PLL for RF and mm-Wave Frequency Synthesis", **Robert Bogdan Staszewski**, *University College Dublin*
3. "Spur Analysis and Mitigation Techniques for Fractional Synthesizer", **Michael Peter Kennedy**, *University College Dublin*
4. "Calibration-Free DSM Noise Suppression in Analog Frequency Synthesizers", **Dihang Yang**, *Broadcom*
5. "Design of a Low-Jitter Ring-Oscillator-Based Fractional-N Digital PLL", **Jaehyouk Choi**, *Seoul National University*
6. "(Voltage-Controlled) Oscillators with Ultra-Low Phase Noise", **Andrea Mazzanti**, *Università di Pavia*
7. "Design and Performance Characterization of PLL-Based Chirp Generators for FMCW Radar Applications", **Pratap Tumkur Renukaswamy**, *imec*

WSB (Full-Day): Sunday 08:00–17:20
Integrated Communications and Sensing: Circuits, Systems, Algorithms, and Applications

Sponsor: **RFIC**

Organizers: **Alberto Valdes-Garcia**, *IBM Research*
Yahya Tousi, *University of Minnesota*
Oren Eliezer, *Samsung*

Abstract: Integrated communication and sensing capabilities are on a strong trajectory to become an integral part of the next generation of wireless systems. While the exploration of these techniques started decades ago, their development has accelerated with the increasing availability of highly integrated Si-based transceivers, baseband compute capabilities, and wireless testbeds for experimentation, and more recently AI. Nevertheless, the development of wireless systems with efficient joint communication and sensing capabilities remains a challenging multi-disciplinary task where EM, circuit design, signal processing, and ML techniques are relevant. The goal of this workshop is to bring together a set of active researchers on these topics to share their vision and expertise and enhance the cross-disciplinary awareness and understanding between the RFIC and systems communities. The speakers span academic and industrial research institutions from across the globe and the presentations will cover circuit, algorithm, and application aspects.

Speakers:

1. "Integrating Sensing Functionality in Mobile Communication Networks", **Henrik Holter**, *Ericsson*
2. "Integrated Beamforming: Where Directional Communication Meets Sensing for Seamless Connectivity and Detection", **Tumay Kanar**, *Renesas*
3. "Toward Integrated mm-Wave Communication and Sensing with Compressive Beam Shaping Techniques", **Yasaman Ghasempour**, *Princeton University*
4. "Sensing with mm-Wave 5G: Extracting Spatial Information Leveraging Directional Beams", **Alexandra Gallyas-Sanhueza**, *IBM Research*
5. "Joint Sensing and Communication Under Hardware Impairments", **Nuria González-Prelcic**, *University of California, San Diego*
6. "Broadband mm-Wave ICs for Joint Sensing and Communication Across 30–100GHz", **Kaushik Sengupta**, *Princeton University*
7. "Adaptive mm-Wave MIMO Front-Ends for Energy-Efficient Sensing", **James F. Buckwalter**, *University of California, Santa Barbara*

WSD (Full-Day): Sunday 08:00–17:20
Low-to-Ultra-Low Power RFIC: Technologies, Architectures and Circuit Design

Sponsor: **RFIC**

Organizers: **Andreia Cathelin**, *STMicroelectronics*
Yann Deval, *University of Bordeaux*

Abstract: The workshop will delve into the design of ultra-low and low-power RF integrated circuits, emphasizing various applications where energy efficiency is paramount. This is particularly relevant within the Internet of Things (IoT) domain, which spans multiple application fields. Given that power consumption is a critical concern for all battery-powered or always-on applications, the workshop will comprehensively address this issue. The workshop will commence with two presentations focusing on Silicon technologies optimized for such applications, specifically FD-SOI, FinFET, and emerging technologies such as gate-all-around nanoribbon transistors. Following this, two additional presentations will explore the trade-offs associated with the most power-intensive components, namely the frequency synthesis unit and power amplifiers. The subsequent four presentations will concentrate on architectural innovations pertinent to low and ultra-low power RFIC solutions. This segment will begin with discussions on novel sensor interface solutions, such as event-driven operation systems. The final three presentations will address comprehensive system solutions designed for wireless environments, achieving power consumption down to sub-microWatt levels, and secure biomedical applications.

Speakers:

1. "Leading-edge Process Technologies for Efficient Low-power Systems", **Rami Said** , *Intel*
2. "FD-SOI: game changer in the IoT arena", **Andreia Cathelin**, *STMicroelectronics*
3. "Design Methodologies for Low-Power Frequency Synthesizers", **Asad Abidi**, *University of California, Los Angeles*
4. "Digital-PA: Ubiquitous from Low-to-High Power", **Jeff Walling**, *Virginia Polytechnic Institute and State University*
5. "Potential of event-driven continuous-time digital signal processing for ultra-low-power applications", **Antoine Frappé**, *Université de Lille*
6. "Next-Gen End-Point Radios Down to Sub-µW — Enabling Ubiquitous and Frictionless Immersion in Existing Wireless Environments", **Massimo Allioto**, *National University of Singapore*
7. "Body Area Network — Connecting and Powering Things Together Around the Human Body", **Jerald Yoo**, *Seoul National University*
8. "Living Networks: Bioelectronic IoT and the Future of Secure, Energy-Efficient Wireless Systems", **Rabia Yazicigil**, *Boston University*

WSF (Full-Day): Sunday 08:00–17:20
RF-FE and Phased Array System for 5.5G and 6G

Sponsor: **RFIC**

Organizers: **Hao Gao**, *Technische Universiteit Eindhoven*
Didier Belot, *STMicroelectronics*
Yun Fang, *Southeast University*

Abstract: With rapid technological advances, the scope of communication systems is expanding significantly. Among the most groundbreaking developments are the use of mm-wave and sub-THz frequencies, which are poised to revolutionize wireless communication by unlocking unprecedented capabilities. This workshop will explore the transformative potential of mm-wave and sub-THz technologies, covering the frequency range from 30GHz to 300GHz. Once underutilized, these high-frequency ranges are now pivotal to major technological breakthroughs. Central to this advancement is the broadband front-end, which is crucial for effectively harnessing these frequencies for cutting-edge applications. A major focus of the workshop is the advancement of high-frequency communication technologies. Attendees will examine innovations in ultra-fast data transfer, low-latency networks, and the integration of mm-wave and sub-THz frequencies within wireless systems. These advances are reshaping connectivity, supporting the rollout of 5.5G and 6G networks, enhancing autonomous vehicles, and enabling smart cities. The workshop will also highlight the potential of 5.5G and 6G technologies to transform various industries. Additionally, the integration of Reconfigurable Intelligent Surfaces (RIS) and Radio-over-Fiber (RoF) technologies will be discussed, showcasing their critical roles in optimizing signal quality and extending network reach in the evolving landscape of 5.5G and beyond.

Speakers:

1. "Wideband TTD Reflectarrays for Multi-Standard 5G/6G Systems", **Gabriel M. Rebeiz**, *University of California, San Diego*
2. "mm-Wave and Sub-THz CMOS Front-Ends for 6G", **Kenichi Okada**, *Science Tokyo*
3. "Challenging CMOS with Beamforming in the D-Band", **Giuseppe Gramegna, Piet Wambacq**, *imec*
4. "Vision on Phased Arrays Using Meta-Surfaces and on the Implementation of LO Phase Shifting Based on ILOs", **José-Luis Gonzalez-Jimenez**, *CEA-Leti*
5. "Navigating the Challenges of 300GHz CMOS Transceivers: A Comparative Analysis with Photonics-Based and D-Band CMOS Configurations", **Minoru Fujishima**, *Hiroshima University*
6. "Multi-Layer Adaptive Hybrid Beamformers for Multi-Standard and Full-Duplex MIMO Communication", **Susnata Mondal**, *Intel*
7. "Mixed-Signal RFIC in SiGe:C BiCMOS for mm-Wave Antenna-in-Package and Antenna-in-Module Solutions", **Andrea Pallotta, Didier Belot**, *STMicroelectronics*
8. "RF Front-End Technology Beyond 5G", **Rui Hou**, *Ericsson*
9. "Phased Array in mm-Wave and Sub-THz for Communication and Sensing", **Yun Fang[1], Hao Gao[2]**, *[1]Southeast University, [2]Technische Universiteit Eindhoven*

WSG (Full-Day): Sunday 08:00–17:20
RFIC Architectures, Circuits and Systems for LEO SATCOM Broadband Access for 6G NTN

Sponsor: **IMS/RFIC**

Organizers: **Didier Belot**, *STMicroelectronics*
Pierre Busson, *STMicroelectronics*
Salvatore Finocchiaro, *Qorvo*

Abstract: In the context of 6G and beyond, the performance demands are geared towards massive parallelization. For instance, the Non-Terrestrial-Network (NTN) is an essential component of future 6G wireless systems, and the next-generation SATCOM network will play an enabling role to support 6G NTN. High throughput, capacity, and low latency, and beamformed wireless links are the key success factors for NTN. Most existing SATCOM terminals, either on the ground or on the satellite payload, require large-sized phased array systems with 1024 elements or more per array. Such massive parallelization results in significant challenges not only in terms of integration density, but also on calibration and practical operation; a particularly challenging task in SATCOM-on-the-Move (SOTM) systems that necessitate fast beam forming and tracking. In this WS we will have an overview of potential process/circuit/system solutions addressing these challenges.

Speakers:

1. "Ku- and Ka-Band Beamformer with Antenna Arrays", **Hua Wang, Thomas Burger, Tzu-Yuan Huang**, *ETH Zürich*
2. "Multi-Orbit SATCOM Terminals for NTN and the Components that Make These Viable", **Kevin Greene, Nitin Jain, Ryan Jennings**, *Qorvo*
3. "SiGe BiCMOS Process for SATCOM Applications", **Pascal Chevalier, Frederic Gianesello, Vincent Knopik**, *STMicroelectronics*
4. "Building Large-Volume SATCOM Phased Arrays Using Silicon", **Gabriel M. Rebeiz**, *University of California, San Diego*
5. "Ka-Band CMOS TX-RX for SATCOM", **Kenichi Okada**, *Science Tokyo*
6. "InGaAs LNAs for SATCOM", **Fabian Thome**, *Fraunhofer IAF*
7. "SiGe LNA for SATCOM", **Benjamin Blampey, Baudouin Martineau**, *CEA-Leti*
8. "Low-Cost Silicon Beamformers in Ku and Ka Band Powering SATCOM User-Terminals", **Naveen Yanduru**, *Axiro*
9. "Bringing Commercial Cellular Access to Space", **Mohamed Abdalla**, *Analog Devices*

WSH (Full-Day): Sunday 08:00–17:20
Addressing Challenges in System-in-Package and 3D Heterogeneous Integration for mm-Wave Phased Array Systems

Sponsor: **IMS/RFIC**

Organizers: **Salvatore Finocchiaro**, *Qorvo*
Yu Cao, *Qorvo*

Abstract: The ever-increasing demand for high-throughput communication links and high-resolution radar sensors is driving the development of future wireless systems at higher operating frequencies. In order to support multiple functionality, the flexibility requested to those systems, is driving the adoption of large phased array antennas and complex System-in-Package (SiP) Bit-to-RF or Optical-to-RF solutions. Heterogeneous technologies and vertical 3D integration will play a vital role in enhancing the performance and functional density, along with reducing the size and costs, of such RF systems. 3DHI will pose a new set of technology (processes and substrates), design (MMICS, RFIC, analog, power management, passives), packaging and thermal challenges, which will be addressed by renowned experts from Academia and Industry in this workshop.

Speakers:

1. "The Defense Advanced Research Agency's (DARPA) Next Generation Microelectronics Manufacturing (NGMM) Program", **Michael Holmes**, *DARPA MTO*
2. "Glass Packaging for 6G Applications", **Madhavan Swaminathan**, *Pennsylvania State University*
3. "Glass-Based Packaging for Bits-to-RF and 3DHI Systems-in-Package", **Jeb Flemming**, *3DGS*
4. "Opportunities for Millimeter-Wave Front-End Solutions Using Heterogeneous Integration", **James Buckwalter**, *PseudolithIC*
5. "Bits to Beams: How do You Simulate a Heterogeneously Packaged, Digitally Steered Phased Array?", **Paul Mosinkskis**, *Cadence*
6. "Wafer-Scale RF Silicon Interposer Packaging Technology for mm-Wave Phased Arrays and Radars", **Siddhartha Sinha**, *imec*
7. "Advances in Wafer-Level Packaging (WLP) and Heterogeneous Integration for mm-Wave Phased Arrays", **Dino Ferizovic**, *Northrop Grumman*
8. "Glass Core Technology as a Building Block for Advanced Packaging Architectures", **Mohanalingam Kathaperumal**, *Georgia Tech*
9. "Development of Co-Packaged Optics Technology for Photonics Applications", **Tarak Railkar**, *Qorvo*

WSI (Full-Day): Sunday 08:00–17:20
Self-Interference Cancellation Techniques for Future Integrated Communication and Sensing Systems

Sponsor: **IMS/RFIC**

Organizers: **Tong Zhang**, *Google*
Song Hu, *Apple*

Abstract: As wireless communication and sensing systems evolve toward higher data rates and greater spectral efficiency, the integration of self-interference cancellation (SIC) techniques becomes crucial, particularly for enabling simultaneous transmit and receive (STAR) operations in full-duplex (FD) and frequency-division duplexing (FDD) systems. This workshop brings together leading experts to explore the challenges and solutions in SIC for advanced communication and sensing systems. The discussions will cover innovative SIC architectures for integrated radios, with a special focus on FD systems and their applications in 5G and beyond, including mmWave, IoT, radar, biomedical, and quantum systems. Attendees will gain insights into state-of-the-art time-domain and frequency-domain SIC techniques, antenna interface designs, and machine learning approaches for adaptive cancellation. The workshop will also address the transition of these technologies from academic research to real-world deployment, especially in high-performance commercial and defense applications.

Speakers:

1. "Lab-to-Fab Transition of CMOS Simultaneous Transmit and Receive (STAR) Research", **Harish Krishnaswamy**, *Columbia University*
2. "Transceiver Techniques for FDD and Full-Duplex Wireless", **Emanuel Cohen**, *Technion*
3. "Integrated Self-Interference Cancellers at RF for Communication and Radar", **Arun Natarajan**, *Oregon State University*
4. "Self-Interference Cancellation Techniques in Frequency Division Duplexing Receiver Front-Ends", **Danilo Manstretta**, *Università di Pavia*
5. "GHz to Sub-THz In-Band Full-Duplex Operations in CMOS Based on Wave Frequency and Mode Conversions", **Ruonan Han**, *MIT*
6. "Antenna Interfaces with Built-In Self-Interference Cancellation for Future Communication and Sensing Systems", **Negar Reiskarimian**, *MIT*
7. "Opportunities and Challenges on the Next Generation Concurrent Reconfigurable Multi-Radio IoT Devices", **Sai-Wang Rocco Tam**, *NXP Semiconductors*
8. "Integrated Self-Interference Cancelers for Fully-Duplex Radios", **Aravind Nagulu**, *Northeastern University*
9. "Intelligent Self-Interference Mitigation for Integrated Radios", **Jacques C. Rudell**, *University of Washington*

WSJ (Full-Day): Sunday 08:00–17:20
Advanced Power Amplifier Design for Sub-20GHz Wireless Infrastructure

Sponsor: **IMS/RFIC**

Organizers: **Alexandre Giry**, *CEA-Leti*
Jennifer Kitchen, *Arizona State University*

Abstract: As the demand for high-speed wireless communication continues to grow, efficient PA design becomes critical for supporting modern communications network infrastructure, especially in the sub-20GHz spectrum (FR1 and FR3 bands). This workshop will delve into comprehensive design and development of power amplifiers (PAs) for sub-20GHz base station applications. The latest processes and technologies will be covered, focusing on semiconductor advances that drive power handling, linearity, and efficiency. Participants will explore theory and modeling principles to predict performance and optimize PA designs for various operational scenarios. The session will also emphasize architecture and design techniques, addressing key challenges such as linearity, efficiency, and bandwidth. Finally, the workshop will cover module design and integration, where participants will learn about packaging considerations and thermal management to ensure optimal performance in real-world deployments. This workshop is ideal for RF engineers, circuit designers, and researchers aiming to enhance their expertise in cutting-edge PA technology for wireless infrastructure. Participants will gain an in-depth understanding of key PA architecture and design techniques through interactive sessions with practical case studies.

Speakers:

1. "Gallium Nitride on Silicon Carbide Technologies for Sub-20GHz Applications", **Kimon Vivien**, *UMS*
2. "From Component Modeling for Circuit Design to Circuit Modeling for System Design", **Wissam Saabe**, *AMCAD Engineering*
3. "Understanding the Harmonic Balance Simulation Technique for use in the Waveform Engineering of Advanced GaN Power Amplifiers", **Damon Holmes**, *MACOM*
4. "Load-Modulated PA Architecture Comparison Using Non-Linear Embedding", **Patrick Roblin, Dominic Mikrut**, *The Ohio State University*
5. "Antenna-VSWR-Resilient Load-Modulated Balanced Amplifier (LMBA) for Massive MIMO Communications", **Kenle Chen**, *University of Central Florida*
6. "How to Ensure Flexible and Efficient Use of Spectrum, from Advanced 5G Doherty Power Amplifiers to Digitally Assisted Wideband PA for 6G BTS", **Emmanuel Gatard[1], Peter Abdelmalak[1], Stéphane Dellier[1], Shuichi Sakata[2], Takuma Torii[2], Shintaro Shinjo[2]**, *[1]Wupatec, [2]Mitsubishi Electric*
7. "A Fully Integrated Power Amplifier Module with Bias Controller to Tackle 5G mMIMO Basestation Applications at 3.5GHz", **Stephan Maroldt**, *Ampleon*
8. "TBD", **Shishir Shukla**, *Axiro*

WSL (Full-Day): Sunday 08:00–17:20
Sub-THz Power Amplifiers in CMOS, SiGe, and III-V

Sponsor: **IMS/RFIC**

Organizers: **Aritra Banerjee**, *University of Illinois at Chicago*
Susnata Mondal, *Intel*

Abstract: The power amplifier is one of the most critical blocks in the transceiver and obtaining the desired performance from the PA at sub-THz frequencies remains a challenge. At sub-THz frequencies, transistors suffer from reduced gain impacting the performance of the PA. Designing sub-THz PAs with improved power added efficiency (PAE), output power, and linearity is an active area of research. SiGe and III-V technologies such as InP and GaN demonstrate higher fT and fmax than CMOS and as a result, sub-THz PAs designed in these technologies outperform their CMOS-based counterparts. On the other hand, CMOS can achieve better yield and higher level of integration compared to III-V technologies. In this workshop, the speakers will present recent developments in sub-THz PA design in CMOS, SiGe, and III-V technologies demonstrating their comparisons and trade-offs.

Speakers:

1. "InP HBT Technologies for Sub-THz Amplifiers", **Miguel Urteaga**, *Teledyne Scientific & Imaging*
2. "100–300GHz Power Amplifiers: Transistor Limits, Circuit Topologies", **Mark Rodwell[1], Amirreza Alizadeh[2], Ahmed Samir Sayed Ahmed[3], Yuya Nemoto[1], Utku Soylu[1], Miguel Urteaga[4]**, *[1]University of California, Santa Barbara, [2]Keysight Technologies, [3]Cairo University, [4]Teledyne Scientific & Imaging*
3. "Transformer-Based mm-Wave PA Design in CMOS, InP and GaAs", **Patrick Reynaert**, *KU Leuven*
4. "High-Power and Highly Efficient Power Amplifiers for D-Band Applications in Silicon", **Omeed Momeni**, *University of California, Davis*
5. "mm-Wave High Efficiency, High Linearity GaN HEMT, GaAs and InP HBT Power Amplifiers", **Andrea Arias-Purdue**, *HRL Laboratories*
6. "E- and D-Band Common-Base Power Amplifiers in SiGe-BiCMOS with Performance Enhanced by Current Clamping and Device Stacking", **Andrea Bilato, Andrea Mazzanti**, *Università di Pavia*
7. "Sub-THz SiGe HBT Cascode Power Amplifiers with Capacitive Feedback and its Use in a Supply Modulated RF Transmitter Front-End", **Suprovo Ghosh[1], Haidong Guo[2], Kenneth K. O[3]**, *[1]Texas Instruments, [2]ams-OSRAM, [3]University of Texas at Dallas*
8. "Stacked-FET CMOS Power Amplifier for mm-Wave and Sub-THz Applications", **Kyunghwan Kim**, *Samsung*

WSM (Full-Day): Sunday 08:00–17:20
The Technology Landscape of the Wireline and Wireless Optical Communication

Sponsor: **IMS/RFIC**

Organizers: **Bahar Jalali Farahani**, *Cisco*
Mahdi Parvizi, *Cisco*

Abstract: According to Global Market Insights Inc., the optical communication and networking market is expected to grow at a compound annual growth rate (CAGR) of 8.6% from 2024 to 2031, reaching $61.92 billion by 2031. The significant revenue comes from emerging technologies such as IoT (Internet-of-Things), machine-to-machine networks, AI, cloud-based services, and web-based applications. Driven by this demand, many innovations are underway to enhance optical communication systems. In this full-day workshop, we will learn about the latest advances in the field of wireless and wireline optical networks. The morning session of this workshop covers four talks on OWC (Optical Wireless Communication) and applications for Free Space Optics. The afternoon session focuses on wireline optical communication systems, with some talks elaborating on the circuit design techniques for high-speed drivers, transimpedance amplifiers, and data converters as the major building blocks of such transceivers.

Speakers:

1. "WDM Fabric for AI clusters", **Vivek Raghunathan**, *Xscape Photonics*
2. "6G Optical Wireless Networks", **Michael Crisp**, *University of Cambridge*
3. "Photonics: The Key to Building Commercial Quantum Computers", **Hossein Hodaei**, *PsiQuantum*
4. "Will Light Communication be the Coming 6G?", **Farid Bichareh**, *AASA*
5. "Future of Optical and Wireline Transceiver", **Cathy Liu**, *Broadcom*
6. "In-Package Silicon Photonic Transceivers for Next-Gen AI/HPC Systems", **Ganesh Balamurugan**, *Celestial AI*

WSO (Full-Day): Sunday 08:00–17:20
RF Challenges in the Design and Characterization of Quantum Computing Hardware

Sponsor: **IMS/RFIC**

Organizers: **Sorin P. Voinigescu**, *University of Toronto*
Vadim Issakov, *Technische Universität Braunschweig*

Abstract: This workshop will cover the latest industry developments and research trends in the design, large volume manufacturing, and characterization of superconducting, ion-trap, and semiconductor spin qubits along with the associated quantum processor architectures. We will start with a systematic and comprehensive comparison of the different qubit families, RF hardware realization challenges and their unique features. Presentations will also delve into cryogenic modeling, packaging, on-die small-signal and noise measurements and calibration at microwave and mm-wave frequencies of CMOS and SiGe HBT technologies needed in the control and readout electronics of these qubit families. We will end with the latest examples of such cryogenic control and readout circuits.

Speakers:

1. "Superconducting Qubits: Wiring up Quantum Entanglement", **Irfan Siddiqi**, *University of California, Berkeley*
2. "Progress in Control Electronics for Scalable Trapped-Ion Quantum Computing", **Jules Stuart**, *IonQ*
3. "Circuit Design for Large-Scale Trapped Ions", **Jae-Yoon Sim**, *POSTECH*
4. "Design, Modeling and Control of Spin Silicon Qubits: from Confinement to Characterization", **Elena Blokhina**, *University College Dublin*
5. "High Throughput Manufacturing and Testing of Semiconductor Spin Qubit Quantum Processors", **Frank Badets**, *CEA-Leti*
6. "SiGe HBT Compact Modeling for Circuit Design at Cryogenic Temperatures", **Michael Schröter**, *Technische Universität Dresden*
7. "MOSFET Modeling with the sEKV Model for the Design of Cryo-CMOS Circuits", **Christian Enz**, *EPFL*
8. "On-Wafer LNA Noise Measurements for Cryogenic LNAs", **Joseph Bardin**, *UMass Amherst*
9. "FDSOI Platform for Quantum Computing", **Tristan Meunier**, *Quobly*
10. "Engineering Quantum Computers for the FTQC Era: A Little About a Lot!", **Imran Bashir**, *Equal1*
11. "Progress in Cryogenic Circuits for Superconducting Qubit-Based Quantum Computing", **Daniel Friedman**, *IBM T.J. Watson Research Center*

WSP (Half-Day): Sunday 13:30–17:20
Designing with Time: Linear Periodically Time-Varying (LPTV) Circuit Approaches Enabling Advanced RFIC Applications

Sponsor: **RFIC**

Organizers: **Travis Forbes**, *Sandia National Laboratories*
Subhanshu Gupta, *Washington State University*

Abstract: While much of RFIC design works in the linear time invariant regime where blocks such as amplifiers provide a constant response during all time, linear time variant circuits bring time variance through clocking and/or mixing to enable significant performance advances. These advances are already showing promise in applications such as increased throughput in phased arrays, enabling full-duplex communication systems, and filtering of RF blockers for high bandwidth receivers. This workshop will bring together multiple research areas of linear periodic time variant (LPTV) circuit techniques from experts in industry and academia to provide attendees with both the theory of operation and the circuit and system implementation. Beginning with theory, the first talk will overview the theory of operation and analysis of LTV circuits with intuitive time-frequency domain analysis for mixing and filtering operations suited towards software-defined radios. The second talk will present advances in discrete-time true-time delay technologies and non-reciprocal components for use in full-duplex systems and circulators. The third talk will discuss sharp filtering through sampling aliases in LPTV filtering applications. The fourth talk will overview non-uniform sampling and engineering the clock to realize time-approximation filters for mixed-signal receiver implementations. The final talk will show significantly increased phased array throughput using joint phase and time array using an LPTV true-time delay as a key component. To end the workshop, we will bring the experts together for cross-pollination of ideas through a panel interaction with attendees.

Speakers:

1. "Highly Linear Time-Variant Mixers/Filters: Operation and Analysis", **Eric Klumperink**, *University of Twente*
2. "Fully Integrated, Time-Varying Non-Reciprocal Components for RF and mm-Wave Systems", **Aravind Nagulu**, *Northeastern University*
3. "Sharp Filtering Using Sampling Aliases: Basics, Benefits, and Challenges", **Sudhakar Pamarti**, *University of California, Los Angeles*
4. "Advanced RFIC Techniques Using Non-Uniform Sampling and Time-Approximation Filters", **Mike Shuo-Wei Chen**, *University of Southern California*
5. "Next Generation mm-Wave Technology: Beamforming with Joint Phase and Time Array", **Navneet Sharma**, *Samsung*

Social Events/Guest Program

SUNDAY, 15 June 2025

RFIC Welcoming Reception
19:00–21:00

RFIC'25 starts with a welcome event on Sunday for all attendees, which will be hosted at rooms 301–304 immediately following the RFIC'25 Plenary Session.

MONDAY, 16 June 2025

IMS Welcome Event
19:30–21:30

IMS'25 starts with a welcome event on Monday for all attendees, which will be hosted at San Francisco Museum of Modern Art (SF MOMA) immediately following the IMS'25 Plenary Session.

TUESDAY, 17 June 2025

Student-Industry-Academia RFIChat
"Battle of the Bands: Matching Career Path to Frequency of Interest"
17:30–19:00

Come and join the special event customized by and for RFIC´25 students, academia, and the RF industry! The event will be held at Moscone Center room 301.

Ham Radio Social Networking Reception
18:30–20:30

All radio amateurs and other interested IMS participants are cordially invited to the event.

Women in Microwaves (WIM) Event
19:00–21:00

This event welcomes all members of IMS to promote collaboration, with a spotlight on the work of female RF engineers and researchers. We will continue our traditional social cocktail party, which grows yearly. The reception will also feature social networking opportunities, games, and more!

Young Professionals (YP's) Networking Reception
19:00–21:00

The reception is a place to celebrate the young professionals, the future of the microwave community, network and interact with like-minded people.

WEDNESDAY, 18 June 2025

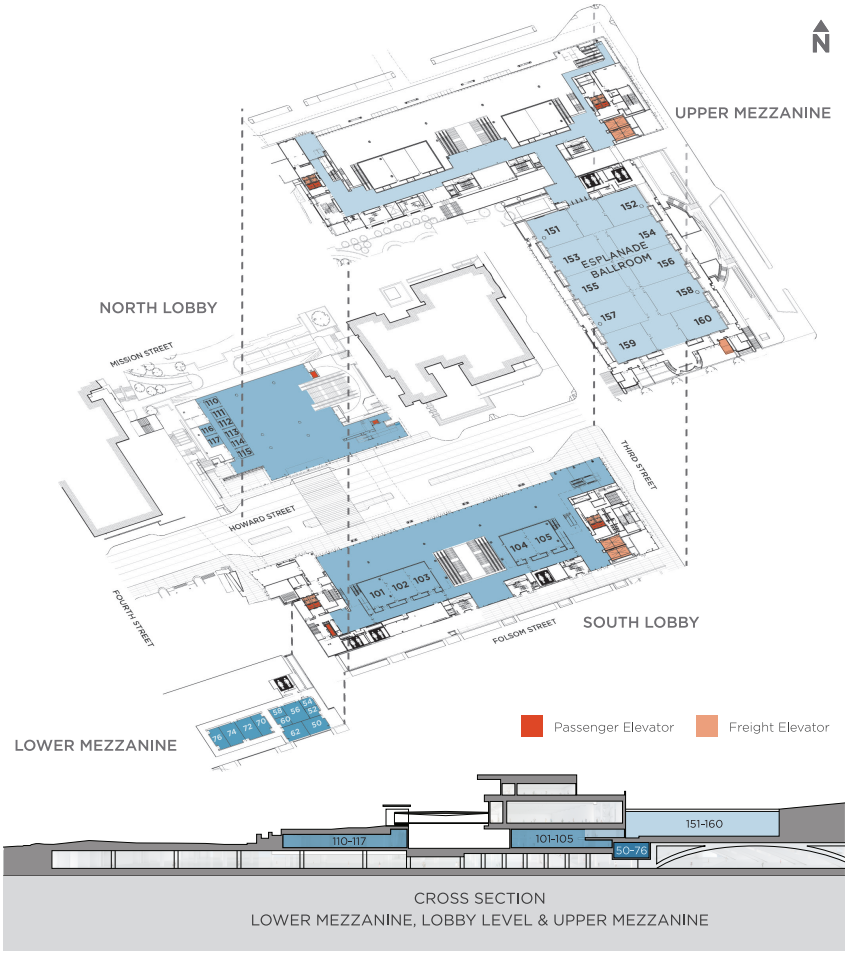
Industry-Hosted Reception
17:00–18:00

The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

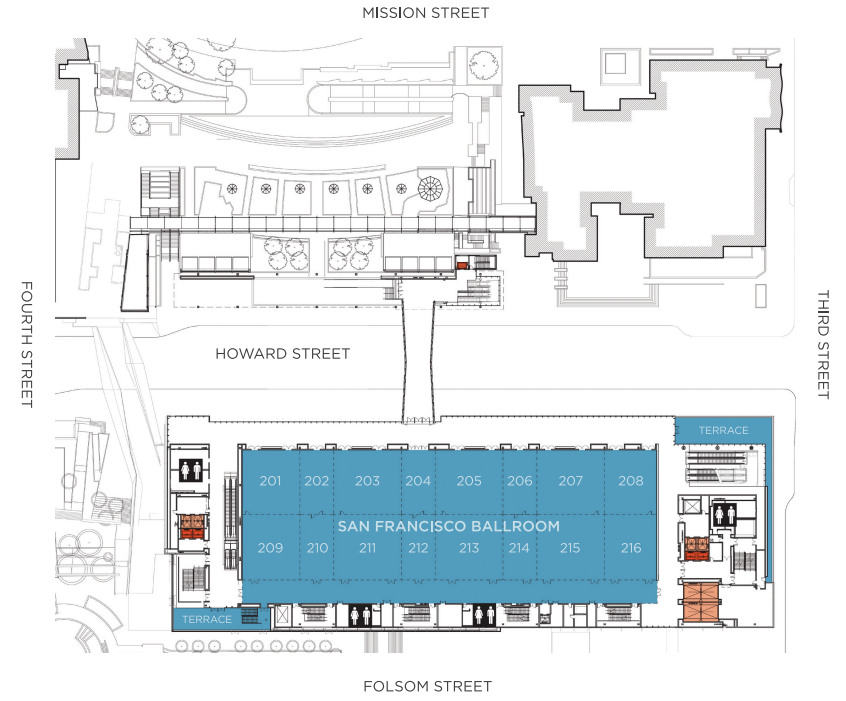
MTT-S Awards Banquet
18:30–20:00

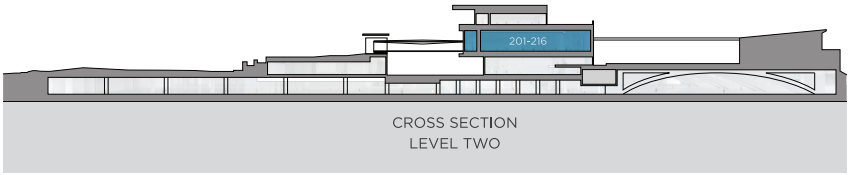
The MTT-S Awards Banquet will be hosted at the San Francisco Marriott Marquis and will feature exciting entertainment. A ticket is required for entry.

Moscone Convention Center Maps

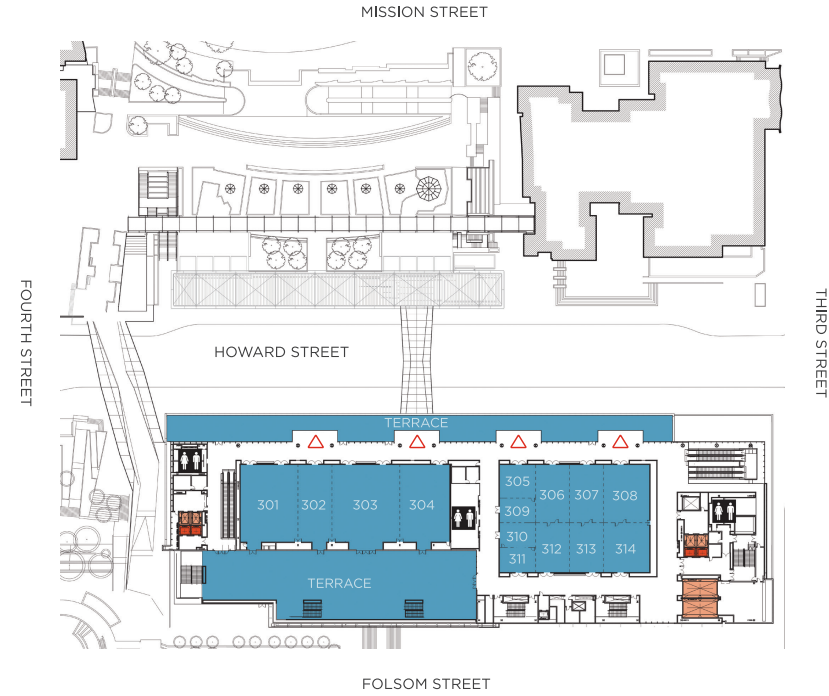


Moscone Convention Center Maps (continued)

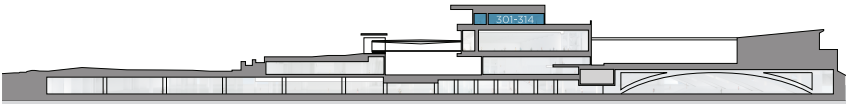




Moscone Convention Center Maps (continued)

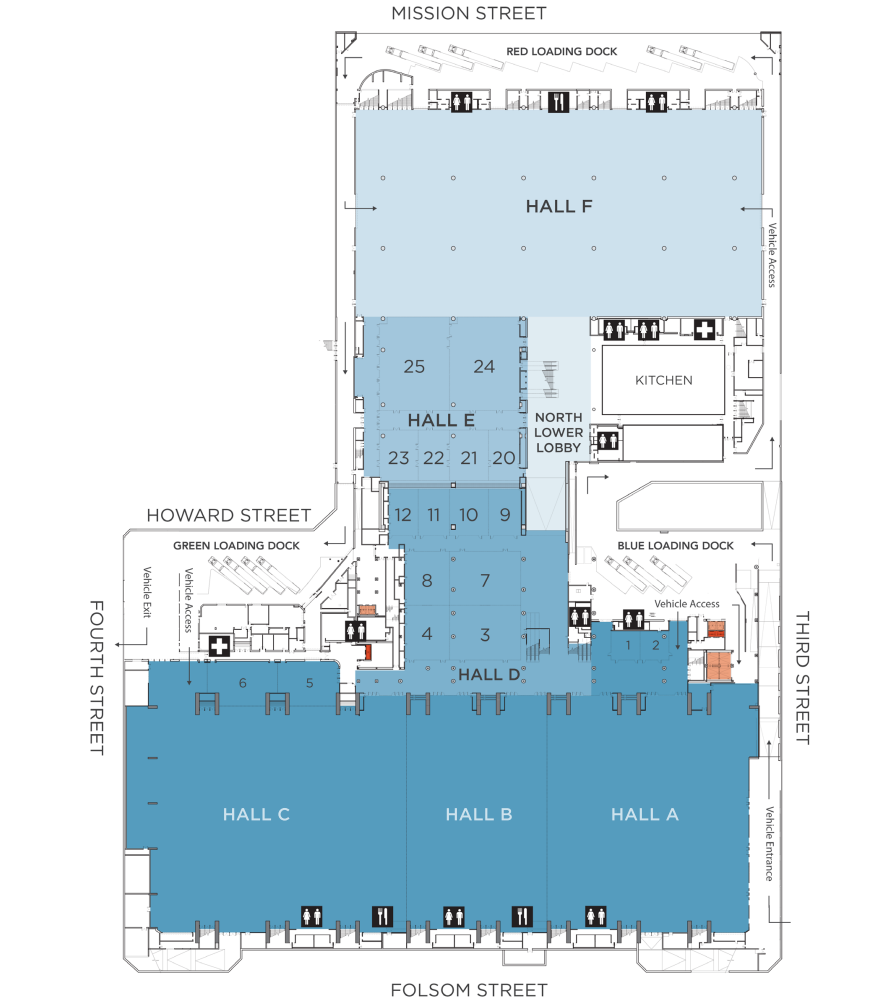


△ Alcoves approximately 400 square feet with 10' ceilings



CROSS SECTION
LEVEL THREE

Moscone Convention Center Maps (continued)



NOTES

IEEE
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Piscataway, NJ 08854, USA

2025 RFIC Symposium
San Francisco, California, USA
15–17 June 2025

RFIC PROGRAM