

2024 IEEE Radio Frequency Integrated Circuits Symposium

Washington, DC, USA 16–18 June 2024



PROGRAM

Walter E. Washington Convention Center

Sponsored by

IEEE Microwave Theory and Technology Society IEEE Electron Devices Society and IEEE Solid-State Circuits Society







RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 16 June 2024 Walter E. Washington Convention Center

After a busy day immersed in RFIC'24 Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held at the Walter E. Washington Convention Center.

17:30–19:00, Plenary Session, Ballroom AB: The evening begins with the Student Paper Awards, Industry Paper Awards, and Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Dr. Peter Vetter, President of Nokia Bell Labs Core Research, and Prof. Tsu-Jae King Liu, Dean of the College of Engineering of University of California, Berkeley.

19:00–21:00, RFIC Symposium Reception and Showcase, Ballroom South Pre-Function: Immediately following the Plenary Session is the RFIC'24 Symposium Reception and Showcase. Food and drinks will be provided while you connect with old friends, make new acquaintances, and catch up on the latest developments in the field.

The RFIC'24 Symposium Showcase is held concurrently with the reception and will feature our industry paper awards finalists, student paper awards finalists and the Systems & Applications Forum. The selected authors will be present to highlight their innovative work, summarized in electronic poster format, and some will also show a live demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss the microwave week's opening event. Please see <u>https://rfic-ieee.org/</u> for more details.

The RFIC Symposium is made possible through the generous support of our corporate sponsors:



Event	Location	Sat 15 June	Sun 16 June	Mon 17 June	Tue 18 June
Registration	Grand Lobby	08:00-17:00	07:00-18:00		
Speakers' Breakfast	Room 202AB		07:00-08:00		
Workshops	Rooms 143–147, 149–152, 201, 204, 209		08:00–11:50 13:30–17:20		
Workshops Lunch	Level 1 Foyer		12:00-13:00		
Technical Lecture	Room 207AB		12:00-13:30		
Plenary Session	Ballroom AB		17:30-19:00		
Reception and Symposium Showcase	Ballroom South Pre-Function		19:00-21:00		
Technical Sessions	Rooms 150AB–152AB			08:00- 10:10- 13:30- 15:40-	-09:40 -11:50 -15:10 -17:20
Panel Sessions	Room 202AB (Mon) Room 207AB (Tue)			12:00-	-13:30
Student-Industry-Academia RFIChat	Room 207AB				17:00-18:30

RFIC Symposium Schedule (15–18 June 2024)



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Welcome Message from Chairs

On behalf of the Executive and Steering Committees, we would like to invite you to join us for the 2024 IEEE Radio Frequency Integrated Circuits (RFIC'24) Symposium. The IEEE RFIC Symposium (RFIC) is the premier annual forum focused on presenting the latest breakthroughs and research results in all areas related to radio frequency (RF), millimeter-wave (mmWave), and wireless integrated circuits (ICs). As an integral part of the Microwave Week, the world's largest RF & microwave technical convention, RFIC continues to be at the forefront of technological innovation.

RFIC'24 will take place at the Walter E. Washington Convention Center, nestled in the heart of Washington, DC, from Sunday morning, 16 June, through Tuesday night, 18 June.

The RFIC'24 Plenary Session is held on Sunday night, followed by a welcome reception and the Symposium Showcase. The RFIC technical sessions will be held on Monday and Tuesday in parallel tracks. The IMS technical exhibition will be held on Tuesday, Wednesday, and Thursday.

RFIC'24 technical papers will be presented through parallel sessions on Monday and Tuesday. Our sessions will span a diverse array of topics, including interference-resilient and energy-efficient transmitters and receivers, mmWave power amplifiers, and silicon-based power amplifiers for D-band and beyond. The sessions will also explore advanced topics such as wireline and localization systems, high-performance multi-mode, multi-core oscillators, and RF and mixed-signal circuits for cryogenic and high-radiation environments. As mmWave and terahertz (THz) technologies continue to gain traction in 5G/6G research, RFIC'24 will feature dedicated sessions on D-band and THz transmitters, and circuit building blocks in the 100–200 GHz frequency range. Moreover, the symposium will delve into novel RF systems and applications, encompassing innovations from 5G to low-power sensing, and covering emerging technologies such as novel THz solutions, advanced packaging, radars, and imagers.

The RFIC'24 enriching educational program on Sunday, 16 June, will feature 13 RFIC-focused workshops and a technical lecture. Covering advanced topics in RFIC technology, workshops include discussions on the following subjects: advanced PA and transmitters design, phased-arrays for communication and sensing, chiplets, 3D packaging and 3D heterogeneous integration, system innovations and design methodologies in AI/ML techniques for communications and sensing, and integrated circuits for quantum processors.

RFIC'24 will also feature an excellent 80 minute short course, which we call a "*Technical Lecture*", delivered by world-renowned Prof. Ali Hajimiri of Caltech, on "Noise in Oscillators: from Understanding to Design". This technical lecture will discuss the fundamentals of noise processes within an oscillator and the associated design insights.

Following the full day of Sunday workshops, the RFIC'24 Plenary Session will be held in the evening beginning with the conference highlights, the presentation of the Student Best Paper Awards and the Industry Best Paper Awards. The RFIC'24 Plenary Session will conclude with two visionary plenary talks:

- In his talk *"The 6G Network at the Center"*, Dr. Peter Vetter, President of Bell Labs Core Research and Bell Labs Fellow, will share his vision on 6G, the main technology areas for 6G, and provide some research highlights.
- Prof. Tsu-Jae King Liu, Dean of the College of Engineering at the University of California at Berkeley, will give a talk on "CMOS Technology Evolution for Revolutionary Impact".

The RFIC'24 Reception and Symposium Showcase will follow immediately after the plenary session, with highlights from our industry showcase and student paper finalists in an engaging

social and technical evening event supported by the RFIC'24 corporate sponsors. The showcase will provide authors the opportunity to demo their work in a lab-like environment for more close-up discussion and interaction. You will not want to miss the RFIC'24 Reception!

On Monday and Tuesday, RFIC'24 will have multiple tracks of oral technical paper sessions and will offer panel sessions during the lunch breaks. Monday's lunchtime panel, titled "*RF and Microwave League of Champions*" will see two teams, one from industry and one from academia, competing with each other to solve practical RF engineering problems. Who is better at combining knowledge, intuition, and creativity: industry or academia? The audience is invited to participate and support their favorite team. Tuesday's lunchtime panel, organized jointly with IMS'24, will discuss the topic of "*AI in RFIC: Opportunities, Threats, and Limitations*". The use of artificial intelligence (AI) has become one of the hottest and most controversial discussion topics of the moment. How will this pervasive technology transform our industry? This lunchtime panel, with both industry and academia experts, will explore the opportunities offered by AI, as well as its limitations (if any!) and its potential threats.

RFIC'24 and the Microwave Week have many educational and professional development opportunities for students, all delivered at an exceptional value. Following its introduction in 2022, RFIC'24 will feature a dedicated Student Session. This year, the RFIC Student Session is called *"Students-Industry-Academia RFIChat"*. It is a forum where students and experts from academia, industry, and research can meet for an open discussion on RFIC careers and future trends. Join us for an engaging discussion (and food!) at the RFIChat event on Tuesday afternoon. Bring your questions and come learn how to kickstart, advance, and optimize your career path for variables such as innovation, work-life balance, positive impact, financial stability and more. Our panelists promise to offer invaluable insights (secrets!?) into the unique landscapes of academia and industry, so come meet them and have a chat!

Last but not least, RFIC'24 will once again conduct a contest to select the top student papers from the symposium. The top student papers will also be featured at our Sunday's *Symposium Showcase*, providing an additional exposure opportunity. As part of IMS, students have the opportunity to participate in design competitions and an RF Bootcamp. Students have the opportunity to purchase the *Student Superpass*, allowing them to experience every activity within Microwave Week, including a workshop, all three conferences (RFIC, IMS, and ARFTG), a technical lecture, and much more. The *Student Superpass* is a deeply discounted price for IEEE student members.

On behalf of the RFIC Steering and Executive Committees, we welcome you all to join us at the 2024 RFIC Symposium in Washington, DC. Please visit the RFIC'24 website (<u>https://rfic-ieee.org/</u>) for more details and updates.



Danilo Manstretta General Chair Università di Pavia



François Rivet TPC Chair University of Bordeaux



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Steering Committee

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RFIC 2024 Schedule Walter E. Washington Convention Center

Saturday, 15 June 2024

08:00–17:00 Registration — Grand Lobby

Sunday, 16 June 2024

- 07:00-18:00 Registration Grand Lobby
- 07:00-08:00 Speakers' Breakfast 202AB
- 08:00–11:50 Workshops 143–147, 149–152, 201, 204, 209
- 12:00–13:00 Workshops Lunch Level 1 Foyer
- 12:00-13:30 Technical Lecture 207AB Noise in Oscillators: From Understanding to Design
- 13:30–17:20 Workshops 143–147, 149–152, 201, 204, 209
- 17:30–19:00 RFIC Plenary Ballroom AB
- 19:00–21:00 Welcoming Reception Featuring Symposium Showcase Ballroom South Pre-Function

Monday, 17 June 2024

- 07:00–18:00 Registration Grand Lobby
- 07:00-08:00 Speakers' Breakfast 202AB
- 08:00–09:40 RMo1A 150AB: mm-Wave Transmitters and Receivers
- 08:00–09:40 RMo1B 151AB: Advanced Packaging Enabling Heterogeneous Integration of SiGe HBT and III-V mm-Wave ICs
- 08:00–09:40 RMo1C 152AB: Unleashing RF Systems: From 5G to Low-Power Sensing
- 09:40–10:10 Coffee Break Level 1 Foyer
- 10:10-11:50 RMo2A 150AB: mm-Wave Transceivers and RF Techniques
- 10:10–11:50 RMo2B 151AB: High-Performance Multi-Mode, Multi-Core Oscillators
- 10:10–11:50 RMo2C 152AB:
- Interference Resilient and Energy Efficient Transmitters and Receivers
- 12:00–13:30 RFIC Panel Session 202AB: RF and Microwave League of Champions
- 13:30-15:10 RMo3A 150AB: mm-Wave Power Amplifiers
- 13:30–15:10 RMo3B 151AB: RF and mm-Wave Frequency Multipliers
- 13:30–15:10 RMo3C 152AB: Wideband Reconfigurable Beamforming Arrays
- 15:10–15:40 Coffee Break Level 1 Foyer
- 15:40-17:20 RMo4A 150AB: Silicon-Based Power Amplifiers for D-Band and Above
- 15:40–17:20 RMo4B 151AB: High Performance RF and mm-Wave CMOS Frequency Synthesis
- 15:40–17:20 RMo4C 152AB: Wireline and Localization Systems

Tuesday, 18 June 2024

- 07:00–18:00 Registration Grand Lobby
- 07:00-08:00 Speakers' Breakfast 202AB
- 08:00-09:40 RTu1B 151AB:
- RF and Mixed-Signal Circuits for Cryogenic and High-Radiation Environments
- 08:00–09:40 RTu1C 152AB: Digital Power Amplifier and Transmitter Systems
- 09:40–10:10 Coffee Break Exhibit Floor
- 10:10–11:50 RTu2B 151AB: Silicon Wireless Systems in the D-Band and Beyond
- 10:10–11:50 RTu2C 152AB: Power Amplifiers for Satellite Applications
- 12:00–13:30 RFIC/IMS Joint Panel Session 207AB:
 - AI in RFIC: Opportunities, Threats, and Limitations
- 13:30–15:10 RTu3B 151AB: Silicon-Based Low-Noise Amplifiers and Mixers
- 13:30-15:10 RTu3C 152AB: D-Band and THz Transmitters
- 15:10–15:40 Coffee Break Exhibit Floor
- 15:40–17:20 RTu4B 151AB: mm-Wave and Beyond Radars and Imagers
- 15:40–17:20 RTu4C 152AB: Circuit Building Blocks in the 100–200GHz Frequency Range
- 17:00–18:30 Student-Industry-Academia RFIChat 207AB: Burning Career Questions? Come Chat with the Pros!

RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 16 June 2024 Walter E. Washington Convention Center

17:30–19:00 RFIC Plenary Ballroom AB

Chair: Danilo Manstretta, Università di Pavia Co-Chair: François Rivet, University of Bordeaux

- 17:30 Welcome Message from General Chair and TPC Chairs Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
 18:00 The 6G Network at the Center Peter Vetter, Nokia Bell Labs Core Research
- 18:30 CMOS Technology Evolution for Revolutionary Impact Tsu-Jae King Liu, University of California, Berkeley

19:00-21:00

RFIC Welcoming Reception Featuring Symposium Showcase Ballroom South Pre-Function

The RFIC Interactive Reception starts immediately after the Plenary Session and will highlight the Student Paper Awards finalists, the Industry Paper Awards finalists, and the Systems & Applications Forum in an engaging social and technical evening event with food and drinks. Authors of these showcase papers will present their innovative work, summarized in poster format. Some showcase papers will also offer live demonstrations. You will not want to miss the RFIC Reception! This event is supported by the RFIC Symposium corporate sponsors.

RFIC Plenary Speaker 1



Dr. Peter Vetter President Nokia Bell Labs Core Research

The 6G Network at the Center

Abstract: 6G is no longer a mere long-term aspiration. It is a framework of technologies that will become reality by the end of the decade. We are transitioning from the idea-generation phase to systematization and proof-of-concept realization. In this talk, we give our vision of the 6G network at the center that is an essential pilar equal to artificial intelligence (AI) and cloud to shape the future of human augmentation. We will summarize the main technologies in the upper midband 7–15 GHz, which the industry identified as a priority for 6G, sub-THz bands, which is essential for future backhaul and has potential for joint high-capacity communication and sensing, AI, which may cause a paradigm shift for air interface design, and energy efficient radio access, which is seen as one of the key requirements for 6G.

About Dr. Peter Vetter

Peter Vetter is President of Bell Labs Core Research and Bell Labs Fellow. He leads an eminent global research organization with the mission to create game changing innovations that define the future of networks and insure portfolio leadership for Nokia's core business. During an international career of thirty years in research leadership mostly in fixed and mobile networks, he and his teams have realized several world-first system demonstrations and successfully transferred industry leading concepts to the business groups. He received a PhD at Ghent University (Belgium) in 1991 and was a post-doctoral fellow at Tohoku University (Japan) until 1993. He then joined the research center of Alcatel (now Nokia) in Antwerp and has worked at Bell Labs in Murray Hill, New Jersey since 2009. He is IEEE Fellow and Honorary Professor of KU Leuven.

RFIC Plenary Speaker 2



Prof. Tsu-Jae King Liu Dean of the College of Engineering University of California, Berkeley

CMOS Technology Evolution for Revolutionary Impact

Abstract: Steady advancement in complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) technology has enabled the capability and affordability of computing and communication devices to improve exponentially over time, giving rise to cloud computing and the Internet of Things, which together with advances in machine learning have ushered in the era of Artificial Intelligence. To date, CMOS technology advancement has been driven primarily by market demand for faster and more energy-efficient digital computing; as such, transistor scaling to sub-10 nm technology nodes has presented challenges for analog/RF IC design. In this keynote presentation I will discuss evolutionary advancements in CMOS technology that can address these challenges, focusing on relevant figures of merit, for revolutionary impact.

About Prof. Tsu-Jae King Liu

Tsu-Jae King Liu received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Stanford University. She joined the Xerox Palo Alto Research Center as a Member of Research Staff in 1992, to research and develop high-performance thin-film transistor technologies for flat-panel display applications. In 1996 she joined the faculty of the University of California, at Berkeley, where she now holds the Roy W. Carlson Distinguished Professorship in Engineering. From 2000 to 2004 and from 2006 to 2008, she served as the Faculty Director of the UC Berkeley Microfabrication Laboratory. From July 2004 through June 2006 she was Senior Director of Engineering in the Advanced Technology Group of Synopsys, Inc. (Mountain View, CA). From 2008 through 2012, Professor Liu was the Associate Dean for Research in the College of Engineering at UC Berkeley. She also served as Faculty Director of the UC Berkeley Marvell Nanofabrication Laboratory in 2012. From 2012 to 2016 she served as Chair of the Electrical Engineering Division, and from 2016 she served as Chair of the EECS Department.

Professor Liu's awards include the Ross M. Tucker AIME Electronics Materials Award (1992) for seminal work in polycrystalline silicon-germanium thin films; an NSF CAREER Award (1998) for research in thin-film transistor technology; the DARPA Significant Technical Achievement Award (2000) for development of the FinFET; the Electrical Engineering Award for Outstanding Teaching at UC Berkeley (2003); the IEEE Kiyo Tomiyasu Award (2010) for contributions to nanoscale MOS transistors, memory devices, and MEMS devices; the UC Berkeley Faculty Mentor Award (2010); the Electrochemical Society Dielectric Science and Technology Division Thomas D. Callinan Award (2011) for excellence in dielectrics and insulation investigations; the Intel Outstanding Researcher in Nanotechnology Award (2012); the Semiconductor Industry Association (SIA) University Researcher Award (2014); and the Semiconductor Research Corporation (SRC) Aristotle Award (2016). Her research activities are presently in advanced materials, fabrication processes and devices for energy-efficient electronics. She has authored or co-authored over 500 publications and holds over 90 patents.

Professor Liu is a Fellow of the IEEE and a member of the U.S. National Academy of Engineering, and serves on the Board of Directors for Intel Corporation.

Sunday, 16 June 2024

The Student Paper Awards Finalists

Chair: Amin Arbabian, Stanford University

The RFIC Symposium's Student Paper Award is devised to both encourage student paper submissions to the conference as well as give the authors of the finalists' papers a chance to promote their research work with the conference attendees after the plenary session during reception time. The outstanding student paper finalists listed below were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of TPC judges selected the top three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top-three Student Papers will be announced during the RFIC Plenary Session on 16 June 2024 in Washington, DC. Each winner will receive a plaque.

A Blocker-Tolerant mm-Wave MIMO Receiver with Spatial Notch Filtering Using Non-

Reciprocal Phase-Shifters for 5G Applications Shahabeddin Mohin, Soroush Araei, Mohammad Barzgari, Negar Reiskarimian MIT, USA RMo1A-4 09:00

A G-Band Glass Interposer Technology for the Integration of an Amplified Noise Source Based on SiGe BiCMOS 55-nm Technology

Maya Alawar¹, Victor Fiorese², Sylvie Lépilliet¹, Daniel Gloria², Guillaume Ducournau¹, Emmanuel Dubois¹ ¹IEMN (UMR 8520), France, ²STMicroelectronics, France

RMo1B-3 08:40

A 2.4GHz, -19 dBm Sensitivity RF Energy Harvesting CMOS Chip with 51% Peak Efficiency and 24dB Power Dynamic Range

Jing-Ren Yan¹, Yao-Wei Huang¹, Wei-Jen Lai², Jen-Hao Liao², Ching-Chun Lin², Yu-Te Liao¹ ¹NYCU, Taiwan, ²Novatek Microelectronics, Taiwan RMo1C-1 08:00

A Reconfigurable Ultra Compact Bi-Directional Amplifier with a Build-in-Self Notch Filter for K/Ka-Band Satellite Communication
 Jian Zhang¹, Ming Zhai¹, Dawei Wang¹, Xiangjie Yi¹, Wei Zhu², Yan Wang¹
 'Tsinghua University, China, ²BIT, China
 RMo2A-2 10:30

A 52.3-to-67.3GHz 35.8-kHz-Resolution Triple-Push DCO Exploiting Source-Combining Technique for Third-Harmonic Enhancement Achieving 196.4dBc/Hz Peak FoMT at 10MHz Offset Qiyao Jiang¹, Jun Yin¹, Quan Pan², Rui P. Martins¹, Pui-In Mak¹ ¹University of Macau, China, ²SUSTech, China RMo2B-3 10:50

A 2.8–4.3GHz Simultaneous Dual-Carrier Transformer-Coupled Passive Mixer-First Receiver Front-End Supporting Blocker Suppression Jamie C. Ye, Alain Antón, Russ H. Huang, Sanaz Sadeghi, Alyosha C. Molnar Cornell University, USA RMo2C-3 10:50 A K-Band 4-Element 8-Beam Phased-Array Receiver with Hybrid Vector Interpolation and Impedance-Adapted Multibeam Combining Techniques for Satellite Communications Hang Lu¹, Nayu Li¹, Huiyan Gao¹, Botao Yang¹, Xuanyu He¹, Shaogang Wang¹, Yiwei Liu¹, Gaopeng Chen¹, Yen-Cheng Kuan², Xiaokang Qi¹, Chunyi Song¹, Qun Jane Gu³, Zhiwei Xu¹ ¹Zhejiang University, China, ²NYCU, Taiwan, ³University of California, Davis, USA RMo3C-2 13:50

Broadband Noise Characterization of SiGe HBTs Down to 4K Jad Benserhir, Yating Zou, Yatao Peng, Hung Chi Han, Edoardo Charbon EPFL, Switzerland RTu1B-1 08:00

- A Switchless Dual-Core Triple-Mode VCO Achieving 7.1-to-15.7GHz Frequency Tuning Range and 202.1dBc/Hz Peak FoM at 3.7 Kelvin Yue Wu, Yatao Peng, Benhao Huo, Jun Yin, Rui P. Martins, Pui-In Mak University of Macau, China RTu1B-3 08:40
- An Efficient, High Power Q-Band SiGe HBT Power Amplifier with a Compact Four-Way Wilkinson Power Combiner Balun for Emerging Very Low-Earth-Orbit SATCOM Hanjung Lee, Insu Han, Jaehyeon Hwang, Inchan Ju Ajou University, Korea RTu2C-1 10:10

A 360GHz Single-Element Multi-Mode Orbital Angular Momentum Cavity Antenna-Based Transmitter in 90nm SiGe BiCMOS Wei Sun, Sidharth Thomas, Aydin Babakhani University of California, Los Angeles, USA RTu3C-1 13:30

<u>Student Paper Contest Eligibility</u>: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

The Industry Paper Awards Finalists

Chair: Oren Eliezer, Samsung

The RFIC Industry Showcase highlights the outstanding industry papers listed below. These papers received nominations for this recognition from the TPC sub-committees and godparents in a doubleblind review. From these top papers, a two-stage double-blind review process was conducted by a committee of TPC judges. Finally, the Best Paper Chair and other key Steering Committee members finalize the top three winners after rigorous reviews and discussions. The top three will be displayed on the RFIC website and on a rolling slideshow prior to the RFIC Plenary Session on 16 June 2024 in Washington, DC. Each winner will receive a plaque and will be recognized in an upcoming Microwave Magazine article.

Heterogeneously-Integrated Gallium Nitride and Indium Phosphide Devices for Ka-Band Amplifiers

Justin J. Kim, Michael D. Hodge, Mark R. Soler, Florian Herrault, Daniel S. Green, James F. Buckwalter PseudolithIC, USA RMo1B-2 08:20

A 22FDX Wi-Fi PA Demonstrating a New LDMOS Device with 10V Breakdown Achieving Output Power of 29.5dBm at 40% PAE

Arul Balasubramaniyan¹, Xuemei Hui², Abdellatif Bellaouar¹, Miguel Meza Campos¹, Apurv Bharadwaj¹, Elan Veeramani¹, Shafi Syed¹ ¹GlobalFoundries, USA, ²GlobalFoundries, China RMo1B-4 09:00

A 45nm RFSOI CMOS-Based 24.25–29.5GHz 2×16-Channel Phased-Array Transceiver IC for 5G NR Applications

Jooseok Lee, Seungjae Baek, Kihyun Kim, Seungwon Park, Hansik Oh, Taewan Kim, Joonho Jung, Jinhyun Kim, Sehyug Jeon, Jee Ho Park, Woojae Lee, Jaehong Park, Dong-hyun Lee, Sangho Lee, Jeong Ho Lee, Ji Hoon Kim, Younghwan Kim, Sangyong Park, Bohee Suh, Soyoung Oh, Dongsoo Lee, Juho Son, Sung-gi Yang Samsung, Korea RMo1C-2 08:20

A 21–27-GHz Frequency Quadrupler in 0.13µm SiGe BiCMOS with 0-dBm POUT and 40-dBc HRR for Wideband 5G Applications

Caglar Ozdag¹, Arun Paidimarri¹, Masayuki Yoshiyama², Yuichiro Yamaguchi², Yujiro Tojo², Bodhisatwa Sadhu¹ ¹IBM T.J. Watson Research Center, USA, ²Fujikura, Japan

RMo1C-4 09:00

A 5G FR2 n260/n259 Phased-Array Transmitter Front-End IC in 28-nm CMOS FD-SOI with 3-Stack Power Amplifier Employing OPA-Based Bias Scheme and Cross-Tied Inductor Topology
Jongwon Yun¹, Hongkie Lim¹, Jaeyeon Jeong¹, Iljin Lee¹, Doyoon Kim¹, Kyunghwan Kim¹, Han-Woong Choi¹, Geonho Park¹, Goeun Baek¹, Eun-Taek Sung¹, Ajaypat Jain², Foad A. Malekzadeh², Venumadhav Bhagavatula², Ivan S.-C. Lu², Sangwon Son², Hyun-Chul Park¹, Joonhoi Hur¹, Sangmin Yoo¹
¹Samsung, Korea, ²Samsung, USA RTu1C-4
09:00

<u>Industry Paper Contest Eligibility</u>: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must present the paper at the symposium.

RFIC Reception and Symposium Showcase Featuring Systems & Applications Forum and Best Student/Industry Paper Showcase

Systems & Applications Forum Chair: Yao-Hong Liu, imec Student Paper Chair: Amin Arbabian, Stanford University Industry Paper Chair: Oren Eliezer, Samsung

The RFIC Interactive Reception, supported by the RFIC Symposium corporate sponsors, starts immediately after the plenary session and highlights the Student and Industry Paper Awards finalists in an engaging social and technical evening event with food and drinks. Furthermore, additional authors, both from academia and industry who choose to showcase/demo work focused on Systems and Applications, will be present. Authors will present their innovative work on large monitors as electronic posters and some will offer live demonstrations. Make sure to attend this event, where you will be able to network and see a preview of selected paper presentations that you can attend during the two days that follow. The following lists of participants were valid on 1 May 2024.

Student Paper Awards Finalists' Showcase/Demonstrations

A Blocker-Tolerant mm-Wave MIMO Receiver with Spatial Notch Filtering Using Non- Reciprocal Phase-Shifters for 5G Applications Shahabeddin Mohin, Soroush Araei, Mohammad Barzgari, Negar Reiskarimian	
MIT, USA RMo1A-4 09:00	
A G-Band Glass Interposer Technology for the Integration of an Amplified Noise Source Based on SiGe BiCMOS 55-nm Technology	ł
Maya Alawar', victor Florese', Sylve Lepiner', Daniel Gioria', Guinaume Ducournau', Emmanuel Dubois ¹ ¹ IEMN (UMR 8520), France, ² STMicroelectronics, France RMo1B-3 08:40	
A 2.4GHz, -19 dBm Sensitivity RF Energy Harvesting CMOS Chip with 51% Peak Efficiency and 24dB Power Dynamic Range Jing-Ren Yan ¹ , Yao-Wei Huang ¹ , Wei-Jen Lai ² , Jen-Hao Liao ² , Ching-Chun Lin ² , Yu-Te Liao ¹ ¹ NYCU, Taiwan, ² Novatek Microelectronics, Taiwan RMo1C-1 08:00	
A Reconfigurable Ultra Compact Bi-Directional Amplifier with a Build-in-Self Notch Filter fo K/Ka-Band Satellite Communication Jian Zhang ¹ , Ming Zhai ¹ , Dawei Wang ¹ , Xiangjie Yi ¹ , Wei Zhu ² , Yan Wang ¹ ¹ Tsinghua University, China, ² BIT, China RMo2A-2 10:30	r
 A 52.3-to-67.3GHz 35.8-kHz-Resolution Triple-Push DCO Exploiting Source-Combining Technique for Third-Harmonic Enhancement Achieving 196.4dBc/Hz Peak FoMT at 10MHz Offset Qiyao Jiang¹, Jun Yin¹, Quan Pan², Rui P. Martins¹, Pui-In Mak¹ ¹University of Macau, China, ²SUSTech, China RMo2B-3 	

Sunday, 16 June 2024

19:00-21:00

Ballroom South Pre-Function

A 2.8–4.3GHz Simultaneous Dual-Carrier Transformer-Coupled Passive Mixer-First Receiver Front-End Supporting Blocker Suppression Jamie C. Ye, Alain Antón, Russ H. Huang, Sanaz Sadeghi, Alyosha C. Molnar Cornell University, USA RMo2C-3 10:50

A K-Band 4-Element 8-Beam Phased-Array Receiver with Hybrid Vector Interpolation and Impedance-Adapted Multibeam Combining Techniques for Satellite Communications Hang Lu¹, Nayu Li¹, Huiyan Gao¹, Botao Yang¹, Xuanyu He¹, Shaogang Wang¹, Yiwei Liu¹, Gaopeng Chen¹, Yen-Cheng Kuan², Xiaokang Qi¹, Chunyi Song¹, Qun Jane Gu³, Zhiwei Xu¹ ¹Zhejiang University, China, ²NYCU, Taiwan, ³University of California, Davis, USA RMo3C-2 13:50

Broadband Noise Characterization of SiGe HBTs Down to 4K Jad Benserhir, Yating Zou, Yatao Peng, Hung Chi Han, Edoardo Charbon EPFL, Switzerland RTu1B-1 08:00

- A Switchless Dual-Core Triple-Mode VCO Achieving 7.1-to-15.7GHz Frequency Tuning Range and 202.1dBc/Hz Peak FoM at 3.7 Kelvin Yue Wu, Yatao Peng, Benhao Huo, Jun Yin, Rui P. Martins, Pui-In Mak University of Macau, China RTu1B-3 08:40
- An Efficient, High Power Q-Band SiGe HBT Power Amplifier with a Compact Four-Way Wilkinson Power Combiner Balun for Emerging Very Low-Earth-Orbit SATCOM Hanjung Lee, Insu Han, Jaehyeon Hwang, Inchan Ju Ajou University, Korea RTu2C-1 10:10

A 360GHz Single-Element Multi-Mode Orbital Angular Momentum Cavity Antenna-Based Transmitter in 90nm SiGe BiCMOS Wei Sun, Sidharth Thomas, Aydin Babakhani University of California, Los Angeles, USA RTu3C-1 13:30

Industry Paper Awards Finalists' Showcase/Demonstrations

Heterogeneously-Integrated Gallium Nitride and Indium Phosphide Devices for Ka-Band Amplifiers
Justin J. Kim, Michael D. Hodge, Mark R. Soler, Florian Herrault, Daniel S. Green, James F. Buckwalter
PseudolithIC, USA
RMo1B-2 08:20

 A 22FDX Wi-Fi PA Demonstrating a New LDMOS Device with 10V Breakdown Achieving Output Power of 29.5dBm at 40% PAE
 Arul Balasubramaniyan¹, Xuemei Hui², Abdellatif Bellaouar¹, Miguel Meza Campos¹, Apurv Bharadwaj¹, Elan Veeramani¹, Shafi Syed¹
 ¹GlobalFoundries, USA, ²GlobalFoundries, China RMo1B-4
 09:00

Sunday, 16 June 2024

Ballroom South Pre-Function

A 45nm RFSOI CMOS-Based 24.25–29.5GHz 2×16-Channel Phased-Array Transceiver IC for 5G NR Applications

Jooseok Lee, Seungjae Baek, Kihyun Kim, Seungwon Park, Hansik Oh, Taewan Kim, Joonho Jung, Jinhyun Kim, Sehyug Jeon, Jee Ho Park, Woojae Lee, Jaehong Park, Dong-hyun Lee, Sangho Lee, Jeong Ho Lee, Ji Hoon Kim, Younghwan Kim, Sangyong Park, Bohee Suh, Soyoung Oh, Dongsoo Lee, Juho Son, Sung-gi Yang Samsung, Korea RMo1C-2 08:20

A 21–27-GHz Frequency Quadrupler in 0.13µm SiGe BiCMOS with 0-dBm POUT and 40-dBc HRR for Wideband 5G Applications

Caglar Ozdag¹, Arun Paidimarri¹, Masayuki Yoshiyama², Yuichiro Yamaguchi², Yujiro Tojo², Bodhisatwa Sadhu¹

¹IBM T.J. Watson Research Center, USA, ²Fujikura, Japan RMo1C-4 09:00

A 5G FR2 n260/n259 Phased-Array Transmitter Front-End IC in 28-nm CMOS FD-SOI with 3-Stack Power Amplifier Employing OPA-Based Bias Scheme and Cross-Tied Inductor Topology

Jongwon Yun¹, Hongkie Lim¹, Jaeyeon Jeong¹, Iljin Lee¹, Doyoon Kim¹, Kyunghwan Kim¹, Han-Woong Choi¹, Geonho Park¹, Goeun Baek¹, Eun-Taek Sung¹, Ajaypat Jain², Foad A. Malekzadeh², Venumadhav Bhagavatula², Ivan S.-C. Lu², Sangwon Son², Hyun-Chul Park¹, Joonhoi Hur¹, Sangmin Yoo¹ ¹Samsung, Korea, ²Samsung, USA RTu1C-4 09:00

Systems & Applications Forum Showcase/Demonstrations

A 32-Element 25.8-to-30.8GHz Phased-Array CMOS Transmitter with Programable Piecewise Linear Temperature-Compensation Technique Achieving ±0.002dB/°C Gain Variation Across -60-to-85°C Dongze Li, Wei Deng, Ziyuan Guo, Haikun Jia, Xintao Li, Xiangyu Nie, Ruiheng Qiu, Baoyong Chi Tsinghua University, China RMo1A-3 08:40

A Reconfigurable Compact Multiband RF Bi-Directional Coupler for Sub-6GHz RF Front-Ends in RF SOI CMOS Switch Technology Ting-Li Hsu¹, Amelie Hagelauer¹, Valentyn Solomko² ¹Technische Universität München, Germany, ²Infineon Technologies, Germany RMo1B-5 09:20

 A Fully Integrated Microplastic Detection SoC with 0.1–3GHz Bandwidth and 35dB Dynamic Range for Narrow-Band Notch RF MEMS Sensor System
 Seung-Beom Ku¹, Jinhyoung Kim², Kwon-Hong Lee¹, Han-Sol Lee¹, Kyeongho Eom¹, Joonghoon Kang¹, Hyungjin Jung¹, Cheolung Cha², Hyung-Min Lee¹
 ¹Korea University, Korea, ²KETI, Korea RMo1C-3 08:40 Design of a Dual-Mode Coil-Reuse Data Acquisition System for Miniaturized Wirelessly Powered Biopotential Sensing Nodes Hamid Jafari Sharemi, Aydin Babakhani University of California, Los Angeles, USA RMo1C-5 09:20

- A ΣΔ-Modulated Linear-in-dB Attenuator for On-Chip Power Detection with 0.12dB Resolution in RF SOI CMOS Switch Technology Ting-Li Hsu¹, Valentyn Solomko², Amelie Hagelauer¹
 ¹Technische Universität München, Germany, ²Infineon Technologies, Germany RMo2A-5
- A 25–31GHz Compact True Power Detector with >33dB Dynamic Range in 40nm Bulk CMOS

Haoqi Qin¹, Junjie Gu¹, Hao Xu¹, Zhiwei Xu², Pengcheng Jia³, Na Yan¹ ¹Fudan University, China, ²Zhejiang University, China, ³Starway Communication, China RMo3A-4 14:30

A D-Band Complex Neutralization Cascode Power Amplifier with A Source-Gate Driven Cascode for Enhanced Bandwidth and Efficiency Mohamed Eleraky, Hua Wang ETH Zürich, Switzerland RMo4A-1 15:40

- A 10ns Delay Range 1.5GHz BW True-Time-Delay Array-Based Passive-Active Signal Combiner with Negative-Cap Stabilized RAMP for Fast Precise Localization Qiuyan Xu¹, Chung-Ching Lin¹, Aditya Wadaskar², Huan Hu¹, Danijela Cabric², Subhanshu Gupta¹
 ¹Washington State University, USA, ²University of California, Los Angeles, USA RMo4C-3
 16:20
- A Fully Integrated Three-Channel Cryogenic Microwave SoC for Qubit State Control in 9Be+ Trapped-Ion Quantum Computer Operating at 4K
 P. Toth¹, P.S. Eugine¹, A. Meyer¹, K. Yamashita², S. Halama³, M. Duwe³, H. Ishikuro², C. Ospelkaus³, Vadim Issakov¹
 ¹Technische Universität Braunschweig, Germany, ²Keio University, Japan, ³Leibniz Universität Hannover, Germany

RTu1B-2 08:20

An Efficient Ku-Band Two-Way Vertical-Like Power-Combining Power Amplifier Using Merged Inter-Stage Transformers Achieving 23–23.4dBm Psat and 45.2–46.6% Peak PAE in 65nm CMOS

Joon-Hyung Kim¹, Jeong-Taek Lim¹, Jae-Eun Lee¹, Jae-Hyeok Song¹, Jeong-Taek Son¹, Min-Seok Baek¹, Eun-Gyu Lee¹, Sunkyu Choi¹, Han-Woong Choi², Seong-Mo Moon³, Dongpil Chang³, Choul-Young Kim¹ ¹Chungnam National University, Korea, ²Samsung, Korea, ³ETRI, Korea

RTu2C-3 10:50

A 200GHz Wideband and Compact Differential LNA Leveraging an Active Balun Input Stage in 16nm FinFET Technology Education Change Designed All Nilmoind

Ethan Chou, Nima Baniasadi, Ali Niknejad University of California, Berkeley, USA RTu4C-3 16:20

RFIC Panel Session

Monday, 17 June 2024 12:00–13:30 Room 202AB

Panel Sessions Chair: Hossein Hashemi, University of Southern California

RF and Microwave League of Champions

Panel Organizers and Moderators:

James Buckwalter, University of California, Santa Barbara Shahriar Shahramian, Nokia Bell Labs

Panelists:

• Team University:

Ramesh Harjani, University of Minnesota Payam Heydari, University of California, Irvine Donald Y.C. Lie, Texas Tech University

• Team Industry:

Debabani Choudhury, Intel Osamu Kusano, Keysight Technologies Bodhisatwa Sadhu, IBM T.J. Watson Research Center

Abstract: Rather than a traditional panel, the RF and Microwave League of Champions will be a quiz show pitting a team of academics against a team of industry veterans to answer technical riddles sourced from RF and microwave history. Each team will comprise three members who will answer as a team on questions about RF/microwave theory, circuits, and systems. This event will be an entertaining diversion from the typical technical panel and hopefully a great deal of fun for participants.

RFIC/IMS Joint Panel Session

Tuesday, 18 June 2024 12:00–13:30 Room **207AB**

Panel Sessions Chairs RFIC: Hossein Hashemi, University of Southern California IMS: Parrish Ralston, Northrop Grumman Zachary Drikas, U.S. Naval Research Laboratory

AI in RFIC: Opportunities, Threats, and Limitations

Panel Organizers and Moderators: Kaushik Sengupta, Princeton University Oren Eliezer, Samsung

Panelists: Thomas Kazior, DARPA MTO David Pan, University of Texas at Austin Michael Thompson, Cadence Design Systems Jian Yang, Synopsys Silvia Zhang, Northeastern University

Abstract: The growth in generative AI has, naturally, raised the question of its impact on RFIC design. The latter has been traditionally regarded as somewhat of a black art, requiring the 'magic' of human intuition and creativity.

But is RFIC design really so, or will AI be able to automate large portions of the design process in the future? Are the days of hand-crafted RFIC design limited? Will AI replace design engineers or only augment their capabilities, to some extent?

This lunch time panel, with both industry and academic experts, will attempt to unentangle the impact of AI in RFIC design.

Student-Industry-Academia RFIChat

Tuesday, 18 June 2024 17:00–18:30 Room **207AB**

Student Paper Chair: Amin Arbabian, Stanford University

Burning Career Questions? Come Chat with the Pros!

Moderators:

Spyridon Baltsavias, Apple Travis Forbes, Sandia National Laboratories

Panelists: Ali Hajimiri, Caltech Jennifer Kitchen, Arizona State University Kostas Doris, NXP Semiconductors Shahriar Shahramian, Nokia Bell Labs Margaret Szymanowski, Crane A&E

Abstract: Join us for an engaging discussion (and food!) at the RFIChat event. Students and experts from academia, industry, and research will converge for an open discussion on RFIC careers and future trends. Bring your questions and come learn how to kickstart, advance, and optimize your career path for variables such as innovation, work-life balance, positive impact, financial stability and more. Our panelists promise to offer invaluable insights (secrets!?) into the unique landscapes of academia and industry, so come meet them and have a chat!

RFIC Technical Lecture

Sunday, 16 June 2024 12:00–13:30 Room 207AB

Chair: Mona Hella, Rensselaer Polytechnic Institute

Noise in Oscillators: From Understanding to Design

Speaker: Ali Hajimiri, Professor, California Institute of Technology



Abstract: In this technical lecture, we will discuss the fundamentals of noise processes within an oscillator and the associated design insights. We will start with understanding evolution of noise from device and external noise sources to phase noise. We will develop the time-varying phase noise model, discuss some of the nuances involved in it, and how a deeper understanding of that process can help us identify additional intuition in design of voltage controlled oscillators (VCO). We will investigate specific applications of this model to various kinds of oscillators, such as LC ad ring VCOs and how it fits with the general picture of frequency generation.

About Prof. Ali Hajimiri

Professor Hajimiri's group does research on electronics and photonics integrated circuits and their applications in various disciplines, including high-frequency and high-speed communications, sensing, imaging, and bio-sensing. His research group engages in both the theoretical analysis of the problems in photonics and electronics integrated circuits and biomedical devices as well as practical implementations of new systems.

Prof. Ali Hajimiri received his B.S. degree in Electronics Engineering from the Sharif University of Technology, and M.S. and Ph.D. degrees in electrical engineering from the Stanford University. Before joining the Faculty of Caltech, he worked for Bell Laboratories, Sun Microsystems, and Signetics (Philips Semiconductor). In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is Bren Professor of Electrical Engineering and Medical Engineering, Director of Caltech Holistic Integrated Circuit Laboratory, and co-Director of the Space-based Solar Power Project. His research interests are high-speed and high-frequency electronics and photonics integrated circuits for applications in sensors, photonics, communication, wireless energy transfer, and biomedical devices.

Prof. Hajimiri is the author of "Analog: Inexact Science, Vibrant Art" (Early Draft pdf) a book on fundamental principles of analog circuit design and "The Design of Low Noise Oscillators" (Boston, MA: Springer). He has authored and coauthored more than 300 refereed journal and conference technical articles and has been granted more than 170 U.S. patents and has many more pending applications.

He is a Fellow of National Academy of Inventors (NAI). Prof. Hajimiri was selected to the TR35 top innovator's list. He is also a Fellow of IEEE and has served as a Distinguished Lecturer of the IEEE Solid-State and Microwave Societies. He won the Feynman Prize for Excellence in Teaching, Caltech's most prestigious teaching honor, as well as Caltech's Graduate Students Council Teaching and Mentoring award. He is also three-times winner of the Associated Students of Caltech (ASCIT)

RFIC Technical Lecture continued...

Undergraduate Excellence in Teaching Award. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, Netherlands. He was a co-recipient of the IEEE Journal of Solid-State Circuits Best Paper Award, the International Solid-State Circuits Conference (ISSCC) Jack Kilby Outstanding Paper Award, a co-recipient of RFIC best paper award, a two-time co-recipient of CICC best paper award, and a three-time winner of the IBM faculty partnership award as well as National Science Foundation CAREER award and Okawa Foundation award. He co-founded Axiom Microdevices Inc., whose fullyintegrated CMOS PA has shipped around 400,000,000 units, and was acquired by Skyworks Inc.

He serves on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) as the chair of the technology directions sub-committee, and has served as an Associate Editor of the IEEE Journal of Solid-State Circuits (JSSC), as an Associate Editor of IEEE Transactions on Circuits and Systems (TCAS): Part-II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE Transactions on Microwave Theory and Techniques, and Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE).

Monday, 17 June 2024 08:00-09:40 Room 150AB

Session RMo1A: mm-Wave Transmitters and Receivers Chair: Giuseppe Gramegna, imec, Belgium Co-Chair: Magnus Wiklund, BeammWave, USA

RMo1A-1 08:00

A 60-GHz Positive-Feedback-Based Transmitter Front-End with 22.8% PAE_{max} in 28-nm Bulk CMOS for Inter-Satellite Communications

Kaijie Ding¹, Dusan Milosevic¹, Vojkan Vidojkovic¹, Khaled Khalaf², Mark Bentum¹, Peter Baltus¹; ¹Technische Universiteit Eindhoven, The Netherlands, ²Pharrowtech, Belgium

Abstract: This paper presents a power and area efficient 60-GHz RF-beamforming transmitter front-end (TXFE) in 28-nm bulk CMOS for inter-satellite communications. It consists of a vector modulator (VM) for phase shifting and gain control, a driver, and a power amplifier (PA). By applying a gain-boosting technique based on positive feedback, the number of cascaded stages is minimized, which reduces the total power consumption and enables chip area saving. Measurement results demonstrate a peak gain of 25.2 dB at 61 GHz, with a 22.6% maximum power-added efficiency (PAE_{max}) and a 12.4-dBm saturated output power (P_{sul}). The minimum stability factor (K_p) is 1.5. Additionally, at 61 GHz, this TXFE supports 2.4-Gbps SC/400-MHz OFDM 64 QAM, achieving 5.6/5.3% Error Vector Magnitude (EVM) and -31.4/-30.8-dBc Adjacent Channel Power Ratio (ACPR), at 5.1/3.7-dBm output power (P_{nup}) with 7.4/5.2% TX efficiency. The core area is 0.66×0.27 mm².

RMo1A-2 08:20

A Ka-Band 8-Element 4-Beam Transmitter Front End With Hybrid VGA and Symmetrical Transformer-Based Doherty PA

Huiyan Gao¹, Hang Lu¹, Shaogang Wang¹, Nayu Li¹, Gaopeng Chen¹, Chunyi Song¹, Yen-Cheng Kuan², Qun Jane Gu³, Zhiwei Xu¹; ¹Zhejiang University, China, ²NYCU, Taiwan, ³University of California, Davis, USA

Abstract: This paper presents a 27.7–31.2 GHz highly integrated 8-element 4-beam transmitter front end in 65-nm CMOS for phased-array applications. The proposed hybrid variable-gain amplifier (VGA) combines digital common-source (CS) VGA and analog Gilbert-cell-based VGA to realize a large tuning range and high resolution simultaneously. Furthermore, the proposed VGA scheme also integrates with an active combining network to implement a compact multi-beam structure. In the vector-modulation-based phase shifter (PS), low/high pass lumped delay lines are inserted between CS transistors and common-gate (CG) transistors to form I/Q signals which drive four pairs of Gilbert-cell based G_m -arrays for different phase states. In addition, the output element leverages a symmetrical transformer-based Doherty power amplifier (PA) and an analog adaptive bias to improve the power-back-off (PBO) efficiency with a high peak-to-average-ratio (PAPR) modulation signal. With a 1.1-V supply voltage, this front end achieves a saturated output power (P_{ext}) of 19.2 dBm with a 20.5% channel efficiency and a 1-dB compression point (OP_{LRB})

of 18.2 dBm. The measured maximum drain efficiency (DE) is 40.8% and 6-dB PBO DE is 28%. Compared with class-B/A PAs, the DE is improved by 40%/180%. The proposed hybrid VGA achieves a 27-dB tuning range and a 0.25-dB gain step with 0.26 dB/1.9° RMS gain/phase errors. The active PS implements 6-bit 360° phase shifting with 0.25 dB/2.5° RMS gain/phase errors.

RMo1A-3 08:40

A 32-Element 25.8-to-30.8GHz Phased-Array CMOS Transmitter with Programable Piecewise Linear Temperature-Compensation Technique Achieving ±0.002dB/°C Gain Variation Across -60-to-85°C

Dongze Li, Wei Deng, Ziyuan Guo, Haikun Jia, Xintao Li, Xiangyu Nie, Ruiheng Qiu, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents a 32-element 25.8-to-30.8 GHz phased-array CMOS transmitter (TX) with programmable piecewise linear temperature-compensation (TC) technique to counteract the increase and decrease in gain under high and low-temperature conditions, maintaining a constant gain within the operational temperature range of the system. The proposed TX is composed of four chips, which consists of a common channel with the TC block and eight elements. The chip is fabricated in 65nm CMOS process, exhibiting a 25.4 dB peak gain and 5 GHz bandwidth (BW) from 25.8-to-30.8 GHz. The measured OP1dB and saturation power are 11.6 dBm and 13.4 dBm, respectively. The corresponding PAE at the OP1dB and Psat are 18.8% and 26.4% at 28GHz, respectively. Results of temperature-variable gain showed ± 0.002 dB/°C gain variation over a range of -60-to-85°C.

RMo1A-4 09:00

A Blocker-Tolerant mm-Wave MIMO Receiver with Spatial Notch Filtering Using Non-Reciprocal Phase-Shifters for 5G Applications

Shahabeddin Mohin, Soroush Araei, Mohammad Barzgari, Negar Reiskarimian; MIT, USA **Abstract:** This work reports a highly-linear blocker-tolerant mm-wave MIMO receiver front-end for 5G and beyond-5G applications. The proposed architecture enhances the RX linearity performance by establishing a mm-wave spatial notch filter (SNF) at the LNA output. The SNF incorporates a low-loss non-reciprocal phase-shifter architecture that can be turned off in the absence of spatial blockers. A 27–31GHz four-element MIMO receiver prototype is implemented in a 45nm SOI technology and exhibits an in-notch IP1dB of -7.8dBm with up to 41dB spatial blocker rejection. Through significant cancellation of co-channel wideband blockers, the RX achieves an EVM of -32.6dB, while receiving a wideband 256-QAM 100MS/s desired signal.

RMo1A-5 09:20

A 56–65GHz Highly-Integrated FMCW Radar Transceiver with 7.8dB NF and 8GHz Chirp-Bandwidth in 65-nm CMOS

Jiangbo Chen¹, Shengjie Wang¹, Jiabing Liu¹, Qizhou Yang¹, Quanyong Li¹, Hui Nie¹, Qun Jane Gu², Chunyi Song¹, Na Yan³, Zhiwei Xu¹, ¹Zhejiang University, China, ²University of California, Davis, USA, ³Fudan University, China

Abstract: This paper proposes a 56–65 GHz highly-integrated frequency modulated continuous wave (FMCW) radar transceiver in 65 nm CMOS, featuring 7.8 dB NF and an 8 GHz chirp-bandwidth. The chip integrates 4-channel receiver (Rx) and 3-channel transmitter (Tx). A 15 GHz PLL and frequency multipliers with reconfigurable capacitor arrays are employed to generate the wideband signal with an 8 GHz chirp bandwidth. The Tx achieves a 14.08 dBm maximum output power, while the Rx exhibits a 7.8 dB NF at 5 MHz IF and a 66 dB conversion gain (CG). The measured phase noise is -97.5 dBc/Hz at 1 MHz offset in 60 GHz. And the measured best phase noise performance is -100.3 dBc/Hz at 1 MHz offset for a 52.4 GHz carrier. The proposed transceiver occupies 4.8 mm × 2.8 mm area including pads, and burns 610 mW power consumption.

Monday, 17 June 2024 08:00–09:40 Room 151AB

Session RMo1B: Advanced Packaging Enabling Heterogeneous Integration of SiGe HBT and III-V mm-Wave ICs Chair: Frédéric Gianesello, STMicroelectronics, France Co-Chair: Harshpreet Bakshi, Texas Instruments, USA

RMo1B-1 08:00

A 24–30GHz GaN Front-End MMIC with Coupled-Resonator Based Transmit/Receive Switch for 5G Millimeter-Wave Applications

Dingyuan Zeng¹, Haoshen Zhu¹, Qi Cai², Guangxu Shen², Outong Gao¹, Wenquan Che¹, Quan Xue¹; ¹SCUT, China, ²NJUPT, China

Abstract: This paper presents a compact wideband front-end MMIC with an integrated transmit/ receive (T/R) switch based on coupled-resonator technique. The output matching network (OMN) of PA is utilized to generate additional resonant pole in the RX mode and enables impedance transformation in the TX mode simultaneously. The RX branch utilizes coupled resonators to broaden gain bandwidth and achieve wideband noise matching in the RX mode. To validate the proposed architecture, a 24–30 GHz front-end MMIC for 5G millimeter-wave applications is implemented using a commercial 0.15- μ m GaN high electron mobility transistor (HEMT) process. In TX mode, it achieves a small signal gain over 17 dB, a 14.3–17% saturated PAE and 27.8–29.3 dBm saturated output power. The average output power, measured with 64QAM 100MSysm/s modulated signal at an EVM of -25 dB, is 21 dBm with an average PAE of 3.7%. Applying a 200-MHz OFDM signal with 10.77 dB PAPR, an ACLR of -29.5 dBc is measured without digital predistortion. The RX branch demonstrates a small-signal gain of over 18.8 dB, a noise figure of less than 4.4 dB, and an OP1dB of 9.7–12.9 dBm. In addition, the chip area is 2.1×2.6 mm².

RMo1B-2 08:20

Heterogeneously-Integrated Gallium Nitride and Indium Phosphide Devices for Ka-Band Amplifiers

Justin J. Kim, Michael D. Hodge, Mark R. Soler, Florian Herrault, Daniel S. Green, James F. Buckwalter; PseudolithIC, USA

Abstract: Heterogeneously-integrated millimeter-wave (mm-wave) amplifiers are fabricated on a common silicon interposer using two compound semiconductor device technologies, demonstrating the potential for high-frequency RFICs consisting of multiple device technologies. An Indium Phosphide (InP) heterojunction bipolar transistor (HBT) and Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) are integrated into a high-resistivity silicon substrate with a 4-metal back-end-of-the-line (BEOL) to support high-quality factor (Q) passives for matching networks. The 21–32 GHz InP amplifier offers more than 10 dB gain and 22.5 dBm saturated output power (P_{sit}). The 26–31 GHz GaN amplifier offers more than 6 dB gain and has an output power exceeding 25 dBm. Both circuits are extremely compact, occupying an area of less than 1.0 mm-sq with pads.

RMo1B-3 08:40

A G-Band Glass Interposer Technology for the Integration of an Amplified Noise Source Based on SiGe BiCMOS 55-nm Technology

Maya Alawar¹, Victor Fiorese², Sylvie Lépilliet¹, Daniel Gloria², Guillaume Ducournau¹, Emmanuel Dubois¹; ¹IEMN (UMR 8520), France, ²STMicroelectronics, France

Abstract: This paper introduces a substrate technology that integrates an amplified noise source (NS) based on SiGe BiCMOS B55 nm technology onto a glass interposer to reduce dielectric and transition losses. Previous work has focused on the development and characterization of the NS in two distinct configurations. In a first flavor, on-wafer noise measurements yielded to an extracted excess noise ratio (ENR_{av}) level of 37 dB in the 140–170 GHz. In an alternative approach, the NS was packaged in a split-block with a WR5.1 flange termination for connection to commercial passive probes, achieving an ENR_{av} level of up to 25 dB in G-band (140–220 GHz) corresponding to a 12 dB ENR reduction when compared to the on-wafer measurements. To reduce dielectric losses due to the substrate, this paper proposes a third integration route based on an ultra-thin glass interposer, AF32 from Schott. This solution implements femtosecond laser micro-machining to structure the interconnects, enabling the integration of the NS chip on the same substrate used to manufacture the coplanar probing tips, with the advantage of simplifying the signal propagation path. This work has achieved a tunable ENR_{av} level of up to 29 dB in the 140–170 GHz range, with constant output impedance matching better than -12 dB across the entire frequency band.

RMo1B-4 09:00

A 22FDX Wi-Fi PA Demonstrating a New LDMOS Device with 10V Breakdown Achieving Output Power of 29.5dBm at 40% PAE

Arul Balasubramaniyan¹, Xuemei Hui², Abdellatif Bellaouar¹, Miguel Meza Campos¹, Apurv Bharadwaj¹, Elan Veeramani¹, Shafi Syed¹; ¹GlobalFoundries, USA, ²GlobalFoundries, China

Abstract: This paper presents a new LDMOS device in 22FDX for Wi-Fi PA applications. The device has significantly better Ft, Fmax, and higher breakdown voltage than conventional LDMOS, thus making it an excellent choice for integrated PA applications. The two stacked PA design with this new LDMOS device achieves 29.5dBm of Saturated Power with 40% PAE and 26dB Low Power Gain at 6GHz. Reliability stress test for 72hours and ruggedness test at a VSWR of 6:1 show almost no degradation in Gain, Psat and PAE. The ruggedness test at VSWR of 6:1 was repeated with the supply voltage increased from nominal supply of 5V to show the new LDMOS device breaks down at 10V, which is one of the highest reported breakdown voltage for a LDMOS device in sub-45nm FDSOI technology. Also, this Wi-Fi PA has excellent measured AM-AM and AM-PM characteristics.

RMo1B-5 09:20

A Reconfigurable Compact Multiband RF Bi-Directional Coupler for Sub-6GHz RF Front-Ends in RF SOI CMOS Switch Technology

Ting-Li Hsu¹, Amelie Hagelauer¹, Valentyn Solomko²; ¹Technische Universität München, Germany, ²Infineon Technologies, Germany

Abstract: In this work, a radio-frequency (RF) bi-directional coupler with tunable operating frequency is presented. To cover the entire sub-6 GHz spectrum, the directivity is optimized for different frequencies with the proposed digitally controlled-tuning network by compensating the frequency dependency of the coupling components and the degradation induced by parasitics. The tuning network with an inductive component and its area-efficient design is proposed. The device is implemented in 90nm RF SOI CMOS switch technology. The designed tuning network allows the coupler to have a directivity of over 30 dB from 700MHz to 6 GHz with a power consumption of only 29 μ W. An input-referred third-order intercept point (IIP3) of 110dBm is reached for the signal through the transmitted path.

Monday, 17 June 2024 08:00-09:40 Room 152AB Session RMo1C:

Unleashing RF Systems: From 5G to Low-Power Sensing Chair: Pierluigi Nuzzo, University of Southern California, USA Co-Chair: Yao-Hong Liu, imec, The Netherlands

RMo1C-1 08:00

A 2.4GHz, -19 dBm Sensitivity RF Energy Harvesting CMOS Chip with 51% Peak Efficiency and 24dB Power Dynamic Range

Jing-Ren Yan¹, Yao-Wei Huang¹, Wei-Jen Lai², Jen-Hao Liao², Ching-Chun Lin², Yu-Te Liao¹; ¹NYCU, Taiwan, ²Novatek Microelectronics, Taiwan

Abstract: This work proposes a 2.4 GHz wireless energy harvesting chip with a meander dipole antenna. The design was fabricated in a 180-nm standard CMOS process and occupies a chip area of $2.3 \times 2.5 \text{ mm}^2$ while consisting of a reconfigurable rectifier, a bandgap reference, a maximum power point tracking controller, a $3 \times$ switched-capacitor charge pump, two regulators, and an ultralow power diode. The design achieves a peak power efficiency of 51.9% at -4 dBm and sensitivity of -19 dBm. The peak power efficiency of SCCP3× is 97.2%, and the reverse leakage current of ULPD is less than 2 nA. The automatic maximum power tracking scheme extends the >20% power efficiency range to 24 dB.

RMo1C-2 08:20

A 45nm RFSOI CMOS-Based 24.25–29.5GHz 2×16-Channel Phased-Array Transceiver IC for 5G NR Applications

Jooseok Lee, Seungjae Baek, Kihyun Kim, Seungwon Park, Hansik Oh, Taewan Kim, Joonho Jung, Jinhyun Kim, Sehyug Jeon, Jee Ho Park, Woojae Lee, Jaehong Park, Dong-hyun Lee, Sangho Lee, Jeong Ho Lee, Ji Hoon Kim, Younghwan Kim, Sangyong Park, Bohee Suh, Soyoung Oh, Dongsoo Lee, Juho Son, Sung-gi Yang; Samsung, Korea

Abstract: This paper presents a broadband 2×16-channel phase-array transceiver IC based on a 45-nm radio frequency silicon-on-insulator CMOS device technology for fifth-generation millimeter-wave frequency band (n257, n258, and n261) applications. The transceiver IC that mainly consists of compact single-transformer based Doherty power amplifiers with frequency-shift capabilities to support wideband operation and low-noise amplifiers shows an outstanding RF performance, occupying the small die area/Ch. of 1.87 mm². When operating in transmitter path, it shows great average power of > 11.0 dBm/Ch. at error vector magnitude of -25 dB, consuming low DC power of < 155 mW/Ch. It also shows remarkable system noise figure of 3.2 -3.7 dB with low DC power consumption of < 48.8 mW/Ch. in receiver path.

RMo1C-3 08:40

A Fully Integrated Microplastic Detection SoC with 0.1–3GHz Bandwidth and 35dB Dynamic Range for Narrow-Band Notch RF MEMS Sensor System

Seung-Beom Ku¹, Jinhyoung Kim², Kwon-Hong Lee¹, Han-Sol Lee¹, Kyeongho Eom¹, Joonghoon Kang¹, Hyungjin Jung¹, Cheolung Cha², Hyung-Min Lee¹; ¹Korea University, Korea, ²KETI, Korea

Abstract: This paper proposes a fully integrated microplastic (MP) detection system-on-chip (SoC) for RF MEMS sensors with a narrow-band notch point operating in 1.19-1.22 GHz range. This 180-nm CMOS MP detection SoC comprises an LC VCO and an envelope-based readout circuit. The RF MEMS sensor is driven by a high linearity LC VCO, providing an output power of 7.98 dBm at 1.22 GHz, while the LC VCO can maintain near-constant output power levels with small variation of 2.13% between 1.19 GHz and 1.22 GHz. Also, the readout circuit with a high dynamic range (DR) can analyze the resonant frequency shifts of the RF MEMS sensor operating at the range of 0.1-3 GHz. The readout circuit employs a time-based 10-bit current-steering digital-to-analog converter (CS-DAC) with a ramp generation, allowing it to detect the input power as low as -20 dBm while accommodating input power variations with 35 dB DR. The RF MEMS sensor driven by the proposed SoC operates as narrow-band notch filter and resonates at 1.2 GHz depending on MP concentration. When 5 μ L of 1% standard polyethylene (PE) dispersion was injected 4, 8, 12 and 16 times, the resonant frequencies were shifted to 0.31 MHz, 0.89 MHz, 1.06 MHz, and 1.17 MHz, respectively.

RMo1C-4 09:00

A 21–27-GHz Frequency Quadrupler in 0.13 μ m SiGe BiCMOS with 0-dBm P_{our} and 40-dBc HRR for Wideband 5G Applications

Caglar Ozdag¹, Arun Paidimarri¹, Masayuki Yoshiyama², Yuichiro Yamaguchi², Yujiro Tojo², Bodhisatwa Sadhu¹; ¹IBM T.J. Watson Research Center, USA, ²Fujikura, Japan

Abstract: A 21–27-GHz frequency quadrupler in 0.13µm SiGe BiCMOS technology with 0-dBm output power (P_{OUT}) and 40-dBc harmonic rejection ratio (HRR) is presented. A method for load-pull based output network design is introduced for co-optimizing HRR and P_{OUT} ; as a result, the design achieves flat and exceptionally high HRR and P_{OUT} across 25% bandwidth (BW) and a wide input power (P_{IN}) range. System integration of LO multipliers in wideband scalable 5G phased-array transceivers (TRX) is discussed. In this context, measurements of 64-element wideband 5G phased-array TRXs including and excluding the quadrupler are presented to further demonstrate the minimal impact of the quadrupler on the output spectrum. The measured total radiated power (TRP) of spurious emissions across the P_{OUT} range of the phased-array is < -20dBm/MHz, well below the 3GPP 5G FR2 requirement of -13dBm/MHz. The quadrupler design has the highest HRR performance reported among wideband mmWave quadruplers and demonstrates, for the first time, the impact of the LO frequency multiplier on the performance of a wideband phased-array system.

RMo1C-5 09:20

Design of a Dual-Mode Coil-Reuse Data Acquisition System for Miniaturized Wirelessly Powered Biopotential Sensing Nodes

Hamid Jafari Sharemi, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: This work introduces a novel coil sharing technique to implement small form factor wirelessly powered biopotential recording systems. Coil used for wireless power transfer is shared with a power oscillator to transmit an on-off keying uplink signal at the same frequency as wireless power transfer (40.68 MHz) when the power signal is turned off for a short time, forming a single-coil, bidirectional, and synchronized data acquisition system. The designed batteryless system drains a current of 1.2 to 16.9 μ A from a 1.1 V harvested voltage when data rate varies from 1 to 20 kbps. A prototype of the proposed design is fabricated in a 180-nm CMOS process and packaged on a compact circular board (5 cm diameter), which achieves a powering and uplink distance of 20 cm and 15 cm, respectively.

Monday, 17 June 2024 10:10-11:50 Room 150AB

Session RMo2A: mm-Wave Transceivers and RF Techniques Chair: Abhishek Agrawal, Intel, USA Co-Chair: Andrea Bevilacqua, Università di Padova, Italy

RMo2A-1 10:10 A Compact Ka-Band Bi-Directional PA-LNA with 17.4-dBm P_{sat} Using Three-Stack Power Amplifier in 28-nm CMOS

Jun Hwang, Byung-Wook Min; Yonsei University, Korea

Abstract: This paper presents a compact Ka-band bi-directional power amplifier-low-noise amplifier (PA-LNA) employing a three-stack PA in a 28-nm CMOS process. In the proposed PA-LNA, the three-stack PA is cross-coupled with a common-source LNA to neutralize gate-drain capacitance (C_{gd}) of the LNA, enhancing stability and gain in LNA mode. Simultaneously, the three-stack PA achieves higher output power and gain in PA mode. Furthermore, transformer-based matching networks enable fully bi-directional operation within a compact die area. In PA mode, the proposed PA-LNA demonstrates a peak gain of 20.4 dB with a 3-dB bandwidth of 8.1 GHz (27.3–35.4 GHz), a saturated output power (P_{sat}) of 17.4 dBm with a peak power-added-efficiency (PAE) of 17.2%, and an error vector magnitude (EVM) of -31.5 dB with 256-quadrature amplitude modulation (QAM) and 800-MBaud symbol rate at 7-dBm average output power. In LNA mode, the proposed PA-LNA demonstrates a peak gain of 17.3 dB with a 3-dB bandwidth of 8 GHz (28.0–36.0 GHz), a noise figure (NF) of 5.3 dB, and an input third-order intercept point (IIP3) of 0 dBm. The core area of the PA-LNA is only 0.1 mm².

RMo2A-2 10:30

A Reconfigurable Ultra Compact Bi-Directional Amplifier with a Build-in-Self Notch Filter for K/Ka-Band Satellite Communication

Jian Zhang¹, Ming Zhai¹, Dawei Wang¹, Xiangjie Yi¹, Wei Zhu², Yan Wang¹, ¹Tsinghua University, China, ²BIT, China

Abstract: Extremely high cost and form factor have become the most important reason limiting the promotion of K/Ka-band satellite communication (SATCOM) devices with thousands of phased-array channels. To address this challenge, a reconfigurable ultra compact bi-directional amplifier with a build-in-self notch filter in 45-nm CMOS SOI technology is presented in this paper. The receiver (RX) and transmitter (TX) can use one such reconfigurable chip rather than two different chips and cut the manufacturing cost by more than half. In this design, the low noise amplifier (LNA) is stacked into the power amplifier (PA) by using a magnetic coupling self-canceling technique, improving area efficiency greatly with negligible performance penalty. The reconfigurable bi-directional amplifier achieves 18.3 dBm max Psat and 15.9 dBm max OP1dB in PA mode while maintaining a minimum NF of 2.46 dB in LNA mode. The core area of this design is only 0.14 mm², which is similar to a conventional LNA or PA. Furthermore, benefiting from the design of build-in-self notch filter, the proposed bi-directional amplifier has good gain suppression (> 45 dB) to block the
interferer from the TX chips in LNA mode. This work contributes a key innovation toward a new lowcost architecture for SATCOM, and it is the first reported high-performance bi-directional amplifier designed for K/Ka band SATCOM to the best of the author's knowledge.

RMo2A-3 10:50

Fully Integrated SiGe HBT BiCMOS Transmit-Receive Front-End IC for 5G mmW Radio with a Reconfigurable Built-In Diode RF Switch

Insu Han, Hanjung Lee, Inchan Ju; Ajou University, Korea

Abstract: This work presents a novel SiGe HBT BiCMOS TRX front-end for 5G mmW radio. A builtin base-to-collector diode (D_{BC}) of a CB HBT in a cascode, with a coupled line impedance inverting balun, is reconfigured to reverse- or forward-biased to act as a PA or an RF switch in TX and RX modes, respectively. This architecture enables to remove any lossy switch in TX path, which leads to improvement in P_{out} , PAE, and NF simultaneously. It attains peak P_{out} of 22.0 dBm, 36.5% PAE, and the minimum NF of 3.08 dB at 28 GHz. It also supports linear amplification of 400 MHz 64 QAM 5G NR FR2 CP signal.

RMo2A-4 11:10 Non-Coherent TX-RX Chipsets for J-Band Communication in 16-nm FinFET CMOS

Berke Gungor, Patrick Reynaert; KU Leuven, Belgium

Abstract: This paper presents a set of Transmit (TX) and Receive (RX) chipsets for J-band (252–325 GHz) communication, implemented in 16-nm FinFET CMOS. Both systems are designed to utilize amplitude-shift-keying (ASK) modulation and to operate non-coherently, alleviating the need for a synchronized LO between TX and RX. Both chips are characterized standalone in a probe station. The TX achieves an output power of -19 dBm at 270 GHz center frequency with a 3-dB bandwidth of 45 GHz. The RX has a conversion gain of 31 dB with a baseband bandwidth of 0–25 GHz. The performance of the RX is verified with modulated measurements, with up to 20 Gbps NRZ at 280 GHz carrier, limited by the measurement setup.

RMo2A-5 11:30

A $\Sigma \Delta$ -Modulated Linear-in-dB Attenuator for On-Chip Power Detection with 0.12dB Resolution in RF SOI CMOS Switch Technology

Ting-Li Hsu¹, Valentyn Solomko², Amelie Hagelauer¹; ¹Technische Universität München, Germany, ²Infineon Technologies, Germany

Abstract: In this work, an innovative scheme to boost the resolution of the variable radio-frequency (RF) attenuator is proposed and examined. The attenuator stage modulated by a first-order sigmadelta modulator ($\Sigma\Delta M$) shows a linear-in-dB attenuation profile for the average RF power with high resolution. The proposed attenuator provides a low-power solution for accurate on-chip power measurement with zero quiescent current. The implemented attenuator shows an effective attenuation tuning step size of 0.12 dB from 700MHz to 6 GHz with a power consumption of only 41.4 μ W. The device is designed and fabricated in 90nm RF SOI CMOS switch technology.

Monday, 17 June 2024 10:10–11:50 Room 151AB

Session RMo2B: High-Performance Multi-Mode, Multi-Core Oscillators Chair: Andrea Mazzanti, Università di Pavia, Italy Co-Chair: Bichoy Bahr, Texas Instruments, USA

RMo2B-110:10An Octave Tuning Range Quad-Core VCO Using a Compact Quad-ModeTransformer-Based Inductor

Hyunjoon Kim, Sangmin Kim, Sanggeun Jeon; Korea University, Korea

Abstract: This work presents an octave tuning range quad-core voltage-controlled oscillator (VCO) using a quad-mode transformer-based inductor with compact size. The proposed inductor comprises outer and inner transformers, leveraging both even- and odd-mode excitation current from the quad VCO cores. In comparison to other works, this approach significantly simplifies design complexity and reduces chip area because the proposed quad-mode inductor involves only four design parameters. Furthermore, quad-mode operations of the proposed inductor are achieved without switch loss by controlling mode switches between adjacent and distant VCO cores. Therefore, wideband inductive frequency tuning can be realized without Q-degradation and high power consumption. The VCO, implemented in a 28-nm CMOS technology, achieves a frequency tuning range of 72.6% from 17 to 36.4 GHz. The chip consumes 9.7-13.3 mW at a 0.6-V supply voltage and core area of 0.065 mm². The proposed VCO attains a peak FoM_T of 196.3 dBc/Hz and peak FoM_{Tx} of 208.1 dBc/Hz.

RMo2B-2 10:30 An 18.5-to-36.5GHz 206.8dBc/Hz FoM_T Quad-Core Triple-Mode VCO with Automatic-Mode-Tracking Output Buffers

Ziyi Lin, Haikun Jia, Wei Deng, Baoyong Chi; Tsinghua University, China

Abstract: In this paper, we propose a quad-core triple-mode VCO with switched inductors. Two identical single-turn coils with high Q factors are implemented symmetrically and are magnetically coupled with each other. Three equivalent inductances are achieved by controlling the current directions in two coils through mode switches. An automatic-mode-tracking buffer with two magnetically coupled inductors is proposed to boost the output amplitude of the VCO and save power. Two stages of cascaded dividers are used for covering a wider output frequency range. Fabricated in a 65-nm CMOS process, the proposed VCO achieves a TR of 65.5% from 18.5 GHz to 36.5 GHz. Under a supply voltage of 0.45 V, the VCO core consumes a power of 3.9 to 5.2 mW. The measured phase noise at 10 MHz offset is -121.6 to -130.3 dBc/Hz. The measured peak FoM is 190.5 dBc/Hz at 10 MHz offset and peak FOM_w is 206.8 dBc/Hz.

RMo2B-3 10:50

A 52.3-to-67.3GHz 35.8-kHz-Resolution Triple-Push DCO Exploiting Source-Combining Technique for Third-Harmonic Enhancement Achieving 196.4dBc/Hz Peak FoM_T at 10MHz Offset

Qiyao Jiang¹, Jun Yin¹, Quan Pan², Rui P. Martins¹, Pui-In Mak¹; ¹University of Macau, China, ²SUSTech, China

Abstract: This paper presents a millimeter-wave (mm-Wave) triple-push digital-controlled oscillator (DCO). The 3rd-harmonic current is boosted by combining the 6-phase outputs through the source nodes of G_m transistors, resulting in high output power and inherent 1st-/2nd-harmonic spurs rejection. The off-resonance oscillation problem of the triple-push structure is eliminated by coupling the auxiliary transconductance cell. A high frequency resolution is achieved by using the phase tuning technique. The DCO in 65nm CMOS occupies 0.095mm² and exhibits a best-inclass FoM_T at 10MHz offset of 194 to 196.4dBc/Hz from 52.3 to 67.3GHz with a 35.8kHz frequency resolution.

RMo2B-4 11:10

An 11GHz 8-Core Series Resonance CMOS VCO with Scalable Ring-Coupling Scheme Achieving Phase Noise of -136.8dBc/Hz at 1MHz Offset

Shiwei Zhang, Wei Deng, Haikun Jia, Baoyong Chi; Tsinghua University, China

Abstract: This paper proposes X-band multi-path ring-coupling dual-core and hybrid-coupling octa-core series resonance VCOs to achieve ultra-low phase noise. The scalable multi-path ring-cross-coupling scheme is suitable for multi-core intrinsic oscillation, through various ring paths in oscillators with multiple resonance cells. The tuning range and FoM variation of the VCO are further improved. Prototyped in a 65-nm CMOS process, the 8-core 16-coil series resonance VCO achieves -136.8dBc/H at 1MHz offset frequency and -157.2 dBc/Hz at 10MHz offset from the carrier frequency of 11.02 GHz. To the best knowledge of the authors, this work reports the VCO with the lowest phase noise in CMOS technology in open literature so far.

RMo2B-5 11:30

A K-Band Voltage-Controlled Oscillator with Gate-Drain Phase Shift Achieving 110kHz $1/f^{3}$ Corner

Zhenhua Jia¹, Dawei Ye²; ¹Fudan University, China, ²HUST, China

Abstract: This work presents a K-band low flicker phase noise (1/f³) corner voltage-controlled oscillator (VCO) utilizing gate-drain phase shift. It incorporates two auxiliary LC tanks to shift the relative phase of the fundamental harmonic between the gate-drain and attenuate the second harmonic components at the output waveform. This design effectively suppresses phase noise caused by flicker noise upconversion without compromising the desired 1/f² phase noise (PN) performance. By utilizing gate-drain phase shift to symmetrize the effective impulse sensitivity function (ISF), the proposed VCO achieves a 1/f³ PN corner of 110kHz while consuming only 4.18mW at 19.64GHz. The design is implemented in a 65nm technology process with an active area of 0.1mm². The measured phase noise at a 1MHz offset frequency is -113.21dBc/Hz, yielding a peak Figure-of-Merit (FoM) of 186.84dBc/Hz at 19.64GHz.

Monday, 17 June 2024 10:10–11:50 Room 152AB Session RMo2C:

Interference Resilient and Energy Efficient Transmitters and Receivers Chair: Chun-Huat Heng, National University of Singapore, Singapore Co-Chair: Justin Wu, AmLogic, Taiwan

RMo2C-1 10:10

A Sub-6GHz Wideband Transmitter with LO Harmonic Rejection RF Front-Ends Using Frequency-Adaptive Calibration

Haoyu Bai, Dong Wang, Keer Gao, Jiaqi He, Jiazheng Zhou, Junhua Liu, Huailin Liao; Peking University, China

Abstract: This paper presents a broadband 0.1–6GHz transmitter that integrated a 0.1–2.5GHz local oscillator (LO) harmonic rejection (HR) RF front-end (RFFE) based on the LO frequency-adaptive calibration scheme. In the HR-RFFE, a programmable RC network is set to achieve the intermediate frequency domain harmonic rejection and pre-calibration. In the 8-phase LO generator, the cross-connected Gilbert phase detector provides the detection of the orthogonality of 90° shifted LO signals for the calibration of the LO phase errors due to the frequency variation. The in-phase (I) and quadrature (Q) signals are calibrated separately and summed in the power amplifier. Implemented in 40nm CMOS, the transmitter occupies 1.1×1.1 mm². With the baseband and RFFE, the transmitter achieves a gain of over 26dB, a P1dB compression point of 16.1dBm, and a system efficiency of 25.9%, while operating at 0.1–6GHz. With the calibration techniques, the 3rd and 5th LO harmonic rejection ratios are over 46.9 dBc and 53.5 dBc, respectively.

RMo2C-2 10:30

An 11.8mW 0.4-to-2.6GHz Blocker-Tolerant Receiver with LO Duty-Cycle Compensation and High-Q Selectivity Achieving +15.4/19.2dBm OB-IIP3 at 10/80MHz Offset

Rundi Wu, Yetong Wang, Ran Hong, Kenan Xie, Keping Wang; Tianjin University, China **Abstract:** This paper presents a mixer-first blocker-tolerant receiver (RX) with LO duty-cycle compensation and high-Q selectivity. A novel technique is proposed to mitigate noise figure (NF) and out-of-band (OB) IIP3 performance degradation caused by reduced LO drive capability at high frequencies. LO duty-cycle compensation is designed with the bias-tunable mixer to improve NF and OB-IIP3 at the high operating frequency while avoiding the large power consumption of LO drivers. Moreover, the proposed RX topology achieves high-Q selectivity by combining an auxiliary N-path filter at RF and an analog finite-impulse-response (AFIR) filter at baseband (BB). The RX prototype, fabricated in a 55-nm CMOS process, achieves wideband tunable high-Q selectivity from 0.4 to 2.6GHz. The RX achieves +15.4/19.2dBm OB-IIP3 (at 10/80MHz offset) and 2.4 to 3.5dB NF, while consuming 5.4 to 11.8mW power consumption, of which the LO drivers only need 2.9mW/GHz. The active chip area is only 0.29 mm².

RMo2C-3 10:50

A 2.8–4.3GHz Simultaneous Dual-Carrier Transformer-Coupled Passive Mixer-First Receiver Front-End Supporting Blocker Suppression

Jamie C. Ye, Alain Antón, Russ H. Huang, Sanaz Sadeghi, Alyosha C. Molnar; Cornell University, USA **Abstract:** This paper presents a high dynamic range N-path passive mixer-first receiver architecture capable of simultaneously down-converting two arbitrary bands through a single RF port. The architecture consists of two passive mixers arranged in a series configuration with a transformer front-end to minimize cross-loading between mixers while still providing impedance transparency and associated interference suppression for both bands. The receiver was fabricated in a 16nm FinFET process and operates from 2.8–4.3 GHz. The measured noise figure (NF) is 6.8–9.7 dB with 25–28mW of power consumption per channel. In single-carrier operation, the architecture enables additional blocker suppression and improves the out-of-band (OOB) blocker compression (B1dB) from 8.9 to 14.4dBm and input-referred 3rd order intercept point (IIP3) from 18.6 to 27.6 dBm.

RMo2C-411:10A 2.3nJ/b 32-APSK Polar Phase-Tracking Receiver with Two-Point Injection
Technique

Xuansheng Ji, Jiahao Zhao, Woogeun Rhee, Zhihua Wang; Tsinghua University, China

Abstract: This paper presents a polar phase-tracking RX (PT-RX) that supports multiple modulation schemes including differential phase shift keying (DPSK), amplitude shift keying (ASK) and amplitude phase shift keying (APSK). By employing a two-point injection method in a wideband digital phase-locked loop (DPLL), the proposed polar PT-RX performs various demodulations without requiring quadrature signal generation or a multi-bit analog-to-digital converter (ADC). Compared with existing PT-RXs, the proposed architecture not only overcomes the trade-off between frequency pulling and image rejection but also provides the equivalent constant gain of a digitally-controlled oscillator (DCO) for robust demodulation. A prototype 5.8mW 2.4GHz polar PT-RX is implemented in 65nm and performs 2.5Mb/s 32-APSK demodulation with -64dBm sensitivity.

RMo2C-5 11:30

A 0.77mW 1.84nJ/Bit Phase Noise Canceling Receiver for QAM and OFDM and Cellular IoT

Trevor J. Odelberg, David D. Wentzloff; University of Michigan, USA

Abstract: A low-power RX is presented for cellular IoT applications. The RX utilizes a phase noise cancelling architecture designed for QPSK/QAM and OFDM and consumes 612μ W for QPSK and 765 μ W for 16QAM. The RX utilizes a mixer-first and self-mixing hybrid architecture and uses an optimized analog squarer to cancel the phase noise of the ring oscillator (RO) with the addition of a pilot tone. The RX can demodulate phase-modulated data despite the use of a high phase noise RO. Additionally, the RX can coherently demodulate QPSK/QAM data without the need for phase synchronization or a PLL. The RX achieves a high data rate at low power and has the lowest energy per bit for a <1mW RX at 1.84nJ/bit. The RX achieves a normalized sensitivity of -98/-93dBm for QPSK/16QAM and OFDM. The RX is the only low-power RX that can support QAM and OFDM.

Monday, 17 June 2024 13:30–15:10 Room 150AB

Session RMo3A: mm-Wave Power Amplifiers

Chair: Jane Gu, University of California, Davis, USA Co-Chair: Gernot Hueber, United Micro Technology, Austria

RMo3A-1 13:30

A Class-J/F 60GHz Power Amplifier with 42.3% Power Added Efficiency in FDSOI CMOS

Mengqi Cui, Jens Wagner, Frank Ellinger; Technische Universität Dresden, Germany

Abstract: A compact 60 GHz class-J/F amplifier in 22 nm FDSOI (fully depleted silicon on insulator) CMOS with high efficiencies at low supply voltages is analyzed and presented in this paper. It utilizes a pseudo-differential common source gain cell with a 0.8 dB insertion loss output transformer balun. At 1.1 V, 0.6 V, and 0.4 V supply, power added efficiencies of 42.3%, 37.7% and 29.8%, and saturated output powers of 14.3 dBm, 9.5 dBm and 6.4 dBm, respectively, are measured. The active circuit area is only 0.0198 mm².

RMo3A-2 13:50

A 25–40GHz Three-Way Power Amplifier with No Load Modulation Achieving Broadband Deep Power Back-Off Efficiency Enhancement

Edward Liu¹, Han Zhou², Christian Fager², Hua Wang¹; ¹ETH Zürich, Switzerland, ²Chalmers University of Technology, Sweden

Abstract: This paper presents a millimeter-wave (mm-Wave) power amplifier (PA) topology that avoids the trade-off between bandwidth and load modulation. The proposed topology uses three PA paths and can achieve efficiency enhancement at power back-off without load modulation. With a 100 MHz 5G NR FR2 1-CC 64-QAM signal, this PA achieves P_{AVG} and PAE_{AVG} of 6.45–12.61 dBm and 5.9–16.4% from 25–40 GHz, respectively. With a 200 MHz, signal, P_{AVG} and PAE_{AVG} are 5.58–11.1 dBm and 4.8–13.3%, respectively.

RMo3A-3 14:10

A 22–44GHz 28nm FD-SOI CMOS 5G Doherty Power Amplifier with Wideband PAE_{6dBPBO} Enhancement and 3:1 VSWR Resiliency

Gwennaël Diverrez¹, Eric Kerherve¹, Magali De Matos¹, Andreia Cathelin²; ¹IMS (UMR 5218), France, ²STMicroelectronics, France

Abstract: This paper presents a broadband 5G power amplifier robust to VSWR variations and featuring high efficiency up to deep power back-off in 28nm FD-SOI CMOS technology. The proposed architecture, based on a quasi-balanced structure and an inductive load, offers an alternative to the conventional Doherty PA to maintain its PAE_{6dBPB0} enhancement up to 3:1 VSWR over a wide bandwidth. Indeed, the degradation of its PAE_{6dBPB0} is kept below 7% between 22 and 44 GHz. The circuit achieves 24% PAE_{6dBPB0} and 16% $PAE_{9,7dBPB0}$ at 28 GHz, while guaranteeing linearity in line with the 5G standard. The PA occupies a surface area of 0.82 mm².

RMo3A-4 14:30

A 25–31GHz Compact True Power Detector with >33dB Dynamic Range in 40nm Bulk CMOS

Haoqi Qin¹, Junjie Gu¹, Hao Xu¹, Zhiwei Xu², Pengcheng Jia³, Na Yan¹; ¹Fudan University, China, ²Zhejiang University, China, ³Starway Communication, China

Abstract: This paper presents a compact mixer-based true power detector (PD) integrated within a Ka-band power amplifier (PA). The proposed compact PD avoids on-chip balun by sensing the voltage and current from the primary coil. Flicker noise suppression by current bleeding and linearity enhancement in the mixer expand the overall dynamic range of power detection. Intrinsic phase compensation in the detection paths removes the need of additional phase shifters, which further saves area cost. Fabricated in a 40nm CMOS process, the PD occupies a core area of 3520 μ m² and maintains a dynamic range of >33dB across 25–31GHz with 12.1mW power consumption.

RMo3A-5 14:50

A Compact Dual-Mode CMOS Power Amplifier Covering both Sub-6GHz and mm-Wave Bands for 5G NR

Jingye Zhang¹, Jiawen Chen², Taotao Xu¹, Pei Qin¹, Xiang Yi¹, Liang Wu³, Haoshen Zhu¹, Wenquan Che¹, Quan Xue¹; ¹SCUT, China, ²University College Dublin, Ireland, ³CUHK-Shenzhen, China

Abstract: This paper presents a dual-mode power amplifier (PA) that covers both the 5G FR1 and FR2 bands. By utilizing the common-mode (CM) path and differential-mode (DM) path simultaneously, this PA achieves 3.5GHz and 27GHz band coverage with only one amplifying stage and consequently compact layout. The proposed PA achieves a PAE_{IdB} and P_{IdB} of 30.9%/17.6dBm and 36.1%/15.3dBm, respectively, at 27GHz in DM and 3.5GHz in CM. The proposed PA exhibits a performance of -25.9dBc ACLR, 17% average PAE, and 12.4dBm average output power at -24.7dB EVM_{RMS} with 64QAM 200MSym/s modulation signal at 26GHz in DM. Similarly, with 256QAM 50MSym/s modulation at 3.6GHz in CM, the PA demonstrates -35.6dBc ACLR, 22.5% average PAE, and 10.7dBm average power at -31.1dB EVM_{RMS}. The PA is fabricated in 65nm CMOS process with chip area of only 0.32mm².

Monday, 17 June 2024 13:30–15:10 Room 151AB Session RMo3B: RF and mm-Wave Frequency Multipliers

Chair: Fa Foster Dai, Auburn University, USA Co-Chair: Salvatore Finocchiaro, Qorvo, USA

RMo3B-1 13:30

A 0.2–25GHz Inductorless Complementary Pseudo-Push-Push Frequency Doubler

Changwenquan Song, Chen Yu, Liang Wu; CUHK-Shenzhen, China

Abstract: An inductorless and buffer-less complementary pseudo-push-push frequency doubler (CP3FD) demonstrating expansive operational bandwidth and low DC power consumption. The pseudo-push-push operation is implemented by a synergistic common-gate and common-source configuration, establishing a single-ended resistive impedance at the input and thereby allowing substantial expansion of the bandwidth. Additionally, a complementary structure is proposed, which not only reduces power consumption by current reuse but also improves the fundamental rejection ratio (FRR) significantly. Fabricated in a 65-nm CMOS process, the proposed CP3FD measures a maximum conversion gain (CG) of -10.1 dB and a 3-dB frequency range from 0.2 to 25 GHz, with an input signal power of 0 dBm. The core area of the chip is only $39 \times 65 \ \mu m^2$.

RMo3B-2 13:50

A Compact D-Band Multiply-by-9 Frequency Multiplier with Inductor-Less Active Balun in 16nm p-FinFET Technology

Runzhou Chen, Hao-Yu Chien, Mau-Chung Frank Chang; University of California, Los Angeles, USA

Abstract: This work presents a compact D-band multiply-by-9 frequency multiplier in TSMC 16nm technology, featuring the RF p-FinFET devices. The design includes elements such as an inductorless active balun at the input stage, two frequency tripler cells, an inter-stage amplifier, and a 2-stage power amplifier (PA) at the output. The proposed frequency multiplier achieves 1.6-dB conversion gain, -2.8-dBm Psat, and 45-dB harmonic rejection ratio while taking a core area of only 0.068 mm² and DC power of 58 mW.

RMo3B-3 14:10

A 17.4–26.4-GHz Dual-Injection Injection-Locked Frequency Tripler Featuring Low Power Consumption and High Harmonic Rejection

Qingfan Zeng, Jingzhi Zhang, Yiming Yu, Huihua Liu, Yunqiu Wu, Chenxi Zhao, Kai Kang; UESTC, China

Abstract: This paper presents a dual-injection injection-locked frequency tripler (ILFT) achieving wide locking range, high harmonic rejection and low power consumption. The injection voltage

drives hard-switched tail transistors of the core oscillator as the first injection path, leveraging high injection strength for a wider locking range. The injection current is coupled to the core oscillator through an injection-current-boosting transformer in another injection path, which isolates the fundamental and the second-harmonic signals to improve the harmonic rejection property. An injection-locked buffer is cascaded to improve the output power flatness and further reject undesired harmonics. Fabricated in 65-nm CMOS process, the ILFT operates from 17.4 to 26.4 GHz with 41.1% locking range. Above 40-dBc harmonic rejection ratio within a 17.4 to 24 GHz bandwidth is achieved, and the power consumption of ILFT core is only 3.2 mW.

RMo3B-4 14:30

A 278–348GHz 6th Harmonic Injection Locking Frequency Multiplier Based on 3rd Harmonic Injection Locking Oscillator in 130nm SiGe Process

Zheng Yan, Jixin Chen, Zhe Chen, Zekun Li, Rui Zhang, Rui Zhou, Peigen Zhou, Wei Hong; Southeast University, China

Abstract: This paper presents a 3rd ILO and a 6th ILFM fabricated in 130-nm SiGe BiCMOS technology. A hybrid-Colpitts model has been proposed to improve the conventional model of the Colpitts oscillator above 100 GHz. The 3rd ILO can be locked from 285 GHz to 345 GHz and the 6th ILFM can be locked from 278 GHz to 348 GHz. The maximum output power of the 3rd ILO is 1.1 dBm at 285 GHz with a peak DC-RF efficiency of 1.92% and the maximum output power of the 6th ILFM is 1.33 dBm at 288 GHz with a peak DC-RF efficiency of 1.5%. The 3-dB BW of the 6th ILFM is from 278 to 333 GHz. To the best knowledge of the authors, the measured locking range of 70GHz (22.3%) and the 3-dB BW of 55 GHz (18%) are the widest for the reported injection locking signal sources above 100 GHz.

RMo3B-5 14:50

A 192–229GHz Frequency Tripler with 4.4dBm Output Power Using Slotline-Based Drain Harmonic Shaping Technique in 40nm CMOS

Yifan Ding, Yizhu Shen, Zhen Lin, Zhenghuan Wei, Yun Qian, Sanming Hu; Southeast University, China

Abstract: A sub-terahertz frequency tripler using slotline-based drain harmonic shaping technique is presented in this work. The drain harmonic shaping technique optimizes harmonic utilization. It shapes the drain waveform by strengthening the nonlinearity at the drain and weakening the nonlinearity at source, thus improving the third harmonic output power. Instead of using center-tapped transformer, the excellent common-mode rejection of slotline is used to realize independent odd- and even-order harmonic tuning. A compact slotline-based output network is designed for simultaneous power combining and harmonic shaping. The proposed frequency tripler is implemented in 40nm bulk CMOS, achieves a saturate output power (P_{sat}) of 4.4 dBm and a 3-dB bandwidth from 192 to 229 GHz, while featuring a compact core area of 0.09 mm². To the best of our knowledge, the proposed tripler achieves the highest P_{sat} among similar CMOS triplers and is comparable to doublers.

Monday, 17 June 2024 13:30–15:10 Room 152AB

Session RMo3C: Wideband Reconfigurable Beamforming Arrays Chair: Emanuel Cohen, Technion, Israel

Co-Chair: Hao Gao, Technische Universiteit Eindhoven, The Netherlands

RMo3C-1 13:30

A 16-Channel W-Band Phased-Array Receiver with a 8-Bit Octant Selector and Reflection-Type Phase Shifter of $0.23^{\circ}/0.21$ -dB RMS Phase and Gain Error for ±30° Scanning Angle

Xianhu Luo¹, Yunbo Rao¹, Xu Cheng¹, Binbin Cheng¹, Hao Yang¹, Renai Chen¹, Yang Yu¹, Jiangan Han¹, Changxuan Han², Liang Zhang¹, Yang Tang¹, Xianjin Deng¹, Hao Gao³; ¹CAEP, China, ²UESTC, China, ³Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper introduces a W-band 16-channel phased array receiver featuring an 8-bit phase shifter and 3-bit VGA, designed for a $\pm 30^{\circ}$ scanning angle within the 92–96 GHz frequency range. To overcome gain limitations for precise phase control, a combination of an octant selector and a reflection-type phase shifter is proposed. Additionally, a VGA-PS-VGA sequence is suggested to address tuning step limitations for accurate gain control. With these methods, each channel achieves a 360° phase shift with a 1.4° per step and 4.8 dB gain tuning with 0.8 dB per step. The rms phase error is 0.23°, and the rms gain error is 0.21 dB. At 94 GHz, each channel exhibits a noise figure of 6.84 dB and a gain of 13.6 dB. The 16-channel array accomplishes $\pm 30^{\circ}$ scanning within the 92–96 GHz frequency range.

RMo3C-2 13:50

A K-Band 4-Element 8-Beam Phased-Array Receiver with Hybrid Vector Interpolation and Impedance-Adapted Multibeam Combining Techniques for Satellite Communications

Hang Lu¹, Nayu Li¹, Huiyan Gao¹, Botao Yang¹, Xuanyu He¹, Shaogang Wang¹, Yiwei Liu¹, Gaopeng Chen¹, Yen-Cheng Kuan², Xiaokang Qi¹, Chunyi Song¹, Qun Jane Gu³, Zhiwei Xu¹; ¹Zhejiang University, China, ²NYCU, Taiwan, ³University of California, Davis, USA

Abstract: This paper presents a K-band four-element eight-beam receiver in 65-nm CMOS for satellite communications. To overcome the high insertion loss of the multibeam combining network, the receiver utilizes a hybrid vector-interpolation-based phase shifting technique. Furthermore, a transmission-line-based impedance tuner is employed to adapt its impedance to enhance the gain at high frequency band, further mitigating the insertion loss. The chip demonstrates a 360° phase-shifting range with 6-bit resolution and a 31.5-dB attenuation range with 0.5-dB step. The measured rms phase and gain errors are 2.9° and 0.41 dB at 19.5 GHz, respectively. Each element achieves a gain of 33 dB, a 3.3–4.2 dB noise figure (NF), and an input-referred 1-dB gain compression point (IP $_{\rm ldB}$) of -45 dBm. This phased-array receiver optimizes the multi-element multi-beam combining network loss and boosts the receiver's performance, which can also benefit other multi-element multi-beam transmitter/receiver designs.

RMo3C-3 14:10

A Frequency Reconfigurable Phased-Array Front-End with Enhanced Image-Rejection and High-Resolution LO Phase Shifter for 5G FR2 n258/n260/ n261 Bands

Qin Chen¹, Jun Lu¹, Xuhao Jiang¹, Xuanxuan Yang¹, Yuchen Liang¹, Yifei Hu¹, Yao Wang¹, Junbo Liu¹, Lin Lu¹, Depeng Cheng², Jing Feng¹, Lei Luo², Long He², Xu Wu¹, Lianming Li¹; ¹Southeast University, China, ²Purple Mountain Laboratories, China

Abstract: This paper presents a frequency reconfigurable phased-array front-end covering 5G FR2 n258/n260/n261 bands in 65-nm CMOS. The front-end adopts a local-oscillator (LO) phase-shifting architecture with a frequency reconfigurable power amplifier (PA) and low noise amplifier (LNA) to realize multi-band operation while relaxing LO phase shifter bandwidth requirements. Benefiting from the proposed passive and active frequency-reconfigurable matching network, an image-rejection ratio (IMRR) of 22.8–43.4 and 37.3–57 dBc can be achieved for TX and RX, respectively. To enhance the phase resolution of the LO vector-summing phase shifter, a layout-flexible transmission line phase shifter as well as PMOS varactors are introduced, resulting in <1° RMS phase error with 7-bit phase control. The measurement results show that the front end can delivers 17.6 and 16.4 dBm saturated output power, 19% and 12.2% peak power added efficiency, and a minimum noise figure of 6.5 and 8.1 dB at 27 and 37 GHz, respectively.

RMo3C-4 14:30

A 10:1 Bandwidth 2.5–25GHz Multi-Standard High-Linearity 6-Bit Phased-Array Receiver Front-End with Quad-Pole I/Q Network and 2.7° RMS Phase Error

Tian Liang, Zhaoxin Hu, Omar Hassan, Gabriel M. Rebeiz; University of California, San Diego, USA **Abstract:** In this paper, a 2.5–25 GHz high-linearity phased-array receiver front-end is proposed and demonstrated. The design is based on a novel phase-shifter (PS) and is implemented using a 4-pole voltage-to-current (V-I) mode quadrature all-pass filter (QAF) and a high linearity common-base (CB) vector modulator (VM). An RMS phase error of 2.7–3.2° over a 10:1 frequency range is achieved without any calibration. An IP1dB of -21 to -28 dBm is measured at a power consumption of 96 mW. The chip is implemented in the Tower Semi 90nm SBC18S5 SiGe BiCMOS process.

RMo3C-5 14:50

A 26.5–35GHz High Linearity VGA with an RMS Phase Error of 0.9°–2.8° Utilizing a Novel Hybrid Coupling Technique in 45RFSOI

Ahmed Afifi, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a high-linearity common-gate VGA with a new gain control technique that uses a hybrid coupling network. This new technique mitigates the drawbacks of the conventional VGAs that results in high phase distortion across gain states. This VGA is implemented in GlobalFoundries 45RFSOI and achieves an RMS phase error of $0.9^{\circ}-2.8^{\circ}$. This low error is maintained across 8.5 GHz of bandwidth. The measured IP_{1dB} and IIP₃ at the maximum gain state is 3.5 dBm and 11.5 dBm, respectively. The NF achieved is also kept low at 4.4–5.2 dB. Application areas are in high linearity beamformers for 5G and mm-wave applications.

Monday, 17 June 2024 15:40–17:20 Room 150AB Session RMo4A: Silicon-Based Power Amplifiers for D-Band and Above

Chair: Alexandre Giry, CEA-Leti, France Co-Chair: Hyun-Chul Park, Samsung, Korea

RMo4A-1 15:40

A D-Band Complex Neutralization Cascode Power Amplifier with A Source-Gate Driven Cascode for Enhanced Bandwidth and Efficiency

Mohamed Eleraky, Hua Wang; ETH Zürich, Switzerland

Abstract: This paper introduces a new cascode Power Amplifier (PA) topology for D-band applications. The utilization of complex neutralization within the common source (CS) stage of the cascode amplifier enhances the amplifier's gain over a broad bandwidth. Moreover, a coupled line coupler is added between the CS and the common gate (CG), allowing the CS to drive the source/ gate nodes of the CG. This efficiently boosts the Psat and linearity of the PA. The stability of the PA is improved by using a series differential inductor between the CS and the coupler. A 3-stage PA with four-way power combining and an integrated Adaptive Bias (AD) is fabricated in GlobalFoundries 45nm. The measurements show a peak PG of 22.33 dB, covering a 3-dB bandwidth of 33.2 GHz (93–126.2 GHz). The corresponding Psat, OP1dB, and PAE with AD OFF/ON are 18.3/17.8 dBm, 12.8 /16.7 dBm, and a PAE of 12.4/11.1%, respectively at 120 GHz.

RMo4A-2 16:00

A D-Band Power Amplifier with Optimized Common-Mode Behaviour Achieving 32Gb/s in 22-nm FD-SOI

Giacomo Venturini, Patrick Reynaert; KU Leuven, Belgium

Abstract: This paper presents a high linearity and high backoff efficiency power amplifier (PA) for D-band (110–170 GHz) communication in 22 nm CMOS FD-SOI technology. Fully differential eightway power combining with extremely low insertion loss is implemented, enhancing the common-mode-rejection-ratio (CMRR), output power and linearity with bypass capacitors placement and sizing. Cascading moderate and deep class AB stages, together with a careful choice of the value of common mode stability resistors, further improves amplifier's linearity. The small-signal gain and bandwidth (BW) are 16 dB and 21GHz. The OP1dB and P_{sat} are 11.4 dBm, 14.6 dBm while maximum PAE and 6dB backoff PAE are 10.6% and 2.8% respectively. The highest demonstrated data-rate is 32 Gb/s, using 16-QAM modulation scheme at an average output power and PAE of 8.1 dBm and 4.2% respectively.

RMo4A-3 16:20 Phased-Array-Compatible Area-Efficient D-Band Power Amplifiers in 45 RF SOI Based on Cascade Stacking

Alfred Davidson, Harish Krishnaswamy; Columbia University, USA

Abstract: This work presents a high-power, area-efficient power amplifier (PA) at 140GHz in 45 RF SOI CMOS. A cascade-stacked architecture that can sustain a larger output voltage swing is utilized to achieve a higher saturated output power ($P_{\rm SNT}$) in an area-efficient manner while allowing the PA to operate at the same standard supply domain. This architecture also allows the DC current of the stacked stages to be decoupled, enabling independent bias optimization for power efficiency. A two-way power-combined PA using this architecture is also implemented to boost the $P_{\rm SNT}$ further. Measured results indicate that the unit PA operating at 1.2V achieves a gain of 32.7dB, $P_{\rm SNT}$ of 16.4dBm, and peak power-added efficiency (PAE) of 12.7% with an active area of 0.098mm², while the two-way power-combined PA achieves a gain of 32.1dB, $P_{\rm SNT}$ of 19.2dBm, and peak PAE of 12.2% with an active area of 0.190mm². The achieved $P_{\rm SNT}$ and ITRS FoM represent the highest among state-of-the-art 140GHz CMOS PAs.

RMo4A-4 16:40

A 15.7-dBm 164–270GHz Power Amplifier with Asymmetric Slotline-Based Series-Parallel Combiner in 130-nm SiGe BiCMOS Technology

Gunwoo Park, Hyunjoon Kim, Sanggeun Jeon; Korea University, Korea

Abstract: This article presents a high-power wideband sub-terahertz power amplifier (PA) in a 130-nm SiGe BiCMOS technology. An asymmetric slotline-based series-parallel combiner (ASSPC) is proposed to enhance the output power and bandwidth. The ASSPC enables low-loss and wideband combining of four differential power cells while facilitating load-pull matching with reduced impedance imbalance between differential transistors. With an aid of the ASSPC, the PA achieves the highest saturated output power (P_{sat}) of 15.7 dBm at 235 GHz and the widest P_{sat} 3-dB bandwidth of 106 GHz among the existing Si-based PAs operating above 200 GHz. It shows a peak gain of 21.2 dB and a wide 5-dB bandwidth of 78 GHz.

Monday, 17 June 2024 15:40–17:20 Room 151AB Session RMo4B:

High Performance RF and mm-Wave CMOS Frequency Synthesis Chair: Andreia Cathelin, STMicroelectronics, France Co-Chair: Xiang Gao, Zhejiang University, China

RMo4B-1 15:40

A 45-fs_{rms}-Jitter, 144-to-162-GHz D-Band Frequency Synthesizer Using a Subsampling PLL and a Harmonic-Boosting Frequency Multiplier

Seohee Jung¹, Jaeho Kim¹, Jooeun Bang¹, Jaehyouk Choi²; ¹KAIST, Korea, ²Seoul National University, Korea

Abstract: This work presents a D-band frequency synthesizer (FS) that can generate an ultralow-jitter output signal over a large frequency-tuning range (FTR). To overcome the structural limitations of conventional sub-THz FSs and concurrently achieve a low jitter and a large FTR, this work was designed with a two-stage architecture in which a 50-GHz-band subsampling PLL with a 3rd-harmonic (HM)-rich class-F VCO at the first stage interoperated with an HM-boosting frequency multiplier (FM) at the second stage. Designed with a 40-nm CMOS, this sub-THz FS exhibited a wide FTR of 11.8% (i.e., 144 to 162 GHz). Due to the high-gain subsampling PD that can suppress in-band phase noise (PN) and the class-F VCO that can achieve low out-of-band PN, the proposed FS achieved the lowest RMS jitter (i.e., $45f_{nms}$). Since the combination of the 3rd-HM-rich class-F VCO and the HM-boosting FM generated a D-band output signal in a power-efficient manner, this work also achieved the best jitter FOM among the state-of-the-art W/D-band FSs with an FTR more than 5%.

RMo4B-2 16:00

A 37.2-fs, -254.6-dB FoM, 47.9-to-56.4GHz PLL Using Tightly Coupled Dual-Core VCO with Implicit 4th Harmonic Extraction Technique

Qixiu Wu, Wei Deng, Mengjiao Xiong, Haikun Jia, Ruichen Wan, Hongzhuo Liu, Baoyong Chi; Tsinghua University, China

Abstract: This paper presents a 47.9-to-56.4 GHz phase-locked loop (PLL) with 37.2-fs jitter and -254.6-dB FoM. The proposed PLL used a tightly-coupled VCO with the implicit 4th harmonic extraction technique, enabling to output both the fundamental and the 4th harmonic frequency simultaneously. The proposed tightly coupled VCO increases the Q factor and reduces the deterioration of capacitive mismatch on phase noise, resulting in improved overall jitter and figure of merit (FOM) of the PLL. The chip prototype is fabricated using a 65 nm CMOS process. The measured PN of the VCO at 10 MHz offset varies from -126.3 dBc/Hz to -129.5 dBc/Hz depending on output frequency. The measured jitter of the PLL using the proposed VCO is 37.2 fs.rms with the FOM of -254.6 dB. The power consumption of the PLL excluding buffers is 25 mW.

RMo4B-3 16:20

A 74GHz-80GHz 1.2GHz/ μ s-Slope 20.9mW FMCW Synthesizer with TDC-Gain-Independent Loop-Bandwidth Employing a TDC-Offset-Free Type-II Digital PLL and a Linearized Hybrid-Tuning DCO

Yi Liu¹, Zixi Jing¹, Zhiyu Liu¹, Chi Chung Yip¹, Zhirui Zong², Howard Cam Luong¹; ¹HKUST, China, ²HKUST(GZ), China

Abstract: A 74–80 GHz self-adapted sawtooth-FMCW frequency synthesizer features a Type-II digital PLL with zero TDC offset independent of chirp rate, TDC-gain-independent loop bandwidth, a 25kHz-resolution glitch-free wideband linear digitally controlled oscillator (DCO) with a dedicated convergence-less digital pre-distortion (DPD). The prototype measures 6-GHz chirp bandwidth with a 1.2GHz/us slope at 77GHz while achieving 0.031% rms chirp error and consuming 20.9mW from 0.9V supply.

RMo4B-4 16:40

A 4.25GHz–8.45GHz 67%-Chirp-Fractional-Bandwidth -121.5dBc/Hz-PN@1MHz 88fs-Jitter FMCW Synthesizer with Bandwidth-Boosting and Phase-Noise-Cancellation Techniques

Yi Liu¹, Zixi Jing¹, Zhiyu Liu¹, Wen Yang¹, Chi Chung Yip¹, Liang Wu², Howard Cam Luong¹, ¹HKUST, China, ²CUHK-Shenzhen, China

Abstract: An FMCW frequency synthesizer features bandwidth boosting, phase-noise cancellation, digital-to-time converter (DTC) dynamic-range reduction, and fast digital controlled oscillator (DCO) look-up table (LUT) initialization scheme. The prototype measures a continuous chirp fractional bandwidth (FBW) of 67.2%, frequency tuning range (FTR) of 111%, PN of -121.5dBc/Hz at 1MHz offset from 7.25GHz, jitter of 88 fs, and 0.06ms LUT convergence time while consuming 31.7 mW, corresponding to FOM_T of -204.7dB.

RMo4B-5 17:00

A 0.2-to-39.2GHz 66.2-fs Jitter and -71.3dBc Spur Sub-Sampling PLL Using DAC-Based Constant Control Voltage Compensator and Quad-Mode 2nd Harmonic Filtering Oscillator

Wen Chen, Yiyang Shu, Xun Luo; UESTC, China

Abstract: In this paper, an ultra-wideband sub-sampling PLL with low jitter and spur is proposed. A digital-to-analog converter based constant control voltage compensator is introduced to achieve constant control voltage of oscillator in PLL. Here, the less control voltage variation leads to short charge/discharge time of charge pump, which obtains fast frequency hopping. To improve the inband phase noise and spur performances, the constant control voltage is optimized in the linear range of oscillator and the current matching range of charge pump. Besides, the mm-wave quadmode 2nd harmonic filtering oscillator is integrated in the PLL to achieve the low out-of-band phase noise within a wide frequency range. The tail resonator is injected in four times of common-mode current, which enhances the 2nd harmonic shaping. The proposed PLL is fabricated in a 40-nm CMOS technology. Measurements exhibit an output frequency range from 0.2 to 39.2GHz. The PLL achieves $66.2f_{\rm sms}$ jitter and -71.3dBc reference spur. The typical power consumption is from 21.5 to 30.8mW. The PLL occupies a core area of 0.4mm².

Monday, 17 June 2024 15:40–17:20 Room 152AB Session RMo4C: Wireline and Localization Systems Chair: Ahmed Elkholy, Broadcom, USA Co-Chair: Sajjad Moazeni, University of Washington, USA

RMo4C-1 15:40

Transimpedance Amplifiers with 95GHz Transimpedance Bandwidth and 1.5% THD for 800G Coherent Optical Communications

Mir H. Mahmud¹, Hasan Al-Rubaye², Gabriel M. Rebeiz¹; ¹University of California, San Diego, USA, ²Broadcom, USA

Abstract: In this work, a linearity enhancement technique is proposed for the output drivers in transimpedance amplifiers (TIA) used in coherent optical receivers. Analysis shows that a pseudodifferential driver has better linearity than the commonly used fully differential driver. This is verified with simulations and measurements. A 3-stage TIA (TIA3S) and a 4-stage TIA (TIA4S) are designed using this technique and fabricated in the GlobalFoundries 9HP+ 90-nm SiGe BiCMOS process. The TIAs achieve 1.50% and 1.59% total harmonic distortion, (THD), at 1 Vppd with >67 GHz and 95 GHz transimpedance bandwidth while consuming 190 mW and 260 mW. The application areas are in 800 Gbps coherent optical communication links.

RMo4C-2 16:00

A 4–26Gbaud Configurable Multi-Mode Non-Uniform EOM with Improved Twin PI for High-Speed Wireline Communication Achieving 3- μ s EW/EH Evaluation and 0.99-R² Accuracy

Shubin Liu, Zhicheng Dong, Menghao Wang, Xiaoteng Zhao, Chenxi Han, Xianting Su, Zhangming Zhu; Xidian University, China

Abstract: This paper presents a configurable multi-mode eye-opening monitor (EOM) with nonuniform sampling and quantization for on-chip high-speed link built-in-self-test (BIST). The EOM can operate in three modes, enabling it to not only capture the colored eye diagram but also rapidly outline its contour, eye height (EH), and eye width (EW). In the non-uniform-scanning mode (NSM), the EH and EW are swiftly measured using an optimization algorithm to adjust the control codes of a 7-bit twin phase interpolator (PI) and a 6-bit R-2R digital-to-analog converter (DAC). In the fast-multi-sampling mode (FMSM), the reduced number of sampled error bits in each pixel facilitates a prompt generation of the eye contour. The EOM can also reconstruct the eye diagram in the multi-sampling mode (MSM) by analyzing the probability density function (PDF) of a 128×63 pixel array. Fabricated in 28-nm CMOS technology, the EOM can operate in 4–26 Gbaud within 0.005-mm² area. At 26 Gbaud, it consumes 14.55 mW with 0.99-R² accuracy and takes up 933 µs in the MSM, 597 µs in the FMSM, and ~3 µs in the NSM, respectively.

RMo4C-3 16:20

A 10ns Delay Range 1.5GHz BW True-Time-Delay Array-Based Passive-Active Signal Combiner with Negative-Cap Stabilized RAMP for Fast Precise Localization

Qiuyan Xu¹, Chung-Ching Lin¹, Aditya Wadaskar², Huan Hu¹, Danijela Cabric², Subhanshu Gupta¹; ¹Washington State University, USA, ²University of California, Los Angeles, USA

Abstract: Maximizing gain in beamforming arrays for emerging communications-on-the-move applications is key in highly resilient networks. Recent studies have demonstrated the rainbow beamtraining method as an effective solution for spatio-spectral mapping in analog/hybrid arrays but require large delay-bandwidth products. In this work, a proof-of-concept 2-channel 1.5GHz bandwidth 10ns maximum delay spatial signal processor is proposed. The angle-of-arrival estimation error is significantly reduced to $\pm 1.5^{\circ}$ compared to prior implementations with a smaller delay range. Multi-stage buffer-less switched-capacitor array enables large delay-bandwidth product of 15. A passive-active amplifier-based combination scheme supports the wideband operation minimizing power and distortion. A negative-capacitance compensated ring-amplifier with stabilization is proposed as part of the wideband signal combiner. The 2-channel system consumes 37.3mW/ channel and 0.45mm² in 65mm CMOS.

RMo4C-4 16:40

An Electro-Optical Synthesizer to Generate Random Chirp Rates for Secure FMCW LiDAR Applications

Marziyeh Rezaei, Liban Hussein, Alana Dee, Sajjad Moazeni; University of Washington, USA **Abstract:** This paper presents an electro-optical (EO) Synthesizer to generate frequency-modulated continuous wave (FMCW) signals with randomly changing chirp rates per frame using an on-chip SRAM-based physically unclonable function (PUF) block in 180nm RF CMOS. This approach is essential to secure FMCW light detection and ranging (LiDAR) against spoofing attacks. The architecture builds on an electro-optical phase-locked loop (EO PLL) integrated with a divide-by-2/3 fractional divider driven by an on-chip random key generator using PUF via a 2nd-order delta-sigma modulator (DSM). The synthesizer provides four various programmable chirp rates ranging from 8.5GHz/ms to 12GHz/ms with a chirp period of 600µs. The EO Synthesizer improves the SFDR of the coherent receiver by ~10dB compared to the open-loop modulation of the laser for FMCW ranging. The proposed method achieves 8× faster transition time compared with SSB-based EO PLLs. The proposed EO Synthesizer can be used for other applications in RF-photonics as well.

Tuesday, 18 June 2024 08:00–09:40 Room 151AB Session RTu1B: RF and Mixed-Signal Circuits for Cryogenic and High-Radiation Environments Chair: Alexandre Siligaris, CEA-Leti, France Co-Chair: Travis M. Forbes, Sandia National Laboratories, USA

RTu1B-1 08:00

Broadband Noise Characterization of SiGe HBTs Down to 4K

Jad Benserhir, Yating Zou, Yatao Peng, Hung Chi Han, Edoardo Charbon; EPFL, Switzerland Abstract: This work presents a comprehensive noise characterization of advanced Si/SiGe:C Heterojunction Bipolar Transistors (HBTs) associated with a 0.13 µm BiCMOS technology. The study was carried out over a broad temperature spectrum (293 to 4 K) and a frequency range (10 kHz to 12 GHz). The noise characteristics of SiGe HBTs are inspected as functions of bias, frequency, and temperature; this is, to the best of our knowledge, the first study to cover these broad temperature and frequency ranges simultaneously. Through meticulous examination, we identify a substantial increase in the flicker noise coefficient K_r, by a factor of 5.5 from 5.52×10^{-10} at 293 K to 3×10^{-9} at 4K. Furthermore, there is an increase in corner frequency for a constant collector current density J when the temperature is reduced to 4 K. Furthermore, to consider the enhancement of the high-frequency parameters (f_r and f_{max}) reaching 500 GHz, related to this technology, we examined the ratio f/f_r , which connects the Low Frequency Noise (LFN) and the transistor speed. At 4 K, this ratio shows a minimum of 2×10⁻⁹ at 2mA/µm², which outperforms other advanced CMOS nodes. By addressing the modeling of HBTs that are the core active components of circuits used with quantum devices and sensors operating at deep cryogenic temperatures, we believe that this study will be beneficial to designers of classical-quantum interfaces in several emerging applications.

RTu1B-2 08:20

A Fully Integrated Three-Channel Cryogenic Microwave SoC for Qubit State Control in ⁹Be⁺ Trapped-Ion Quantum Computer Operating at 4K

P. Toth¹, P.S. Eugine¹, A. Meyer¹, K. Yamashita², S. Halama³, M. Duwe³, H. Ishikuro², C. Ospelkaus³, Vadim Issakov¹; ¹Technische Universität Braunschweig, Germany, ²Keio University, Japan, ³Leibniz Universität Hannover, Germany

Abstract: This paper presents a fully integrated System-on-Chip operating from 295 K down to 4 K, capable of generating 0.7 GHz to 1.5 GHz microwave signals for ${}^{9}\text{Be}^{+}$ trapped-ion quantum computer realizations. The proposed design comprises a three-channel waveform generator with integrated 48 kbit memory to generate arbitrary envelope-modulated control signals while consuming only 94 mW, which in the targeted system results in 1.9 mW/qubit. The IC is capable of driving multiple electrodes as required for all gate operations. The chip was fabricated in a 0.13µm SiGe BiCMOS technology. To the best of the authors' knowledge, this is the first reported integrated SoC solution for qubit state control in a trapped-ion quantum computer.

RTu1B-3 08:40 A Switchless Dual-Core Triple-Mode VCO Achieving 7.1-to-15.7GHz Frequency Tuning Range and 202.1dBc/Hz Peak FoM at 3.7 Kelvin

Yue Wu, Yatao Peng, Benhao Huo, Jun Yin, Rui P. Martins, Pui-In Mak; University of Macau, China **Abstract:** We reported a dual-core triple-mode voltage-controlled oscillator (VCO) to adapt to the low power consumption and large frequency tuning range (FTR) of the signal source in quantum interface systems. We proposed using only magnetic and inductive tuning elements for resonance splitting to construct the VCO's triple-mode LC tank. This avoids the FTR sacrifice when using a conventional capacitive tuning element to build the multi-mode tank. To reduce the power consumption of the negative trans-conductance ($-G_M$) cells in the multicore multi-mode VCO, we proposed a structure that provides a triple oscillating mode with only two $-G_M$ cores. In addition, to overcome the deterioration of phase noise (PN) due to the switch-on resistances, we introduced a switching $-G_M$ technique for mode selection without using the MOSFET switches. The wideband VCO was specifically designed for cryogenic operation, utilizing a 28 nm CMOS technology. The measured results demonstrate an FTR of 7.1–15.7 GHz (75.4%) and a peak figure-of-merit (FoM) of 202.1 dBc/Hz at 3.7 Kelvin.

RTu1B-4 09:00

A 46.7-dB Gain 9.3-K Noise Temperature 5.8-mW Two-Fold Current Reuse Dual Noise-Canceling LNA in 28-nm CMOS for Qubit Readout

Mahesh Kumar Chaubey¹, Yin-Cheng Chang², Po-Chang Wu², Hann-Huei Tsai², Shawn S.H. Hsu¹; ¹National Tsing Hua University, Taiwan, ²NARLabs-TSRI, Taiwan

Abstract: This paper presents a novel cryogenic high gain, low power two-fold current-reuse with dual noise-canceling (NC) low-noise amplifier (LNA) in 28-nm CMOS. The proposed LNA consists of the current reuse cascode inverting input stage with shunt-resistive feedback and self-body bias (SBB) to mitigate the variation of V_{th} and r_{out} under cryogenic temperatures. A common-source (CS) main amplifier is used, followed by a current reuse dual NC stage with LC networks to form an equivalent parallel CS configuration, which can suppress the noise of both the main amplifier and auxiliary amplifier. At 4 K, the LNA attains a measured peak gain (S_{21}) of 46.7 dB with a 3-dB bandwidth of 0.01–2.2 GHz and minimum NF of 0.136 dB (9.3 K noise temperature) at 0.6 GHz under power dissipation of only 5.8 mW. The circuit occupies a core area of 0.17 mm². The proposed work achieves FoM among the best in the sub-3 GHz cryogenic CMOS LNA reported to date.

RTu1B-5 09:20

A Study of Total Dose Radiation Effects in Ka-Band Fractional-N PLLs in 45nm SiGe BiCMOS

David Dolt¹, Lauren Pelan², Samantha Mcdonnell², Shane Smith³, Trevor Dean², David Reents¹, Will Gouty², Tony Quach², Waleed Khalil³, Samuel Palermo¹; ¹Texas A&M University, USA, ²AFRL, USA, ³Ohio State University, USA

Abstract: Two fractional-N phase locked loops (PLLs) with high-performance CMOS and bipolar VCO permutations were designed in a 45nm SiGe BiCMOS process to study their sensitivity to total ionizing dose (TID) radiation effects. Special attention is paid to the total dose degradation mechanisms in the VCO, charge pump, and divider design, with wafer level device characterization carried out to support system level radiation measurements. The PLL designs operate with a tuning range of 21.53% from 29GHz to 36GHz, while achieving a jitter FOM of -228dB in fractional-N mode. Furthermore, the PLLs were tested using a TRIGA reactor to verify post-irradiation phase noise performance up to a total dose of 350krad.

Tuesday, 18 June 2024 08:00–09:40 Room 152AB

Session RTu1C: Digital Power Amplifier and Transmitter Systems Chair: Xun Luo, UESTC, China Co-Chair: Zhiming Deng, MediaTek, USA

RTu1C-1 08:00 A Watt Level, 5–7GHz All Digital Polar TX Based on 3.3V Switched Capacitor Digital PA in 16nm Fin-FET for Wi-Fi7 Applications

Naor R. Shay¹, Elad Solomon², Limor Zohar², Assaf Ben-Bassat², Eran Socher¹, Ofir Degani¹; ¹Tel Aviv University, Israel, ²Intel, Israel

Abstract: This work presents a fully integrated 5-7GHz all digital polar transmitter (DPTX) capable of supporting 320M/4096-QAM (MCS13) OFMD modulation for WiFi 7 applications in 16-nm Fin-FET CMOS technology. The DPTX is based on a novel transistor stacking with capacitive feedback topology, allowing a switch capacitor digital power amplifier (SC-DPA) to work directly from 3.3V supply. The DPA demonstrates a maximum power (Pmax)/power efficiency (PE) of 30.15dBm/34.7% at 5.2GHz. An error vector magnitude (EVM)/power consumption of -38dB/830mW is measured at 6.1GHz and 9-dB backoff (dBBO) from Pmax, thus meeting MCS13 4096-QAM OFDM Wi-Fi7 requirement.

RTu1C-2 08:20

A SAW-Less 3F_{L0}-Suppression RF Transmitter with a Transformer-Based N-Path Switched-Capacitor Modulator Achieving -157.6dBc/Hz Output Noise and -61dBc CIM₃

Gengzhen Qi¹, Haonan Guo¹, Pui-In Mak², Yunchu Li¹; ¹Sun Yat-sen University, China, ²University of Macau, China

Abstract: This paper reports a SAW-less RF transmitter with a passive-intensive I/Q modulator. Specifically, without the noisy and nonlinear transconductor (g_m), our proposed linear I/Q modulator features a transformer-based N-path switched-capacitor (SC) topology to enable high-Q bandpass filtering at a flexible RF, rejecting the out-of-band (OB) noises in baseband (BB) and the modulator. The intrinsic lowpass characteristic of the transformer also reduces the harmonic terms at $3 \times f_{10}$ at the output of the modulator, thereby effectively suppressing CIM₃. For the power amplifier (PA) driver, it is aided by a paralleled- g_m linearizer to improve the performance. Prototyped in a 65nm CMOS process, our transmitter manifests a consistently low OB noise (\leq -157dBc/Hz) for 2 to 3GHz. Under a 2.3dBm output power, the transmitter shows a high transmitter efficiency (5.1%) and a high linearity (CIM3 <-60dBc and ACLR1 <-46dBc). The power consumption is 32.5mW at 2.5GHz, and the active area is 0.21mm².

RTu1C-3 08:40

A 32.3dBm Quadrature Complex Domain Doherty Power Amplifier Based on Switched Constant-Current and Symmetrical Transformer Achieving 21.6% Average Power-Added Efficiency

Tao Wang, Lingyun Shi, Di Hua, Peng Cao, Jiawei Xu, Zhiliang Hong; Fudan University, China **Abstract:** This paper presents a power-efficient quadrature switched constant-current power amplifier (PA) based on IQ sharing. This PA, combining the complex domain Doherty and a symmetrical transformer that absorbs a $\lambda/4$ impedance converter, can generate four power efficiency peaks to significantly improve the power-added efficiency (PAE) at the PA's power back-offs (PBOs). Fabricated in a 28 nm CMOS process, the PA achieves a peak output power (P_{out}) of 32.3 dBm and a peak PAE of 37% at a 2 GHz carrier. The PAEs at 3-, 6-, and 9-dB PBOs are 35.7%, 25.1%, and 23.7%, respectively. When testing an LTE 20-MHz 256-QAM signal with 5.8-dB PAPR, this PA achieves an average P_{out} of 26.5 dBm, an average PAE of 21.6%, -31.2 dB EVM, and -32.5/-32.3 dBc ACLR.

RTu1C-4 09:00

A 5G FR2 n260/n259 Phased-Array Transmitter Front-End IC in 28-nm CMOS FD-SOI with 3-Stack Power Amplifier Employing OPA-Based Bias Scheme and Cross-Tied Inductor Topology

Jongwon Yun¹, Hongkie Lim¹, Jaeyeon Jeong¹, Iljin Lee¹, Doyoon Kim¹, Kyunghwan Kim¹, Han-Woong Choi¹, Geonho Park¹, Goeun Baek¹, Eun-Taek Sung¹, Ajaypat Jain², Foad A. Malekzadeh², Venumadhav Bhagavatula², Ivan S.-C. Lu², Sangwon Son², Hyun-Chul Park¹, Joonhoi Hur¹, Sangmin Yoo¹; ¹Samsung, Korea, ²Samsung, USA

Abstract: This paper presents a 16-element 5G FR2 n260/n259 phased-array transmitter frontend integrated circuit implemented in a 28-nm CMOS fully depleted silicon on insulator device technology. A differential 3-stack configuration, an operational amplifier-based bias scheme, and a cross-tied inductor topology are employed in the power amplifier for high output power, stability, and reliability. The developed transmitter achieves output power of >14.2/9.4 dBm/element at an errorvector-magnitude of 5.6% (DFT-s OFDM 64QAM) with transmitter efficiency of >10/4.8%/element for n260/n259 bands.

RTu1C-5 09:20

A 0.48mm² Sub-2.4GHz Transceiver with Reused Matching Network and Duty-Cycle Controlled Class-E PA for Medical Band

Heng Huang¹, Xiliang Liu², Zijian Tang³, Wei Song³, Yuan Ma³, Yuwei Zhang², Xiaoyan Ma², Milin Zhang³, Jintao Wang³, Kai Lu¹, Zhihua Wang³, Guolin Li³; ¹NUDT, China, ²Beijing Ningju Technology, China, ³Tsinghua University, China

Abstract: This paper presents a compact low-power sub-2.4GHz transceiver (TRX) for medical band, consisting of an all-digital phase-locked loop (ADPLL) based transmitter (TX) and a single-path phase tracking receiver (RX). A single-ended duty-cycle controlled class-E power amplifier (PA) with an on-chip harmonic distortion suppression strategy is proposed. The matching network is reused for gate-boosting and noise-canceling in a single-ended low-noise transconductance amplifier (LNTA). This proposed structure needs only two on-chip transformers/inductors as matching networks reducing the silicon area, and embed transmitter/receiver (T/R) switch function without insertion loss. The design of an 8-port transformer makes the layout more compact. The prototype was fabricated in 40-nm CMOS technology, occupying an active silicon area of 0.48 mm². Experimental results show a 2.27mW power consumption with -10dBm output power in TX, The measured 2nd and 3rd harmonic distortion are -52.36dBm and -50.67dBm, respectively. The RX achieves a sensitivity of -93dBm while consuming 2.25mW.

Tuesday, 18 June 2024 10:10–11:50 Room 151AB

Session RTu2B: Silicon Wireless Systems in the D-Band and Beyond Chair: Minoru Fujishima, Hiroshima University, Japan Co-Chair: Shahriar Shahramian, Nokia Bell Labs, USA

RTu2B-1 10:10

A 210-to-250GHz Sliding-IF Frequency-Interleaved Transceiver with On-Chip Bow-Tie Antenna and 4th-Order FIR-Embedded Digital Modulator

Linjun Gu, Wei Deng, Junlong Gong, Taikun Ma, Haikun Jia, Qixiu Wu, Jiamin Xue, Dongfang Li, Hongzhuo Liu, Yaqian Sun, Baoyong Chi; Tsinghua University, China

Abstract: This paper introduces a THz sliding-IF frequency-interleaved transceiver with an onchip bow-tie antenna and a 4th-order FIR-embedded digital modulator. As for the transmitter (TX), two independent baseband signals are dual-up converted to the THz band and then interleaved. As for the receiver (RX), the interleaved signals are dual-down converted and separated back to each independent baseband signal. The quadrature LO signal generator with one input port is realized for both IF and RF conversion. The 4th-order FIR-embedded direct-modulation digital modulator using a 1-bit D/A interface is introduced for performing the quadrature up-conversion and modulation. The ultra-wide-band on-chip bow-tie antenna provides a solution for interconnections between chips and antennas. The three-line balun based LNA and PA are proposed for achieving wideband performance in the THz band. While limited by the measurement equipment, this work still demonstrates 16 Gb/s data transmission through two independent 2Gbaud data streams in 16-QAM modulation.

RTu2B-2 10:30

A 2×40Gb/s Ultra-Wideband 131–173GHz Dual Receiver for Point-to-Point Communication Systems with NF of 5.7dB in RFSOI

Ahmed Afifi, Amr Ahmed, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents an ultra-wideband 131–173 GHz dual-channel receiver with a measured gain of 22–25 dB, a measured NF of 5.7–8.4 dB, and an IP_{1dB} of -30 \pm 2 dBm, implemented in Global Foundries 45RFSOI technology. The chip contains a ×6 LO multiplier network and high-power buffers to drive high-linearity active mixers. An IF of 26–34 GHz is chosen for high image rejection. The chip achieves a data rate of 2×40 Gb/s for a channel bandwidth of 8 GHz using 32QAM modulation. Application areas are for point-to-point (backhaul) communication systems employing V and H polarization for 2×2 polarization MIMO systems.

RTu2B-3 10:50

A 112.64-Gb/s CMOS D-Band Channel-Aggregation RX System-in-Package

Abdelaziz Hamani, Jose Luis Gonzalez-Jimenez, Alexandre Siligaris, Francesco Foglia-Manzillo, Cedric Dehos, Jean-Baptiste David, Nicolas Cassiau, Antonio Clemente; CEA-Leti, France

Abstract: This paper presents an energy-efficient wideband D-band wireless receiver (RX) module based on channel-aggregation. It is composed of a multi-channel receiver integrated circuit (IC) in 45-nm CMOS technology and an in-package antenna fabricated using a low-cost multi-layer printed circuit board (PCB). The receiver comprises four down-conversion chains with dedicated millimeter-wave local oscillator (mmW LO) generators and operates over contiguous sub-bands around 139.32 GHz. A 34-GHz bandwidth signals composed of four sub-bands is received where each sub-band, containing at its turn several base-band channels, is down-converted separately by the multi-channel receiver IC. Overall, the presented wireless system demonstrates a data rate of 112.64 Gb/s by receiving and demodulating a signal composed of 16×2.16 GHz channels from 122.04 to 156.6 GHz using 16-QAM scheme at a maximum distance of 2.5 m from a commercial transmitter. The chip consumes 710 mW and occupies an area of 8.6 mm². The energy efficiency is 6.3 pJ/bit, including the multiple LOs on-chip generation circuitry.

RTu2B-4 11:10

A D-Band Scalable 128-Channel Dual-Polarized Receive Phased-Array with On-Chip Down Converters for 2×2 MIMO Achieving 2×42Gbps

Minjae Jung, Linjie Li, Amr Ahmed, Omar Hassan, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper demonstrates a scalable dual-polarized receive (RX) phased array at D-band (132–142 GHz) with on-chip down converters. The wafer-scale beamformer chip is composed of 128 RX channels for an 8×8 dual-polarized array. RF beamforming is employed with 4-bit phase and gain controls on every element, and on-chip dual down-converters are used for an intermediate-frequency (IF) interface at 9–14 GHz. Also, a ×6 local-oscillator (LO) multiplier chain is used with an input at 20–23 GHz for both channels. Two 64:1 Wilkinson combiners are employed for the RF distribution network with signal amplification within the combining network. The 8×8 dual-polarization chip is fabricated in the GlobalFoundries CMOS 45RFSOI process and occupies an overall area of 9.7×9.6 mm². To construct the phased array, the chip is flipped on a low loss organic interposer (RF PCB) containing the RF transitions, LO, and IF distribution networks, and which feeds an 8×8 dual-polarized microstrip antenna array with a spacing of $0.57\lambda \times 0.57\lambda$ (at 140 GHz) in azimuth and elevation planes. The array scans to $\pm 45^{\circ}$ in all planes for both polarizations, and the measured response supports 64 QAM operation with 2×42 Gb/s links. Application areas are in D-band dual-polarized 2×2 MIMO communication links and phased arrays.

Tuesday, 18 June 2024 10:10-11:50 Room 152AB

Session RTu2C: Power Amplifiers for Satellite Applications Chair: Tolga Dinc, Texas Instruments, USA Co-Chair: Aritra Banerjee, University of Illinois at Chicago, USA

RTu2C-1 10:10

An Efficient, High Power Q-Band SiGe HBT Power Amplifier with a Compact Four-Way Wilkinson Power Combiner Balun for Emerging Very Low-Earth-Orbit SATCOM

Hanjung Lee, Insu Han, Jaehyeon Hwang, Inchan Ju; Ajou University, Korea

Abstract: This work presents an energy-efficient, high power Q-band SiGe HBT cascode power amplifier (PA). A novel four-way Wilkinson power combiner balun (WPCB), realized by two coupled line impedance inverting baluns, is proposed not only to simplify signal routing for compact size, but also to obtain efficient power combining with an excellent signal balance. A prototype Q-band PA attains measured peak P_{out} , peak PAE, and power gain of 24.0 dBm, 35.3%, and 23.0 dB at 43.0 GHz, respectively, the highest power density among any Q-band Si-based PAs. Its 1 dB P_{out} bandwidth (BW) ranges from 37.0 to 43.0 GHz, covering downlink of Very Low Earth orbit (VLEO) satellite communication (SATCOM). The PA delivers P_{avg} of 18.1 dBm with PAE_{avg} of 21.0% at 250MHz symbol rate DVB-S2X 64 APSK modulation.

RTu2C-2 10:30

A Compact, Highly Linear Ku-Band SiGe HBT Power Amplifier Using Shared Single Center-Tap Four-Way Output Transformer Balun for Emerging Low Earth Orbit SATCOM Phased-Array Transmitter

Byeongcheol Yoon¹, Insu Han², Junghyun Kim¹, Inchan Ju²; ¹Hanyang University, Korea, ²Ajou University, Korea

Abstract: This paper presents a compact, highly linear Ku-band SiGe HBT PA for Low Earth orbit (LEO) satellite communication (SATCOM). A four-way output transformer (TF) balun with a shared single center-tap (SSCT) is proposed not only for simplifying signal routing for compact chip size, but also obtaining high power combining efficiency. A prototype Ku-band SiGe PA, which merely occupies a core area of 0.21 mm², attains measured peak output power (P_{OUT}) and power added efficiency (PAE) of 24.4 dBm and 32.1% at 11.7 GHz, respectively, with the highest power density of 1311.5 mW/mm². The PA also delivers average P_{OUT} (P_{avg}) of 18.6/16.6 dBm with average PAE (PAE_{avc}) of 16.0/12.6% at 250 MHz symbol rate DVB-S2X 64/256 APSK modulation.

RTu2C-3 10:50

An Efficient Ku-Band Two-Way Vertical-Like Power-Combining Power Amplifier Using Merged Inter-Stage Transformers Achieving 23–23.4dBm Psat and 45.2–46.6% Peak PAE in 65nm CMOS

Joon-Hyung Kim¹, Jeong-Taek Lim¹, Jae-Eun Lee¹, Jae-Hyeok Song¹, Jeong-Taek Son¹, Min-Seok Baek¹, Eun-Gyu Lee¹, Sunkyu Choi¹, Han-Woong Choi², Seong-Mo Moon³, Dongpil Chang³, Choul-Young Kim¹; ¹Chungnam National University, Korea, ²Samsung, Korea, ³ETRI, Korea

Abstract: We propose a novel power combining PA architecture that cleverly utilizes metal stacks to achieve both high output power and efficiency while maintaining a compact chip size in CMOS. Through the adoption of a two-way vertical-like power combining PA architecture featuring the merged inter-stage transformers, a PA with high efficiency and an area reduction of approximately 50% (about the size of a single PA) can be obtained. This architecture was implemented using a 65nm bulk CMOS process, and its feasibility was verified through precise measurements. The proposed PA demonstrates a gain of 26–27.3 dB, a P_{sat} of 23–23.4 dBm, peak PAE of 45.2–46.6%, a P_{1dB} of 22.7–22.9 dBm, and PAE_{1dB} of 44.2–45.5% in the 13–15 GHz range. When tested using a 1-CC 64-QAM OFDM signal (PAPR 11.2 dB), the PA achieves an average output power of 16.9–17.7 dBm and an average PAE of 22–24.1% at 13–15 GHz (at -25 dB EVM_{ms}).

RTu2C-4 11:10

A K-Band CMOS Power Amplifier Using an Analog Predistortion Linearizer with 22.1dBm $\rm P_{sat}$ and 0.9° AM-PM Distortion

Junhan Lim¹, Wonseob Lee², Seong-Mo Moon¹, Euijin Oh², Seunghun Wang¹, Dongpil Chang¹, Jinseok Park²; ¹ETRI, Korea, ²Chonnam National University, Korea

Abstract: This paper presents a K-band CMOS power amplifier (PA) using the 65-nm CMOS process. To improve linearity, an analog predistortion linearizer using a cold-FET and a variable inductor is proposed. Unlike conventional cold-FET linearizers, which face limitations in improving amplitude-to-phase (AM-PM) distortion at high output power, the proposed linearizer compensates both AM-PM distortion and amplitude-to-amplitude (AM-AM) distortion of the PA. Especially, the linearizer has a phase-lag characteristic at medium output power and phase-lead characteristic at high output power, which compensates for AM-PM distortion of the PA up to high output power. The implemented PA achieved a peak power-added efficiency (PAE) of 34.4%, saturation output power (P_{sat}) of 22.1 dBm, and P_{1dB} of 19.44 dBm at 27 GHz. Also, AM-PM distortion of only 0.9° was achieved through the proposed linearization technique. Linear output power satisfying error vector magnitudes (EVMs) of -25 dB and -30 dB were measured at 16.5 dBm and 14.9 dBm, respectively.

RTu2C-5 11:30

A 2–18GHz Frequency Reconfigurable Nonuniform Distributed Power Amplifier with 13.3W Average Power and 39% Average Efficiency

Shu Ma, Xinyan Li, Ze Yu, Dexin Shi, Xiaochen Tang, Yong Wang; UESTC, China

Abstract: This paper presents a high-power ultra-wideband nonuniform distributed power amplifier (NDPA) with significantly high power-added-efficiency (PAE). The proposed NDPA is reconfigurable with three operation modes with frequency overlaps inbetween. A π -type reconfigurable transmission-line-feeding (RT) module is proposed to improve the NDPA's bandwidth and PAE. Lower parasitic capacitance and higher SRF brought by the RT module are beneficial for bandwidth expansion. Smaller parasitic resistance reduces power consumption, leading to the improvement of PAE. Moreover, saturated output power (Psat) is further enhanced by the RT module and a proposed reconfigurable interstage matching network (RIMN). The RT module provides a better load to approach the optimal load. The RIMN features better power transfer capability, improving Psat and PAE at medium and high frequency bands. This work is fabricated with a 0.15-µm GaN process. Measurements show 39.7-to-42.4 dBm Psat, presenting an impressive 39% average PAE over the entire bandwidth of 2-to-18 GHz.

Tuesday, 18 June 2024 13:30–15:10 Room 151AB

Session RTu3B: Silicon-Based Low-Noise Amplifiers and Mixers Chair: Tong Zhang, Google, USA Co-Chair: Hsieh-Hung Hsieh, TSMC, Taiwan

RTu3B-1 13:30 A 4.4-mW 19–46-GHz Low-Noise Amplifier with Pole-Converging Gain Flattening and Triple-Resonance Input Matching

Jiahan Fu, Changwenquan Song, Yihui Wang, Liang Wu; CUHK-Shenzhen, China

Abstract: A cascode low-noise amplifier (LNA) features wide frequency bandwidth with low power consumption. At the cascode stage, a pole-converging gain flattening technique is employed, simultaneously extending its -3-dB bandwidth and flattening the gain response across the entire frequency range. To substantially expand the frequency bandwidth of the input matching, a transformer-based triple-resonance network is proposed. In addition, the current reuse embedded helps reduce the DC power consumption. Prototyped in a 40-nm CMOS process, the proposed LNA measures a frequency range from 19 to 46 GHz, gain of 12.4 dB with 1.76-dB ripple, noise figure (NF) between 3.4 and 4.6 dB, and IP_{1dB} from -15 to -19.4 dBm. It consumes only 4.4-mW power from a 1-V supply, resulting in a figure of merit (FoM) of 21.6. The core area occupied is 0.096 mm².

RTu3B-2 13:50

A Compact 28/39GHz Dual-Band Concurrent/Band-Switching LNA for 5G Multi-Band Multi-Stream Applications

Depeng Cheng¹, Qin Chen¹, Jing Feng¹, Xin Chen¹, Xujun Ma², Lianming Li¹, ¹Purple Mountain Laboratories, China, ²IP Paris, France

Abstract: This paper presents a 28/39 GHz multi-mode low noise amplifier (LNA) for 5G flexible dual-band beamforming MIMO applications. In the proposed LNA, its input stage leverages a compact three-winding transformer coupling technique to achieve wideband power gain and low noise figure (NF) in both 28/39 GHz bands. With two parallel g_m -boosting reconfigurable common-gate amplifiers, the band-multiplexer block is realized, and the wideband signals could be split into two signal paths independently to support concurrent/band-switching modes. Based on the independent band splitting feature, the LNA output stages could be customized with the g_m -boosting active gain cell and narrow-band passive matching network, achieving both enhanced power gain and out-of-band rejection. Fabricated in a 65-nm CMOS process, the proposed LNA occupies a compact core size of only 0.1 mm². With measurements, the LNA achieves 26.3/25.5 dB peak gain, 3.6/3.8 dB minimum NF, -18.5/-16.4 dBm IIP3 in the 28/39 GHz band-switching mode, and 22.9/23 dB peak gain, 4.97/4.9 dB minimum NF, -14.7/-12.4 dBm IIP₄ in the 28/39 GHz concurrent mode.

RTu3B-3 14:10

A High-Gain D-Band LNA with Compact Gm-Boosting Core Based on Slow-Wave Feedback Achieving 6.1dB NF in 40nm CMOS

Yun Qian, Xinge Huang, Yizhu Shen, Yifan Ding, Zhenghuan Wei, Qunfei Han, Sanming Hu; Southeast University, China

Abstract: This study presents a 3-stage D-band low-noise amplifier (LNA) with novel feedback for wide-angle scannable array. The proposed slow-wave feedback provides the simultaneous broadband matching for noise and input impedance, and significantly enhances gain by parasitic elimination. Each common-source (CS) stage effectively leverages the g_m -boosting core consisting slow-wave feedback for promoting the maximum available gain (G_{ma}) and noise rejection. To demonstrate the feasibility of the proposed circuit configuration, the LNA is implemented in a 40 nm bulk CMOS process. The fabricated LNA achieves decent measured power gain of 18.4 dB, 3-dB bandwidth of 16.5 GHz from 131 to 147.5 GHz and minimum in-band noise figure (NF) of 6.1 dB with 17.1 mW power consumption. The core area of the LNA is 0.057 mm².

RTu3B-4 14:30

A Multi-Band and High-IRR Down-Conversion Mixer for 5G NR FR2 Using Compact Transformer-Based Mutual-Image-Rejection Filter

Haipeng Duan, Qin Chen, Xu Wu, Dongming Wang, Lianming Li, Xiaohu You; Southeast University, China

Abstract: This paper presents a multi-band 5G NR FR2 down-conversion mixer with high mutual image rejection ratio (IRR) and compact area, while relaxing the requirements for local oscillator (LO) bandwidth. To achieve a broadband mutual image rejection within a small area, this paper proposes an on-chip compact transformer-based mutual-image-rejection (MIR) filter with an area of only 0.023 mm², which exhibits the ability to track the pole and zero frequencies simultaneously, and realizes the broadband IRR. Moreover, the MIR filter also serves as the broadband impedance matching network between low noise amplifier (LNA) and down-conversion mixer, avoiding the use of additional matching network. To the best of our knowledge, this is the first on-chip mutual-image-rejection filter in the multi-band 5G NR FR2 system. Fabricated in a 65-nm CMOS process, the proposed multi-band down-conversion mixer achieves a maximum IRR of 70 and 60 dBc in 28- and 39-GHz band operations, respectively.

RTu3B-5 14:50

A Compact Ultra-High-Linearity 7-to-20GHz Passive Mixer Achieving up to 37dBm IIP3 and 25.1dBm IP1dB in 45nm CMOS SOI

Omar Hassan, Amr Ahmed, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents an ultra-high-linearity 7–20 GHz passive mixer demonstrating stateof-the-art linearity performance at a relatively low power consumption. The design adopts multiple techniques like low-impedance operation, series-stacked transistors, and semi-floating switch gates to boost the mixer linearity. Power-efficient stacked LO drivers are used to drive the mixer resulting in improved mixer IIP3 efficiency. The mixer prototype is fabricated in GlobalFoundaries 45nm CMOS SOI technology and has a measured conversion loss of 8–11.7 dB with a 3-dB RF bandwidth of 7–20 GHz. The mixer achieves an input P1dB of 20.3–25.1 dBm and has a measured IIP3 of 25.3–37 dBm at 7–20 GHz while consuming 0.07–0.43 W. To the best of the authors' knowledge, this is the highest linearity performance for a mixer implemented in a scaled CMOS technology. Application areas are wideband receivers for base stations and wideband phased-arrays.

Tuesday, 18 June 2024 13:30–15:10 Room 152AB

Session RTu3C: D-Band and THz Transmitters

Chair: Vadim Issakov, Technische Universität Braunschweig, Germany Co-Chair: Mona M. Hella, Rensselaer Polytechnic Institute, USA

RTu3C-1 13:30

A 360GHz Single-Element Multi-Mode Orbital Angular Momentum Cavity Antenna-Based Transmitter in 90nm SiGe BiCMOS

Wei Sun, Sidharth Thomas, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: This paper introduces a fully integrated multi-mode orbital angular momentum (OAM) transmitter featuring a single-element on-chip antenna. Notably, it represents an on-chip transmitter capable of concurrently operating three orthogonal OAM modes ($|l_{oam}| = 0, 1, 2$). This allows different OAM modes to share a common phase center, facilitating the potential use of passive gain elements such as a lens or a reflector. The transmitter utilizes an oscillator at 120 GHz followed by a PIN diode frequency tripler to generate a 360 GHz signal. Implemented in GlobalFoundries 90 nm BiCMOS process, the radiator achieves a maximum radiated power of -8.1 dBm with 153 mW DC power dissipation, corresponding to a DC-THz efficiency of 0.1%. It also exhibits a wide frequency tuning range of 14.2%. This paper also presents measured OAM amplitude and phase distribution. It introduces a new method for measuring phase distribution without necessitating frequency and phase coherency.

RTu3C-2 13:50 A 300-GHz-Band 40-Gb/s 2D Phased-Array CMOS Transmitter with Near-Half-Wave Antenna Pitch

Kyoya Takano¹, Shun Beppu¹, Hayato Yagi¹, Yoshiki Sugimoto², Kunio Sakakibara², Shinsuke Hara³, Mohamed H. Mubarak³, Akifumi Kasamatsu³, Shunichi Kubo⁴, Kosuke Katayama⁵, Satoshi Tanaka⁶, Takeshi Yoshida⁶, Shuhei Amakawa⁶, Minoru Fujishima⁶, ¹Tokyo University of Science, Japan,

²Nagoya Institute of Technology, Japan, ³NICT, Japan, ⁴THine Electronics, Japan, ⁵Tokuyama KOSEN, Japan, ⁶Hiroshima University, Japan

Abstract: The free-space wavelengths in the 300-GHz band are so short that it is extremely challenging to realize phased arrays with a half-wave antenna pitch, required for preventing grating lobes. This paper presents a CMOS 2D phased-array transmitter (TX) with a near-half-wave antenna pitch. The 3×3 near-half-wave pitch antenna array prototype consists of four main antennas at the corners and five auxiliary antennas. The main antennas are fed directly by a 2×2 array of CMOS TX elements (upconversion mixers), disposed with a near-full-wave pitch. Each of the auxiliary antennas is fed with leaked signals from two or more neighboring TX elements. The superposition of leaked signals gives the right phase for each auxiliary antenna. This interpolated feeding architecture relaxes the area reduction requirement for the arrayed TX elements and still enables near-half-wave phased arrays. The 2D phased-array TX, prototyped using a 40-nm CMOS process, operates in the

frequency range of 263–279 GHz, and the antenna pitch is approximately 0.54 times the wavelength. It achieves a maximum EIRP of -6.9 dBm and a highest data rate of 40 Gb/s with 16QAM over a link distance of 0.05 m. The beam steering range is $\pm 30^{\circ}$ in the E- and H-planes.

RTu3C-3 14:10 A 110-to-170-GHz OOK Transmitter with 40-Gb/s Data Rate and 40-dB On-Off Ratio in 28-nm CMOS

Chun Yang, Dawei Tang, Peigen Zhou, Zhe Chen, Jixin Chen, Wei Hong; Southeast University, China **Abstract:** This paper presents a D-band on-off keying (OOK) transmitter fabricated in 28-nm CMOS process. A current-controlled OOK modulator with always-off cancellation technique is proposed to enhance the data rate and the on-off ratio. The transmitter exhibits an output power exceeding 10 dBm and an on-off ratio of 40 dB. Its 3-dB output power bandwidth is from 110 to 170 GHz, covering the full D band to support a high data rate. Without the assistance of DSP for equalization, the measurements demonstrate an on-wafer data rate up to 40 Gb/s and over-the-air (OTA) data rates of 21 Gb/s and 15 Gb/s at distances of 3 cm and 8 cm respectively with a bit error rate (BER) of less than 10⁻¹².

RTu3C-4 14:30

A CMOS Fully Integrated 120-Gbps RF-64QAM F-Band Transmitter with an On-Chip Antenna for 6G Wireless Communication

Zisong Wang¹, Huan Wang², Youssef O. Hassan¹, Payam Heydari¹; ¹University of California, Irvine, USA, ²Qualcomm, USA

Abstract: This paper presents a single-chip bits-to-antenna transmitter (TX) for >100 Gbps in 45nm CMOS SOI. The construction of the 64QAM constellation is achieved directly in the RF domain by utilizing three QPSK sub-TXs with weighted amplitude. This method significantly reduces the need to address power amplifier nonlinear effects in high-order modulation, thereby creating room for TX enhancements in both bandwidth and output power. To further improve TX performance, multi-step phase alignment strategies, and a local oscillator leakage suppression technique have been incorporated. With 40-GHz RF bandwidth, the RF-64QAM TX prototype is able to achieve a measured data rate of 120 Gbps with 15dBm effective isotropic radiated power (EIRP).

RTu3C-5 14:50

A 56Gb/s Zero-IF D-Band Transmitter for a Beamformer in 22nm FD-SOI

Y. Zhang, K. Vaesen, G. Mangraviti, S. Park, Z. Zong, P. Wambacq, G. Gramegna; imec, Belgium **Abstract:** We present a transmitter (TX) suitable for a beamformer operating between 118GHz and 147GHz. The TX is one antenna path of a 4-way beamforming TRX chip: it supports up to 64QAM modulation (30Gb/s at -25dB EVM) and achieves a data rate of 56Gb/s with a 17dB EVM at an output power P_{OUT} of 3dBm using 16QAM modulation. The zero-IF TX comprises a baseband section, I/Q generation, upconverter, a PA with a P_{SNT} of 11dBm, and a cascade of two frequency triplers for LO generation using an external LO reference. The LO beamforming scheme ensures a phase resolution of 0.1°. A single TX channel draws 232mW from a 0.8V supply and has an area of 1.17×0.3 mm² in a 22nm FD-SOI process.

Tuesday, 18 June 2024 15:40–17:20 Room 151AB Session RTu4B: mm-Wave and Beyond Radars and Imagers Chair: Raja Pullela, MaxLinear, USA Co-Chair: Vito Giannini, UHNDER, USA

RTu4B-1 15:40 A 90–98-GHz FMCW Radar Transceiver Supporting Broadband Modulation in 65nm CMOS

Shengjie Wang¹, Jiangbo Chen¹, Jiabing Liu¹, Quanyong Li¹, Qizhou Yang¹, Xiaopeng Yu¹, Chunyi Song¹, Qun Jane Gu², Zhiwei Xu¹; ¹Zhejiang University, China, ²University of California, Davis, USA Abstract: A 90-98-GHz frequency-modulation-contiguous-wave (FMCW) radar with four transmitters (4TX), four receivers (4RX), a frequency synthesizer and a local oscillator (LO) distribution network is fabricated in 65-nm CMOS. An ultra-wideband mixer without stacked transconductance is proposed to operate across 20-110 GHz. A multi-state cascaded topology using a magnetically coupled resonator (MCR) with two resonant peaks is employed for the low noise amplifier and the power amplifier. An LO distribution network integrates three frequency doublers for frequency octupling from an 11-13 GHz frequency synthesizer, which facilitates broadband modulation. Measurements show the transmitters deliver a maximum output power of 13.2 dBm with 11.9% efficiency and 1.4 dB flatness across 90-99 GHz. The receivers achieve a conversion gain of 63.4 dB and a minimum single-sideband noise figure $\rm NF_{sch}$ of 8.3 dB @3MHz across 88–98 GHz. The measured phase noise is -93.83 dBc/Hz at 1-MHz offset with a 90.4-GHz carrier. The root-meansquare (rms) frequency error is 9.36 MHz (0.12%) for a sawtooth chirp with an 8-GHz chirp-range and a 160-MHz/µs chirp-rate. The radar chip occupies a chip area of 4.5×3.8mm² including TRX front end, synthesizer and baseband, where the power consumptions are 210/78 mW for each TX and RX element, respectively.

RTu4B-2 16:00

A 200-GHz Modulable Transceiver With 35-dB TX ON/OFF Isolation and 16Gb/s Code Rate for MIMO Radar in 130nm SiGe Process

Rui Zhou, Jixin Chen, Siyuan Tang, Zekun Li, Dawei Tang, Peigen Zhou, Feng Xie, Zhe Chen, Wei Hong; Southeast University, China

Abstract: This paper presents a 200-GHz modulable transceiver for multiple-input multiple-output (MIMO) radar applications. The transmitter consists of a \times 6 amplifier multiplier chain, a mode-switchable modulator, an ON/OFF-isolation-enhanced PA, and an on-chip self-filtering folded-dipole antenna. The mode-switchable modulator provides phase and amplitude modulation capabilities, suitable for achieving waveform orthogonality in MIMO radars. PA with ON/OFF isolation enhance technology can provide high switching isolation at the saturated output. To obtain a low noise figure (NF), the receiver consists of a wideband low-noise amplifier and an I/Q mixer. The measurement results show a peak output power of 10.3 dBm at 184 GHz, and a peak EIRP of 12 dBm with a 4-dB

bandwidth from 180 to 232 GHz without lens. The receiver exhibits 24 dB conversion gain and 12 dB single sideband NF. Furthermore, phase and amplitude modulation ability is demonstrated by a Non-Return-to-Zero (NRZ) signal with 35-dB ON/OFF isolation and 16 Gb/s code rate.

RTu4B-3 16:20

An On-Chip Antenna-Coupled Preamplified D-Band to J-Band Total Power Radiometer Chip in 130 nm SiGe BiCMOS Technology

Janusz Grzyb¹, Marcel Andree¹, Holger Rücker², Ullrich Pfeiffer¹; ¹Bergische Universität Wuppertal, Germany, ²IHP, Germany

Abstract: This paper presents a dual-path single-chip total-power radiometer front-end in 130nm SiGe HBT technology ($f_t=f_{max}$ of 470/650 GHz) operating across D- and J-band with a high equivalent noise bandwidth of up to 150GHz and minimum in-band optical NEP of 23 fW/ \sqrt{Hz} . Each path comprises a high gain-bandwidth product 5-stage LNA followed by a broadband power detector and is driven from a separate polarization of the lens-coupled polarization-diversity on-chip slot antenna. The radiometer demonstrates an optical NETD of 0.31K for a standard integration time of 3.125 ms with peak thermal responsivity of 55 μ V/K and low LFN (low-frequency noise) corner near 100 Hz.

RTu4B-4 16:40

An E-Band FMCW Radar Receiver Achieving 38dB Cancellation for Arbitrary-Path Spillover Up to -10dBm and 5.7dB NF in 65nm CMOS

Bolin Chen, Zhirui Zong; HKUST(GZ), China

Abstract: This paper presents an E-band receiver (RX) with spillover cancellation for frequencymodulated continuous-wave (FMCW) radars. To reject spillover from both TX-RX coupling and undesired spatial reflections (such as bumper reflection), a spillover replication method based on frequency-delay translation through a single-sideband (SSB) modulator is introduced. To keep the RX performance immune from strong spillover, we propose an in-LNA isolated voltage-mode canceller. It provides high isolation between the RX signal chain and cancellation path, minimizing noise figure (NF) degradation. Spillover is rejected in the input voltage domain before entering the critical LNA stage and inducing current, thereby preserving the linearity. Prototyped in 65nm CMOS, the RX rejects spillover with offset frequency up to 3.6MHz and power up to -10.4dBm, while exhibiting $5.7 \sim 7.2$ dB NF and -11.4dBm IP_{LdB} across $69 \sim 76.5$ GHz range.

Tuesday, 18 June 2024 15:40-17:20 Room 152AB Session RTu4C:

Circuit Building Blocks in the 100–200GHz Frequency Range

Chair: Teerachot Siriburanon, University College Dublin, Ireland Co-Chair: Rocco Tam, NXP Semiconductors, USA

RTu4C-1 15:40

110–170GHz 25% Duty-Cycle Gilbert-Cell Frequency Doubler with 6.5dBm Peak Output Power in BiCMOS 55nm Technology

Lorenzo Piotto, Guglielmo De Filippi, Andrea Mazzanti; Università di Pavia, Italy

Abstract: Frequency multipliers are key components for signal generation above 100 GHz. Pushpush frequency doublers are popular but suffer from low conversion gain and limited fundamental rejection. Mixers with quadrature inputs offer higher gain and better fundamental suppression but need a bandwidth-limiting 90° phase shifter. This work leverages Gilbert-cells mixers driven by inphase signals but operated at a reduced duty-cycle (δ), allowing to retain the superior conversion gain and fundamental rejection without the 90° phase shifter. A simple low-frequency loop controls δ and gives maximum conversion gain by suppressing the output DC component. The signal driving the mixer switching-quad is generated and routed by a transmission-line network which compensates for the undesirable phase shift introduced by transistors parasitics, critical in the sub-THz band. Realized in SiGe BiCMOS, the circuit proves $P_{out} = 6.5dBm$ at 148GHz with 7.4% power efficiency and 8 dB conversion gain. With -3 dB bandwidth of 125–170 GHz, $P_{out} > 0dBm$ from 110 to 170GHz and a fundamental rejection always above 40 dB, the frequency doubler compares favorably against previous works.

RTu4C-2 16:00

A Low Conversion Loss 120GHz Passive IQ Down-Conversion Subharmonic Mixer with Multiphase LO Distribution in 28nm CMOS

Sarah Koop-Brinkmann¹, Victor Lasserre¹, Michele Caruso², Daniele Dal Maistro², Giovanni Volpato², Christian Ziegler¹, Finn Stapelfeldt¹, Vadim Issakov¹; ¹Technische Universität Braunschweig, Germany, ²Infineon Technologies, Austria

Abstract: This paper presents a passive IQ down-conversion subharmonic mixer (SHM) operating around 120GHz realized in a 28nm CMOS process. The use of a subharmonic mixer enables the local oscillator (LO) signal distribution at a lower frequency, in this case at $f_0/2$ of 60GHz, and hence lower DC power consumption. However, the conversion loss of a passive subharmonic mixer is typically much higher than that of a passive fundamental mixer. In this work we enhance the SHM multiphase concept by a shunt resonant inductance attached between two cascaded mixer cores. This enables the mixer conversion loss reduction concept, reported so far typically only below 30 GHz, to be applied here at frequencies around 120GHz. We achieve a very low voltage conversion loss of 3.8 dB for a single SHM channel, without integrating any amplifiers in the RF or IF path. The multiphase
LO distribution for both I and Q channels dissipates only 39.6mW in total. With the high measured 2LO-RF isolation above 66.8 dB over the entire RF bandwidth of 17GHz, the LO self-mixing is highly suppressed, resulting in a minimized DC-offset voltage.

RTu4C-3 16:20

A 200GHz Wideband and Compact Differential LNA Leveraging an Active Balun Input Stage in 16nm FinFET Technology

Ethan Chou, Nima Baniasadi, Ali Niknejad; University of California, Berkeley, USA

Abstract: This paper presents a wideband and compact 200 GHz differential low-noise amplifier implemented in 16nm FinFET technology. A differential topology is enabled by employing an active balun input stage to avoid the losses of a conventional passive balun and to minimize the overall noise figure, as well as to provide wideband input matching across the signal bandwidth. Dual-peak transformer inter-stage matching networks and stagger-tuning are used in the remaining stages to achieve a wideband gain of 12 dB across a 172–220 GHz 3-dB bandwidth, limited by the measurement setup. The integrated noise figure across this bandwidth is 9.0 dB, with a minimum inband noise figure of 8.3 dB. The amplifier consumes 28 mW and occupies an ultra-compact core area of 0.064 mm². Compared to other CMOS low-noise amplifiers at similar frequencies, a competitive combination of bandwidth, noise figure, power consumption, and area enable the proposed low-noise amplifier to be suitable for use in next-generation high-capacity sub-THz receiver array frontends.

RTu4C-4 16:40 A D-Band Bi-Directional Current-Reuse Common-Gate Amplifier in 45nm RFSOI

Syed Mohammad Ashab Uddin, Liwen Zhong, Wooram Lee; Pennsylvania State University, USA **Abstract:** This paper presents a low-power 140-GHz bi-directional amplifier exploiting the sourcedrain symmetry of CMOS transistors in a common-gate amplifier. The proposed bi-directional amplifier uses symmetric inter-stage matching networks to minimize the use of lossy switches on RF signal paths. The current-reuse technique is applied to share the same supply current between two adjacent stages for low power consumption. As a proof-of-concept implementation, a prototype 140-GHz 3-stage bi-directional amplifier is implemented using a 45nm RFSOI process. The fabricated chip reports a measured peak gain of 14 dB with a 3-dB bandwidth of 21 GHz and only consumes 28.5 mW of DC power. The measured input return loss is higher than 10 dB over a bandwidth > 46 GHz, and the measured average noise figure (NF) over the 3 dB bandwidth is 6.8 dB.

WORKSHOPS

Workshops are offered on Sunday, Monday and Friday at the Walter E. Washington Convention Center. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

Sunday, 16 June 2024

WSB (Half-Day): 08:00–11:50 Highly Reconfigurable Mixed-Signal RF Front-End Approaches for 5G and Beyond

Sponsor: RFIC/IMS

Organizers: Hao Wang, MediaTek Anis Ben Arfi, Analog Devices

Abstract: The pursuit of ubiquitous connectivity and the rapid evolution of wireless communication technologies such as 5G and mm-wave have spurred a growing demand for RF front-end design that can operate across a wide frequency spectrum for various communication standards. However, achieving highly reconfigurable transceivers for multiple communication standards and frequencies presents a series of challenges. Accommodating various frequency bands necessitates multiple bulky filters in both transmitter and receiver, leading to increased form factor, cost, and insertion loss. High-speed communications typically with high peak-to-average power ratios (PAPR) require more power backoff in power amplifier (PA) for good linearity while compromising transmitter efficiency. Moreover, ultra-high-speed communications such as 5G mm-wave call for ultra-low-jitter local oscillator (LO) and clock generation with fine frequency resolutions. This workshop focuses on addressing these challenges through the approaches of RF/analog/digital hybrid design techniques. Critical circuit topologies including RF digital-to-analog converter (RFDAC), digital power amplifier (DPA), N-path filter/mixer, magnet-free circulator, and fractional-N sub-sampling all-digital phaselocked loop (ADPLL) are presented. The audiences are invited to explore the integration of these techniques to achieve unified transceiver architectures with exceptional reconfigurability. Five prominent speakers from leading institutes and companies will present their latest works and share insights on the development of advanced RF front-end design. Two speakers will delve into the design of RFDACs and DPAs in high-efficiency transmitters. Afterwards, another two speakers will discuss N-path filters and mixers, as well as magnet-free circulators, for high-selectivity receivers and fullduplex transceivers. Finally, the fifth speaker will guide our attentions to the LO and clock generation, by presenting the design of ultra-low-jitter fractional-N all-digital sampling phase-locked loops. The workshop serves as a collaborative platform, bringing together experts from academia and industry to discuss and envision the future of highly reconfigurable transceiver IC design. Through the presentations and the panel discussion session, attendees will gain valuable insights into the cuttingedge techniques driving the development of RFIC design.

- 1. "Emerging Techniques for RF Digital-to-Analog Converter", **Mike Shuo-Wei Chen**, *University of Southern California*
- 2. "Reconfigurable Digital PAs for Backoff Efficiency, Output Power, Bandwidth, and Linearity Enhancement", **Huizhen Jenny Qian**, *Xidian University*

- 3. "Interference Mitigation in RF and mm-Wave Circuits and Systems for Future Wireless Networks", Negar Reiskarimian, *MIT*
- 4. "High Dynamic-Range Passive Mixers for Flexible mm-Wave Communications", Alyosha Christopher Molnar, *Cornell University*
- 5. "Low-Jitter PLLs for Advanced Wireless Transceivers", Wanghua Wu, Samsung

WSF (Half-Day): 08:00–11:50 3D Heterogeneous Integration and 3D-Packaging Targeting B5G-6G mm-Wave and Sub-THz Communication and Sensing

Sponsor: RFIC/IMS

Organizers: Didier Belot, STMicroelectronics Pierre Busson, STMicroelectronics

Abstract: The 6G Telecom generation forecasts mm-wave and sub-THz applications as Fronthaul and Backhaul mm-wave and sub-THz wireless links; Reflective Intelligent Surface between minicell station and devices mainly in mm-wave frequency range; Short distance ultra-high data-rate mm-wave and sub-THz wireless data storage transfer; Automotive Joint communication and Sensing Radars; Health and Industrial mm-wave and sub-THz Radars and imagers; and other applications which are not yet defined. A Key challenge facing us is how to manage multi-processes dies with antennas integrated in the same object, reducing losses, and then increasing power efficiency and, at the same time targeting the cost efficiency. The workshop will discuss the trade-off Power Efficiency/ Cost Efficiency of different 3D assembly strategies and will try to have a picture of the most promising research in the domain, through topics which will address as III-V GaN/Si and InP/Si, with SiGe and or CMOS Heterogeneous Integration; Wafer to Wafer; Die to Wafer, Backend of line co-integration; mm-wave sub-THz packaging, including Antenna integration, Si-Interposers, organic interposers, and other packaging 3D approach. The power efficiency can be defined as the max data rate ability, with the max distance covered by the transceiver over its power consumption, the cost efficiency is max data rate ability, with the max distance covered by the transceiver over its cost. This simple relation does not take into account the cooling equipment, if necessary, the reliability, and finally the environmental impact of the different strategies. These last points are difficult to quantify at the research level.

- 1. "System-on-Wafer: 2D and 3D Technologies for Heterogeneous Systems", **Hervé Boutry**, **Olivier Valorge, Christophe Dubarry**, *CEA-Leti*
- 2. "RF-Heterointegration at Wafer-Level and Panel-Level for mm-Wave Applications", Siddhartha Sinha, Nadine Collaert, *imec*
- 3. "Material and Packaging Trends for High Frequency mm-Wave Applications", **Tanja Braun**, *Fraunhofer IZM*
- 4. "Heterointegration Approaches for InP-HBT Technologies for 5G Applications and Beyond", **Hady Yacoub, Wolfgang Heinrich**, *FBH*

WSH (Half-Day): 08:00–11:50 Operating at the Extreme: RFIC Design Techniques for Operation Beyond the PDK Limits

Sponsor: RFIC

Organizers: Travis Forbes, Sandia National Laboratories Amrita Masurkar, BAE Systems

Abstract: Emerging applications such as satellite-based internet, quantum computing, hightemperature sensors and communications systems, and massive Internet-of-Things (IoT) wireless networks are enabling disruptive advances in computational ability, global internet coverage, device-to-device communications, and industrial and military sensing abilities. However, all of these extreme environments require integrated circuits to operate well beyond environmental ranges and operating voltages provided by the standard Process Development Kits (PDK) and require a combination of design skills traditionally held in non-overlapping design communities. This workshop will bring together these design communities through experts from academia and industry to provide attendees with a holistic view on overcoming these challenges. Starting near zero Kelvin, the first talk will give an overview of circuit design at cryogenic temperatures including effects on devices, matching, and how to overcome these effects. Taking it hotter, the next talk will cover device effects operating well above 150C and ongoing research to enable high yield systems at these temperatures. Making the workshop RAD, the third talk will give an overview of radiation effects on CMOS circuits and ways to design RF and analog circuits to overcome these effects. Taking it out of this world, the fourth talk will cover challenges of both radiation and temperature effects found in space-based applications and design techniques to overcome these challenges. The final talk will cover dense wireless environments with high-power RF blockers pushing the limits of the supported process supply voltage and RFIC design techniques to filter and operate through this interference. To end the workshop, we will bring the experts together for cross-pollination of ideas through a panel interaction with attendees. Can this panel create a space radiation hardened, any temperature-stable, high-power handling device? ... Come and find out!

- 1. "Challenges and Approaches for Mixed-Signal Cryogenic CMOS Design", **Kevin Tien**, *IBM*
- 2. "Operating at the Extreme: Design of Electronics at High Temperatures", **Matt Francis**, *Ozark Integrated Circuits*
- 3. "Effects of Radiation on CMOS RF and Analog Circuits, and Mitigation Techniques", **Samuel Palermo**, *Texas A&M University*
- 4. "RFIC Techniques for Deep Space Planetary Exploration", Adrian Tang, JPL
- 5. "Maintaining Receiver Sensitivity in the Presence of High-Power RF Blockers", **Eric Klumperink**, *University of Twente*

WSJ (Half-Day): 08:00–11:50 Ultra-Wideband Efficient PAs and Broadband Matching Design Techniques

Sponsor: IMS/RFIC

Organizers: Salvatore Finocchiaro, Qorvo Teerachot Siriburanon, University College Dublin

Abstract: The evolution of 5G and the need for increased capacity drive new transmitter requirements. Broadband and multiband operation requires the Power Amplifiers (PAs) to support a wider operating frequency range and high data rate require large instantaneous bandwidths, further extended by carrier aggregation, while delivering high power and maintaining high efficiency. Additionally, modern systems require complex modulation schemes exhibiting high Peak-to-Average-Power Ratio (PAPR) of more than 10dB. When operating at high Output-BackOff (OBO), Drain and Power Added Efficiency (DE and PAE) of traditional PA is typically low, with the majority of power dissipated in heat! New efficiency enhancement architectures and design techniques, from Waveform Engineering, to Load Modulation (Doherty, Outphasing and LMBA) and Supply Modulation (Envelope Tracking), have been explored in recent years. The desire for the widest possible operational bandwidth (operating frequency range) to reduce system complexity and cost is driving new broadband design techniques exploring broadband combining and broadband matching. This workshop will introduce recent trends in PA architectures, PA design and broadband matching techniques addressing the three major challenges listed above, ie wide operating bandwidth, wide instantaneous bandwidth, and large PAPR. We will look at design trade-offs to improve and maintain efficiency while satisfying system requirements which include ACLR, EVM, and other metrics for 5G New Radio (5GNR) waveforms. The concept of linearization and Digital Predistortion (DPD) will be introduced in the context of evaluating the PA performance with respect to system requirements. Experts from industry and academia that are at the frontline of these developments are invited to address these issues and inform the audience about the latest advances in this field.

- 1. "The Load Modulated Balanced Amplifier as a Frequency Agile PA Technique", **Roberto Quaglia**, *Cardiff University*
- 2. "Design Challenges of Broadband High-Power Load-Modulated Power Amplifiers", **Luís C. Nunes**, *Instituto de Telecomunicações*
- 3. "Wideband Power Amplifier Design Through Active Impedance Matching", **Taylor Barton**, *University of Colorado Boulder*
- 4. "Power, Efficiency, and Linearity Trade-Off in Designing GaN Solid-State Power Amplifiers (SSPAs) for SATCOM Applications", **Rocco Giofrè**, *Università di Roma "Tor Vergata"*
- 5. "MISO Load Modulated Power Amplifiers with Digital Predistortion", **Noureddine Outaleb**, *Analog Devices*
- 6. "mm-Wave Power Amplifiers with Wideband Efficiency, Ultra-Compactness and Built-in Sensors", **Hua Wang**, *ETH Zürich*

WSL (Full-Day): 08:00–17:20 From Waves to Insights: AI/ML Techniques for Wireless Communications and Radar

Sponsor: RFIC

Organizers: Alberto Valdes-Garcia, IBM T.J. Watson Research Center Young-Kai Chen, Coherent Arun Paidimarri, IBM T.J. Watson Research Center

Abstract: Algorithms and processing pipelines based on Artificial-Intelligence (AI) and Machine-Learning (ML) techniques are on a solid trajectory to become an integral part of the next generation of wireless systems. While the exploration of AI/ML to RF applications started decades ago, their development has accelerated recently with the increasing availability of advanced AI knowledge, high-capacity compute infrastructure, and wireless testbeds for generation and training data sets. Nevertheless, the development of AI-enhanced wireless systems remains a challenging multidisciplinary task, where EM, RF, IC design, signal processing, and ML expertise are all equally important. Emerging 6G wireless communications systems and mm-wave radar applications call for accelerated developments in this area. In particular, power consumption and latency requirements may require the implementation of optimized feature extraction methods in mixed-signal ICs closer to the antennas. The goal of this workshop is to bring together a set of active researchers to share their vision and expertise on these topics in order to bring a cross-disciplinary awareness and understanding among RFIC, AI, and systems communities. The speakers span academic and industrial research institutions from across the globe and the presentations will cover both wireless communications and radar.

- 1. "AI/ML Empowered High-Order Modulations for 6G High Capacity Communications", **Caleb Lo**, *Samsung*
- "ML for Rapid Network Reconfiguration: Radar Detection Using Open RAN and Multimodal Fusion for Vehicular mm-Wave Beamforming", Kaushik Chowdhury, Northeastern University
- 3. "Machine-Learning Physical-Layer Receivers for Future 6G Networks", **Mikko** Valkama, *Tampere University of Technology*
- 4. "Neural Networks and Dictionary Learning for Compressive, Phase-less, mm-Wave Beam Alignment", **Danijela Cabric**, *University of California, Los Angeles*
- 5. "Multi-Modal Sensing Front-Ends Using Wireless Above 100GHz and Lidar", **James F. Buckwalter**, *University of California, Santa Barbara*
- 6. "Adaptive Analog Feature Extraction: Algorithm and Hardware Primitives", **Saibal Mukhopadhyay**, *Georgia Tech*
- 7. "High-Resolution mm-Wave Imaging and Detection for Self-Driving Cars", **Jungfeng Guan, Haitham Al-Hassanieh**, *EPFL*
- 8. "Concealed Object Detection with 3D Radar and DNN-Based Feature Extraction", **Asaf Tzadok**, *IBM T.J. Watson Research Center*

- 9. "Deep mm-Wave Gait Analysis: Challenges and Opportunities", Amin Arbabian, *Stanford University*
- "Machine-Learning Application in Surveillance and Infrastructure Radars Small Target Detection and Identification of Vulnerable Road Users", Simon Wagner, Fraunbofer FHR

WSM (Full-Day): 08:00–17:20 Future of Chiplet Technology and 3D Heterogeneous Integration

Sponsor: RFIC/IMS

Organizers: Bahar Jalali Farahani, Cisco Mahdi Parvizi, Cisco Salvatore Finocchiaro, Qorvo Ko-Tao Lee, Qorvo

Abstract: As the Moore's law is coming to an end, separating large systems into smaller chips based on their functionality is not only a cost-benefit solution but it allows the complex system to expand beyond theoretical size limits. Although chiplet technology has been around for many years, it has not been till the rise of the AI supercomputers and the accompanied unprecedented computational demand that put the spotlight on SiPs (System in Package). There are different aspects to the design of chiplets including the packaging, the high-speed chip-to-chip interconnect and the interoperability and standardization which allow the SiP built by the combination of chips from different vendors. There are multiple benefits to the chiplet-based architectures. Breaking down the large complex systems into smaller chips based on their functionality means better yields and lower cost due to the lower probability of manufacturing defects. Cost reduction can also come with customizing the process technology for each chiplet (eg using advanced nodes for GPUs and CPUs and less expensive technologies for memories and analog interfaces). Design upgrades can also be done on certain functional blocks without the need for redesigning the whole system. To take full advantage of chiplet-based architectures, the D2D (die-to-die) interface needs to be standardized. The interoperability allows the developer to use multiple vendors. In terms of the packaging, development of 3DHI (3D Heterogeneous Integration) that enables stacking up separately manufactured components, is the perfect technology choice for chiplet-based architectures. Additionally, the everincreasing demand for high-throughput communication links and high-resolution radar sensors is driving the development of future wireless systems at higher operating frequencies. In order to support multiple functionality, the flexibility requested to those systems, is driving the adoption of large phased array antennas. Heterogeneous technologies and vertical 3D integration will play a vital role in enhancing the performance and functional density, along with reducing the size and costs, of such RF systems. In addition to the already mentioned standardization, both on the digital and RF side, 3DHI will pose a new set of technology (processes and substrates), design (MMICS, RFIC, analog, power management, passives), packaging and thermal challenges. This workshop will address some of the challenges mentioned above both from the digital and RF point of view, combining commercial and defense perspectives with state-of-the-art research in the field. Experts from industry and academia that are at the frontline of these developments are invited to address these issues and inform the audience about the latest advances in this field.

Speakers:

- 1. "Chiplets' Central Role in Connectivity and AI Everywhere", **Tony Chan Carusone**, *University of Toronto*
- 2. "Chiplet Interconnect Solutions", Syrus Ziai, Eliyan
- 3. "Package-to-Package Scale-Out Interconnect Solutions Based on In-Package Optical I/O", **Miloš Popović**, *Ayar Labs*
- 4. "Die-to-Die Interconnect Based on Micro-LED Arrays", Bardia Pezeshki, Avicena
- 5. "Vertical Stacking with Si-Cored Substrates", Steven Verhaverbeke, Applied Materials
- 6. "Glass-Based Stitch-Chip Technologies and Advanced Packaging for mm-Wave HI", Muhannad S. Bakir, *Georgia Tech*
- 7. "Building >100GHz Phased Array Systems using Standard 3D Integration Technologies", **Gabriel M. Rebei**z, *University of California, San Diego*
- 8. "3D Integration of ICs and Antennas for Ubiquitous mm-Wave Arrays", **Arun Natarajan**, *Oregon State University*
- 9. "Thermal Management for 3DHI and Advanced Packaging", **Robert Pearson**, *Lockheed Martin*
- 10. "3D Heterogenous Integration (3DHI) for Advanced Communications", **Madhavan** Swaminathan, *Penn State University*

WSN (Full-Day): 08:00–17:20 Integrated Circuits for Control and Characterization of Quantum Processors

Sponsor: RFIC

Organizers: Vadim Issakov, Technische Universität Braunschweig Joseph C. Bardin, Google Quantum AI and UMass Amherst

Abstract: Large-scale quantum computers promise to enable the solution to certain classes of problems for which no other efficient approaches are currently available. The realization of such a computer is hence a major open challenge that is being aggressively researched by academic and industrial teams across the globe. There are several types of competing qubit realizations, each offering different advantages. Yet, all of these realizations require some form of cryogenic cooling and most require RF electronics for control and potentially for readout (in several realizations the readout is optical). Moreover, integrating the control and/or readout electronics at an intermediate temperature stage within the cryostat is an attractive option. However, the circuits still need to fulfill stringent requirements on power consumption, spectral purity, noise budget etc, making their optimization challenging. As such, there is a growing opportunity for the RFIC community to influence this emerging field. In this full-day workshop the state-of-the-art in cryogenic RF circuits for various types of qubit realizations is reviewed. System considerations for various qubit modalities will be discussed, leading to the circuit-level specifications that drive the architectural considerations associated with control ICs targeting different qubit types. The talks will present different RF circuit

design solutions for various types of qubits including silicon spin qubits, superconducting qubits, and trapped-ion qubits. The workshop features distinguished speakers from leading companies and academia, who will present their latest advances on cryogenic circuits for quantum computer applications. A brief concluding discussion will round-off the workshop to summarize the key learnings on the wide range of aspects presented during the day.

Speakers:

- 1. "Control of Frequency Tunable Superconducting Processors", **Juhwan Yoo**, *Google Quantum AI*
- 2. "Cryogenic Circuits for Superconducting Qubit-Based Quantum Computing", **Daniel** Friedman, *IBM T.J. Watson Research Center*
- 3. "Circuit Design for Large-Scale Quantum Controller SoC", Jae-Yoon Sim, POSTECH
- 4. "Cryogenic CMOS Mixed-Signal Circuits for Quantum Computer", **Hiroki Ishikuro**, *Keio University*
- 5. "Circuit and System-Level Considerations Towards Scalable Trapped Ion Quantum Computer", **Vadim Issakov**, *Technische Universität Braunschweig*
- 6. "Multiplexed Qubit Control with Ultra-Low-Power, Base-Temperature Cryo-CMOS Multiplexer", **Anton Potočnik**, *imec*
- 7. "Cryo-CMOS Electrical Interfaces for Large-Scale Quantum Computers", **Niels Fakkel**, *Technische Universiteit Delft*
- 8. "Cryo-CMOS Integrated Circuits Across a Silicon Qubit Quantum Computing Stack", **Sushil Subramanian**, *Intel*

WSO (Full-Day): 08:00–17:20 Linearity and Efficiency Challenges in Wide Modulation Bandwidth Power Amplifier Design

Sponsor: RFIC

Organizers: Debopriyo Chowdhury, Broadcom Hyun-Chul Park, Samsung

Abstract: The rapid increase in data throughput in recent 5G (FR1 and FR2), Wi-Fi (6E and 7), and 6G (FR3 in the near future) requires high-efficiency, linear and wideband RF power amplifiers. However, it is extremely challenging to simultaneously enhance the linearity and efficiency of the power amplifier, especially for spectrally-efficient and wide modulation bandwidths (eg 320MHz for Wi-Fi 7, 100MHz for 5G FR1, and >400MHz for FR2). Higher order constellations like 4k-QAM for Wi-Fi 7, 256-QAM for FR2 make PA design a challenging task. This workshop will cover the "practical" and "most promising" linearity and efficiency improvement techniques for RF power amplifiers and transmitters. Several techniques like wideband envelope tracking, Doherty power amplifiers, digital transmitters, mm-wave power amplifiers etc, will be covered in a tutorial type fashion, with emphasis on practical aspects of the design.

Speakers:

- "Power Amplifiers for High Peak-to-Average-Ratio Signals Architectures and Tradeoffs of Efficiency, Linearity and Bandwidth", Peter Asbeck, University of California, San Diego
- 2. "Design Techniques for Doherty Power Amplifiers to Enable Deep Backoff Efficiency Enhancement and Wide Modulation Bandwidth", **Taiyun Chi**, *Rice University*
- 3. "Digital Envelope Tracking to Address 5G, 6G, and WiFi7 Power Efficiency", **John Hoversten**, *Eta Wireless*
- 4. "Design, Characterization and Linearization of Wideband Outphasing Power Amplifiers Operating within the Doherty-Chireix Continuum", **Patrick Roblin**, *The Obio State University*
- 5. "Efficiency Enhancement Techniques for Digital Power Amplifiers", **Yun Yin**, *Fudan* University
- 6. "Efficient Wideband Digital Predistortion for Power Amplifier Linearization", **Paul Draxler**, *MaXentric Technologies*
- 7. "Highly Efficient and Linear mm-Wave Power Amplifiers for 5G FR2 Communication", **Joonhoi Hur**, *Samsung*
- 8. "Recent Progress on Wideband Integrated SOI CMOS Power Amplifiers for Mobile and Wi-Fi Applications", **Ayssar Serhan**, *CEA-Leti*

WSP (Full-Day): 08:00–17:20 mm-Wave and Sub-THz Broadband Phased Array FE for Communication and Sensing

Sponsor: RFIC

Organizers: Didier Belot, STMicroelectronics Wanghua Wu, Samsung Hao Gao, Technische Universiteit Eindhoven

Abstract: With technological advancement, the spectrum of possibilities within the realms of communication and sensing is expanding astonishingly. One of the most exciting frontiers in this domain is the utilization of mm-wave and sub-THz frequencies, offering a gateway to revolutionary advances in wireless communication and sensing. The workshop collects the transformative capabilities of mm-Wave and Sub-THz technologies, which collectively span the frequency range from 30GHz to 300GHz. This previously underutilized spectrum is now at the forefront of technological breakthroughs. At the heart of this paradigm shift lies the broadband front-end, a critical component that enables the seamless harnessing of mm-Wave and Sub-THz frequencies for applications that were once considered futuristic. One of the central themes of the workshop is the advancement of high-frequency networks, and the mm-wave and Sub-THz spectrum integration in wireless systems. Witness how these innovations reshape the connectivity landscape, enabling applications like 6G, autonomous vehicles, smart cities, etc. The workshop takes participants on

a journey through the diverse applications of mm-wave and Sub-THz sensing, from radar systems that can revolutionize wireless communication to high-resolution imaging techniques that can potentially transform human life.

Speakers:

- "28GHz, 60GHz and 140GHz mm-Wave Phased Arrays for Communication and Sensing Systems: a Common Platform", Gabriel M. Rebeiz, University of California, San Diego
- 2. "6G Architectures and Technology Partitioning for Communication and Sensing", **Yang Zhang**, *imec*
- 3. "Energy Efficient Communication and Sensing Front-Ends Enabled by Innovative Frequency Generation Techniques", **Jose-Luis Gonzalez-Jimenez**, *CEA-Leti*
- 4. "Pioneering Ultrahigh-Speed Terahertz Communication for 6G: Challenges and Opportunities", **Minoru Fujishima**, *Hiroshima University*
- 5. "SiGe: BiCMOS Technology is Enabling D-Band Link with Active Phased Antenna Array", Andrea Pallotta, Didier Belot, *STMicroelectronics*
- 6. "The Impact of Joint Communication and Sensing to Radio Front-End", **Rui Hou**, *Ericsson*
- 7. "The Evolution of Automotive Radar Circuits from Gunn Diodes to CMOS SoCs", **Christoph Wagner**, *Silicon Austria Labs*
- 8. "Broadband mm-Wave Front-End Design Methodology for Radar and Wireless Communication", **Hao Gao**, *Technische Universiteit Eindhoven*

WSQ (Full-Day): 08:00–17:20 Phased Arrays and MIMO for mm-Wave 6G/WiFi and Sensing Systems

Sponsor: IMS/RFIC

Organizers: Rocco Tam, NXP Semiconductors Oren Eliezer, Samsung Jin Zhou, MediaTek Kostas Doris, NXP Semiconductors

Abstract: The reliance on digital beamforming and large arrays in mm-wave is increasing as communication and sensing systems migrate to higher frequency bands and occupy wider bandwidths. In this workshop experts in communications, automotive radar/sensing, antennas and silicon and packaging technologies will share their related experience and vision and discuss various challenges and solutions at the system, circuit, and technology levels.

- 1. "Re-Thinking the mm-Wave MIMO Radar Architecture for Future Automotive Radars", **Kostas Doris**, *NXP Semiconductors*
- 2. "Integrated mm-Wave (IMMW) Wi-Fi", **Carlos Cordeiro**, *Intel*

- 3. "Design of Advanced mm-Wave Phased Array Modules", **Bodhisatwa Sadhu**, *IBM T.J. Watson Research Center*
- 4. "ICs and Transceivers for 100–300GHz Wireless (Comm and Sensing)", **Mark Rodwell**, *University of California, Santa Barbara*
- 5. "True-Time-Delay Large Scale Array for Next-Generation Wireless", **Subhanshu Gupta**, *Washington State University*
- 6. "Emerging Devices and Heterogeneous Integration for Future mm-Wave Systems", Nadine Collaert, *imec*
- 7. "Beamforming Challenges in 5G FR-2 Base Stations", Yuuichi Aoki, Samsung
- 8. "Architecture, Design and Deployment Challenges of E-Band and D-Band Communication Systems", **Shahriar Shahramian**, *Nokia Bell Labs*

WSR (Full-Day): 08:00–17:20 Sensing Modalities for the Road to Autonomy and Beyond

Sponsor: IMS/RFIC

Organizers: Zeshan Ahmad, Cambridge Terabertz Matt Markel, Spartan Radar

Abstract: Sensing modalities are enabling technologies for the ongoing revolution in autonomy. This is evident from the global sensor market that was valued at \$166B in 2019 and is projected to reach over \$345B by 2028. Camera, LiDAR, and RADAR dominate the autonomy field, and IR/ thermal is now emerging as an important modality in that space. However, today none of the sensing modalities alone can solve the abundant challenges needed for robust, reliable, and trust-worthy autonomy in difficult environments. To that end, this workshop brings together a unique mix of top industry, academic, and regulatory body speakers to discuss these challenges, the current solutions, and what we can expect today's research to bring for tomorrow. The speakers bring a breadth of expertise and experiences ranging from electronics to photonics, integrated systems to sensor fusion, and OEMs to regulators; this insight comes together in a workshop-concluding panel discussion that dives deep into key forces pushing us towards — and holding us back from — autonomy.

- 1. "Brief Workshop Introduction", Zeshan Ahmad, Cambridge Terabertz
- 2. "Software Defined Radars with the Resolution of Lidar", Antonio Puglielli, Zendar
- 3. "Navigating Frequencies A Comprehensive Exploration of Radar Applications and Beyond", **Francisco Salmeron**, *A4Radar*
- 4. "Digital Radar for Convergence of Sensing and Communications", **Jungah Lee**, *Aura Intelligent Systems*
- 5. "Silicon Photonics for Solid-State LiDAR and Beyond", Jelena Notaros, MIT
- 6. "From IoT (Internet-of-Things) to AoT (Autonomy-of-Things)", **Sabbir Rangwala**, *Patience Consulting*

- 7. "Advanced Sensing for Autonomy", Abdullah Zaidi, Rivian
- 8. "Enhanced Pedestrian Safety with 3D Thermal Ranging using AI for ADAS/AV Applications", **Chuck Gershman**, *Owl Autonomous Imaging*
- 9. "How are AVs regulated?", Sam Loesche, Waabi
- 10. "Panel Discussion", Matt Markel, Spartan Radar

WSG (Half-Day): 13:30–17:20 Digital Intensive Transmitters From RF to mm-Wave: Empowering Intelligent and High Data-Rate Wireless Communication

Sponsor: IMS/RFIC

Organizers: Huizhen Jenny Qian, Xidian University Jeffrey Walling, Virginia Tech Austin Chen, Independent Consultant

Abstract: Advanced CMOS technologies enable direct bits-to-RF conversion, which provides higher energy-efficiency and more compact die area, especially for sub-7GHz. Meanwhile, such digital intensive transmitters, with highly reconfigurable nature are well adapted for multifunction and intelligent communication systems. When the operation bands extend to mm-wave to meet the increasing data streaming requirements of modern communication systems (eg 5G, 6G, etc), digital intensive transmitters also exhibit potential advantages compared to traditional Cartesian transmitters. This workshop discusses techniques of digital intensive transmitters operating from sub-7GHz to mm-wave with continuous evolution of higher output power, efficiency, data-rate, and multi-functions such as distortion self-calibration, multi-band, multi-mode, etc.

- 1. "Highly Efficient, Wideband, Frequency-Agile Digital Transmitters", **Masoud Babaie**, **Marco Spirito**, **Leo de Vreede**, **Morteza S. Alavi**, *Technische Universiteit Delft*
- 2. "Data-Rate Enhancement Techniques for Digital Transmitters", **Huizhen Jenny Qian**, *Xidian University*
- 3. "Versatile RF-DACs, from RF-to-mm-Wave, to Enable the Sixth Generation of Wireless Communication", **Jeffrey Walling**, *Virginia Tech*
- 4. "Design of Digital-Intensive Wireless Transmitters", Yun Yin, Fudan University
- 5. "Road to Digitally Intensive Transmitter Architectures at mm-Waves", **Khaled Khalaf**, *Pharrowtech*

WSI (Half-Day): 13:30–17:20 From Prototype to Product: Overcoming Productization Challenges

Sponsor: RFIC

Organizers: Joseph Cali, Raytheon Bichoy Bahr, Texas Instruments Oren Eliezer, Samsung

Abstract: Are you a student or a professional researcher seeking insights into the process of productizing ideas? Perhaps you are an experienced designer keen on understanding how fellow professionals have surmounted challenges during product development. If so, this workshop is tailored for you! Industry experts representing high-volume commercial integrated circuit (IC) companies. IP developers, aerospace, and defense sectors will share their experiences of navigating the journey from conceptualization to fielded product. Engaging discussions will encompass a diverse array of topics, spanning high-speed analog to digital converters, digital to analog converters, mm-wave packaging, multi-antenna beam steering calibration, RF front-ends and the benefits of RF/packaging co-simulation. During the developmental phase of prototypes, constraints related to budgets and schedules often hinder thorough validation, verification, and testing procedures. Consequently, this limitation can lead to the emergence of latent defects that remain undetected until later stages of productization. In these scenarios, research teams and start-ups may be primarily focused on core innovations and transformative concepts, only to encounter obstacles when the company aims to expedite the implementation of these ideas. For instance, in startup environments lacking dedicated facilities for environmental testing, issues like low-temperature oscillations (which are unobservable during simulations) may go unnoticed until far too late. The instances discussed within this workshop serve as valuable examples that can form the basis of a comprehensive checklist, enabling a smoother transition from the prototype phase to the final product. We hope this workshop could potentially prevent the need for extensive reiterations, saving both time and resources for you and your colleagues.

- 1. "mm-Wave LGA and BGA Package Design and Assembly Challenges", **Eamon Nash**, *Analog Devices*
- 2. "mm-Wave and RF Data Converter Design Challenges", **Farhan Adil, Joseph Cali**, *Raytheon*
- 3. "High Frequency IC/Package Co-Design using Integrated Toolsets", **Paul Mosinkskis**, *Cadence*
- 4. "Transitioning RF SiGe Designs from R&D into Production for Defense Systems", Gregory M. Flewelling, *BAE Systems*
- 5. "Phased Array Calibration: Overcoming Productization Challenges in CMOS Analog Beamforming Arrays", **Oren Eliezer**, *Samsung*

WSK (Half-Day): 13:30–17:20 Flexible Arrays as the Next Frontier in Wireless Communications

Sponsor: IMS/RFIC

Organizers: Subhanshu Gupta, Washington State University Antoine Frappé, IEMN (UMR 8520) Najme Ebrahimi, University of Florida

Abstract: With global networking data traffic predicted to reach petabytes in the next few years, mm-wave wireless communications enabled by silicon-based phased arrays is poised as a game-changer for new infrastructure applications. Emergence of untethered space constellations such as low-earth orbit (LEO) satellite communications approximately lying between 500km to 800km altitude such as Amazon Kuiper (590–630km), SpaceX Starlink (550–750km), OneWeb (1200km), and Telesat Lightspeed (1015–1325km) will further benefit global connectivity. By utilizing the fallow spectrum at mm-wave, it is expected to provide gigabits-per-second data rates to multiple users including under-served and remote areas. While planar mm-Wave phased arrays have cemented their position in communication systems, the future of satellite constellation hosting thousands of antenna elements is dependent on the choice of frequency, application, field-of-view, and form factor. Conformal phased arrays, which encompass mechanically flexible, foldable, or stretchable arrays, are one of the promising new frontiers of array development. Conformal antennas provides multiple degrees of freedom to the scan angle that is typically limited by antenna aperture. Recent works have demonstrated new viable research directions at the antenna-RF interface with the adaptive control that will be presented in this workshop.

- 1. "Shape-Morphing Origami-Based Microwave Arrays for Reconfigurable Computational Imaging", **Kaushik Sengupta**, *Princeton University*
- 2. "A Scalable Heterogeneous AiP Module for a 256-Element 5G Phased Array", **Atom Watanabe**, *IBM T.J. Watson Research Center*
- "Additively Manufactured Flexible Tile-Based Massively Scalable Phased Arrays for 5G+ Enabled Smart Skins and Reconfigurable Intelligent Surfaces", Manos M. Tentzeris, *Georgia Tech*
- 4. "Large-Aperture Flexible Phased Array with CMOS Beamformer for Small Satellites", **Kenichi Okada**, *Tokyo Tech*

Social Events/Guest Program

SUNDAY, 16 June 2024 RFIC Welcoming Reception 19:30–21:00

RFIC'24 starts with a welcome event on Sunday for all attendees, which will be hosted at Ballroom South Pre-Function immediately following the RFIC'24 Plenary Session.

MONDAY, 17 June 2024 IMS Welcome Event 19:30–21:30

IMS'24 starts with a welcome event on Monday for all attendees, which will be hosted at the The National Museum of African American History and Culture Center immediately following the IMS'24 Plenary Session.

MONDAY, 17 June 2024 – THURSDAY, 20 June 2024 Guest Lounge

The Guest Lounge will be open to all registered guests Monday, 17 June 2024 through Thursday, 20 June 2024. Light refreshments will be provided for all registered guests.

TUESDAY, 18 June 2024

Women in Microwaves Networking Event 15:45–16:30 and 19:30–21:30

The Women in Microwaves will host a joint panel session with the Young Professionals, entitled "Developing Your Personal Brand". The panel session will be held at the Walter E. Washington Convention Center, Room 144AB. After the panel session, the annual WIM reception will be held International Spy Museum in Washington, DC in the evening.

RFIC Student-Industry-Academia RFIChat "Burning Career Questions? Come Chat with the Pros!" 17:00–18:30

Come and join the special event customized by and for RFIC'24 students, academia, and the RF industry! The event will be held at the Walter E. Washington Convention Center, Room 207AB.

WIM, YP Receptions, Ham Radio Social, and Scavenger Hunt 17:30–21:30

The annual WIM, YP, and Ham Radio receptions will be held at The Spy Museum. The receptions are a place to network over cocktails and snacks and be sure to participate in the scavenger hunt!

Social Events/Guest Program continued...

TUESDAY, 18 June 2024 – THURSDAY, 20 June 2024

Startup Program at IMS

The Startup Program at IMS2024 fosters a dynamic environment where ideas meet opportunity, paving the way for fruitful collaborations and groundbreaking partnerships between visionary entrepreneurs, industry giants, and potential investors. IMS2024 brings forth a series of events curated to propel start-ups toward success. These events will be held during the course of the week and embody the excitement and passion that start-ups are known for.

WEDNESDAY, 19 June 2024 Industry-Hosted Cocktail Reception 17:00–18:00

The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

Awards Banquet 18:30-20:00

The MTT-S Awards Banquet will be hosted at the Marquis Ballroom, Marriot Marquis Washington, DC and will feature exciting entertainment. A ticket is required for entry.

NOTES

Hotel	Rate	Distance
Marriott Marquis Washington, DC(HQ)	\$335	0.0
AC Hotel by Marriott Washington DC	\$299	0.2
Cambria Hotel Washington, DC	\$269	0.5
Comfort Inn Downtown DC	\$249	0.4
Conrad Washington, DC	\$409	0.2
Courtyard by Marriott Washington Downtown	\$309	0.1
Embassy Suites by Hilton Washington, DC	\$339	0.2
Grand Hyatt Washington	\$306	0.3
Hampton Inn Washington Downtown	\$315	0.3
Henley Park Hotel	\$335	0.3
Homewood Suites by Hilton Washington, DC	\$312	0.3
JW Marriott Washington, DC	\$355	0.7
Morrison Clark Historic Inn	\$335	0.2
Motto by Hilton	\$269	0.3
Moxy Washington, DC Downtown	\$279	0.2
Westin Washington, DC Downtown	\$335	0.1
Residence Inn by Marriott Washington Downtown	\$319	0.1
The Mayflower Hotel, Autograph Collection	\$319	0.9
Washington Marriott at Metro Center	\$319	1.0
Washington Plaza Hotel	\$309	0.6

Conference Hotel Accommodations

The above conference rates include complimentary wireless internet.

The conference rates, shown in USD, are subject to applicable state and local taxes. The conference rates are available for the dates of three days prior to and three days following the main convention dates, based on availability.

The distance shown in miles is the walking distance to Walter E. Washington Convention Center.

445 Hoes Lane Piscataway, NJ 08854, USA **2024 RFIC Symposium** Washington, DC, USA 16–18 June 2024

