



# 2023 IEEE Radio Frequency Integrated Circuits Symposium

San Diego, California, USA  
11–13 June 2023



## PROGRAM

San Diego Convention Center

*Sponsored by*

IEEE Microwave Theory and Technology Society  
IEEE Electron Devices Society  
and  
IEEE Solid-State Circuits Society



# RFIC Plenary, Reception, and Symposium Showcase

**Sunday Evening, 11 June 2023**  
**San Diego Convention Center**

After a busy day immersed in RFIC'23 Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in the 4<sup>th</sup> (Upper) Level of the San Diego Convention Center Ballroom 20.

**17:30–19:00, Plenary Session, Ballroom 20BCD:** The evening begins with the Student Paper Awards, Industry Paper Awards, and Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Dr. Todd Younkin, President and CEO of the Semiconductor Research Corporation (SRC), USA, and Prof. Mau-Chung Frank Chang, the Wintek Chair in Electrical Engineering and Distinguished Professor of University of California, Los Angeles (UCLA) and the former President of the National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan.

**19:00–21:00, RFIC Symposium Reception and Showcase, Sails Pavilion (across the hallway from Ballroom 20):** Immediately following the Plenary Session is the RFIC'23 Symposium Reception and Showcase. Food and drinks will be provided while you connect with old friends, make new acquaintances, and catch up on the latest developments in the field.

The RFIC'23 Symposium Showcase is held concurrently with the reception and will feature our industry paper awards finalists, student paper awards finalists and the Systems & Applications Forum. The selected authors will be present to highlight their innovative work, summarized in electronic poster format, and some will also show a live demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss the microwave week's opening event. Please see <https://rfic-ieee.org/> for more details.

The RFIC Symposium is made possible through the generous support of our corporate sponsors:

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**RFIC Symposium Schedule (11–13 June 2023)**

Event	Location	Sat 10 June	Sun 11 June	Mon 12 June	Tue 13 June
Registration	Lobby D	08:00–17:00		07:00–18:00	
Speakers' Breakfast	Ballroom 20A			07:00–08:00	
Workshops	Rooms 23–25, 29–33		08:00–11:50 13:30–17:20		
Workshops Lunch	Meeting Room Foyer, Terrace Side		11:45–13:00		
Technical Lecture	Ballroom 20A		12:00–13:20		
Plenary Session	Ballroom 20BCD		17:30–19:00		
Reception and Symposium Showcase	Sails Pavilion		19:00–21:00		
Technical Sessions	Rooms 23–25			08:00–09:40 10:10–11:30 13:30–15:10 15:40–17:00	
Panel Sessions	Ballroom 20A, Room 32AB			12:00–13:30	
Student/Industry Chat	Room 32AB				17:00–19:00

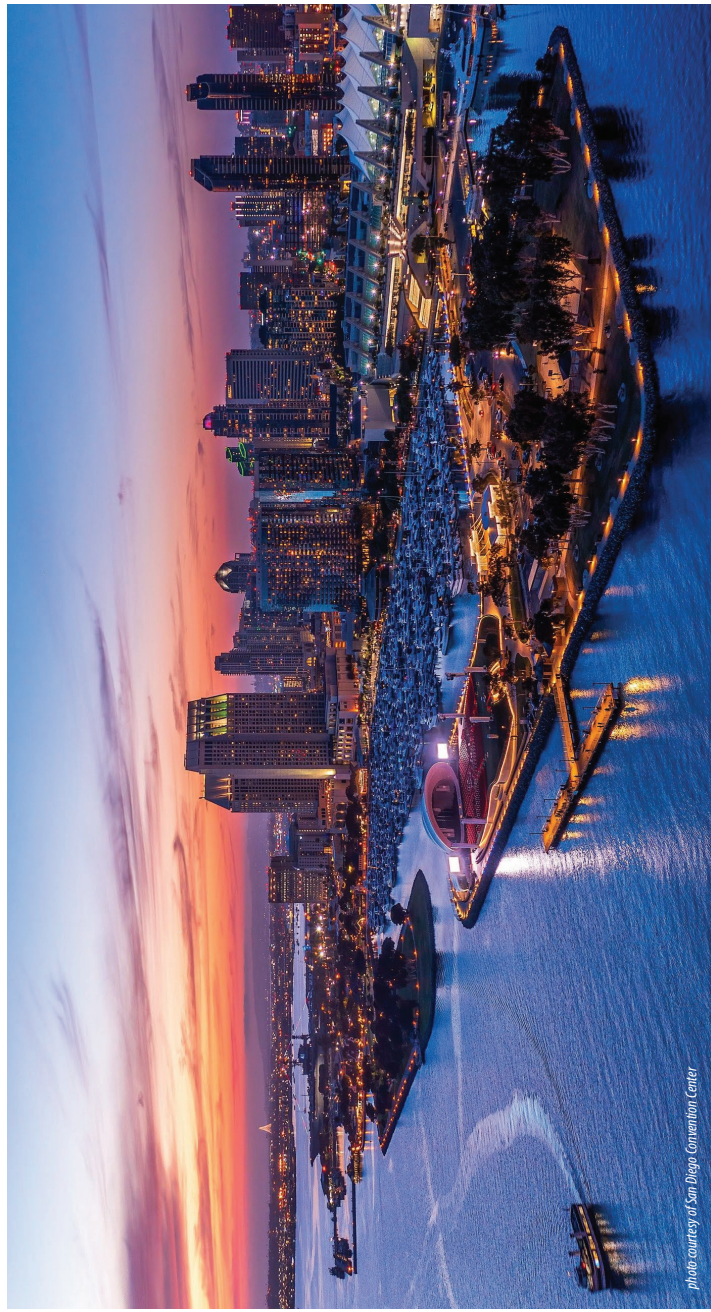


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## Welcome Message from Chairs

On behalf of the Executive and Steering Committees, we would like to invite you to join us for the *2023 IEEE Radio Frequency Integrated Circuits (RFIC'23) Symposium*. The IEEE RFIC Symposium (RFIC) is the premier annual forum focused on presenting the latest breakthroughs and research results in all areas related to radio frequency (RF), millimeter-wave (mmWave), and wireless integrated circuits (ICs). The RFIC Symposium, combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition, forms the “IMS Week”, the world’s largest RF and microwave technical meeting of the year. Fortunately, since the world has finally been recovering from the unprecedented COVID-19 pandemic, we are organizing the RFIC’23 Symposium as an in-person only event.

RFIC’23 will be held at the beautiful San Diego Convention Center, in the heart of the “America’s Finest City”, San Diego, California, from Sunday morning, 11 June, through Tuesday night, 13 June. The event starts with our workshops and technical lecture program on Sunday. The RFIC’23 Plenary Session is held on Sunday night, followed by a welcome reception and the Symposium Showcase. The RFIC technical sessions will be held on Monday and Tuesday in parallel tracks. The IMS technical exhibition will be held on Tuesday, Wednesday, and Thursday.

RFIC’23 technical papers will be presented through parallel sessions on Monday and Tuesday. Our sessions will include topics spanning from highly integrated wireless systems-on-chip and low-power radios to new power amplifiers (PAs), voltage-controlled oscillators (VCOs), and front-end circuitry designs. As mmWave 5G/6G research continues to gain attention, increasingly more mmWave and terahertz (THz) IC content is being published at RFIC. RFIC’23 also continues to expand its scope and has included a new RF Systems and Applications session dedicated to novel applications of RFICs at the systems level. This includes innovations in IC and system architectures, usage models, calibration techniques, and integration approaches. This systems initiative brings together researchers and practicing engineers at the boundary of RFICs and systems to the benefit of all. Additionally, RFIC’23 continues to cover emerging technologies in RF, such as on novel THz solutions, 3D ICs, silicon photonics, quantum computing ICs, hardware security, MEMS-based sensors and actuators, and AI/machine learning applied to RF circuits.

The 2023 RFIC Symposium will feature a rich educational program on Sunday 11 June with eleven RFIC focused workshops and one technical lecture. The RFIC workshops cover a wide range of advanced topics in RFIC technology as follows: mmWave, Advanced High-Speed Circuits and Systems, Low Power, Tutorial Style.

RFIC’23 will also feature an excellent 80 min short course, which we call a “Technical Lecture”, delivered by world-renowned educator and author Prof. Behzad Razavi of UCLA, on “Modern Radio Receivers — From WiFi to 5G and Beyond”. This lecture covers both RFIC and radio system design aspects, and would be instructive and beneficial for both students and newcomers as well as for senior practicing designers.

Following the full day of Sunday workshops, the RFIC Plenary Session will be held in the evening beginning with conference highlights, the presentation of the Student Paper Awards and the Industry Best Paper Awards. The RFIC’23 Plenary Session will conclude with two visionary plenary talks. In his talk “The Roaring 20s: A Renaissance for the Semiconductor Industry?”, Dr. Todd Youngkin, President and CEO of the Semiconductor Research Corporation (SRC), will share his vision for the future of global semiconductor technologies and design, especially those that will enable future RFIC breakthroughs. Prof. Mau-Chung Frank Chang, the Wintek Chair in Electrical Engineering and Distinguished Professor of University of California, Los Angeles (UCLA) and the former President of the National Yang Ming Chiao Tung University (NYCU), Hsinchu, Taiwan, will deliver his exciting vision on “Future System-on-Chip for Full Spectrum Utilization from RF to Optics”.

Immediately after the plenary session, the RFIC Reception and Symposium Showcase will follow, with highlights from our industry showcase and student paper finalists in an engaging social and technical evening event supported by the RFIC Symposium 2023 corporate sponsors. The showcase will provide



authors the opportunity to demo their work in a lab-like environment for more close-up discussion and interaction. You will not want to miss the 2023 RFIC Reception!

On Monday and Tuesday, RFIC will have multiple tracks of oral technical paper sessions and will offer panel sessions during the lunch breaks. Monday's lunchtime panel, titled "How Soon Will We Become Cyborgs?" will be dedicated to the debate on the expected impact of the increased use of various technologies, such as augmented reality and smart hearing aids, on our everyday lives. Tuesday's lunchtime panel, organized jointly with IMS'23, will discuss the topic of "AI/ML Based Wireless System Design and Operation — Hope or Hype?". This topic is interesting and controversial as the use of machine learning (ML), or more broadly, artificial intelligence (AI), has already been demonstrated in a wide range of applications, including even music composition and artistic design. This lunchtime panel, with both industry and academia experts, will explore how we may harness AI in wireless system design and operation, and will attempt to distinguish hope from hype.

RFIC'23 and the Microwave Week have many educational and professional development opportunities for students, all delivered at an exceptional value. Following its introduction in 2022, RFIC'23 will feature a new, dedicated Student Session, where students can meet, interact, and learn about exciting technology trends and their potential future careers from industry experts. This RFIC'23 Student Session includes an Industry ChipChat and reception on late Tuesday afternoon in Room 32AB, where future leaders meet prominent industry professionals to confess their secrets about their first years in their career. The industry executives/representatives will be talking about "3 Things to Know to Start your RFIC Design Career with a Bang". Bring your questions for an open discussion about the metamorphosis from student to professional RFIC designer, negotiate your salary and how to manage your talent to impact lives and more especially yours. Not enough time to extract all the secrets? Everyone is invited to stay and continue chip-chatting at the RFIC nacho station! Come and join this RFIC'23 special event customized by and for students and the RF industry! Free Food and drinks!

Last but not the least, the RFIC'23 will once again conduct a contest to select the top student papers from the symposium. The top student papers will also be featured at our Sunday's Symposium Showcase, providing an additional exposure opportunity. As part of IMS, students have the opportunity to participate in design competitions and an RF Bootcamp. Lastly, MTT-S offers a Ph.D. Student Sponsorship Initiative for new students to become engaged with Microwave Week, providing learning, networking, and volunteer experiences along with complimentary registration and accommodations to qualified and selected students. Students have the opportunity to purchase the Student Superpass, allowing them to experience every activity within Microwave Week, including a workshop, all three conferences (RFIC, IMS, and ARFTG), the Future Summit, a technical lecture, and much more, all at a deeply discounted price for IEEE student members

On behalf of the RFIC Steering and Executive Committees, we welcome you all to join us at the 2023 RFIC Symposium in beautiful San Diego, CA. Please visit the RFIC'23 website (<https://rfic-ieee.org/>) for more details and updates.



**Donald Y.C. Lie**  
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# RFIC 2023 Schedule

## San Diego Convention Center

### Saturday, 10 June 2023

08:00–17:00 Registration — Lobby D

### Sunday, 11 June 2023

07:00–18:00 Registration — Lobby D

07:00–08:00 Speakers' Breakfast — 20A

08:00–11:50 Workshops — 23–25, 29–33

11:45–13:00 Workshops Lunch — Meeting Room Foyer, Terrace Side

12:00–13:20 Technical Lecture — 20A

*Modern Radio Receivers — From WiFi to 5G and Beyond*

13:30–17:20 Workshops — 23–25, 29–33

17:30–19:00 RFIC Plenary — 20BCD

19:00–21:00 Welcoming Reception Featuring Symposium Showcase — Sails Pavilion

### Monday, 12 June 2023

07:00–18:00 Registration — Lobby D

07:00–08:00 Speakers' Breakfast — 20A

08:00–09:20 RMo1A — 23ABC:

*Circuits and Systems for High-Speed Optical and Wireline Communication*

08:00–09:40 RMo1B — 24ABC: *Silicon-Based Front-Ends and Building-Blocks*

08:00–09:20 RMo1C — 25ABC: *5G & mm-Wave Transceivers and Beamforming ICs*

09:40–10:10 Coffee Break — Foyer Outside Meeting Rooms

10:10–11:30 RMo2A — 23ABC: *GaN Modeling, RFSOI Device and Chip Layout Automation*

10:10–11:30 RMo2B — 24ABC: *III/V Front-Ends and Building-Blocks*

10:10–11:30 RMo2C — 25ABC: *Systems and Applications at RF and mm-Wave*

12:00–13:30 RFIC Panel Session — 20A: *How Soon Will We Become Cyborgs?*

13:30–14:50 RMo3A — 23ABC: *Reference Clock and Frequency Generation Techniques*

13:30–15:10 RMo3B — 24ABC: *High-Performance mm-Wave Low-Noise Amplifiers*

13:30–14:50 RMo3C — 25ABC: *THz & mm-Wave Communication Transceivers & Circuits*

15:10–15:40 Coffee Break — Foyer Outside Meeting Rooms

15:40–17:00 RMo4A — 23ABC: *CMOS mm-Wave Frequency Multipliers*

15:40–16:40 RMo4B — 24ABC: *Advances in NB-IoT and WiFi Radios*

15:40–17:00 RMo4C — 25ABC: *High-Efficiency and Linear 5G mm-Wave Power Amplifiers*

### Tuesday, 13 June 2023

07:00–18:00 Registration — Lobby D

07:00–08:00 Speakers' Breakfast — Ballroom 20A

08:00–09:20 RTu1A — 23ABC: *RF to THz LO Generation Solutions*

08:00–09:20 RTu1B — 24ABC: *Self-Interference Cancellation Techniques*

08:00–09:40 RTu1C — 25ABC:

*mm-Wave & Sub-THz Circuits & Systems for Radar Sensing and Metrology*

09:40–10:10 Coffee Break — Exhibition Floor

10:10–11:30 RTu2B — 24ABC: *Emerging Circuits and Systems for Quantum Computing, Quantum Sensing, Photonics, and Built-In Self-Test (BIST) Applications*

10:10–11:30 RTu2C — 25ABC: *Systems for Applications: 5G and SATCOM*

12:00–13:30 RFIC/IMS Joint Panel Session — 32AB:

*AI/ML Based Wireless System Design and Operation — Hope or Hype?*

13:30–14:50 RTu3B — 24ABC: *Advanced Building Blocks for mm-Wave & Beyond*

13:30–14:50 RTu3C — 25ABC: *IoT Transmitter and Sub-THz Power Amplifiers*

15:10–15:40 Coffee Break — Exhibition Floor

15:40–16:40 RTu4C — 25ABC: *Invited Industry Presentations*

# **RFIC Plenary, Reception, and Symposium Showcase**

**Sunday Evening, 11 June 2023**

**San Diego Convention Center**

**17:30–19:00**

**RFIC Plenary**

**Ballroom 20BCD**

**Chair: Donald Y.C. Lie, Texas Tech University**

**Co-Chair: Danilo Manstretta, Università di Pavia**

- 17:30      Welcome Message from General Chair and TPC Chairs  
            Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
- 18:00      *The Roaring 20s: A Renaissance for the Semiconductor Industry?*  
            Todd Younkin, Semiconductor Research Corporation
- 18:30      *Future System-on-Chip for Full Spectrum Utilization from RF to Optics*  
            Mau-Chung Frank Chang, University of California, Los Angeles

**19:00–21:00**

**RFIC Welcoming Reception Featuring Symposium Showcase**

**Sails Pavilion**

The RFIC Interactive Reception starts immediately after the Plenary Session and will highlight the Student Paper Awards finalists, the Industry Paper Awards finalists, and the Systems & Applications Forum in an engaging social and technical evening event with food and drinks. Authors of these showcase papers will present their innovative work, summarized in poster format. Some showcase papers will also offer live demonstrations. You will not want to miss the RFIC Reception! This event is supported by the RFIC Symposium corporate sponsors.



## RFIC Plenary Speaker 1

**Dr. Todd Younkin**  
**President and CEO**  
**Semiconductor Research Corporation**

### ***The Roaring 20s: A Renaissance for the Semiconductor Industry?***

**Abstract:** Dr. Younkin will share his vision for the future of global semiconductor technologies and design, especially those that will enable future RFIC breakthroughs. Dr. Younkin will discuss the status of government investments and opportunities arising from the CHIPS and SCIENCE ACT of 2022, Korea's K-Belt strategy, Europe's CHIPS ACT, and more. Dr. Younkin leads a global research agenda of about \$100M annually, supported by ~3k academic and industrial researchers, 27 international companies, and 3 U.S. government agencies (DARPA, NSF, and NIST). They have defined the opportunities for future compute and communication systems, as outlined by SRC's 2030 Decadal Plan for Semiconductors, and are now working with over 90 organizations to define the semiconductor hardware opportunities that will deliver that required system performance, via the NIST Microelectronic and Advanced Packaging Technologies (MAPT) Roadmap, awarded in April 2022 and scheduled for completion by September 2023.

## **RFIC Plenary Speaker 1 continued...**

### **About Dr. Todd Younkin**

Dr. Todd Younkin is a talented and seasoned executive with more than 20 years of experience in technology innovation. His extensive Research and Development experience spans Intel's 0.18 $\mu$ m to 5 nm nodes with technical contributions in novel materials, nanotechnology, integration, advanced lithography, and integrated photonics. Todd brings a wealth of expertise with strengths in areas such as cultivating relationships with strategic partners, entrepreneurship and investment strategies, technology innovation, operational excellence, and talent management. He has spent much of his career working alongside young minds that are aspiring to influence the ever-changing world of smart and autonomous electronics. He has built programs from the ground up, leveraging his entrepreneurial leadership to drive new business development that has generated multi-millions in funding. He has been a key contributor in introducing new technology advances and starting new global research in the U.S., Europe, and Asia. Dr. Younkin holds a Ph.D. from the California Institute of Technology in Pasadena, California. He completed his Bachelor of Science at the University of Florida in Gainesville, Florida. He aspires to continue to influence the next generation of technology and inventors, bringing ideas and investors together to drive heterogeneous electronic solutions that will deliver a smarter, shared future.

In August of 2020, Dr. Todd Younkin became the President & CEO of SRC. Recently, he engineered, launched, and led all programmatic aspects of the five-year, \$240 million JUMP research initiative. It has six multi-university, multi-disciplinary innovation Centers with 133 faculty, 835 students, and 360 industrial engineering liaisons. It emphasizes the advancement of Computer Science, Electrical Engineering, and Materials to secure continued U.S. thought leadership. Following his appointment, SRC released its 2030 Decadal Plan for Semiconductors, where it identified the five "seismic shifts" shaping the future of information and communication technologies (ICT). Working closely with SIA, SRC called for greatly increased federal investments throughout the decade to establish a smarter pipeline for semiconductor R&D, aligned to SRC's Decadal Plan. This drove and resulted in the passage of the CHIPS and SCIENCE ACT of 2022 on 9 August 2022.

Dr. Todd Younkin is excited by the worldwide call for a renewed investment in semiconductor materials, hardware, and design, as well as the equally important calls for an emphasis on education and workforce development and our need for environmental sustainability. Only by investing in a bright, collective future, will we rise to the meet the opportunities presented by the next industrial revolution.



## RFIC Plenary Speaker 2

**Prof. Mau-Chung Frank Chang**  
**Wintek Chair in Electrical Engineering and**  
**Distinguished Professor of**  
**University of California, Los Angeles**

***Future System-on-Chip for***  
***Full Spectrum Utilization from RF to Optics***

**Abstract:** The ever-increasing bandwidth requirement due to explosively growing 5/6G and AIoT data flows has compelled global commission authorities to release EM-spectra up to millimeterwave (30–300GHz) and even (sub)-millimeter-wave frequency regimes (>300GHz) for massively expanded sensing and network applications. In this talk, we will exemplify novel CMOS embedded technologies and methodologies developed at UCLA to enable System-on-Chip (SoC) realizations for multi-broadband radio, wideband radar, contactless/plastic interconnect, 3D-imaging and gas-phase rotational spectrometry at (sub)-mm-Wave frequencies, including:

- DiCAD (Digitally Controlled Artificial Dielectric), the only proven Digital-to-Permittivity Converter (DPC), embedded in CMOS-switched interconnects that can vary transmission-line permittivity in real-time (up to  $\times 20$  in practice) for (sub)-mm-wave frequency synthesis, direct-frequency modulation and reconfigurable (software defined) radio/radar/spectrometer implementations
- Self-Healing Radio (57–64GHz) with self-diagnosis and self-healing capabilities to secure high performance-yield and counter temperature/process variations & aging effects
- Multiband RF-Interconnect, beyond traditional baseband-only interconnect, to enable contactless and/or plastic waveguide communications up to Terahertz with unprecedented bandwidth, efficiency, dynamic re-configurability & multi-cast capabilities
- Fully integrated frequency synthesizer (PLL) at 560GHz and realized 1st active and passive CMOS imagers at 110GHz; 3-color (349/201/153GHz) and 3D imaging radars for sensing/ranging concealed objects
- Single-chip CMOS heterodyne  $H_2O$ -Detecting Spectrometer at 183 GHz to enable NASA's space exploration missions with reduced mass ( $6.5\times$ ) & power ( $5.5\times$ ) to meet strict payload and energy consumption requirements

We will also address challenges encountered in both design and implementations that may hinder further development of such systems, especially the major shortcomings in silicon technologies with limited dynamic range and power handling capabilities. We therefore propose replacing CMOS n-FET's drain with selectively grown wide bandgap cubic-phase GaN (c-GaN) for  $>10\times$  improved breakdown voltages to secure desired sensing/communication range/coverage with cost-effectiveness.

We also elaborate on the possible growth of multi-wavelength light-emitting sources and detectors directly atop n-FET's c-GaN Drain with various indium contents of InGaN/GaN superlattice for RF-optical combined radio/radar/interconnect applications by creating unprecedented "Photonic System-on-Chip" with full EM-spectrum utilization from RF to optics.



## RFIC Plenary Speaker 2 continued...

### About Prof. Mau-Chung Frank Chang

Dr. Mau-Chung Frank Chang is the Wintek Chair in Electrical Engineering and Distinguished Professor at the University of California, Los Angeles. Prior to joining UCLA, he was the Assistant Director of the High Speed Electronics Laboratory of Rockwell Science Center (1983–1997), Thousand Oaks, California. In this tenure, he led the team to develop and transfer the MOCVD based AlGaAs/GaAs & InGaP/GaAs Heterojunction Bipolar Transistor (HBT) and BiFET (Planar HBT/MESFET) integrated circuit technologies from the research laboratory to production line (later became Skyworks Solutions). The HBT/BiFET productions have grown into multi-billion dollar businesses and dominated the cellphone power amplifier and front-end module markets for the past 30 years (currently exceeding 10 billion units/year and exceeding 50 billion units in the past decade). Throughout his career, his research has focused on the research & development of high-speed semiconductor devices and integrated circuits for radio, radar, imager, spectrometer and interconnect System-on-Chip applications. He invented the multiband, reconfigurable RF-Interconnects for Chip-Multi-Processor (CMP) inter-core communications and inter-chip CPU-to-Memory communications. He and his students were the 1st to demonstrate CMOS active and passive imagers at mm-Wave (100–180GHz) frequencies. His Lab also pioneered the development of self-healing 57–64GHz radio-on-a-chip (DARPA's HEALICS program) with embedded sensors, actuators and self-diagnosis/curing capabilities; and invented the Digitally Controlled Artificial Dielectric (DiCAD) embedded in CMOS technologies to vary transmission-line permittivity in real-time (up to 20× in practice) for realizing reconfigurable multiband/mode radios in (sub)-mm-Wave frequency bands. His UCLA Lab also realized the first CMOS Frequency Synthesizer for Terahertz operation (PLL at 560GHz) and devised the first tri-color CMOS active imager at 180–500GHz based on a Time-Encoded Digital Regenerative Receiver and the first 3-dimensional SAR imaging radar with sub-centimeter range resolution at 144GHz. More recently, his Lab has devised a Reconfigurable Convolution Neuron Network (RCNN) Accelerator for IoT applications, spun-off an Edge-AI startup company Kneron in San Diego, and won IEEE's 2021 Darlington Best Paper Award.

Prof. Chang is a Member of the US National Academy of Engineering, the European Academy of Sciences and Arts, the US National Academy of Inventors, the Academia Sinica of Taiwan, and a Fellow of the IEEE. He was also recognized with the IEEE David Sarnoff Award (2006), IET JJ Thomson Medal for Electronics (2017) and IEEE/RSE James Clerk Maxwell Medal (2023) for his seminal contributions to the heterojunction technology and realizations of (sub)-mm-Wave System-on-Chip with unprecedented bandwidth and re-configurability.

Prof. Chang has published more than 460 peer-reviewed technical papers and 60 US patents in various areas of high speed electronic devices and integrated circuits & systems. During his tenure with UCLA, he has graduated more than 50 Ph.D. students and 100 MS students. He also served as the President of the National Chiao Tung University, Hsinchu, Taiwan (2015–2019).

# The Student Paper Awards Finalists

Chair: François Rivet, University of Bordeaux

Co-Chair: Debopriyo Chowdhury, Broadcom

The RFIC Symposium's Student Paper Award is devised to both encourage student paper submissions to the conference as well as give the authors of the finalists' papers a chance to promote their research work with the conference attendees after the plenary session during reception time. The outstanding student paper finalists listed below were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of TPC judges selected the top three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top-three Student Papers will be announced during the RFIC Plenary Session on 11 June 2023 in San Diego. Each winner will receive a plaque.

*A 112-Gbps, 0.73-pJ/Bit Fully-Integrated O-Band I-Q Optical Receiver in a 45-nm CMOS SOI-Photonic Process*

Ghazal Movaghar, Viviana Arrunategui, Junqian Liu, Aaron Maharry, Clint Schow,  
James F. Buckwalter

University of California, Santa Barbara, USA

RMo1A-1

*A 100-Gb/s 3-m Dual-Band PAM-4 Dielectric Waveguide Link with 1.9 pJ/Bit/m Efficiency in 28-nm CMOS*

Kristof Dens<sup>1</sup>, Joren Vaes<sup>1</sup>, Christian Bluemm<sup>2</sup>, Gabriel Guimaraes<sup>1</sup>, Berke Gungor<sup>1</sup>,  
Changsong Xie<sup>2</sup>, Alexander Dyck<sup>2</sup>, Patrick Reynaert<sup>1</sup>

<sup>1</sup>KU Leuven, Belgium, <sup>2</sup>Huawei Technologies, Germany

RMo1A-3

*A 140GHz Scalable On-Grid 8×8-Element Transmit-Receive Phased-Array with Up/Down Converters and 64QAM/24Gbps Data Rates*

Amr Ahmed, Linjie Li, Minjae Jung, Gabriel M. Rebeiz

University of California, San Diego, USA

RMo2C-2

*A 0.75mW Receiver Front-End for NB-IoT*

Hossein Rahmadian Kooshkaki, Patrick P. Mercier

University of California, San Diego, USA

RMo4B-1

*A 26–40GHz 4-Way Hybrid Parallel-Series Role-Exchange Doherty PA with Broadband Deep Power Back-Off Efficiency Enhancement*

Edward Liu, Hua Wang

ETH Zürich, Switzerland

RMo4C-1

*Mono/Multistatic Mode-Configurable E-Band FMCW Radar Transceiver Module for Drone-Borne Synthetic Aperture Radar*

Kangseop Lee, Sirous Bahrami, Kyunghwan Kim, Jiseul Kim, Seung-Uk Choi, Ho-Jin Song

POSTECH, Korea

RTu1C-2

*A Diamond Quantum Magnetometer Based on a Chip-Integrated 4-Way Transmitter in 130-nm SiGe BiCMOS*

Hadi Lotfi<sup>1</sup>, Michal Kern<sup>1</sup>, Nico Striegler<sup>2</sup>, Thomas Unden<sup>2</sup>, Jochen Scharpf<sup>2</sup>,  
Patrick Schalberger<sup>1</sup>, Ilai Schwartz<sup>2</sup>, Philipp Neumann<sup>2</sup>, Jens Anders<sup>1</sup>

<sup>1</sup>Universität Stuttgart, Germany, <sup>2</sup>NVision Imaging Technologies, Germany  
RTu2B-1

*A D-Band Calibration-Free Passive 360° Phase Shifter with 1.2° RMS Phase Error in 45nm RFSOI*

Mohammadreza Abbasi, Wooram Lee  
Pennsylvania State University, USA  
RTu3B-2

*A D-Band 20.4dBm OP<sub>1dB</sub> Transformer-Based Power Amplifier with 23.6% PAE in a 250-nm InP HBT Technology*

Senne Gielen<sup>1</sup>, Yang Zhang<sup>2</sup>, Mark Ingels<sup>2</sup>, Patrick Reynaert<sup>1</sup>

<sup>1</sup>KU Leuven, Belgium, <sup>2</sup>imec, Belgium  
RTu3C-3

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

# The Industry Paper Awards Finalists

Chair: Debopriyo Chowdhury, Broadcom

Co-Chair: François Rivet, University of Bordeaux

The RFIC Industry Showcase highlights the outstanding industry papers listed below. These papers received nominations for this recognition from the TPC sub-committees and godparents in a double-blind review. From these top papers, a two-stage double-blind review process was conducted by a committee of TPC judges. Finally, the Best Paper Chair and other key Steering Committee members finalize the top three winners after rigorous reviews and discussions. The top three will be displayed on the RFIC website and on a rolling slideshow prior to the RFIC Plenary Session on 11 June 2023 in San Diego. Each winner will receive a plaque and will be recognized in an upcoming Microwave Magazine article.

## *Optimizing RFSOI Performance Through a T-Shaped Gate and Nano-Second Laser Annealing Techniques*

L. Lucci<sup>1</sup>, S. Crémer<sup>2</sup>, B. Duriez<sup>1</sup>, T. Fache<sup>1</sup>, S. Kerdiles<sup>1</sup>, Y. Morand<sup>1</sup>, J.-M. Hartmann<sup>1</sup>,  
J. Azevedo-Goncalves<sup>2</sup>, F. Gaillard<sup>1</sup>, P. Chevalier<sup>2</sup>

<sup>1</sup>CEA-Leti, France, <sup>2</sup>STMicroelectronics, France

RM02A-2

## *A Fast-Startup 80MHz Crystal Oscillator with 96×/368× Startup-Time Reductions for 3.0V/1.2V Swings Based on Un-Interrupted Phase-Aligned Injection*

Chien-Wei Chen, Chao-Ching Hung, Yu-Li Hsueh

MediaTek, Taiwan

RM03A-3

## *Transformer-Coupled 2.5GHz BAW Oscillator with 12.5fs RMS-Jitter and 1-kHz Figure-of-Merit (FOM) of 210dB*

Bichoy Bahr, Sachin Kalia, Baher Haroun, Swaminathan Sankaran

Texas Instruments, USA

RM03A-4

## *A Double Balanced Frequency Doubler Achieving 70% Drain Efficiency and 25% Total Efficiency*

Jesse Moody

Sandia National Laboratories, USA

RM04A-1

## *A Wi-Fi Tri-Band Switchable Transceiver with 57.9fs-RMS-Jitter Frequency Synthesizer, Achieving -42.6dB EVM Floor for EHT320 4096-QAM MCS13 Signal*

Tsung-Ming Chen<sup>1</sup>, Ming-Chung Liu<sup>1</sup>, Pi-An Wu<sup>1</sup>, Wei-Kai Hong<sup>1</sup>, Ting-Wei Liang<sup>1</sup>,  
Wei-Pang Chao<sup>1</sup>, Po-Yu Chang<sup>1</sup>, Yu-Ting Chou<sup>1</sup>, Chien-Wei Chen<sup>1</sup>, Sen-You Liu<sup>1</sup>,  
Chang-Cheng Huang<sup>1</sup>, Hsiu-Hsien Ting<sup>1</sup>, Min-Shun Hsu<sup>1</sup>, Yao-Chi Wang<sup>1</sup>, Chao-Ching Hung<sup>1</sup>,  
Yu-Li Hsueh<sup>1</sup>, Eric Lu<sup>2</sup>, Yuan-Hung Chung<sup>1</sup>, Jing-Hong Conan Zhan<sup>1</sup>

<sup>1</sup>MediaTek, Taiwan, <sup>2</sup>MediaTek, USA

RM04B-3

*A 15.6-GHz Quad-Core VCO with Extended Circular Coil Topology for Both Main and Tail Inductors in 8-nm FinFET Process*

Suoping Hu, Zhiyu Chen, Wanghua Wu, Pei-Yuan Chiang, Zhanjun Bai, Chih-Wei Yao, Sangwon Son  
Samsung, USA  
RTu1A-1

*A 28nm CMOS Dual-Band Concurrent WLAN and Narrow Band Transmitter with On-Chip Feedforward TX-to-TX Interference Cancellation Path for Low Antenna-to-Antenna Isolation in IoT Devices*

Sai-Wang Tam, Alireza Razzaghi, Alden Wong, Sridhar Narravula, Weiwei Xu, Timothy Loo, Akash Kambale, Andrew Liu, Ovidiu Carnu, Yui Lin, Randy Tsang  
NXP Semiconductors, USA  
RTu1B-1

*A 14-nm Low-Cost IF Transceiver IC with Low-Jitter LO and Flexible Calibration Architecture for 5G FR2 Mobile Applications*

Wanghua Wu<sup>1</sup>, Jeiyoun Lee<sup>2</sup>, Pak-Kim Lau<sup>1</sup>, Taeyoung Kang<sup>1</sup>, Kim Kiu Lau<sup>1</sup>, Si-Wook Yoo<sup>1</sup>, Xingliang Zhao<sup>1</sup>, Ashutosh Verma<sup>1</sup>, Ivan Siu-Chuang Lu<sup>1</sup>, Chih-Wei Yao<sup>1</sup>, Hou-Shin Chen<sup>1</sup>, Gennady Feygin<sup>1</sup>, Pranav Dayal<sup>1</sup>, Kee-Bong Song<sup>1</sup>, Sangwon Son<sup>1</sup>  
<sup>1</sup>Samsung, USA, <sup>2</sup>Samsung, Korea  
RTu2C-3

*A 140GHz RF Beamforming Phased-Array Receiver Supporting >20dB IRR with 8GHz Channel Bandwidth at Low IF in 22nm FDSOI CMOS*

Shenggang Dong<sup>1</sup>, Navneet Sharma<sup>1</sup>, Sensen Li<sup>1</sup>, Michael Chen<sup>1</sup>, Xiaohan Zhang<sup>2</sup>, Yaolong Hu<sup>2</sup>, Jiantong Li<sup>1</sup>, Yong Su<sup>1</sup>, Xinguang Xu<sup>1</sup>, Vitali Loseu<sup>1</sup>, Eunyoung Seok<sup>1</sup>, Taiyun Chi<sup>2</sup>, Won-Suk Choi<sup>1</sup>, Gary Xu<sup>1</sup>  
<sup>1</sup>Samsung, USA, <sup>2</sup>Rice University, USA  
RTu3B-3

*A 110–170GHz Phase-Invariant Variable-Gain Power Amplifier Module with 20–22dBm  $P_{sat}$  and 30dBm OIP3 Utilizing SiGe HBT RFICs*

Mustafa Sayginer, Michael Holyoak, Mike Zierdt, Mohamed Elkhoully, Joe Weiner, Yves Baeyens, Shahriar Shahramian  
Nokia Bell Labs, USA  
RTu3C-2

Industry Paper Contest Eligibility: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must present the paper at the symposium.

# **RFIC Reception and Symposium Showcase Featuring Systems & Applications Forum and Best Student/Industry Paper Showcase**

**Systems & Applications Forum Chair: Gernot Hueber, United Micro Technology**

**Student Paper Chair: François Rivet, University of Bordeaux**

**Industry Paper Chair: Debopriyo Chowdhury, Broadcom**

The RFIC Interactive Reception, supported by the RFIC Symposium corporate sponsors, starts immediately after the plenary session and highlights the Student and Industry Paper Awards finalists in an engaging social and technical evening event with food and drinks. Furthermore, additional authors, both from academia and industry who choose to showcase/demo work focused on Systems and Applications, will be present. Authors will present their innovative work on large monitors as electronic posters and some will offer live demonstrations. Make sure to attend this event, where you will be able to network and see a preview of selected paper presentations that you can attend during the two days that follow. The following lists of participants were valid on 1 May 2023.

## *Student Paper Awards Finalists' Showcase/Demonstrations*

*A 112-Gbps, 0.73-pJ/Bit Fully-Integrated O-Band I-Q Optical Receiver in a 45-nm CMOS SOI-Photonic Process*

Ghazal Movaghar, Viviana Arrunategui, Junqian Liu, Aaron Maharry, Clint Schow,

James F. Buckwalter

University of California, Santa Barbara, USA

RM01A-1

*A 100-Gb/s 3-m Dual-Band PAM-4 Dielectric Waveguide Link with 1.9 pJ/Bit/m Efficiency in 28-nm CMOS*

Kristof Dens<sup>1</sup>, Joren Vaes<sup>1</sup>, Christian Bluemm<sup>2</sup>, Gabriel Guimaraes<sup>1</sup>, Berke Gungor<sup>1</sup>,

Changsong Xie<sup>2</sup>, Alexander Dyck<sup>2</sup>, Patrick Reynaert<sup>1</sup>

<sup>1</sup>KU Leuven, Belgium, <sup>2</sup>Huawei Technologies, Germany

RM01A-3

*A 140GHz Scalable On-Grid 8×8-Element Transmit-Receive Phased-Array with Up/Down Converters and 64QAM/24Gbps Data Rates*

Amr Ahmed, Linjie Li, Minjae Jung, Gabriel M. Rebeiz

University of California, San Diego, USA

RM02C-2

*A 0.75mW Receiver Front-End for NB-IoT*

Hossein Rahmadian Kooshkaki, Patrick P. Mercier

University of California, San Diego, USA

RM04B-1



*A 26–40GHz 4-Way Hybrid Parallel-Series Role-Exchange Doherty PA with Broadband Deep Power Back-Off Efficiency Enhancement*  
Edward Liu, Hua Wang  
ETH Zürich, Switzerland  
RMo4C-1

*Mono/Multistatic Mode-Configurable E-Band FMCW Radar Transceiver Module for Drone-Borne Synthetic Aperture Radar*  
Kangseop Lee, Sirous Bahrami, Kyunghwan Kim, Jiseul Kim, Seung-Uk Choi, Ho-Jin Song  
POSTECH, Korea  
RTu1C-2

**DEMO** *A Diamond Quantum Magnetometer Based on a Chip-Integrated 4-Way Transmitter in 130-nm SiGe BiCMOS*  
Hadi Lotfi<sup>1</sup>, Michal Kern<sup>1</sup>, Nico Striegler<sup>2</sup>, Thomas Unden<sup>2</sup>, Jochen Scharpf<sup>2</sup>, Patrick Schalberger<sup>1</sup>, Ilai Schwartz<sup>2</sup>, Philipp Neumann<sup>2</sup>, Jens Anders<sup>1</sup>  
<sup>1</sup>Universität Stuttgart, Germany, <sup>2</sup>NVision Imaging Technologies, Germany  
RTu2B-1

**DEMO** *A D-Band Calibration-Free Passive 360° Phase Shifter with 1.2° RMS Phase Error in 45nm RFSOI*  
Mohammadreza Abbasi, Wooram Lee  
Pennsylvania State University, USA  
RTu3B-2

*A D-Band 20.4dBm OP<sub>1dB</sub> Transformer-Based Power Amplifier with 23.6% PAE in a 250-nm InP HBT Technology*  
Senne Gielen<sup>1</sup>, Yang Zhang<sup>2</sup>, Mark Ingels<sup>2</sup>, Patrick Reynaert<sup>1</sup>  
<sup>1</sup>KU Leuven, Belgium, <sup>2</sup>imec, Belgium  
RTu3C-3

#### Industry Paper Awards Finalists' Showcase/Demonstrations

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L. Lucci<sup>1</sup>, S. Crémer<sup>2</sup>, B. Duriez<sup>1</sup>, T. Fache<sup>1</sup>, S. Kerdiles<sup>1</sup>, Y. Morand<sup>1</sup>, J.-M. Hartmann<sup>1</sup>, J. Azevedo-Goncalves<sup>2</sup>, F. Gaillard<sup>1</sup>, P. Chevalier<sup>2</sup>  
<sup>1</sup>CEA-Leti, France, <sup>2</sup>STMicroelectronics, France  
RMo2A-2

*A Fast-Startup 80MHz Crystal Oscillator with 96×/368× Startup-Time Reductions for 3.0V/1.2V Swings Based on Un-Interrupted Phase-Aligned Injection*  
Chien-Wei Chen, Chao-Ching Hung, Yu-Li Hsueh  
MediaTek, Taiwan  
RMo3A-3

**DEMO** *Transformer-Coupled 2.5GHz BAW Oscillator with 12.5fs RMS-Jitter and 1-kHz Figure-of-Merit (FOM) of 210dB*  
 Bichoy Bahr, Sachin Kalia, Baher Haroun, Swaminathan Sankaran  
 Texas Instruments, USA  
 RMo3A-4

*A Double Balanced Frequency Doubler Achieving 70% Drain Efficiency and 25% Total Efficiency*  
 Jesse Moody  
 Sandia National Laboratories, USA  
 RMo4A-1

*A Wi-Fi Tri-Band Switchable Transceiver with 57.9fs-RMS-Jitter Frequency Synthesizer, Achieving -42.6dB EVM Floor for EHT320 4096-QAM MCS13 Signal*  
 Tsung-Ming Chen<sup>1</sup>, Ming-Chung Liu<sup>1</sup>, Pi-An Wu<sup>1</sup>, Wei-Kai Hong<sup>1</sup>, Ting-Wei Liang<sup>1</sup>, Wei-Pang Chao<sup>1</sup>, Po-Yu Chang<sup>1</sup>, Yu-Ting Chou<sup>1</sup>, Chien-Wei Chen<sup>1</sup>, Sen-You Liu<sup>1</sup>, Chang-Cheng Huang<sup>1</sup>, Hsiu-Hsien Ting<sup>1</sup>, Min-Shun Hsu<sup>1</sup>, Yao-Chi Wang<sup>1</sup>, Chao-Ching Hung<sup>1</sup>, Yu-Li Hsueh<sup>1</sup>, Eric Lu<sup>2</sup>, Yuan-Hung Chung<sup>1</sup>, Jing-Hong Conan Zhan<sup>1</sup>  
<sup>1</sup>MediaTek, Taiwan, <sup>2</sup>MediaTek, USA  
 RMo4B-3

**DEMO** *A 28nm CMOS Dual-Band Concurrent WLAN and Narrow Band Transmitter with On-Chip Feedforward TX-to-TX Interference Cancellation Path for Low Antenna-to-Antenna Isolation in IoT Devices*  
 Sai-Wang Tam, Alireza Razzaghi, Alden Wong, Sridhar Narravula, Weiwei Xu, Timothy Loo, Akash Kambale, Andrew Liu, Ovidiu Carnu, Yui Lin, Randy Tsang  
 NXP Semiconductors, USA  
 RTu1B-1

*A 14-nm Low-Cost IF Transceiver IC with Low-Jitter LO and Flexible Calibration Architecture for 5G FR2 Mobile Applications*  
 Wanghua Wu<sup>1</sup>, Jeiyong Lee<sup>2</sup>, Pak-Kim Lau<sup>1</sup>, Taeyoung Kang<sup>1</sup>, Kim Kiu Lau<sup>1</sup>, Si-Wook Yoo<sup>1</sup>, Xingliang Zhao<sup>1</sup>, Ashutosh Verma<sup>1</sup>, Ivan Siu-Chuang Lu<sup>1</sup>, Chih-Wei Yao<sup>1</sup>, Hou-Shin Chen<sup>1</sup>, Gennady Feygin<sup>1</sup>, Pranav Dayal<sup>1</sup>, Kee-Bong Song<sup>1</sup>, Sangwon Son<sup>1</sup>  
<sup>1</sup>Samsung, USA, <sup>2</sup>Samsung, Korea  
 RTu2C-3

**DEMO** *A 140GHz RF Beamforming Phased-Array Receiver Supporting >20dB IRR with 8GHz Channel Bandwidth at Low IF in 22nm FDSOI CMOS*  
 Shenggang Dong<sup>1</sup>, Navneet Sharma<sup>1</sup>, Sensen Li<sup>1</sup>, Michael Chen<sup>1</sup>, Xiaohan Zhang<sup>2</sup>, Yaolong Hu<sup>2</sup>, Jiantong Li<sup>1</sup>, Yong Su<sup>1</sup>, Xinguang Xu<sup>1</sup>, Vitali Loseu<sup>1</sup>, Eunyoung Seok<sup>1</sup>, Taiyun Chi<sup>2</sup>, Won-Suk Choi<sup>1</sup>, Gary Xu<sup>1</sup>  
<sup>1</sup>Samsung, USA, <sup>2</sup>Rice University, USA  
 RTu3B-3

**DEMO** *A 110–170GHz Phase-Invariant Variable-Gain Power Amplifier Module with 20–22dBm  $P_{sat}$  and 30dBm OIP3 Utilizing SiGe HBT RFICs*  
 Mustafa Sayginer, Michael Holyoak, Mike Zierdt, Mohamed Elkhoully, Joe Weiner, Yves Baeyens, Shahriar Shahramian  
 Nokia Bell Labs, USA  
 RTu3C-2

Systems & Applications Forum Showcase/Demonstrations

*A CMOS 183GHz Millimeter-Wave Spectrometer for Exploring the Origins of Water and Evolution of the Solar System*

Adrian Tang<sup>1</sup>, Mau-Chung Frank Chang<sup>2</sup>, Yanghyo Kim<sup>3</sup>, Goutam Chattopadhyay<sup>1</sup>

<sup>1</sup>JPL, USA, <sup>2</sup>University of California, Los Angeles, USA, <sup>3</sup>Stevens Institute of Technology, USA  
RMo2C-1

*A 57.6Gb/s Wireless Link Based on 26.4dBm EIRP D-Band Transmitter Module and a Channel Bonding Chipset on CMOS 45nm*

Jose Luis Gonzalez-Jimenez, Alexandre Siligaris, Abdelaziz Hamani,  
Francesco Foglia-Manzillo, Pierre Courouve, Nicolas Cassiau, Cedric Dehos, Antonio Clemente  
CEA-Leti, France

RMo2C-3

*A 14.2mW 29–39.3-GHz Two-Stage PLL with a Current-Reuse Coupled Mixer Phase Detector*

Yuan Liang<sup>1</sup>, Chirn Chye Boon<sup>2</sup>, Qian Chen<sup>2</sup>

<sup>1</sup>Guangzhou University, China, <sup>2</sup>NTU, Singapore

RMo3A-1

*A C-Band Compact High-Linearity Multibeam Phased-Array Receiver with Merged Gain-Programmable Phase Shifter Technique*

Jingying Zhou<sup>1</sup>, Nayu Li<sup>1</sup>, Yuxiaozhou Yuan<sup>1</sup>, Huiyan Gao<sup>1</sup>, Shaogang Wang<sup>1</sup>, Hang Lu<sup>1</sup>,  
Chunyi Song<sup>1</sup>, Yen-Cheng Kuan<sup>2</sup>, Qun Jane Gu<sup>3</sup>, Zhiwei Xu<sup>1</sup>

<sup>1</sup>Zhejiang University, China, <sup>2</sup>NYCU, Taiwan, <sup>3</sup>University of California, Davis, USA

RMo4B-2

*A CMOS 160GHz Integrated Permittivity Sensor with Resolution of 0.05%  $\Delta\epsilon_r$*

Hai Yu<sup>1</sup>, Xuan Ding<sup>1</sup>, Jingjun Chen<sup>2</sup>, Sajjad Sabbaghi Saber<sup>1</sup>, Qun Jane Gu<sup>1</sup>

<sup>1</sup>University of California, Davis, USA, <sup>2</sup>Qualcomm, USA

RTu1C-4

*A mm-Wave CMOS/Si-Photonics Hybrid-Integrated Software-Defined Radio Receiver Achieving >80-dB Blocker Rejection of <-10dBm In-Band Blockers*

Ramy Rady, Yu-Lun Luo, Christi Madsen, Samuel Palermo, Kamran Entesari  
Texas A&M University, USA

RTu2B-3

*A Quad-Band RX Phased-Array Receive Beamformer with Two Simultaneous Beams, Polarization Diversity, and 2.1–2.3dB NF for C/X/Ku/Ka-Band SATCOM*

Zhaoxin Hu, Oguz Kazan, Gabriel M. Rebeiz

University of California, San Diego, USA

RTu2C-4

DEMO

*A mm-Wave Blocker-Tolerant Receiver Achieving <4dB NF and -3.5dBm B1dB in 65-nm CMOS*

Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen

Technion, Israel

RTu3B-4

## RFIC Panel Session

Monday, 12 June 2023

12:00–13:30

Ballroom 20A

Panel Sessions Chair: Oren Eliezer, Samsung

### How Soon Will We Become Cyborgs?

*Panel Organizers and Moderators:*

**Alyssa Apsel**, *Cornell University*

**Travis Forbes**, *Sandia National Laboratories*

**Oren Eliezer**, *Samsung*

*Panelists:* **Renaldi Winoto**, *Mojo Vision*

**Carlos Morales**, *Ambiq*

**Larry Larson**, *Brown University*

**J.-C. Chiao**, *Southern Methodist University*

**Gert Cauwenberghs**, *University of California, San Diego*

**Abstract:** Augmented-reality contact lenses, cochlear implants, AI-aided earbuds, and thought-activated prosthetics have already demonstrated the restoration and enhancement of human capabilities, and the incorporation of artificial intelligence (AI) into these technologies can further increase their potential.

This lunchtime panel will host academia researchers and industry pioneers who are developing these technologies, and will debate how they will affect our near and long term lifestyles.

## RFIC/IMS Joint Panel Session

Tuesday, 13 June 2023

12:00–13:30

Room 32AB

Panel Sessions Chairs

RFIC: Oren Eliezer, Samsung

IMS: Nuno Borges Carvalho, Universidade de Aveiro

Ke Wu, Polytechnique Montréal

### AI/ML Based Wireless System Design and Operation – Hope or Hype?

*Panel Organizers and Moderators:*

**Costas Sarris**, *University of Toronto*

**Qi-Jun Zhang**, *Carleton University*

**Bodhisatwa Sadhu**, *IBM T.J. Watson Research Center*

**Oren Eliezer**, *Samsung*

*Panelists:* **Mike Shuo-Wei Chen**, *University of Southern California*

**Anding Zhu**, *University College Dublin*

**Elyse Rosenbaum**, *University of Illinois Urbana-Champaign*

**Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*

**Sadasvan Shankar**, *Stanford University*

**Joonyoung Cho**, *Samsung*

**Abstract:** The use of machine learning (ML), or more broadly, artificial intelligence (AI), has already been demonstrated in a wide range of applications, including even music composition and artistic design.

This lunchtime panel, with both industry and academia experts, will explore how we may harness AI in wireless system design and operation, and will attempt to distinguish hope from hype.

# Student/Industry ChipChat

Tuesday, 13 June 2023

17:00–19:00

**Room 32AB**

Student Paper Chair: François Rivet, University of Bordeaux

## The 3 Things to Start Your Career with a Bang

*Moderators:*

**Travis Forbes**, *Sandia National Laboratories*

**Romane Dumont**, *STMicroelectronics*

*Panelists:*

**Osama Shana'a**, *MediaTek*

**Domine Leenaerts**, *NXP Semiconductors*

**Stefano Pellerano**, *Intel*

**Kevin Tien**, *IBM*

**Ken Barnett**, *GlobalFoundries*

**S.C. Wong**, *RichWave*

**Abstract:** Come and join the RFIC'23 special event customized by and for the students and the industry! A ChipChat and reception, where future leaders meet prominent industry professionals to confess their secrets about their first years in their career. Bring your questions for an open discussion on topics such as the metamorphosis from students to RFIC professionals, negotiation of your first salary and making use of your talent to impact lives, especially yours, and more.

Not enough time to extract all the secrets? Everyone is invited to continue chip-chatting at the RFIC nacho station.



# RFIC Technical Lecture

Sunday, 11 June 2023

12:00–13:20

Ballroom 20A

**Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center**

**Co-Chair: Amin Arbabian, Stanford University**

## Modern Radio Receivers – From WiFi to 5G and Beyond

*Speaker:* **Behzad Razavi**, *Professor, University of California, Los Angeles*



**Abstract:** CMOS radios continue to evolve so as to satisfy the demands of new applications. Below 7 GHz, cellular and WiFi standards have been pushing the performance to support increasingly higher data rates while consuming less power. Such endeavors require novel architectures that also lend themselves to efficient circuit design. In addition, new radios have emerged around 30 GHz for 5G, around 60 GHz for WiGig, around 140 GHz for 6G, and around 300 GHz for sub-terahertz communications. Each of these frequency bands presents interesting and unique challenges, but a unifying principle among them is the need for beamforming.

This presentation deals with recent developments in receiver design for this broad range of applications. We examine the shortcomings of standard direct-conversion architectures and draw concepts from the state of the art to improve their performance. We also contend that heterodyne reception may outperform direct conversion in some cases. We then study beamforming techniques with emphasis on solutions that draw minimal power.

## RFIC Technical Lecture continued...

### About Prof. Behzad Razavi

Behzad Razavi (Fellow, IEEE) received the B.S.E.E. degree from the Sharif University of Technology, Tehran, Iran, in 1985, and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, Stanford, CA, USA, in 1988 and 1992, respectively. He was an Adjunct Professor at Princeton University, Princeton, NJ, USA, from 1992 to 1994, and Stanford University in 1995. He was with AT&T Bell Laboratories, Holmdel, NJ, USA, and Hewlett-Packard Laboratories, Palo Alto, CA, USA, until 1996. Since 1996, he has been an Associate Professor and a Professor of electrical engineering at the University of California at Los Angeles, Los Angeles, CA, USA. He is the author of the book *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998, 2012) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001 and 2016) (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003, and Wiley, 2012), *Design of CMOS Phase-Locked Loops* (Cambridge University Press, 2020), and *Fundamentals of Microelectronics* (Wiley, 2006, 2014, and 2021) (translated to Korean, Portuguese, and Turkish); and an editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996) and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003). His current research interests include wireless and wireline transceivers and data converters. Dr. Razavi is a member of the U.S. National Academy of Engineering and a fellow of the U.S. National Academy of Inventors. He received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the Best Paper Award at the IEEE Custom Integrated Circuits Conference in 1998, the McGraw-Hill First Edition of the Year Award in 2001, the 2012 Donald Pederson Award in Solid-State Circuits, the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, and the CICC Best Invited Paper Award in 2009 and 2012. He was a co-recipient of the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence at the 2001 ISSCC, the 2012 and the 2015 VLSI Circuits Symposium Best Student Paper Awards, and the 2013 CICC Best Paper Award. He was also recognized as one of the top 10 authors in the 50-year history of ISSCC. He was a recipient of the American Society for Engineering Education PSW Teaching Award in 2014 and the 2017 IEEE CAS John Choma Education Award. He served on the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and the VLSI Circuits Symposium from 1998 to 2002. He has also served as a Guest Editor and an Associate Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and International Journal of High Speed Electronics. He served as the founding Editor-in-Chief for the IEEE SOLID-STATE CIRCUITS LETTERS. He has served as an IEEE Distinguished Lecturer.

**Monday, 12 June 2023**

**08:00–09:20**

**23ABC**

**Session RMo1A: Circuits and Systems for  
High-Speed Optical and Wireline Communication**

**Chair: Bahar Jalali Farahani, Cisco, USA**

**Co-Chair: Antoine Frappé, Université de Lille, France**

**RMo1A-1**

**A 112-Gbps, 0.73-pJ/Bit Fully-Integrated O-Band I-Q Optical Receiver in a 45-nm CMOS SOI-Photonic Process**

Ghazal Movaghar, Viviana Arrunategui, Junqian Liu, Aaron Maharry, Clint Schow, James F. Buckwalter; University of California, Santa Barbara, USA

**Abstract:** A 1310-nm (O-band) coherent optical receiver (CORX) is demonstrated with a monolithic electronic/photonic integrated circuit (MEPIC) process for short range optical interconnects. The CORX is designed using a 45-nm CMOS SOI photonic process for quadrature phase shift keying (QPSK) and includes I/Q channels that are characterized up to 56 GBaud (112 Gbps) with FEC-acceptable BER. The receiver achieves 0.73 pJ/bit energy efficiency and, to our knowledge, is the best energy efficiency reported for a coherent optical receiver.

**RMo1A-2**

**A 42.7Gb/s Optical Receiver with Digital CDR in 28nm CMOS**

Hyungryul Kang<sup>1</sup>, Inhyun Kim<sup>1</sup>, Ruida Liu<sup>1</sup>, Ankur Kumar<sup>1</sup>, Il-Min Yi<sup>1</sup>, Yuan Yuan<sup>2</sup>, Zhihong Huang<sup>2</sup>, Samuel Palermo<sup>1</sup>; <sup>1</sup>Texas A&M University, USA, <sup>2</sup>Hewlett Packard Enterprise, USA

**Abstract:** This paper presents a broadband optical receiver that employs multiple bandwidth extension techniques in the analog front-end (AFE) and has efficient digital clock and data recovery (CDR). Total AFE bandwidth is extended by 5.5× with continuous-time linear-equalizer (CTLE) peaking, series inductances between each AFE stage, and active inductors in the CTLE output and variable gain amplifier (VGA) stages. The resolution of a digitally controlled oscillator (DCO) is optimized at 9-bit to balance quantization and random noise-induced jitter from the CDR. Fabricated in 28nm CMOS, the 42.7Gb/s optical receiver achieves an optical modulation amplitude (OMA) sensitivity of -3.6dBm at a bit error rate (BER) < 10<sup>-12</sup>, 10MHz CDR bandwidth, and 3.4pJ/bit energy efficiency.

### **RMo1A-3**

#### **A 100-Gb/s 3-m Dual-Band PAM-4 Dielectric Waveguide Link with 1.9 pJ/Bit/m Efficiency in 28-nm CMOS**

Kristof Dens<sup>1</sup>, Joren Vaes<sup>1</sup>, Christian Bluemm<sup>2</sup>, Gabriel Guimaraes<sup>1</sup>, Berke Gungor<sup>1</sup>, Changsong Xie<sup>2</sup>, Alexander Dyck<sup>2</sup>, Patrick Reynaert<sup>1</sup>; <sup>1</sup>KU Leuven, Belgium, <sup>2</sup>Huawei Technologies, Germany

**Abstract:** This work presents a plastic fiber link in 28-nm CMOS, operating in two adjacent bands centered on 117.5 and 152.5 GHz. Each band supports multi-level (PAM-4) intensity-modulated signaling, which can be detected non-coherently, obviating the need for carrier synchronization. Data rates up to 100 Gb/s are reported for fiber lengths up to 3 m and links up to 11 m are demonstrated at a reduced data rate. A rectification-based detector is proposed to support linear non-coherent demodulation.

### **RMo1A-4**

#### **A 12-Bit 1.1GS/s Single-Channel Pipelined-SAR ADC with Adaptive Inter-Stage Redundancy**

Xianshan Wen, Tao Fu, Ping Gui; Southern Methodist University, USA

**Abstract:** This paper presents a 12-bit single-channel Pipelined-SAR ADC capable of operating at 1.1GS/s. An adaptive inter-stage redundancy scheme is proposed to mitigate the speed overhead caused by inter-stage redundancy bit. A new switching scheme is proposed in the first stage that largely reduces the switching power of the capacitive DAC. Implemented in a 28nm CMOS process, it achieves an SNDR of 60.1dB with power consumption of 8.5mW, corresponding to a Walden FOM of 9.3fJ/conv.-step and a Schreier FOM of 168.2dB.

**Monday, 12 June 2023**

**08:00–09:40**

**24ABC**

**Session RMo1B: Silicon-Based Front-Ends and Building-Blocks**

**Chair: Hao Gao, Technische Universiteit Eindhoven, The Netherlands**

**Co-Chair: Ramesh Harjani, University of Minnesota, USA**

**RMo1B-1**

**A 65nm CMOS Current-Mode Receiver Frontend with Frequency-Translational Noise Cancellation and 425MHz IF Bandwidth**

Benqing Guo<sup>1</sup>, Haishi Wang<sup>1</sup>, Lei Li<sup>2</sup>, Wanting Zhou<sup>2</sup>; <sup>1</sup>CUIT, China, <sup>2</sup>UESTC, China

**Abstract:** An LNA-first receiver frontend including the main/auxiliary paths is proposed. A frequency-translational noise cancellation is attained at the input of a transimpedance amplifier (TIA) shared by the dual paths. The RF input matching is examined, based on an up-conversion of baseband (BB) parasitic. The TIA is customized to provide wideband coverage and high-order filtering. With current mirrors applied to the RF/BB, the presented current-mode frontend has been fabricated in a 65 nm CMOS. Measurements show that the BB bandwidth covers 425 MHz while the  $S_{11} < -10$  dB is maintained up to  $\sim 4.7$  GHz. At typical 2 GHz LO, a 40 dB conversion gain and a 2.2 dB NF are obtained within the passband. The in-band and out-of-band IIP3 linearity are measured with -13 dBm and 14.5 dBm, respectively. The presented circuit core dissipates 44 mW in the signal path and occupies a chip area of 0.52 mm<sup>2</sup>.

**RMo1B-2**

**IIP2-Enhanced Receiver Front-End with Notch-Filtered Low-Noise Transconductance Amplifier for 5G New Radio Cellular Applications**

Donggu Lee, Sukju Yun, Kuduck Kwon; Kangwon National University, Korea

**Abstract:** This study presents an IIP2-enhanced receiver front-end with a notch-filtered low-noise transconductance amplifier (LNTA) for 5G new radio (NR) cellular applications. The LNTA employs a dual-band third-order LC notch filter with a band-switchable differential inductor to reject TX leakages and out-of-band blockers. Consequently, the receiver front-end has enhanced blocker tolerance and satisfies the IIP2 specification with no IIP2 calibration. Fabricated through a 65-nm CMOS process, the receiver front-end was primarily characterized in the low band and mid band of 5G NR. It achieved a noise figure of 3.5 dB, conversion gain of 41.5 dB, out-of-band IIP3 of 2.1 dBm, and calibration-free IIP2 of more than 59 dBm.

**RMo1B-3**

**A Band-Shifting Millimeter-Wave T/R Front-End with Enhanced Imaging and Interference Rejection Covering 5G NR FR2 n257/n258/n259/n260/n261 Bands**

Fuyuan Zhao, Wei Deng, Haikun Jia, Wenjing Ye, Ruichen Wan, Baoyong Chi; Tsinghua University, China

**Abstract:** For achieving multi-band fusion within the fifth-generation (5G) new radio (NR) frequency range 2 (FR2), a band-shifting transmit/receive (T/R) front-ends (FEs) with the reconfigurable auxiliary paths, covering n257/n258/n259/n260/n261, is proposed in this paper. To overcome the deterioration from capacitance-based frequency tuning, an inductance-mutation transformer technique is proposed in the interstage matching of both TX and RX FEs, to enable operation band shifting between low frequency (LF) and high frequency (HF). The proposed transceiver FE chip, composed of a differential power amplifier (PA) with cascade output stage, a two-stage cascade low-noise amplifier (LNA), and a compact dual-resonance T/R switch at antenna interface, is designed and fabricated in standard 28-nm CMOS process. The measured results show the FE can cover 24.25–29.5/37–43.5GHz at LF/HF with enhanced interference and imaging rejection, and realizes <-25 dB EVM for 400 Msym/s 64-QAM wireless communication with >9 dBm average output power in the target band.

## RMo1B-4

### A 6–22GHz CMOS Phase Shifter with Integrated mm-Wave LO

Natan Ershengoren, Eran Socher; Tel Aviv University, Israel

**Abstract:** In this work we propose a new architecture for a wideband phase shifter, based on upconversion and downconversion of the wideband input signal using phase-shifted mm-wave local oscillator (LO) signals. Phase shifting of the LO at a single frequency is achieved using an on-chip quadrature voltage-controlled oscillator (QVCO) and vector modulation (VM). The issue of mixer image band phase shift interference is mitigated using filtering at the mm-wave intermediate frequency (IF). The concept is demonstrated in 65nm CMOS in the design of a 6–22 GHz full 360° phase shifter using a 84 GHz LO and 62–78 GHz IF range. The phase shifter achieves phase error <1.05° and amplitude error <0.2 dB for 7-bit resolution with power consumption of 137 mW (including buffers) and core area of 0.26 mm<sup>2</sup>.

## RMo1B-5

### A 300–320GHz Sliding-IF I/Q Receiver Front-End in 130nm SiGe Technology

Sumit Pratap Singh, Mostafa Jafari Nokandi, Mohammad Hassan Montaseri, Timo Rahkonen, Marko E. Leinonen, Aarno Pärssinen; University of Oulu, Finland

**Abstract:** This paper presents a 300–320 GHz sliding-IF I/Q receiver front-end in 130 nm SiGe BiCMOS technology with  $f/f_{\max}$  of 300 GHz/450 GHz. The architecture, unlike direct conversion receiver at sub-THz/THz frequency range, removes the need of LO frequency same as carrier frequency. Consequently, power consumption of the LO chain is significantly reduced. Signal amplification is performed at IF stage. LO frequency at two-third and one-third of carrier frequency is generated, from external 50 GHz LO signal, using on-chip frequency doublers for RF and I/Q mixers, respectively. The receiver provides 15.2 dB of conversion gain at 310 GHz. The 3-dB RF and BB bandwidths are measured to be 26 GHz and 8 GHz, respectively. Input referred compression point (ICP) and SSB noise figure of the receiver are measured to be -17 dBm and 29.5 dB, respectively. RF and LO chain of the receiver consume 296 mW and 110 mW, respectively.



**Monday, 12 June 2023**

**08:00–09:20**

**25ABC**

**Session RMo1C: 5G & mm-Wave Transceivers and Beamforming ICs**

**Chair: Hongtao Xu, Fudan University, China**

**Co-Chair: Gernot Hueber, United Micro Technology, Austria**

**RMo1C-1**

**A V-Band Four-Channel Phased Array Transmitter Beamforming IC with 0.7-Degree Phase Step in 20dB Dynamic Range**

Cheol So, Eun-Taek Sung, Songcheol Hong; KAIST, Korea

**Abstract:** This paper presents a V-band 4-channel transmitter beamforming IC fabricated in 28-nm CMOS process, which includes power amplifiers (PA), active vector modulators, and power dividers. The PA is linearized by a cold-FET controlled coupled inductor, improving the AM-AM and AM-PM. The vector modulator consists of a summing amplifier that combines I and Q vectors to determine the amplitude and phase of a synthesized signal, along with an active I/Q generator. The nonlinearity of the vector summing amplifier is overcome by introducing a CLC network of a 45° phase shifter. It shows the 0.1 dB RMS gain and 2° RMS phase error at 60 GHz, with 3-bit gain and 9-bit phase control. An OP1dB of 10.8 dBm and a peak gain of 14.3 dB are achieved in the 3-dB frequency bandwidth of 57 GHz to 63.3 GHz. The chip area is 4.4 mm<sup>2</sup>, and the power consumption is 295 mW.

**RMo1C-2**

**A 28/37GHz Frequency Reconfigurable Dual-Band Beamforming Front-End IC for 5G NR**

Jaehun Lee<sup>1</sup>, Hyoungkyu Jin<sup>1</sup>, Gyuha Lee<sup>1</sup>, Eun-Taek Sung<sup>2</sup>, Songcheol Hong<sup>1</sup>; <sup>1</sup>KAIST, Korea, <sup>2</sup>Samsung, Korea

**Abstract:** A 28/37 GHz frequency reconfigurable dual-band beamforming front-end IC is presented. It integrates frequency reconfigurable structures in a power amplifier and a vector-summing type phase shifter to cover widely separated dual frequency bands with a single front-end IC. A wideband variable-gain low-noise amplifier and switches are also included to cover the dual bands. It has a 6-bit phase control resolution and a 16 dB gain control range with 0.9° and 0.62° RMS phase errors at 28 and 37 GHz, respectively. It achieves 13.5 and 13.5 dBm 1-dB compressed output power, 15.5% and 14.1% transmitter efficiency, and a noise figure of 4.4 and 4.9 dB at 28 and 37 GHz, respectively. The front-end IC delivers linear output power of 9.3 and 8.6 dBm with a 64-quadrature amplitude modulation 200 MHz signal at 28 and 37 GHz, respectively.

### **RMo1C-3**

#### **A 26.5-GHz 4×2 Array Switched Beam-Former Based on 2-D Butler Matrix for 5G Mobile Applications in 28-nm CMOS**

Youngjoo Lee, Juwon Kim, Sungwon Kwon, Bosung Suh, Jun Hwang, Kyutae Park, Dohoon Chun, Kyujong Choi, Hongseok Choi, Dongho Yoo, Byung-Wook Min; Yonsei University, Korea

**Abstract:** This paper demonstrates a 26.5-GHz 2-D Butler matrix based 4×2 array switched beam-former. By using a 2-D Butler matrix, feed lines between IC and antennas are uniform, which is a critical problem in an integrated Butler matrix for a 1-D array since it requires complex phase matched routing on PCB. A proposed switched beam-former consists of a signal distribution IC and two switched beam-former ICs. Reconfigurable switches with a function of power divider/combiner are integrated for additional beam patterns. The proposed switched beam-former can generate total 22 beams, which cover a whole scan angle with a low gain variation. Measured beam patterns show that the proposed switched beam-former can cover any 3-D spatial angle of  $\pm 44^\circ$  in azimuth and  $\pm 43^\circ$  in elevation even with a low spatial beam resolution. To our knowledge, this is the first 2-D array switched beam-former based on the Butler matrix in millimeter wave bands.

### **RMo1C-4**

#### **A Phased-Array Receiver Front-End Using a Compact High Off-Impedance T/R Switch for n257/n258/n261 5G FR2 Cellular**

Ying Chen, Xiaohua Yu, Samrat Dey, Venumadhav Bhagavatula, Chechun Kuo, Tienyu Chang, Ivan Siu-Chuang Lu, Sangwon Son; Samsung, USA

**Abstract:** This paper presents a low-power and compact phased-array receiver (RX) front-end (FE) in 28nm CMOS FD-SOI for n257/n258/n261 5G FR2 cellular applications. A compact high off-impedance SPST T/R switch with an embedded 2-bit 18dB variable attenuator is proposed to minimize TX degradation while maintaining a low insertion loss with additional gain control for RX. With the T/R switch and PA output matching network (OMN), the TX/RX interface is co-optimized for TX output power and RX NF. Over the frequency band of 24.25–29.5GHz the RXFE achieves measured RX NF of 4.4–5.6dB with  $\sim 41$ dB gain control range and  $\sim 35$ dB IP1dB range. The RXFE occupies a small die area of 0.14mm<sup>2</sup>. The RX operation consumes only 13.4mW and 4.7mW DC power in sensitivity mode and low-gain/high-linearity mode respectively.

**Monday, 12 June 2023**

**10:10–11:30**

**23ABC**

**Session RMo2A:**

**GaN Modeling, RFSOI Device and Chip Layout Automation**

**Chair: Alvin Joseph, GlobalFoundries, USA**

**Co-Chair: Renyuan Wang, BAE Systems, USA**

### **RMo2A-1**

#### **Exploration of Design/Layout Tradeoffs for RF Circuits Using ALIGN**

Jitesh Poojary, Ramprasad S., Sachin S. Sapatnekar, Ramesh Harjani; University of Minnesota Twin Cities, USA

**Abstract:** The extended manual layout process for RF and analog/mixed-signal design restricts design space exploration and limits design productivity. This work demonstrates the efficacy of an automated layout generator versus a manual approach using a state-of-the-art MIMO receiver. Multiple smaller floorplans of the layout are generated automatically in hours compared to weeks for a single manual layout. Measured results from an automatically generated layout fabricated in TSMC 65nm CMOS show performance numbers comparable to the manual design. Measured in-band/in-notch IIP<sub>3</sub> and out-of-band/in-notch IIP<sub>3</sub> are 18.3dBm and 23.64dBm, respectively.

### **RMo2A-2**

#### **Optimizing RFSOI Performance Through a T-Shaped Gate and Nano-Second Laser Annealing Techniques**

L. Lucci<sup>1</sup>, S. Crémer<sup>2</sup>, B. Duriez<sup>1</sup>, T. Fache<sup>1</sup>, S. Kerdiles<sup>1</sup>, Y. Morand<sup>1</sup>, J.-M. Hartmann<sup>1</sup>, J. Azevedo-Goncalves<sup>2</sup>, F. Gaillard<sup>1</sup>, P. Chevalier<sup>2</sup>; <sup>1</sup>CEA-Leti, France, <sup>2</sup>STMicroelectronics, France

**Abstract:** We report on two experiments that were carried out in order to boost the RF performances of PD-SOI devices. In the first experiment we implemented a T-shaped gate on a nominally 40 nm long device to mimic on an advanced RFSOI platform the mushroom gate shape that is usually found in III-V devices. T-shaped gate more than halved the longitudinal gate resistance improving RF figure-of-merits for long finger devices. In a second experiment we used a nano-second laser anneal of the gate poly-Si layer. The reduction of the vertical component of the gate resistance helped to improve the performances of short finger devices.

## RMo2A-4

### Artificial Neural Networks for GaN HEMT Model Extraction in D-Band Using Sparse Data

Andrea Arias-Purdue, Eythan Lam, Jonathan Tao, Everett O'Malley, James F. Buckwalter; University of California, Santa Barbara, USA

**Abstract:** We describe the application of Artificial Neural Networks (ANNs) for Gallium Nitride (GaN) High-Electron Mobility Transistor (HEMT) model parameter extraction to improve the model accuracy between 110 and 170 GHz. Fully-connected ANNs trained by backpropagation relate the physics-based ASM-HEMT model parameters to RF transistor measurements. The effects of ANN activation function, number of layers, number of nodes and number of training set data points on training accuracy are studied. For the 12 model parameters that dominate the 40-nm GaN HEMT RF characterization, we obtained a combined root-mean-squared (RMS) error of 2.5% between the ANN prediction and the training set, which is acceptable for most design tasks.

## RMo2A-5

### Benchmarking Measurement-Based Large-Signal FET Models for GaN HEMT Devices

Rafael Perez Martinez<sup>1</sup>, Masaya Iwamoto<sup>2</sup>, Jianjun Xu<sup>2</sup>, Philipp Pahl<sup>2</sup>, Srabanti Chowdhury<sup>1</sup>;

<sup>1</sup>Stanford University, USA, <sup>2</sup>Keysight Technologies, USA

**Abstract:** This paper compares the accuracy and attributes of measurement-based large-signal FET models in the context of GaN HEMT modeling. We compare three FET models that have been implemented within PathWave Advanced Design System. In particular, the benefits and drawbacks of using neural networks to model the I-V and Q-V relations in a general way are analyzed. This is done by characterizing a 150 nm gate length  $8 \times 50 \mu\text{m}$  GaN-on-SiC HEMT and extracting the respective FET models based on DC-IV, small-signal, and large-signal data in the device's operating range. The three models are validated and benchmarked at different operating conditions and higher frequencies than their extraction frequency to show how neural network technology can serve as a powerful tool for the accurate modeling of thermal and trapping effects of GaN HEMTs.

**Monday, 12 June 2023**

**10:10–11:30**

**24ABC**

**Session RMo2B: III/V Front-Ends and Building-Blocks**

**Chair: Marcus Granger-Jones, Qorvo, USA**

**Co-Chair: Emanuel Cohen, Technion, Israel**

**RMo2B-1**

**A DC-to-12GHz 1.4–2.5dB IL 4×8 Switch Matrix with Three-Port Reconfigurable Inter-Stage Matching Network**

Zhenyu Wang<sup>1</sup>, Zhaowu Wang<sup>1</sup>, Yicheng Wang<sup>1</sup>, Xiaochen Tang<sup>2</sup>, Yong Wang<sup>1</sup>; <sup>1</sup>UESTC, China, <sup>2</sup>New Mexico State University, USA

**Abstract:** An ultra-wideband low insertion loss (IL) reconfigurable 4×8 switch matrix is proposed in this paper. With the proposed three-port reconfigurable inter-stage matching network and symmetrically-routed structure, the switch matrix breaks the limits between bandwidth (BW), IL, and the number of branches. The proposed switch matrix is fabricated in a commercial 0.25-μm GaN HEMT process and achieves a favourable IL of 1.4–2.5 dB over DC-to-12 GHz. The switch matrix is operated in dual-band mode. In low-band mode (DC-to-5 GHz), isolation is higher than 35 dB and input 1-dB compression is higher than 40.3 dBm; in high-band mode (4-to-12 GHz), isolation is higher than 28 dB and input 1-dB compression is higher than 35 dBm. The core area is 1.5×1.6 mm<sup>2</sup>.

**RMo2B-2**

**A DC-to-18GHz High Power and Low Loss Band-Divided SP3T Switch with Reconfigurable Pole-to-Throw Network in 0.25-μm GaN**

Zhaowu Wang<sup>1</sup>, Yicheng Wang<sup>1</sup>, Zhenyu Wang<sup>1</sup>, Xiaochen Tang<sup>2</sup>, Yong Wang<sup>1</sup>; <sup>1</sup>UESTC, China, <sup>2</sup>New Mexico State University, USA

**Abstract:** A high power and low loss band-divided single-pole three-throw (SP3T) switch is presented in this work. A reconfigurable pole-to-throw network (RPTN) is proposed to minimize insertion loss (IL). The RPTN enables the three throws to operate in different bands, with overlays to each other. Thanks to the RPTN, parasitic of off-state elements can be either bypassed or adsorbed into the filtering networks; transistor sizes in the series-shunt units can be increased to reduce resistive losses since large parasitic capacitances can be either bypassed or absorbed. Fabricated in a 0.25-μm GaN HEMT process, the SP3T shows better than 1.47 dB IL, over 14.6 dB RL, over 20 dB isolation, and 35.2-to-39.8 dBm input 0.1 dB compression point ( $IP_{0.1dB}$ ) in an ultra-wideband from DC to 18 GHz.

## **RMo2B-3**

### **A 4.8–6.4-GHz GaN MMIC Front-End Module with Enhanced Back-Off Efficiency and Compact Size**

Guansheng Lv, Wenhua Chen, Xiaofan Chen, Long Chen, Zhenghe Feng; Tsinghua University, China

**Abstract:** A back-off efficient transmit/receive (T/R) front-end module (FEM) architecture is presented in this paper. On one hand, switchless class-G (SLCG) topology is adopted for power amplifier (PA) to improve the back-off efficiency in TX mode. On the other hand, co-design asymmetric T/R switch scheme is applied to reduce the switch loss in TX path. A 4.8–6.4-GHz FEM is implemented in a 0.15- $\mu\text{m}$  GaN-HEMT process for validation, and the chip size is only 1.45 mm  $\times$  1.6 mm. The TX mode realizes a saturated power of 37.2–38.9 dBm and a 6-dB back-off drain efficiency (DE) of 40.2%–43.4%. Applying a 160-MHz LTE signal with 8.5-dB PAPR, an average DE of 33.3%–37% at an average power of 28.3–30 dBm is measured, and the ACPR is better than -46 dBc after digital predistortion. The RX mode achieves a noise figure of 1.8–2.2 dB and an IIP3 of 20.8–25 dBm.

## **RMo2B-4**

### **A 280GHz InP HBT Direct-Conversion Receiver with 10.8dB NF**

Utku Soyly<sup>1</sup>, Amirreza Alizadeh<sup>1</sup>, Munkyo Seo<sup>2</sup>, Mark J.W. Rodwell<sup>1</sup>; <sup>1</sup>University of California, Santa Barbara, USA, <sup>2</sup>Sungkyunkwan University, Korea

**Abstract:** We report a fully integrated 280 GHz direct-conversion receiver in 250 nm InP HBT technology. The receiver has > 17 dB conversion gain over 264–297 GHz, consumes 455 mW, and has 10.8–11.6 dB DSB noise figure over 261–300 GHz. Its -3 dB bandwidth is 16.5 GHz, while its -6 dB bandwidth is 34.5 GHz. The local oscillator is generated by an internal 8:1 active frequency multiplier. To the authors' knowledge, the IC demonstrates record noise performance for an integrated receiver operating near 280 GHz.

**Monday, 12 June 2023**

**10:10–11:30**

**25ABC**

**Session RMo2C: Systems and Applications at RF and mm-Wave**

**Chair: Mona Mostafa Hella, Rensselaer Polytechnic Institute, USA**

**Co-Chair: Rocco Tam, NXP Semiconductors, USA**

### **RMo2C-1**

#### **A CMOS 183GHz Millimeter-Wave Spectrometer for Exploring the Origins of Water and Evolution of the Solar System**

Adrian Tang<sup>1</sup>, Mau-Chung Frank Chang<sup>2</sup>, Yanghyo Kim<sup>3</sup>, Goutam Chattopadhyay<sup>1</sup>; <sup>1</sup>JPL, USA,

<sup>2</sup>University of California, Los Angeles, USA, <sup>3</sup>Stevens Institute of Technology, USA

**Abstract:** This paper discusses advanced CMOS-based remote sensing emission spectrometers towards measuring the D/H (Deuterium/Hydrogen) ratio throughout the solar system. These isotopic measurements are critical to gain a clearer understanding of the water on Earth and its origins. We briefly review the MIRO instrument aboard the ESA/Rosetta mission, the isotopic measurements performed at a Jovian comet 67P and the challenges they pose to the cometary hypothesis for the origin of water on Earth. We then present the next generation low-cost CMOS-based water sensing spectrometer and describe how it can help address these critical science questions. We discuss design and development of the CMOS spectrometer and its first space test flight aboard the NASA ReckTangLE sub-orbital mission in 2019.

### **RMo2C-2**

#### **A 140GHz Scalable On-Grid 8×8-Element Transmit-Receive Phased-Array with Up/Down Converters and 64QAM/24Gbps Data Rates**

Amr Ahmed, Linjie Li, Minjae Jung, Gabriel M. Rebeiz; University of California, San Diego, USA

**Abstract:** This paper presents a scalable wafer-scale transmit-receive phased array at 140 GHz. The chip is composed of 2-D 8×8 140 GHz channels employing radio-frequency (RF) beamforming with 4-bit phase and gain controls at 135–145 GHz. An up/down-converter (UDC) channel with a ×6 LO chain and an IF of 9–14 GHz is also integrated on the chip. The on-chip RF distribution network is composed of Wilkinson divider/combiner networks, along with line amplifiers (LAs) to provide signal amplification. The chip is fabricated in GlobalFoundries CMOS 45RFSOI technology with an area of 9.84×8.27 mm<sup>2</sup> and is flipped on a low-cost organic RF PCB containing 8×8 patch antenna array placed at 1.07×1.22 mm grid ( $0.5\lambda \times 0.57\lambda$  at 140 GHz). The array can scan  $\pm 60^\circ$  for both transmit and receive operations. The measured TX EIRP is 37.5 dBm at 140 GHz. The measured RX array input 1-dB compression point is -11 dBm with an electronic gain of 20 dB at 140 GHz. The array supports 16/64 QAM operation with up to 24 Gb/s with  $<4\%$  EVM<sub>rms</sub> for both transmit and receive operations. This work presents the first phased-array at 140 GHz with wide-angle scanning and full scalability in the X and Y directions.

## **RMo2C-3**

### **A 57.6Gb/s Wireless Link Based on 26.4dBm EIRP D-Band Transmitter Module and a Channel Bonding Chipset on CMOS 45nm**

Jose Luis Gonzalez-Jimenez, Alexandre Siligaris, Abdelaziz Hamani, Francesco Foglia-Manzillo, Pierre Courouve, Nicolas Cassiau, Cedric Dehos, Antonio Clemente; CEA-Leti, France

**Abstract:** This paper presents a baseband to D-band wireless link based on a transmitter module integrating a 45-nm CMOS channel bonding chipset and a high-gain antenna in PCB technology. The link realized using a commercial receiver at 42 cm achieves a data rate of 57.6 Gb/s using a multi-channel 16-QAM with a transmitting energy efficiency of 27.4 pJ/b.

## **RMo2C-4**

### **A mm-Sized Implantable Glucose Sensor Using a Fluorescent Hydrogel**

Hyeonkeon Lee<sup>1</sup>, Honghyeon Park<sup>2</sup>, Taein Kim<sup>3</sup>, Mi Song Nam<sup>3</sup>, Yun Jung Heo<sup>3</sup>, Sanghoek Kim<sup>3</sup>;

<sup>1</sup>LIG Nex1, Korea, <sup>2</sup>Silicon Mitus, Korea, <sup>3</sup>Kyung Hee University, Korea

**Abstract:** This work proposes a millimeter-sized implantable glucose sensor using a fluorescent hydrogel based on boronic acids. The readout system is configured to provide an efficient wireless power transfer to the implantable sensor at 920-MHz frequency. The 675×959- $\mu\text{m}^2$  die fabricated in 180-nm CMOS consists of a rectifier, a bandgap reference, two regulators, a trans-impedance amplifier, two voltage-controlled ring oscillators, and a digital control with the total power consumption of 150  $\mu\text{W}$ . The die is assembled with a 2.2×2.5-mm<sup>2</sup> antenna on PCB, an off-chip decoupling capacitor, an LED, and a photodiode. When the implantable sensor is surrounded by the fluorescent hydrogel and powered by the reader, the frequency of backscattered signals is encoded with the light intensity of the fluorescent glucose sensor, informing the glucose concentration. The miniaturization of the sensor minimizes the invasiveness, the potential discomfort, and immunity reaction against sensor, making it suitable for a long-term use after the implantation.



**Monday, 12 June 2023**

**13:30–14:50**

**23ABC**

**Session RMo3A:**

**Reference Clock and Frequency Generation Techniques**

**Chair: Salvatore Finocchiaro, Qorvo, USA**

**Co-Chair: Teerachot Siriburanon, University College Dublin, Ireland**

### **RMo3A-1**

#### **A 14.2mW 29–39.3-GHz Two-Stage PLL with a Current-Reuse Coupled Mixer Phase Detector**

Yuan Liang<sup>1</sup>, Chirn Chye Boon<sup>2</sup>, Qian Chen<sup>2</sup>; <sup>1</sup>Guangzhou University, China, <sup>2</sup>NTU, Singapore

**Abstract:** A Ka-band millimeter wave (mmW) integer-N phase-locked loop (PLL) exploiting a novel current-reuse coupled mixer (CRCM) phase detector (PD) is proposed. Aiming to attenuate the reference spurs in the PLL, the CRCM PD is realized by a pair of coupled mixers folded to each other, achieving mutual spur compensation without consuming extra power or narrowing the PLL loop bandwidth. A mmW signal source is constructed by a two-stage PLL followed by a frequency tripler. Realized in a 28 nm CMOS process, the signal source attains a locking range of 29–39.3-GHz, maximum reference spur of -73.7 dBc, and 160.6 fs<sub>rms</sub> integrated jitter (integrated from 1 k to 100 MHz). It consumes 14.2 mW power and occupies an active area of only 0.1 mm<sup>2</sup>, achieving a figure of merit (FoM) of -244.4 dB when using a 150-MHz reference.

### **RMo3A-2**

#### **A Radiation-Hardened by Design 15–22GHz LC-VCO Charge-Pump PLL Achieving -240dB FoM in 22nm FinFET**

David Dolt, Samuel Palermo; Texas A&M University, USA

**Abstract:** This work presents a 15.0–22.0 GHz radiation hardened PLL for space applications designed in a 22nm FinFET process with radiation hardening techniques for single event upset (SEU) mitigation implemented in all key blocks of the PLL. The performance tradeoffs in the VCO, PFD, and CP with regards to the proposed radiation hardening techniques are analyzed and experimentally verified with the PLL characterization yielding a jitter FoM of -240.89dB at 15GHz with -64dB spur levels and heavy ion testing performed at the Texas A&M Cyclotron validating our robust radiation hardened performance across an LET range from 10 to 70 MeV.cm<sup>2</sup>/mg.

### **RMo3A-3**

#### **A Fast-Startup 80MHz Crystal Oscillator with 96×/368× Startup-Time Reductions for 3.0V/1.2V Swings Based on Un-Interrupted Phase-Aligned Injection**

Chien-Wei Chen, Chao-Ching Hung, Yu-Li Hsueh; MediaTek, Taiwan

**Abstract:** This paper presents an 80MHz crystal oscillator with fast-startup capability based on phase-aligned clock injection. The instantaneous phase misalignment due to frequency error is detected in real time without interrupting the injection process. The injection clock's frequency is corrected accordingly and gradually approaches the crystal oscillator's intrinsic oscillation frequency. Very effective start-up acceleration is demonstrated as benchmarked against ideal injections with zero frequency error. A prototype circuit in 55nm CMOS process achieves 96× and 368× startup time reductions for 3.0V and 1.2V target swings, respectively.

### **RMo3A-4**

#### **Transformer-Coupled 2.5GHz BAW Oscillator with 12.5fs RMS-Jitter and 1-kHz Figure-of-Merit (FOM) of 210dB**

Bichoy Bahr, Sachin Kalia, Baher Haroun, Swaminathan Sankaran; Texas Instruments, USA

**Abstract:** This paper reports two high-performance parallel resonance 2.5GHz BAW oscillators in 130nm SiGe BiCMOS technology. The proposed architecture concurrently improves 1kHz-FOM by more than 3.8dB together with jitter, and close-in phase-noise performance over prior works and further extends the state of the art in MEMS oscillator design. The design optimizes multiple transformer windings to step-down the high-Q resonator impedance and gain multiple benefits: i) cross-coupled pair size increase without performance tradeoff, ii) reduction in base swing, non-linearity and, flicker noise up-conversion and iii) low-voltage compatible operation. Resistive degeneration and inductive coupling at the BJT emitter are considered. Both topologies achieves <12.5fs RMS-Jitter. Resistive degeneration achieves 1kHz-FOM of 210dB, while the inductively coupled emitter allows for more robust operation.

**Monday, 12 June 2023**

**13:30–15:10**

**24ABC**

**Session RMo3B: High-Performance mm-Wave Low-Noise Amplifiers**

**Chair: Vadim Issakov, Technische Universität Braunschweig, Germany**

**Co-Chair: Andrea Bevilacqua, Università di Padova, Italy**

**RMo3B-1**

**A mm-Wave Wideband/Reconfigurable LNA Using a 3-Winding Transformer Load in 22-nm CMOS FDSOI**

Mohammad Ghaedi Bardeh, Jierui Fu, Navid Naseh, Jeyanandh Paramesh, Kamran Entesari; Texas A&M University, USA

**Abstract:** A mm-Wave wideband/reconfigurable LNA using a 3-winding transformer load has been implemented in 22-nm CMOS FDSOI technology for 5G applications. The proposed LNA has three stages with the first two stages utilizing a novel 3-winding transformer as a load to provide three parallel paths, one main and two auxiliary paths. The load expands the frequency band of interest in the wideband mode when the main path is active and reconfigures the LNA bandwidth in the reconfigurable mode when either of the auxiliary paths are active. The third stage acts as a buffer. The LNA shows a measured S21 by the peak gain of 32 at 30 GHz and 3-dB bandwidth of 12.6 GHz for the wideband mode and peak gains of 32.4 dB and 33.4 dB at 22 and 29 GHz for 3-dB bandwidths of 5 and 5.3 GHz for two auxiliary paths in the reconfigurable mode, respectively. The measured NF is lower than 4.5 dB for the entire frequency band and measured OP1dB and OIP3 are better than -6 dBm and 2 dBm for the entire frequency band of interest, respectively. The total power consumption of the proposed LNA is 35 mW in each mode of working, and the chip area is  $1155 \mu\text{m} \times 642 \mu\text{m}$  excluding pads.

**RMo3B-2**

**High-Performance Broadband CMOS Low-Noise Amplifier with a Three-Winding Transformer for Broadband Matching**

Joon-Hyung Kim<sup>1</sup>, Jeong-Taek Son<sup>1</sup>, Jung-Taek Lim<sup>1</sup>, Jae-Eun Lee<sup>1</sup>, Jae-Hyeok Song<sup>1</sup>, Min-Seok Baek<sup>1</sup>, Han-Woong Choi<sup>1</sup>, Eun-Gyu Lee<sup>1</sup>, Sunkyu Choi<sup>1</sup>, Chong-Min Lee<sup>2</sup>, Sung-Ku Yeo<sup>2</sup>, Choul-Young Kim<sup>1</sup>; <sup>1</sup>Chungnam National University, Korea, <sup>2</sup>Samsung, Korea

**Abstract:** This study presents a 32-to-46-GHz two-stage low noise amplifier (LNA) with a three-winding transformer-based input matching network. The proposed matching network provides a broadband noise and input matching for the entire operating range without performance degradation. To demonstrate the feasibility of the proposed circuit configuration, the LNA is implemented using a 65-nm bulk complementary metal-oxide-semiconductor (CMOS) process. The measured LNA achieved a gain of > 19.2 dB at 32–46 GHz with a peak of 21.5 dB at 32 and 45 GHz, simultaneously. The minimum noise figure of the fabricated LNA was 2.2 dB at 36.5 GHz, and remains below 3.2 dB across 14 GHz. The input and output return losses were < -10dB from 32 to 45.5 GHz (effective bandwidth). The third-order input intercept (IIP3) point was -7.6 dBm at 38 GHz at the lowest gain when dissipating 22 mA with a 1-V supply voltage.

### RMo3B-3

#### A 28-GHz 12-dBm IIP3 Low-Noise Amplifier Using Source-Sensed Derivative Superposition of Cascode for Full-Duplex Receivers

Jonghoon Myeong, Byung-Wook Min; Yonsei University, Korea

**Abstract:** This paper presents a highly linear CMOS low-noise amplifier (LNA) to handle self-interference in a full-duplex array. This LNA is designed using the derivative-superposition technique and source-sensed cascode topology. The third-order intermodulation (IM3) suppression is performed by applying different biases to each of the two cascode amplifiers. By using a thick-oxide transistor for the auxiliary amplifier, it operates reliably even at high VDD of cascode. The LNA achieves noise figure (NF) of 3.3–4.3 dB, 8.6-dB peak gain, -8-dBm input 1-dB gain compression point (IP1dB) and 12-dBm third-order input intercept point (IIP3) while consuming 14-mA current from 1.8-V supply voltage. The measured results show IM3 suppression of 8 dB depending on whether the auxiliary amplifier is turned on/off for linearization.

### RMo3B-4

#### A SiGe BiCMOS D-Band LNA with Gain Boosted by Local Feedback in Common-Emitter Transistors

Guglielmo De Filippi, Lorenzo Piatto, Andrea Bilato, Andrea Mazzanti; Università di Pavia, Italy

**Abstract:** The performance of silicon amplifiers in D-band is limited by the low gain of transistors operated close to  $f_{\max}$ . Cascode stages, yielding higher gain than a single device, are commonly preferred, but the issue is only partially alleviated. Recognizing that the common-emitter (CE) transistor limits the gain of the cascode, this work investigates the use of a local reactive feedback to trade gain for stability. Feedback shifts the CE into a conditionally-stable operating region, and enables a gain beyond its maximum available gain (MAG). Then, when the CE is combined with a common-base, by properly selecting impedance terminations, the resulting cascode displays unconditional stability with superior gain. The concept is exploited in the design of a D-band LNA in BiCMOS 55nm technology which shows 22.8 dB gain, 130–165 GHz operating frequency and NF down to 5 dB with 40mW power consumption. Measured results compare favorably against state of the art.

## RMo3B-5

### A D-Band to J-Band Low-Noise Amplifier with High Gain-Bandwidth Product in an Advanced 130nm SiGe BiCMOS Technology

Marcel Andree<sup>1</sup>, Janusz Grzyb<sup>1</sup>, Bernd Heinemann<sup>2</sup>, Ullrich Pfeiffer<sup>1</sup>; <sup>1</sup>Bergische Universität Wuppertal, Germany, <sup>2</sup>IHP, Germany

**Abstract:** In this work, a broadband low noise amplifier fabricated in an advanced 130 nm SiGe BiCMOS technology with  $f_t/f_{\max}$  of 470/650 GHz is presented. The amplifier comprises 5 pseudo-differential cascode stages. Double-peak transformer-based matching stages in the first 3 stages are used to achieve high gain and low noise across a large bandwidth. A suitable set of baluns was developed to facilitate on-wafer measurements from 100 GHz to 325 GHz. The amplifier provides a peak small-signal gain of 34.6 dB at 160 GHz and 235 GHz. The 3 dB bandwidth is 131 GHz – 277 GHz. The measured noise figure is between 8.4 dB to 12 dB, including baluns. With the balun losses de-embedded, the amplifier's peak small-signal gain increases to 37 dB and stays above 30 dB from 117 GHz to 285 GHz, while the lowest noise figure is 7.1 dB at 155 GHz. The achieved  $OP_{1dB}$  stays in between 0 dBm – 1 dBm from 150 GHz to 265 GHz. The amplifier consumes 152 mW with a  $V_{cc}$  of 3 V.

**Monday, 12 June 2023**

**13:30–14:50**

**25ABC**

**Session RMo3C:**

**THz & mm-Wave Communication Transceivers & Circuits**

**Chair: Omeed Momeni, University of California, Davis, USA**

**Co-Chair: Hossein Hashemi, University of Southern California, USA**

### **RMo3C-1**

#### **A 0.32-THz 6.6-dBm Single-Chain CW Transmitter Using On-Chip Antenna with 2.65% DC-to-THz Efficiency**

Georg Zachl, Christoph Mangiavillano, Rohish Kumar Reddy Mitta, Tim Schumacher, Harald Pretl, Andreas Stelzer, Johannes Kepler Universität Linz, Austria

**Abstract:** A 0.324-THz multiplier-based ( $\times 16$ ) transmitter with an on-chip patch antenna has been implemented in a 130-nm SiGe:C BiCMOS technology with an  $f_p/f_{\max}$  of 350/450 GHz. Power management and biasing are integrated on-chip for post-silicon optimizations of output power and dc-to-THz efficiency. Each circuit block can be programmed over a serial peripheral interface for bias current. Three individually programmable low-dropout voltage regulators supply the  $\times 8$  20-to-160-GHz multiplier chain, the two-stage 160-GHz power amplifier, and the 0.32-THz frequency doubler, respectively. Measurements after optimization reveal a dc-to-THz efficiency of 2.65% with an output power of 6.6dBm and a dc power consumption of 170mW operating at 0.324 THz.

### **RMo3C-2**

#### **A 26-Gb/s 140-GHz OOK CMOS Transmitter and Receiver Chipset for High-Speed Proximity Wireless Communication**

Qiyu Peng<sup>1</sup>, Haikun Jia<sup>1</sup>, Ran Fang<sup>2</sup>, Pingda Guan<sup>1</sup>, Mingxing Deng<sup>1</sup>, Jiamin Xue<sup>1</sup>, Wei Deng<sup>1</sup>, Xin Liang<sup>2</sup>, Baoyong Chi<sup>1</sup>, <sup>1</sup>Tsinghua University, China, <sup>2</sup>BriRadio Technology, China

**Abstract:** This paper presents a high data rate 140-GHz on-off keying (OOK) CMOS transmitter and receiver chipset implemented in 28nm CMOS process for short-range wireless communications. The transmitter comprises a power amplifier (PA), modulator, CML-to-CMOS converter, and a fundamental voltage-controlled oscillator (VCO). The receiver consists of a low-noise amplifier (LNA), demodulator, and a single-ended to differential converting amplifier. Continuous-time linear equalizers (CTLE) are implemented on transmitter and receiver baseband to extend the baseband bandwidth. The proposed chipset is wire-bonded to an on-board Vivaldi antenna and a FR4 PCB carrier board to reduce the system cost. Despite the low-cost packaging, it demonstrates measured 26-Gb/s and 17-Gb/s error-free ( $\text{BER} < 10^{-12}$ ) wireless OOK links at 1 cm and 5 cm distance, respectively. The transmitter and receiver consume 99 mW and 63 mW power consumption, respectively.

### RMo3C-3

#### A 189GHz Three-Stage Super-Gain-Boosted Amplifier with Power Gain of 10.7dB/Stage at Near- $f_{\max}$ Frequencies in 65nm CMOS

Fei He, Menghu Ni, Qian Xie, Zheng Wang; UESTC, China

**Abstract:** In this paper, a 189GHz three-stage super-gain boosted amplifier with power gain of 10.7dB/stage in 65nm CMOS is presented. Based on the U-boosted core and Y/Z-embedding network, a super-gain-boosting technique is proposed to improve the power gain of amplifier at near- $f_{\max}$  frequency. The cross-conductance technique is analyzed and exhibits the potential to improve the mason's U of an active two port network leading to the further improvement of the theoretical upper limit of the maximum available gain ( $G_{\max}$ ). Furthermore, by employing the sensitized inductor, the sensitivity to improve mason's U due to the process variations and modeling errors can be decreased. On top of the U-boosted core, additional Y/Z-embedding networks are employed to make  $G_{\max}$  reach the boosted  $G_{\max\_upper\_limit}$ . Based on the proposed super-gain-boosting technique, a three-stage amplifier is implemented in 65nm CMOS process, exhibits a peak small-signal gain of 32.1dB and a saturated power of -1.96dBm at 189GHz.

### RMo3C-4

#### A Fully Integrated 400GHz OOK Transceiver with On-Chip Antenna in 90nm SiGe BiCMOS for Multi Gbps Wireless Communication

Sidharth Thomas, Sam Razavian, Aydin Babakhani; University of California, Los Angeles, USA

**Abstract:** This paper demonstrates a fully integrated 400 GHz OOK transceiver in 90nm SiGe BiCMOS. The transmitter employs a PIN diode quadrupler driven by an on-chip oscillator to generate a 0.4 THz signal, which is modulated with OOK data. The receiver employs a fundamentally driven passive mixer-first architecture. The LO for this mixer is generated from two mutually locked PIN diode quadruplers, which generate sufficient power at 0.4 THz to demonstrate fundamental mixing. The transmitter has an EIRP of 17 dBm and consumes 80 mW DC power. The receiver has 25 dB noise figure, 17.3 dB conversion gain, and consumes 184 mW DC power. The transmitter achieves a data rate of 8 Gbps at 20 cm distance and 1 Gbps at 85 cm distance. The transmitter-receiver system achieves 2 Gbps at 20 cm distance. This is the first demonstration of a fully integrated multi-Gbps wireless transceiver above 300 GHz in silicon.

**Monday, 12 June 2023**

**15:40–17:00**

**23ABC**

**Session RMo4A: CMOS mm-Wave Frequency Multipliers**

**Chair: Andrea Mazzanti, Università di Pavia, Italy**

**Co-Chair: Foster Dai, Auburn University, USA**

**RMo4A-1**

**A Double Balanced Frequency Doubler Achieving 70% Drain Efficiency and 25% Total Efficiency**

Jesse Moody; Sandia National Laboratories, USA

**Abstract:** This work presents a compact double-balanced frequency doubler achieving better than 70% drain and 25% total power efficiency. Complementary NMOS and PMOS devices enable a truly double-balanced frequency doubler. This work's complementary current reuse structure implements voltage scaling in the device. Voltage scaling enables each device to operate at half the effective supply voltage improving efficiency. The stacked design with inverted NMOS and PMOS positions allows deep class C biasing for an effective VGS of negative 0.5V without on-chip negative voltage generation. These techniques enable a high-efficiency frequency doubler, showing nearly 3× higher drain efficiency and 25% higher total efficiency than previously published frequency doublers. This device offers almost 60% higher efficiency than devices without active second harmonic gain. This work also shows wide-band operation with over 23GHz RF BW and excellent output power of 9.8dBm. Implemented in a commercial 45nm SOI technology, this device presents one of the smallest area consumptions in the literature thanks to the complementary current reuse implementation.

**RMo4A-2**

**A 47GHz to 70GHz Frequency Doubler Exploiting 2<sup>nd</sup>-Harmonic Feedback with 10.1dBm  $P_{\text{sat}}$  and  $\eta_{\text{total}}$  of 22% in 65nm CMOS**

Amin Aghighi, Mostafa Essawy, Arun Natarajan; Oregon State University, USA

**Abstract:** A wideband millimeter wave (mm-wave) frequency doubler (FDB) architecture is proposed, where a feedback network is employed to increase the 2<sup>nd</sup>-harmonic signal at the output. Unlike traditional approaches where the 2<sup>nd</sup>-harmonic is nulled at the input, common-mode/differential-mode signals are exploited to create frequency-dependent networks at  $f_0$  and  $2f_0$ . The stand-alone FDB in 65-nm CMOS achieves a saturated output power ( $P_{\text{sat}}$ ) of >10.1 dBm. A wideband power amplifier (PA) follows the FDB to achieve a total  $P_{\text{sat}}$  of 15dBm with a maximum DC-to-RF efficiency ( $\eta_{\text{total}}$ ) of 24.5%, demonstrating the applicability of the FDB for mm-wave radar.



### RMo4A-3

#### A 91.9–113.2GHz Compact Frequency Tripler with 44.6dBc Peak Fundamental Harmonic-Rejection-Ratio Using Embedded Notch-Filters and Area-Efficient Matching Network in 65nm CMOS

Xiangrong Huang, Haikun Jia, Wei Deng, Zhihua Wang, Baoyong Chi; Tsinghua University, China

**Abstract:** This article presents a W-band mixer-based frequency tripler. The folded four-coil transformer is proposed to achieve the input matching and input power distribution to the push-push frequency doubler and the mixer simultaneously. The mixer mixes the second-harmonic current with the input fundamental harmonic to obtain the third harmonic. A single-stage class-AB amplifier follows to drive the output load. The fundamental harmonic notch-filters composed of parallel inductor and capacitance tanks are embedded into the interstage and output matching networks to save the chip area and improve the harmonic-rejection-ratio (HRR). The proposed frequency tripler has been fabricated in 65nm CMOS process with a  $160\text{ }\mu\text{m} \times 420\text{ }\mu\text{m}$  core chip area. Measurement results show a conversion gain of -2.35 dB, a 44.6 dBc peak fundamental HRR and a 3.88% DC-RF efficiency for an input power of 6 dBm at 102 GHz. The measured output 3 dB bandwidth is 91.9–113.2 GHz.

### RMo4A-4

#### A Compact 70–86GHz Bandwidth Frequency Quadrupler with Transformer-Based Harmonic Reflectors in 28nm CMOS

Paolo Ricco<sup>1</sup>, Gianfranco Avitabile<sup>2</sup>, Danilo Manstretta<sup>1</sup>; <sup>1</sup>Università di Pavia, Italy, <sup>2</sup>Politecnico di Bari, Italy

**Abstract:** A frequency quadrupler based on cascaded push-push frequency doublers is presented in this work. Push-push frequency doublers suffer from limited power efficiency and conversion gain, mainly due to second-harmonic feedback. Conventional harmonic reflectors minimize this undesired feedback introducing a common-mode second-harmonic resonance, at the price of increased area and reduced bandwidth. In this design the harmonic reflector is embedded into the input matching network, resulting in a more compact design. The coupling coefficient between the multiple windings of the transformer secondary is used to decouple the differential-mode inductance from the common-mode inductance, that acts as a wideband harmonic reflector. A common-gate transistor is stacked with the push-push pair to further boost the output power while reusing the same current. Two push-push frequency doublers are cascaded without additional power amplification stages. The quadrupler, implemented in 28nm CMOS, achieves a peak output power of 0 dBm and peak power efficiency of 5% at 77 GHz and the 3-dB bandwidth is from 70 to 86 GHz.

**Monday, 12 June 2023**

**15:40–16:40**

**24ABC**

**Session RMo4B: Advances in NB-IoT and WiFi Radios**

**Chair: Arun Paidimarri, IBM T.J. Watson Research Center, USA**

**Co-Chair: Roxann Broughton-Blanchard, Analog Devices, USA**

**RMo4B-1**

**A 0.75mW Receiver Front-End for NB-IoT**

Hossein Rahmanian Kooshkaki, Patrick P. Mercier; University of California, San Diego, USA

**Abstract:** This paper presents a sub-mW receiver front-end for Narrowband IoT (NB-IoT) applications. A low-power low noise amplifier (LNA) provides a sub-3dB minimum noise figure (NF) using a transformer with a turns ratio of less than 1 and further improves the linearity and NF using a local feedback and derivative superposition techniques, without any power overhead. Mathematical expressions are presented to enable an optimum choice of a small head resistor in a low-power class-D voltage-controlled oscillator to improve the phase noise and reduce power consumption. A feed-forward technique is proposed in a baseband amplifier to increase gain and reduce the input-referred noise while maintaining linearity. Measurement results of a prototype fabricated in a 65nm CMOS process achieved a sensitivity of -110dBm and an  $IIP_3$  of -5dBm, which meet NB-IoT requirements, all while dissipating 0.75mW.

**RMo4B-2**

**A C-Band Compact High-Linearity Multibeam Phased-Array Receiver with Merged Gain-Programmable Phase Shifter Technique**

Jingying Zhou<sup>1</sup>, Nayu Li<sup>1</sup>, Yuexiaozhou Yuan<sup>1</sup>, Huiyan Gao<sup>1</sup>, Shaogang Wang<sup>1</sup>, Hang Lu<sup>1</sup>, Chunyi Song<sup>1</sup>, Yen-Cheng Kuan<sup>2</sup>, Qun Jane Gu<sup>3</sup>, Zhiwei Xu<sup>1</sup>; <sup>1</sup>Zhejiang University, China, <sup>2</sup>NYCU, Taiwan, <sup>3</sup>University of California, Davis, USA

**Abstract:** This paper presents a C-band four-element eight-beam phased-array receiver. By utilizing the proposed merged gain-programmable phase shifter (GPS) technique, the chip achieves a 360° phase-shifting range with <2.4° rms phase error and a 20.5-dB gain range with <0.18 dB rms amplitude error at 4.5–7 GHz. The chip demonstrates a 23.5-dB gain and a 6.5-dB noise figure (NF) at 5 GHz. By utilizing the multigated transistor (MGTR) technique, the receiver realizes a -10.8-dBm input 1-dB gain compression point ( $IP_{1dB}$ ) and a -4.7-dBm input third-order intercept point ( $IIP_3$ ) at 5.5 GHz. The proposed receiver occupies  $6.4 \times 3.1 \text{ mm}^2$  area and consumes 1265 mW, which achieves a state-of-the-art number of concurrent reconfigurable beams and an excellent linearity among silicon-based beamformers.

## RMo4B-3

### A Wi-Fi Tri-Band Switchable Transceiver with 57.9fs-RMS-Jitter Frequency Synthesizer, Achieving -42.6dB EVM Floor for EHT320 4096-QAM MCS13 Signal

Tsung-Ming Chen<sup>1</sup>, Ming-Chung Liu<sup>1</sup>, Pi-An Wu<sup>1</sup>, Wei-Kai Hong<sup>1</sup>, Ting-Wei Liang<sup>1</sup>, Wei-Pang Chao<sup>1</sup>, Po-Yu Chang<sup>1</sup>, Yu-Ting Chou<sup>1</sup>, Chien-Wei Chen<sup>1</sup>, Sen-You Liu<sup>1</sup>, Chang-Cheng Huang<sup>1</sup>, Hsiu-Hsien Ting<sup>1</sup>, Min-Shun Hsu<sup>1</sup>, Yao-Chi Wang<sup>1</sup>, Chao-Ching Hung<sup>1</sup>, Yu-Li Hsueh<sup>1</sup>, Eric Lu<sup>2</sup>, Yuan-Hung Chung<sup>1</sup>, Jing-Hong Conan Zhan<sup>1</sup>; <sup>1</sup>MediaTek, Taiwan, <sup>2</sup>MediaTek, USA

**Abstract:** This paper presents a Wi-Fi RF transceiver with a 2.4GHz/5GHz/6GHz tri-band switchable design. To support the wide 320MHz channel BW for Wi-Fi 7, the RF LC-tank response and TXLPF drooping are compensated via a proposed TX flatness calibration scheme that flattens the amplitude difference over the 320MHz signal bandwidth and improves the EVM over each sub-carrier. This work also proposes a reset-pulse XO design to significantly reduce the XO phase noise. A VCO pushing compensation and calibration technique is developed to suppress the sensitivity to LDO noise and DC-DC spurs. The integrated PLL RMS jitter is 57.9fs at 7.115GHz. The measured TX EVM floor achieves -42.6dB at 0dBm output power with EHT320 4096-QAM signals. This RF Transceiver occupies 3.74mm<sup>2</sup> in 55nm CMOS technology.

**Monday, 12 June 2023**

**15:40–17:00**

**25ABC**

**Session RMo4C:**

**High-Efficiency and Linear 5G mm-Wave Power Amplifiers**

**Chair: Debopriyo Chowdhury, Broadcom, USA**

**Co-Chair: Patrick Reynaert, KU Leuven, Belgium**

### **RMo4C-1**

#### **A 26–40GHz 4-Way Hybrid Parallel-Series Role-Exchange Doherty PA with Broadband Deep Power Back-Off Efficiency Enhancement**

Edward Liu, Hua Wang; ETH Zürich, Switzerland

**Abstract:** This paper presents a hybrid parallel-series Doherty power amplifier (PA) architecture that supports broadband operation and deep power back-off (PBO) efficiency enhancement to support next-generation wireless communication. The architecture builds on hybrid use of broadband parallel- and series-type coupled-line Doherty power combiners with four PA paths. The wide carrier bandwidth is achieved by exploiting different frequency dependent active load-modulations of the parallel/series Doherty combiners and PA path biasing reconfigurations, while the deep PBO is realized by the optimum turn-on sequences of the four PA paths. As a proof-of-concept design, a 26–40 GHz PA is implemented in GlobalFoundries 45nm CMOS SOI process. The PA measures 22.5–23.9 dBm OP<sub>1dB</sub>, 26.2–38.2% PAE<sub>OP1dB</sub>, 18.1–34.5% PAE<sub>6dB PBO</sub>, and 10.7–22.1% PAE<sub>12dB PBO</sub>. Note the PBO levels are referenced from OP<sub>1dB</sub>. Compared to a normalized ideal class B PA, this design achieves 1.3–1.8× PAE boost at 6dB PBO, and 1.6–2.3× boost at 12dB PBO. With a 250MSym/s 64-QAM signal, this PA achieves 16.1 dBm P<sub>ave</sub> and PAE<sub>ave</sub> of 30.7% at an EVM<sub>rms</sub> of -25.3 dB. With a 100MSym/s 256-QAM signal, this PA achieves P<sub>ave</sub> of 13.5 dBm and PAE<sub>ave</sub> of 26.2% at an EVM<sub>rms</sub> of -31.3 dB.

### **RMo4C-2**

#### **A 26GHz Balun-First Three-Way Doherty PA in 40nm CMOS with 20.7dBm Psat and 20dB Power Gain**

Anil Kumar Kumaran<sup>1</sup>, Masoud Pashaeifar<sup>1</sup>, Hossein Mashad Nemati<sup>2</sup>, Leo C.N. de Vreede<sup>1</sup>, Morteza S. Alavi<sup>1</sup>, <sup>1</sup>Technische Universiteit Delft, The Netherlands, <sup>2</sup>Huawei Technologies, Sweden

**Abstract:** This paper presents a 40nm CMOS mm-wave 3-way Doherty power amplifier (PA) suitable for 5G mm-wave transmitters. It features a bandwidth-enhanced technique using a compact single-supply balun-first 3-way Doherty combiner. The realized front-end with a core area of 0.77mm<sup>2</sup> delivers a peak power/gain of more than 20 dBm/16 dB and a drain efficiency (DE) of better than 15%/22%/33% at 9.5 dB/6 dB/0 dB power back-off across a 24-to-30GHz band. At 26 GHz, it achieves an EVM/ACLR of -23.5 dB/-29.5 dBc for an 800MHz 64-OFDM signal with 9.8dBm average output power and a 15% average DE.

## RMo4C-3

### A 26-GHz Linear Power Amplifier with 20.8-dBm OP1dB Supporting 256-QAM Wideband 5G NR OFDM for 5G Base Station Equipment

Zhilin Chen<sup>1</sup>, Xiyu Wang<sup>2</sup>, Xiaoxiao Ma<sup>1</sup>, Min Lu<sup>1</sup>, Jie Hu<sup>1</sup>, Keqing Ouyang<sup>1</sup>, Zhijun Long<sup>1</sup>;

<sup>1</sup>Sanechips Technology, China, <sup>2</sup>ZTE, China

**Abstract:** This paper presents a high output power and linearity power amplifier (PA) in 65nm CMOS SOI process for 5G communications. A two-way power combining topology with peaking inductive technique is utilized for high output power. Additionally, the PMOS compensate capacitor, second-order harmonic traps and low impedance network are proposed to improve linearity for wideband modulation. The PA achieves a gain of 19 dB at 26 GHz with 3-dB bandwidth from 22.3 GHz to 28.6 GHz. The PA also realizes 20.8 dBm OP1dB and 21.3 dBm Psat with a peak PAE of 26.15% at 26 GHz. In modulation signal test, using a 5G NR 400 MHz 1-CC 64-QAM and 256-QAM OFDM signal, this PA demonstrates 5% and 3% rms error vector magnitude (EVM) with average output power (Pavg) of 15.5 dBm and 14.4 dBm, respectively.

## RMo4C-4

### A 23–30GHz 4-Path Series-Parallel-Combined Class-AB Power Amplifier with 23dBm $P_{sat}$ , 38.5% Peak PAE and 1.3° AM-PM Distortion in 40nm Bulk CMOS

Junjie Gu<sup>1</sup>, Haoqi Qin<sup>1</sup>, Hao Xu<sup>1</sup>, Weitian Liu<sup>1</sup>, Kefeng Han<sup>2</sup>, Rui Yin<sup>1</sup>, Lei Deng<sup>3</sup>, Xiaoliang Shen<sup>3</sup>, Zongming Duan<sup>4</sup>, Hao Gao<sup>5</sup>, Na Yan<sup>1</sup>; <sup>1</sup>Fudan University, China, <sup>2</sup>Jiashan Fudan Institute, China, <sup>3</sup>NICIC, China, <sup>4</sup>ECRIIE, China, <sup>5</sup>Technische Universiteit Eindhoven, The Netherlands

**Abstract:** This paper presents a 4-path series-parallel combined highly-efficient class-AB power amplifier (PA) with broad bandwidth and low AM-PM distortion in CMOS process. Frequency staggered tuning scheme enables a wide passband of 23–30GHz. AM-PM distortion is minimized by utilizing PMOS varactors that mitigate the voltage dependence of transistor intrinsic capacitors and harmonic traps that minimize common-mode voltage swings at the second-harmonic frequency. Complete electromagnetic modeling ensures the proposed PA achieve its full potential. Fabricated in a 40nm CMOS process, the PA achieves 38.5% peak power added efficiency (PAE), 23.0dBm saturated output power ( $P_{sat}$ ) and 20.4dBm output 1-dB compression point ( $P_{1dB}$ ) with 29.5% PAE. The peak PAE is above 35% and  $P_{sat}/P_{1dB}$  remains above 21.5dBm/19.5dBm across 23–30GHz respectively. The minimum normalized AM-PM distortion is less than 1.3° at 26 GHz and remains less than 4.4° across 26–30GHz. Measured EVM/ACLR is below -29dB/-29dBc with 64QAM 5G-NR modulated signal at 28GHz.

**Tuesday, 13 June 2023**

**08:00–09:20**

**23ABC**

**Session RTu1A: RF to THz LO Generation Solutions**

**Chair: Andreia Cathelin, STMicroelectronics, France**

**Co-Chair: Wanghua Wu, Samsung, USA**

**RTu1A-1**

**A 15.6-GHz Quad-Core VCO with Extended Circular Coil Topology for Both Main and Tail Inductors in 8-nm FinFET Process**

Suoping Hu, Zhiyu Chen, Wanghua Wu, Pei-Yuan Chiang, Zhanjun Bai, Chih-Wei Yao, Sangwon Son; Samsung, USA

**Abstract:** Although process scaling has brought numerous benefits in digital circuit design, it is still very challenging to design high-performance RF circuitry in advanced FinFET processes due to the increased flicker noise, reduced supply voltage, and worsened non-linearity. This paper explores the RF oscillator design in an 8-nm FinFET process and presents a quad-core oscillator with an extended circular inductor frame for both the main and tail inductors. Thanks to the extended circular topology, the tail inductance, and its quality factor are significantly increased to provide resonance efficiently at 2<sup>nd</sup>-order harmonic for better flicker noise suppression. Designed and fabricated in an 8-nm FinFET process, this oscillator achieves a record-low PN of -115.4 dBc/Hz at 1-MHz frequency offset and a competitive Figure-of-Merit (FoM) of -185 dBc/Hz at 15.6GHz with a wide tuning range of 30%.

**RTu1A-2**

**A 10.8–14.5GHz 8-Phase 12.5%-Duty-Cycle Non-Overlapping LO Generator with Automatic Phase-and-Duty-Cycle Calibration for 60-GHz 8-Path-Filtering Sub-Sampling Receivers**

Khoi T. Phan, Yang Gao, Howard C. Luong; HKUST, China

**Abstract:** A 10.8–14.5GHz 8-phase 12.5%-duty-cycle non-overlapping LO generator is proposed for 60-GHz 8-path-filtering sub-sampling receivers. A 4-stage ring oscillator is followed by reconfigurable injection-locked-oscillator NOR gates to generate 8-phase 12.5%-duty-cycle signals featuring automatic successive phase calibration and automatic frequency-domain duty-cycle calibration. The generator prototype measures minimum phase errors of  $\sim 0.1^\circ$  and maximum 4<sup>th</sup>-harmonic output power of -5dBm with >30dB improvement while consuming 77.8mW from a 1V supply.

## RTu1A-3

### A 4.4mW Inductorless 2–20GHz Single-Ended to Differential Frequency Doubler in 45nm RFSOI CMOS Technology

A. Meyer<sup>1</sup>, M.L. Leyrer<sup>2</sup>, C. Ziegler<sup>1</sup>, M. Maier<sup>1</sup>, V. Lammert<sup>2</sup>, V. Issakov<sup>1</sup>; <sup>1</sup>Technische Universität Braunschweig, Germany, <sup>2</sup>Infineon Technologies, Germany

**Abstract:** This work presents a miniature inductorless frequency doubler with high fundamental rejection, wide bandwidth, and single-ended to differential conversion. By utilizing an NMOS/PMOS pair with symmetrical loads attached to drain and source terminals, the second harmonic of an input signal is extracted. Fundamental rejection of up to 35 dB and a wide output range of 2 to 20 GHz is shown in measurement. The doubler is implemented in 45nm CMOS RFSOI technology and draws 4.4mW including biasing and buffer stages. The circuit consumes an active area excluding pads of only  $50 \times 70 \mu\text{m}^2$ .

## RTu1A-4

### An Efficient 0.4THz Radiator with 20.6dBm EIRP and 0.2% DC-to-THz Efficiency in 90nm SiGe BiCMOS

Sidharth Thomas, Sam Razavian, Aydin Babakhani; University of California, Los Angeles, USA

**Abstract:** This paper presents an efficient 0.4 THz single-element radiator implemented in 90nm SiGe BiCMOS. It consists of a PIN diode quadrupler, where a mm-wave Colpitts oscillator at 100 GHz drives a PIN diode switching-reactance-multiplier into reverse recovery. Because of this, the PIN diode abruptly switches between two impedance states and produces strong harmonics. Harmonic injection locking is also presented in this work, where two quadrupler cells are mutually interlocked, and their fourth harmonic power at 0.4 THz combines at the antenna. The radiator achieves a peak EIRP of +20.6 dBm and -5.8 dBm radiated power at 398 GHz, with a 10.7% tuning range, and consumes 130 mW DC power. This work has a DC-to-THz generation efficiency of 0.2%, the highest reported efficiency above 320 GHz, and achieves the highest power and EIRP generated by a single-element radiator.

**Tuesday, 13 June 2023**

**08:00–09:20**

**24ABC**

**Session RTu1B: Self-Interference Cancellation Techniques**

**Chair: Jin Zhou, MediaTek, USA**

**Co-Chair: Oren Eliezer, Samsung, USA**

**RTu1B-1**

**A 28nm CMOS Dual-Band Concurrent WLAN and Narrow Band Transmitter with On-Chip Feedforward TX-to-TX Interference Cancellation Path for Low Antenna-to-Antenna Isolation in IoT Devices**

Sai-Wang Tam, Alireza Razzaghi, Alden Wong, Sridhar Narravula, Weiwei Xu, Timothy Loo, Akash Kambale, Andrew Liu, Ovidiu Carnu, Yui Lin, Randy Tsang; NXP Semiconductors, USA

**Abstract:** A dual-band, concurrent 2.4G WLAN and 2.4G narrow band (NB) transmitter (TX) with on-chip feedforward TX-to-TX interference cancellation path for low antenna-to-antenna isolation in IoT devices is proposed. An on-chip cancellation path generates a replica signal of the same magnitude but  $180^\circ$  out-of-phase with respect to the “aggressor” TX signal appeared at the “victim” TX output. With cancellation path properly calibrated, the measured IMD3 product is reduced by 25 dB. Additionally, the maximum output power during concurrent transmission, while meeting the FCC out-of-band emission specification, improves from 10 to 17 dBm across all WLAN channels. With this proposed architecture, the issue of TX-to-TX interference in multi-radio coexistence is finally addressed, opening the door to future high power concurrent multi-band transmitters in reconfigurable IoT devices.

**RTu1B-2**

**A Distributed Cascode Power Amplifier with an Integrated Analog SIC Filter for Full-Duplex Wireless Operation in 65nm CMOS**

Itamar Melamed, Nimrod Ginzberg, Omer Malka, Emanuel Cohen; Technion, Israel

**Abstract:** In this work, we propose a fully integrated transmitter front-end based on a balanced distributed cascode power amplifier and a passive second-order reconfigurable reflective self-interference cancellation (SIC) filter for full-duplex wireless applications. The balanced topology provides inherent passive transmit-receive (TX-RX) isolation complemented by the passive SIC filter, which accounts for the signal, noise, and nonlinearity components of the direct TX-RX leakages and the reflections from a commercial Wi-Fi antenna. A front-end chip prototype fabricated in TSMC's 65 nm CMOS process operating between 5–6 GHz and occupying the area of  $1.2 \text{ mm}^2$  achieves 19.5 dBm  $P_{\text{sat}}$  with 31% peak PAE, 17 dBm OP1dB, and 8–10 dB RX noise figure, along with 40 dB of TX-RX isolation and -30 dB TX EVM at 10 dB power backoff using a 20 MHz Wi-Fi OFDM signal without DPD.



### RTu1B-3

#### Frequency-Domain-Equalization-Based Full-Duplex Receiver with Passive-Frequency-Shifting N-Path Filters Achieving >53dB SI Suppression Across 160MHz BW

Sastry Garimella<sup>1</sup>, Sasank Garikapati<sup>1</sup>, Aravind Nagulu<sup>2</sup>, Igor Kadota<sup>1</sup>, Alfred Davidson<sup>1</sup>, Gil Zussman<sup>1</sup>, Harish Krishnaswamy<sup>1</sup>; <sup>1</sup>Columbia University, USA, <sup>2</sup>Washington University in St. Louis, USA

**Abstract:** Wideband full-duplex (FD) transceivers pose a significant challenge as they require >100dB of self-interference cancellation (SIC) over large bandwidths. This work utilizes (i) a near-zero-power rotary clock-path passive frequency shifting technique for N-path filters while requiring only a single common LO signal across all filters, and (ii) a closed-loop adaptation algorithm to find the optimal configurations of various RF canceler filters using analytical modelling of tap non-idealities caused by frequency shifting and quality factor variations. The FD receiver achieves (i) tunable operation from 200MHz to 1GHz, (ii) wideband SI suppression of up to 53dB across 160MHz BW when operating at 720MHz (4.44× more fractional bandwidth (FBW) compared to [1]), (iii) a power consumption of 1.8mW/DoF (degree of freedom for each tap, almost 2× better than [1]), while (iv) handling TX power of up to +15dBm across an initial circulator isolation of 26dB.

### RTu1B-4

#### A Frequency-Tunable Dual-Path Frequency-Translated Noise-Cancelling Self-Interference Canceller RX with >16dBm SI Power-Handling in 65nm CMOS

Mostafa Essawy, Kareem Rashed, Amin Aghighi, Arun Natarajan; Oregon State University, USA

**Abstract:** A dual-path self-interference (SI) cancellation architecture is presented for high-power SI cancellation (SIC) for simultaneous transmit and receive. The proposed approach breaks SIC trade-offs between operating frequency, SI power and canceller noise/distortion by using a frequency-translated (FT) SI canceller and an auxiliary FT noise-cancelling path that cancels the noise/distortion from the primary canceller. The 65nm CMOS implementation achieves ~45 dB SIC for 12dBm RX SI peak power with only 4 dB NF degradation, blocker-1dB of >16dBm with respect to SI (8× higher than prior work) while operating from 0.5 GHz to 1.3 GHz.

**Tuesday, 13 June 2023**

**08:00–09:40**

**25ABC**

**Session RTu1C: mm-Wave & Sub-THz Circuits & Systems for  
Radar Sensing and Metrology**

**Chair: Zeshan Ahmad, Texas Instruments, USA**

**Co-Chair: Ruonan Han, MIT, USA**

**RTu1C-1**

**High-Linearity 76–81GHz Radar Receiver with an Intermodulation  
Distortion Cancellation and High-Power Limiter**

N. Landsberg<sup>1</sup>, M. Gordon<sup>1</sup>, O. Asaf<sup>1</sup>, N. Weisman<sup>1</sup>, K. Ben-Atar<sup>1</sup>, S. Levin<sup>1</sup>, S. Pellerano<sup>2</sup>, W. Shin<sup>3</sup>, D. Nahmanny<sup>1</sup>; <sup>1</sup>Mobileye, Israel, <sup>2</sup>Intel, USA, <sup>3</sup>Apple, USA

**Abstract:** A highly linear 76–81 GHz direct conversion receiver has been fabricated in a 16 nm FinFet CMOS process for phased array radar applications. The receiver includes a Low Noise Amplifier (LNA), a semi active mixer, a passive filter and a baseband amplifier. A third order intermodulation distortion cancellation technique is implemented in the LNA and it is used to compensate for distortions in the entire receiver. The peak gain of the receiver is 36 dB with Input IP<sub>3</sub> of -8.1 dBm and Noise Figure (NF) of 5.5 dB. The total power consumption of the receiver is 68 mW. To protect the LNA from high input power levels that affect the reliability of the transistors, an innovative limiter circuit is suggested to monitor the operating point of the first stage of the LNA, whereas the mmW signal path is not affected from this monitoring circuitry at tolerable power levels.

**RTu1C-2**

**Mono/Multistatic Mode-Configurable E-Band FMCW Radar Transceiver  
Module for Drone-Borne Synthetic Aperture Radar**

Kangseop Lee, Sirous Bahrami, Kyunghwan Kim, Jiseul Kim, Seung-Uk Choi, Ho-Jin Song;  
POSTECH, Korea

**Abstract:** Drone-borne synthetic aperture radar (SAR) systems are attractive for small and mid-area applications due to easy and temporal deployment capability. In this paper, we present a 77-GHz drone-borne multistatic frequency-modulated continuous-wave radar transceiver (TRX) which enables multiple drones to cooperate for SAR imaging by wirelessly sharing the reference chirp signal between the drones. The TRX can be configured in the monostatic or multistatic (master/slave) mode by integrated RF switches. The antenna module in this work includes microstrip comb-line and planar Yagi-Uda array antennas for SAR signals and wireless synchronization of the reference chirp signal, respectively. The fabricated radar TRX chip size, including PADs, is 2.20 mm<sup>2</sup>. From the on-ground measurement, the SAR module detected a metallic object up to 20 meters away with around 11.2-dB SNR in multi-static mode. The TRX consumes 0.92, 1.3 and 0.4 W for monostatic, multistatic master, and multistatic slave modes, respectively.

### RTu1C-3

#### A W-Band Spillover-Tolerant Mixer-First Receiver for FMCW Radars

Jingzhi Zhang, Sherif S. Ahmed, Amin Arbabian; Stanford University, USA

**Abstract:** This paper presents a highly linear, low-noise W-band N-path mixer-first receiver for frequency-modulated continuous-wave (FMCW) radar applications. By adopting a high-impedance quarter-wavelength transmission line as the matching network, the input impedance at the fundamental and third-harmonic frequencies has been enhanced, thereby increasing the passive voltage gain and eliminating the reradiation current. Hence, the linearity and noise figure (NF) can be improved. Fabricated in 40 nm CMOS process, the receiver achieves -0.7 dBm out-of-band (OOB) P1dB and 8.0-to-9.5 dB NF simultaneously while consuming 37 mW power.

### RTu1C-4

#### A CMOS 160GHz Integrated Permittivity Sensor with Resolution of 0.05%

$\Delta\epsilon_r$

Hai Yu<sup>1</sup>, Xuan Ding<sup>1</sup>, Jingjun Chen<sup>2</sup>, Sajjad Sabbaghi Saber<sup>1</sup>, Qun Jane Gu<sup>1</sup>; <sup>1</sup>University of California, Davis, USA, <sup>2</sup>Qualcomm, USA

**Abstract:** This paper presents a high-resolution permittivity sensor at 160GHz in 28nm CMOS. It incorporates a THz high Q silicon whispering gallery mode resonator sensor that boosts the system's permittivity sensitivity. Multifold noise reduction techniques are adopted. A novel complementary BPSK signaling suppresses the common mode noise and the low frequency noise from within the system and the environment. Transmitter (TX) local oscillator (LO) feedforward that injection-locks the receiver (RX) mitigates the TX phase noise. The sensing system achieves the best permittivity sensing resolution of 0.05%  $\Delta\epsilon_r$  among the state-of-the-art permittivity sensors within 14us of integration time and 54mW power consumption.

### RTu1C-5

#### A 160-GHz FMCW Radar Transceiver with Slotline-Based High Isolation Full-Duplexer in 130nm SiGe BiCMOS Process

Xingcun Li, Huibo Wu, Shuyang Li, Wenhua Chen, Zhenghe Feng; Tsinghua University, China

**Abstract:** In this paper, a slotline-based electrical balance duplexer (EBD) with high geometrical symmetry topology and high common mode rejection is proposed to realize high isolation between the transmitter (TX) and receiver (RX). With the proposed EBD structure, a 160-GHz frequency modulated continuous wave (FMCW) radar transceiver with TX/RX antenna sharing architecture is achieved in the 130nm SiGe BiCMOS process. The chirp signal can be generated covering 147 GHz to 165 GHz by adjusting the operating frequency of the push-push voltage-controlled oscillator (VCO) with the external input control voltage. Using spatial power combining slotline-based antennas and a high resistivity silicon lens, the measured effective isotropic radiated power (EIRP) is over 20 dBm. The chip has a die area of 2.21mm<sup>2</sup> and consumes 0.6 W of DC power.

**Tuesday, 13 June 2023**

**10:10–11:30**

**24ABC**

**Session RTu2B: Emerging Circuits and Systems for  
Quantum Computing, Quantum Sensing, Photonics, and  
Built-In Self-Test (BIST) Applications**

**Chair: Fabio Sebastiano, Technische Universiteit Delft, The Netherlands**

**Co-Chair: Duane Howard, Amazon, USA**

**RTu2B-1**

**A Diamond Quantum Magnetometer Based on a Chip-Integrated 4-Way  
Transmitter in 130-nm SiGe BiCMOS**

Hadi Lotfi<sup>1</sup>, Michal Kern<sup>1</sup>, Nico Striegler<sup>2</sup>, Thomas Unden<sup>2</sup>, Jochen Scharpf<sup>2</sup>, Patrick Schalberger<sup>1</sup>, Ilai Schwartz<sup>2</sup>, Philipp Neumann<sup>2</sup>, Jens Anders<sup>1</sup>; <sup>1</sup>Universität Stuttgart, Germany, <sup>2</sup>NVision Imaging Technologies, Germany

**Abstract:** Solid-state magnetometers based on color centers in diamond are emerging as one of the leading quantum sensors due to their outstanding room-temperature properties, such as high sensitivity and calibration-free long-term stability. However, their integration into compact systems is still an active area of research. To tackle this challenge, in this paper, we present a quantum magnetometer based on negatively charged nitrogen-vacancy (NV) centers using a custom-designed, chip-integrated 4-way transmitter. In combination with a custom-designed microcoil array, the 4-way transmitter delivers microwave magnetic fields up to 226  $\mu\text{T}$  for carrier frequencies around 7 GHz with a conversion gain of  $\geq 32$  dB to NV centers. The local oscillator (LO) signal required to drive the on-chip quadrature upconversion mixer is generated by a custom-designed quadrature PLL, which provides a 22% tuning range between 6.4 and 8 GHz, and a low phase noise of -122 dBc/Hz at 1 MHz offset from a 7 GHz carrier, to enable broadband, low-noise magnetometry. To verify the excellent performance of the integrated electronics, we have embedded them into a widefield diamond magnetometer using off-chip scanning optics, achieving a state-of-the-art AC-magnetic field limit of detection of 300 pT/Hz<sup>1/2</sup>.

**RTu2B-2**

**A Cryo-CMOS DAC-Based 40Gb/s PAM4 Wireline Transmitter for Quantum  
Computing Applications**

Niels Fakkkel, Mohsen Mortazavi, Ramon Overwater, Fabio Sebastiano, Masoud Babaie; Technische Universiteit Delft, The Netherlands

**Abstract:** State-of-the-art quantum computers already comprise hundreds of cryogenic quantum bits (qubits), and prototypes with over 10k qubits are currently being developed. Such large-scale systems require local cryogenic electronics for qubit control and readout, leaving the digital controllers for algorithm execution and quantum error correction (QEC) at room temperature due to the limited cryogenic cooling budget. The entire process, including qubit readout, data transmission, QEC, and algorithm execution, should be completed well within the qubit decoherence time, thus

requiring a low-power high-speed communication link between the cryogenic quantum processor and classical processor located at room temperature. To this end, this paper presents the first cryo-CMOS high-speed 4-level pulse amplitude modulation (PAM4) wireline transmitter. Thanks to a power-efficient serializing architecture driving a 6-bit digital-to-analog converter (DAC), the 40-nm CMOS chip achieves a data rate of 40 Gb/s PAM4 with an efficiency of 2.46 pJ/b and a ratio of level mismatch (RLM) of 97.8% at 4.2 K. While demonstrating an energy efficiency comparable to state-of-the-art transmitters in more advanced CMOS nodes, the extremely wide temperature operating range (4.2K–300 K) will enable future large-scale quantum computers.

## RTu2B-3

### A mm-Wave CMOS/Si-Photonics Hybrid-Integrated Software-Defined Radio Receiver Achieving >80-dB Blocker Rejection of <-10dBm In-Band Blockers

Ramy Rady, Yu-Lun Luo, Christi Madsen, Samuel Palermo, Kamran Entesari; Texas A&M University, USA

**Abstract:** This paper presents a hybrid-integrated mm-wave software-defined radio (SDR) receiver front-end implemented with silicon photonics and CMOS chips. The proposed SDR leverages a programmable silicon photonics IC (PIC) with high-Q filters to perform re-configurable channel-selection/image-rejection and jammer-rejection with tunable center frequency of 30–45 GHz, and 3–5 GHz bandwidth. Up to four out-of-band blockers are automatically detected and rejected simultaneously. Also, the desired mm-wave signal is mixed with a tunable local oscillator (LO) carrier and down-converted to a 2.5-GHz IF center frequency. Subsequently, the CMOS IC converts the current signal into an amplified voltage signal, thus compensating for PIC losses. The PIC is fabricated using a silicon-over-insulator (SOI) process, and the CMOS is fabricated using 28nm process. The receiver achieves > 80-dB rejection for two blockers and > 65-dB rejection for four blockers. The EVM measures -30-dB using a 100-MSymbol/s 64-QAM signal at the presence of a 10-dBc out-of-band blocker.

## RTu2B-4

### Mixer-Free Phase and Amplitude Comparison Method for Built-In Self-Test of Multiple Channel Beamforming IC

Seonjeong Park, Eun-Taek Sung, Seunghun Wang, Songcheol Hong; KAIST, Korea

**Abstract:** This paper presents a built-in self-test (BIST) method of a multiple channel beamforming IC, based on successive comparisons of phase and amplitude differences between a pair of signals in beamforming channels. This is implemented with a simple difference detection circuit without a mixer and a reference LO. The phase and gain differences of the channels are obtained independently using the proposed simple detector. The phase difference detection accuracy is improved by removing the DC offset caused by the amplitude difference of the signals. The detection circuit is integrated into a 4-channel beamforming IC and the BIST concept verified for both the transmitter and receiver paths. The errors of phase and gain differences between the pair of channels measured through the proposed circuits are as low as -18.1° to 9.8° and -0.29dB to 0.38dB for the transmitter and -8.8° to 15.3° and -0.31dB to 0.41dB for the receiver, respectively.

**Tuesday, 13 June 2023**

**10:10–11:30**

**25ABC**

**Session RTu2C: Systems for Applications: 5G and SATCOM**

**Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center, USA**

**Co-Chair: Raja Pallela, MaxLinear, USA**

## **RTu2C-1**

### **A 24–30GHz 4-Stream CMOS Transceiver Based on Dual-LO Phase-Shifting Fully Connected Architecture**

Qingfeng Zhang<sup>1</sup>, Yiming Yu<sup>1</sup>, Dongming Duan<sup>1</sup>, Xin Xie<sup>1</sup>, Shaoyu Meng<sup>1</sup>, Haoran Wang<sup>1</sup>, Chenxi Zhao<sup>1</sup>, Huihua Liu<sup>1</sup>, Yunqiu Wu<sup>1</sup>, Wenquan Che<sup>2</sup>, Quan Xue<sup>2</sup>, Kai Kang<sup>1</sup>; <sup>1</sup>UESTC, China, <sup>2</sup>SCUT, China

**Abstract:** This paper presents a wideband low-complexity multi-stream beamforming transceiver (TRX) based on multiple local-oscillator (multi-LO) phase-shifting fully-connected (FC) architecture for MIMO communication. In supporting the same beams, the proposed architecture halves the complexity of the FC combiners as well as the ADCs/DACs overhead. Meanwhile, the FC combining network of each stream is implemented at IF-domain, which benefits from avoiding the mutual overlap between the combiners in the RF-domain, but also reducing combiner loss. To verify the proposed architecture, a 24–30 GHz 4-stream dual-LO phase-shifting FC TRX chip is fabricated in 65-nm CMOS process. Each single-stream path integrates a TX and RX channel with independent up/down-mixer, 0.4-dB gain and 6-bit phase control, where the whole TRX IC only has one PA and LNA to amplify 4-stream incoherent signals saving chip area and power consumption. The measured peak conversion gain (CG) of the TX is 31.4 dB, with a 3-dB bandwidth of 24.4–30.1 GHz. In the RX mode, the measured CG versus IF is 18.3 dB, with a 3-dB bandwidth of 3.3–11.8 GHz (112.6% fractional bandwidth). Besides, the TRX IC achieves a maximum OP1dB of 15.4 dBm and minimum NF of 4.6 dB including T/R switch. Additionally, it demonstrates a 26 dB gain control and 360° tuning range, where the maximum gain variation of only  $\pm 0.1$  dB during 360° phase tuning at 27.5 GHz without any calibration.

## **RTu2C-2**

### **A 39GHz 2×16-Channel Phased-Array Transceiver IC with Compact, High-Efficiency Doherty Power Amplifiers**

Joonho Jung, Jooseok Lee, Daehyun Kang, Jinhyun Kim, Woojae Lee, Hansik Oh, Jae-hong Park, Kihyun Kim, Dong-hyun Lee, Sangho Lee, Jeong Ho Lee, Ji Hoon Kim, Younghwan Kim, Taewan Kim, Sangyong Park, Seungwon Park, Seungjae Baek, Bohee Suh, Soyoung Oh, Dongsoo Lee, Juho Son, Sung-gi Yang; Samsung, Korea

**Abstract:** This paper presents a 39 GHz 2×16-channel phased-array transceiver IC with compact, high-efficiency Doherty power amplifiers. The IC was implemented using a 28-nm bulk CMOS process with flip-chip packaging and evaluated using 100 MHz 8-carrier component (CC) fifth-generation

(5G) new radio (NR) signal (total 800 MHz). With single transformer-based compact Doherty power amplifiers in transmitter (TX) path, the phased-array IC shows excellent TX performance, achieving high average output power of  $>8$  /  $>9.3$  dBm/ch. at error-vector-magnitude (EVM) of  $-32$  /  $-28$  dB while consuming low DC power of  $<109$  /  $<118$  mW/ch. Furthermore, the receiver (RX) path demonstrates low system noise figure (NF) of 5.8–6.5 dB, and an EVM of  $-29.8$  dB with low DC power consumption of  $<42.3$  mW/ch.

## **RTu2C-3**

### **A 14-nm Low-Cost IF Transceiver IC with Low-Jitter LO and Flexible Calibration Architecture for 5G FR2 Mobile Applications**

Wanghua Wu<sup>1</sup>, Jeiyoun Lee<sup>2</sup>, Pak-Kim Lau<sup>1</sup>, Taeyoung Kang<sup>1</sup>, Kim Kiu Lau<sup>1</sup>, Si-Wook Yoo<sup>1</sup>, Xingliang Zhao<sup>1</sup>, Ashutosh Verma<sup>1</sup>, Ivan Siu-Chuang Lu<sup>1</sup>, Chih-Wei Yao<sup>1</sup>, Hou-Shin Chen<sup>1</sup>, Gennady Feygin<sup>1</sup>, Pranav Dayal<sup>1</sup>, Kee-Bong Song<sup>1</sup>, Sangwon Son<sup>1</sup>; <sup>1</sup>Samsung, USA, <sup>2</sup>Samsung, Korea

**Abstract:** We present a low-cost dual-stream IF transceiver IC (IFIC) for 5G mm-wave mobile applications. It up/down-converts the baseband signal to an intermediate frequency of 8.4–10 GHz and forms a heterodyne transceiver system together with beamforming ICs to support all FR2 bands. The IFIC features a compact transceiver RF circuitry, low-jitter reconfigurable LO suitable for 256-QAM and non-contiguous carrier aggregation, and an integrated MCU in the digital baseband for flexible calibration and control of both transceiver ICs. The IFIC is implemented in 14-nm FinFET and occupies 16.2 mm<sup>2</sup>. The overall chain IPN measured at 39-GHz band is as low as 114 fs. Thanks to the flexible calibration architecture, digital-pre-distortion (DPD) is demonstrated in TX, which allows for  $>1$  dB of increase in EIRP for both DFT-s- and CP-OFDM signals at EVM of 5.5% at 39-GHz band.

## **RTu2C-4**

### **A Quad-Band RX Phased-Array Receive Beamformer with Two Simultaneous Beams, Polarization Diversity, and 2.1–2.3dB NF for C/X/Ku/Ka-Band SATCOM**

Zhaoxin Hu, Oguz Kazan, Gabriel M. Rebeiz; University of California, San Diego, USA

**Abstract:** This paper presents a wideband 16-channel dual-beam receive (RX) phased-array beamformer in a 90-nm SiGe BiCMOS process. Radio-frequency (RF) beamforming is implemented, and each channel has 5-bit phase control and 25 dB gain control. The dual-beam channel outputs are combined with two wideband Wilkinson networks. The chip has 27.3 dB electronic gain with a 3.4–28.7 GHz 3-dB bandwidth and a 2.1–2.3 dB noise figure (NF) up to 21 GHz. To the authors' knowledge, this work achieves the widest operating bandwidth among RX beamformers for satellite communication (SATCOM). Application areas are in phased arrays for C/X/Ku/Ka-band SATCOM ground terminals.

**Tuesday, 13 June 2023**

**13:30–14:50**

**24ABC**

**Session RTu3B: Advanced Building Blocks for mm-Wave & Beyond**

**Chair: Yahya Tousi, University of Minnesota, USA**

**Co-Chair: Qun Jane Gu, University of California, Davis, USA**

### **RTu3B-1**

#### **An Ultra-Wideband and Compact Active Quasi-Circulator with Phase Alternated Differential Amplifier**

Dongho Yoo, Jun Hwang, Byung-Wook Min; Yonsei University, Korea

**Abstract:** This paper presents a new design for an active quasi-circulator that utilizes a phase alternated differential amplifier to achieve ultra-wideband and compact size in a 28-nm CMOS process. The proposed active quasi-circulator is based on a differential two-stage distributed amplifier, where the differential outputs of the phase alternated amplifier in second stage are cross-connected to the differential outputs of the amplifier in first stage. The use of the phase alternated differential amplifier allows for wideband isolation regardless of frequency. Furthermore, interstage inductor, which is located between two transistors of amplifier makes the circulator more wideband by maintaining frequency response of two transmission lines identically. The measured transmitter (TX) to receiver (RX) isolation is  $>21$  dB,  $-3$  dB bandwidth of TX to antenna (ANT) is from 20 to 38.5 GHz with 4.5 dB of peak gain at 29.8 GHz, minimum insertion loss of ANT to RX is 4.3 dB. The measured TX to ANT output power 1 dB compression point is 7.3 dBm at 28 GHz with DC power consumption of 107 mW. The circulator occupies only  $0.07 \text{ mm}^2$ , thanks to coupled inductors which contribute to compact size.

### **RTu3B-2**

#### **A D-Band Calibration-Free Passive 360° Phase Shifter with 1.2° RMS Phase Error in 45nm RFSOI**

Mohammadreza Abbasi, Wooram Lee; Pennsylvania State University, USA

**Abstract:** This paper presents a new concept of passive phase shifters based on manipulating propagation delay through two parallel transmission lines periodically connected via digitally controlled switch networks. The proposed approach enables precise phase control and flat amplitude response across different phase settings. The prototype IC is fabricated in a 45 nm RFSOI process and occupies only  $0.033 \text{ mm}^2$ . The phase control operates with  $11.25^\circ$  steps over  $360^\circ$  at 140 GHz while maintaining an RMS phase error of  $1.2^\circ$ . The insertion loss is 11.5 dB with  $< \pm 0.8$  dB variation. Among published D-band phase shifters, this work achieves the lowest RMS phase error and reports bi-directional phase control over  $360^\circ$  and calibration-free operation.



### RTu3B-3

#### A 140GHz RF Beamforming Phased-Array Receiver Supporting >20dB IRR with 8GHz Channel Bandwidth at Low IF in 22nm FDSOI CMOS

Shenggang Dong<sup>1</sup>, Navneet Sharma<sup>1</sup>, Sensen Li<sup>1</sup>, Michael Chen<sup>1</sup>, Xiaohan Zhang<sup>2</sup>, Yaolong Hu<sup>2</sup>, Jiantong Li<sup>1</sup>, Yong Su<sup>1</sup>, Xinguang Xu<sup>1</sup>, Vitali Loseu<sup>1</sup>, Eunyoung Seok<sup>1</sup>, Taiyun Chi<sup>2</sup>, Won-Suk Choi<sup>1</sup>, Gary Xu<sup>1</sup>; <sup>1</sup>Samsung, USA, <sup>2</sup>Rice University, USA

**Abstract:** A 140GHz 4-element RF beamforming phased-array receiver (RX) has been demonstrated in 22nm FDSOI CMOS. The proposed single-side-band architecture provides >25dB and >20dB measured image rejection ratio (IRR) across 4GHz and 8GHz channel bandwidth centered at 7GHz intermediate frequency (IF). Each front-end element consists of a wideband low-noise amplifier (LNA) and a vector-modulator phase shifter. The 4 elements are combined on chip through power combiners and driver amplifiers before the double-balanced mixer, which is driven by an on-chip multiplier ( $\times 9$ ). The receiver consumes 480mW DC power and provides <10dB noise figure from 135 to 147 GHz. The RX is measured up to 32 and 24Gb/s in the probe and over-the-air test. To the authors' knowledge, this CMOS RF beamforming RX presents the largest channel bandwidth (8GHz) with 20dB IRR<sub>min</sub> at low IF consuming the lowest DC power per element (120mW) among the published phased-array RX in the 140GHz band.

### RTu3B-4

#### A mm-Wave Blocker-Tolerant Receiver Achieving <4dB NF and -3.5dBm B1dB in 65-nm CMOS

Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen; Technion, Israel

**Abstract:** Digital beam-forming requires highly linear receivers (RXs), as null steering is performed only in digital baseband (BB). This paper presents a highly linear RX, with a high out-of-band (OOB) blocker tolerance without sacrificing performance or power, utilizing a highly linear inverter low-noise amplifier (LNA), followed by an N-path mixer with tunable filtering properties and a BB transimpedance (TIA) amplifier for linearity enhancement. The N-path mixer design trade-offs are discussed, and several linear LNA topologies are presented and compared. A chip prototype was manufactured in a TSMC 65 nm CMOS process. In our implementation, a <4 dB noise figure (NF) is achieved, with an RX gain of 40 dB, in-band (IB) IIP3 of -20 dBm and -3.5 dBm B1dB at a 500 MHz offset, while occupying an active area of 1.62 mm<sup>2</sup> and drawing a total power of 76.8 mW, at a frequency range of 22–31 GHz.

**Tuesday, 13 June 2023**

**13:30–14:50**

**25ABC**

**Session RTu3C: IoT Transmitter and Sub-THz Power Amplifiers**

**Chair: Alexandre Giry, CEA-Leti, France**

**Co-Chair: Hyun-Chul Park, Samsung, Korea**

**RTu3C-1**

**A Reactive Passive Mixer for 16-QAM Cartesian IoT Transmitters in 22nm FD-SOI CMOS**

Lorenzo Tomasin, Daniele Vogrig, Andrea Neviani, Andrea Bevilacqua; Università di Padova, Italy

**Abstract:** The use of a reactive passive mixer is proposed to implement an efficient Cartesian transmitter for IoT applications, capable of supporting high-order modulations, and high data rates. Prototypes in a 22nm FD-SOI CMOS technology show a 5.5dBm output-referred 1 dB compression point with 34.1% system efficiency in CW operation. Under a 2.4 Mbaud, 16-QAM modulation at 2.7dBm average output power, they achieve 9.6 Mb/s data rate, EVM = -24.5 dB, ACLR = -32 dBc, and P<sub>alt</sub> = -36dBm with 22% system efficiency.

**RTu3C-2**

**A 110–170GHz Phase-Invariant Variable-Gain Power Amplifier Module with 20–22dBm P<sub>sat</sub> and 30dBm OIP3 Utilizing SiGe HBT RFICs**

Mustafa Sayginer, Michael Holyoak, Mike Zierdt, Mohamed Elkhoully, Joe Weiner, Yves Baeyens, Shahriar Shahramian; Nokia Bell Labs, USA

**Abstract:** A phase-invariant variable-gain PA RFIC in 130-nm SiGe BiCMOS supporting multi-QAM waveforms over the entire D-band (110–170 GHz) is presented. The chip has a very low phase variation of  $\pm 2^\circ$  over a 15 dB gain control range as well as self-testing and fault-detection features (power detectors, temperature sensors, ADC, SPI control) to ease the implementation and testing of multi-chip PA modules. A WR-6 interface packaged module combining four RFICs on a glass substrate achieves an average P<sub>sat</sub>, OIP3 and gain of 21 dBm, 30 dBm and 14 dB, respectively over 110–170 GHz while the return-losses are better than 10 dB. TX constellations of 256-QAM (16-Gb/s with 3.6% EVM at 11 dBm P<sub>out</sub>) and 64-QAM (36-Gb/s with 8.6% EVM at 15.5 dBm P<sub>out</sub>) are demonstrated at 140 GHz. The output power×bandwidth performance of the packaged all-silicon module is better than the state-of-the-art commercially available III-V parts.

### RTu3C-3

#### A D-Band 20.4dBm OP<sub>1dB</sub> Transformer-Based Power Amplifier with 23.6% PAE in a 250-nm InP HBT Technology

Senne Gielen<sup>1</sup>, Yang Zhang<sup>2</sup>, Mark Ingels<sup>2</sup>, Patrick Reynaert<sup>1</sup>, <sup>1</sup>KU Leuven, Belgium, <sup>2</sup>imec, Belgium

**Abstract:** This paper presents a high-efficiency transformer-based D-band power amplifier (PA) in 250-nm InP HBT. The PA has a saturated output power of 21 dBm and peak power-added efficiency (PAE) of 23.6%. The small-signal gain and bandwidth are 19.8 dB and 24.4 GHz respectively. Careful design of the biasing networks results in a record OP<sub>1dB</sub> and associated PAE of 20.4 dBm and 23% respectively. To the authors best knowledge this is the highest PAE ever reported at P<sub>1dB</sub> for D-band power amplifiers, resulting in record output power and efficiency during modulated measurements up to 20 Gb/s.

### RTu3C-4

#### 305-GHz Cascode Power Amplifier Using Capacitive Feedback Fabricated Using SiGe HBT's with f<sub>max</sub> of 450GHz

Suprovo Ghosh, Frank Zhang, Haidong Guo, Kenneth K. O; University of Texas at Dallas, USA

**Abstract:** A 305-GHz power amplifier (PA) fabricated in a 130-nm SiGe HBT BiCMOS technology with HBT f<sub>t</sub>/f<sub>max</sub> = 350/450 GHz is presented. The PA employs 4 cascode amplification stages with capacitive feedback between the collector of common base stage and the base of common emitter stage that increases power gain of each stage by ~4 dB and a 4-way power combiner at the output. The PA achieves a measured P<sub>sat</sub> of 7.5 dBm and OP<sub>1dB</sub> of 4.5 dBm at 290 GHz. The design reaches a peak small signal gain of 14.5 dB at 305 GHz. The circuit consumes 1008 mW DC power from a 4-V supply and achieves a PAE<sub>max</sub> of 0.39%. The PA exhibits the highest P<sub>sat</sub> and OP<sub>1dB</sub> at 290 GHz, and the highest small signal gain at 305 GHz among the PA's fabricated using SiGe HBT's with f<sub>max</sub> less than 500 GHz.

**Tuesday, 13 June 2023**

**15:40–16:40**

**25ABC**

**Session RTu4C: Invited Industry Presentations**

**Chair: Debopriyo Chowdhury, Broadcom, USA**

### **RTu4C-1**

#### **D-Band Circuits and Systems Application in 55nm SiGe BiCMOS**

Andrea Pallotta<sup>1</sup>, Pascal Roux<sup>2</sup>, David del Rio<sup>3</sup>, Juan Francisco Sevillano<sup>3</sup>, Mahmoud Pirbazari<sup>1</sup>, Andrea Mazzanti<sup>4</sup>, Vladimir Ermolov<sup>5</sup>, Jussi Säily<sup>5</sup>, Mario Giovanni Frecassetti<sup>6</sup>, Maurizio Moretto<sup>6</sup>; <sup>1</sup>STMicroelectronics, Italy, <sup>2</sup>Nokia Bell Labs, France, <sup>3</sup>Ceit, Spain, <sup>4</sup>Università di Pavia, Italy, <sup>5</sup>VTT, Finland, <sup>6</sup>Nokia, Italy

**Abstract:** While 5G wireless network is being currently deployed around the world, preliminary research activity has begun to look beyond 5G and conceptualize 6G standard. From analog and RF point of view, the need to address new frequency spectrum to increase achievable link capacity has its implication on the development of More-than-Moore mixed-signal RFIC technologies. This presentation reports the exploitation of the radio spectrum in D-band (130–174.8GHz), by relying on power efficient BiCMOS chipset for an active phased antenna array system (APAAS) with beam steering functionality.

### **RTu4C-2**

#### **Thermal Challenges in GaAs PA Design for 5G Applications**

S.H. Tsai<sup>1</sup>, C.S. Yeh<sup>1</sup>, C. Potier<sup>1</sup>, B. Thota<sup>2</sup>, H. Andersen<sup>1</sup>, B. François<sup>2</sup>; <sup>1</sup>iCana, Taiwan, <sup>2</sup>iCana, Belgium

**Abstract:** This presentation highlights the thermal challenges in GaAs power amplifier design and demonstrates how improved thermal modeling and layout optimizations can result into state-of-the-art performance. This design approach is applied in the development of iCana's 4.4–5.0 GHz 4W PA for 5G small cell applications.

## RTu4C-3

### 22FDX Technology Solutions for 5G mmWave

Shafiullah Syed<sup>1</sup>, Zhixing Zhao<sup>2</sup>, Shih Ni Ong<sup>3</sup>, Lye Hock Kelvin Chan<sup>3</sup>, Kirby Kheng Seong Tan<sup>3</sup>, Chee Wai Wan<sup>3</sup>, Wai Heng Chow<sup>3</sup>, Koi Wai Chew<sup>3</sup>, Amit Kumar Sahoo<sup>3</sup>, Raghavendra Kammar Nagaraja<sup>4</sup>, Andreas Knorr<sup>1</sup>, Qiao Yang<sup>5</sup>, Chris Boyer<sup>1</sup>, Stephen Moss<sup>1</sup>, Ming-Cheng Chang<sup>2</sup>, Jen Shuang Wong<sup>3</sup>, Dieter Lipp<sup>2</sup>, Peter Javorka<sup>2</sup>, Jan Hoentschel<sup>2</sup>, <sup>1</sup>GlobalFoundries, USA, <sup>2</sup>GlobalFoundries, Germany, <sup>3</sup>GlobalFoundries, Singapore, <sup>4</sup>GlobalFoundries, India, <sup>5</sup>GlobalFoundries, China

**Abstract:** 22FDX+ next generation technology offers a suite of enhancements that enable 5G mmWave front-end beamformer circuits with smaller area, improved reliability and state-of-art performance for Psat and PAE for 5G handsets and infrastructure applications. The presentation highlights some of the novel devices including MREP SLVT, ENBFMOAT, and EDNMOS, BEOL updates and new PDK enablement for accurate prediction of thermal behavior in the FET devices. A single-stage 28GHz 2-stack PA design is shown with ENBFMOAT device having peak PAE of 50% with high power density and linearity. A 14G DCO is shown with superior phase noise of -117.5 dBc/Hz at 1 MHz offset.

# WORKSHOPS

**Sunday, 11 June 2023**

Workshops and Short Courses are offered on Sunday, Monday and Friday at the San Diego Convention Center. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

**WSB (half-day): 08:00–11:50**

## **A Deep Dive into Circuit Design for Wireline/Optical and Wireless Transceivers: Commonalities and Differences**

*Sponsor:*     **RFIC**

*Organizers:* **Mahdi Parvizi**, *Cisco*  
**Bahar Jalali Farahani**, *Cisco*

**Abstract:** This workshop presents the similarities and differences between wireless and wireline/optical communication along with circuit design innovations that enable the next generation of these systems. There are undeniable similarities between the systems and electronic building blocks in wireline/optical and wireless transceivers. In this event, first commonalities and differences of wireline/optical system versus an advanced wireless link will be discussed, next advanced modulation schemes to close the gap with Shannon limit in wireline links will be reviewed. Next, advanced circuit design techniques for wireless and optical transmitters, which is power amplifiers and modulator drivers will be presented. The last talk covers the optical and wireless receiver front-ends where novel circuit design techniques for low-noise, low-power LNAs and TIAs will be highlighted.

*Speakers:*

1. “Wireless-Inspired Wireline Communication Systems”, **James F. Buckwalter**, *University of California, Santa Barbara*
2. “How Close are we to the Shannon Limit? The Role of Modulation Schemes to Close the Gap”, **Ali Sheikholeslami**, *University of Toronto*
3. “Energy Efficiency and Linearity Improvements for Next Generation of Power Amplifiers and Modulator Drivers”, **Munehiko Nagatani**, *NTT*
4. “Design of Low-Power, Low-Noise Receiver Front-Ends: Wireless vs. Wireline”, **Behzad Razavi**, *University of California, Los Angeles*

**WSC (full-day): 08:00–17:20**  
**6G Challenge:**  
**Overpass RF Bandwidth Limitation to Reach 100Gbs to 1Tbs**

*Sponsor:*     **RFIC**

*Organizers:* **Didier Belot**, *CEA-Leti*  
                  **Hao Gao**, *Technische Universiteit Eindhoven*  
                  **Pierre Busson**, *STMicroelectronics*

**Abstract:** Wireless systems with small RF bandwidths, high-order modulations, and advanced signal-processing techniques have reached a saturation point. They run into spectrum saturation and interference troubles under the sub-6GHz frequency band. International Telecommunication Union (ITU) announced the opening of 275GHz to 450GHz for super high data-rate communication applications. 5G is becoming a reality worldwide, and 6G is in a championship worldwide. The complete paradigm change of this new generation implies the evolution from today, and one of the elements to be defined will be the revolution in the transceiver functions: The data-rate is targeted beyond 100Gbps, and the carrier frequency to support such data transfer will be in the combination of mm-wave and sub-THz. In the 6G, the mm-wave/sub-THz front-end has challenges on bandwidth, power consumption, antenna coupling, array integration, etc. In this workshop, we also dedicate attention to silicon-based building blocks' present realizations targeting 5G to 6G evolution.

*Speakers:*

1. “Revolutionary Ideas for 6G (and Next-G) Transceivers Overcoming Fundamental Limitations of Conventional Architectures”, **Payam Heydari**, *University of California, Irvine*
2. “140GHz Two-Dimensional 8×8 Phased Arrays for 6G MIMO Systems”, **Amr Ahmed, Gabriel M. Rebeiz**, *University of California, San Diego*
3. “A Channel Aggregation Architecture TX-RX in D-Band with 84Gbps Data-Rate in RFSOI Process”, **Jose Luis Gonzalez-Jimenez**, *CEA-Leti*
4. “Sub-THz Base Station Radio Architecture”, **Rui Hou**, *Ericsson*
5. “THz Waveforms for Communication and Sensing”, **Sofie Pollin**, *KU Leuven*
6. “Silicon-Based mm-Wave Broadband RF Front-End”, **Hao Gao**, *Technische Universiteit Eindhoven*

**WSD (half-day): 08:00–11:50**  
**EM Circuit Co-Design and Conflation of**  
**Passive/Active Circuits at mm-Wave Frequency**

*Sponsor:*     **RFIC**

*Organizers:* **Vadim Issakov**, *Technische Universität Braunschweig*  
                  **Ruonan Han**, *MIT*

**Abstract:** Integration of passive electromagnetic structures and particularly integration of antennas on silicon becomes feasible at frequencies above 100GHz due to wavelength-related size reduction. The goal of this workshop is to give inspiration on the various novel circuit techniques relying on conflation of passive and active devices. Furthermore, this workshop discusses potential emerging applications towards THz and presents the latest developments on integrated EM devices and co-design with active circuits at high mm-wave frequencies. We discuss how to realize passive on-chip components, such as transformers, coupler baluns and antennas and how to combine them with the active circuitry. Furthermore, novel techniques involving antennas to realize certain functions are discussed. Antennas can be co-designed synergistically with active circuits to realize novel hybrid antenna-electronics with “on-radiator” and near-field functions, such as power combining/splitting, impedance scaling/filtering, active load modulation, noise cancellation and reconfigurability. A significant research challenge in hybrid active circuit/electromagnetic electronics is the application of suitable multi-physics simulation tools and co-design/co-optimization methodologies. This requires 3D full-physics solutions for electromagnetic simulation. Several world renowned speakers will provide an overview on the techniques, applications and the practical design considerations on realization of these approaches. In this half-day workshop we will discuss emerging techniques for on-chip mm-wave active/passive circuit co-design and applications of these new techniques. Distinguished speakers from leading companies and academia will present a wide range of topics to cover various aspects of EM-circuit co-design. A brief concluding discussion will round-off the workshop to summarize the key learnings of aspects presented during the day.

*Speakers:*

1. “Co-Design Techniques of mm-Wave Circuits with Electromagnetics and Radiation”, **Hua Wang**, *ETH Zürich*
2. “EM-to-Information Approach for Reconfigurable THz Sensors and Surfaces”, **Kaushik Sengupta**, *Princeton University*
3. “Embedding Networks and Automation to Enhance Power Gain and Compression in Amplifiers Above 100GHz”, **James F. Buckwalter**, *University of California, Santa Barbara*
4. “Advanced Circuit Techniques Using Integrated Transformers”, **Andrea Bevilacqua**, *Università di Padova*
5. “Co-Design and Coupling Effect in Highly Integrated mm-Wave Systems on Chip”, **Fabio Padovan**, *Infineon Technologies*



## WSF (full-day): 08:00–17:20

### Enabling Quantum Computing: A Survey of Readout Technologies

*Sponsor:* **RFIC**

*Organizers:* **Duane Howard**, *Amazon*  
**Fabio Sebastiano**, *Technische Universiteit Delft*  
**Kevin Tien**, *IBM*

**Abstract:** The continued prevalence of microwave system techniques for interacting with superconducting transmon qubits and spin qubits have driven a resurgence of interest in cryogenic circuit and systems for quantum computing. Moreover, quantum computing applications demand low power, high scalability, and high precision in control signal generation and readout signal processing, which has led to several recent demonstrations of innovative system building blocks, as well as end-to-end control and readout chains. In this workshop, we introduce the state-of-the-art in system architectures for qubit control and readout, and then focus on the recent developments in technologies related to qubit readout. We will examine current building blocks found in high-end systems, then look at the next generation of high performance cryo-LNA technologies. Finally, we conclude with deep dives into full readout chain construction, and test and metrology for this very challenging ecosystem of components.

*Speakers:*

1. “Workshop Introduction”, **Duane Howard**<sup>1</sup>, **Fabio Sebastiano**<sup>2</sup>, **Kevin Tien**<sup>3</sup>,  
<sup>1</sup>*Amazon*, <sup>2</sup>*Technische Universiteit Delft*, <sup>3</sup>*IBM*
2. “Probing Spin Qubits with Radiofrequency Reflectometry”, **M. Fernando González-Zalba**, *Quantum Motion*
3. “Readout Chains for Transmon Qubits in Production Scaled Quantum Computers”,  
**David Lokken-Toyli**, *IBM*
4. “State-of-the-Art Cryo-LNAs in III-V Technology for Scalable Quantum Computing”,  
**Arsalan Pourkabirian**, *Low Noise Factory*
5. “Scaling Considerations for Superconducting Quantum-Limited Amplifiers”, **José Aumentado**, *NIST*
6. “SiGe and CMOS Cryogenic Amplifiers for Superconducting Qubit Readout”, **Joseph Bardin**, *UMass Amherst*
7. “Wideband-Noise-Matching Considerations for Cryo-CMOS LNAs”, **Leonid Belostotski**,  
*University of Calgary*
8. “Panel Discussion: the Ecosystem for Cryo-LNAs — What’s Next?”
9. “A Cryogenic CMOS RF Receiver for Multiple Spin Qubit Readout: From Specifications to Implementation and Qubit Testing”, **Masoud Babaie**, *Technische Universiteit Delft*
10. “Scaling Measurement Methodologies using Cryogenic TaaS Framework for Higher Quality Cryo-LNAs and Reliable Qubit Readout Chains”, **Brandon Boiko**, *FormFactor*

**WSG (full-day): 08:00–17:20**

**Fundamentals of RF Power Amplifiers: From the Basics to Advanced PA Architectures, Practical Design Aspects, and Process Technologies**

*Sponsor:*     **RFIC/IMS**

*Organizers:* **Debopriyo Chowdhury**, *Broadcom*  
                  **Jennifer Kitchen**, *Arizona State University*

**Abstract:** The RF Power Amplifier (PA) is a performance bottleneck of most RF wireless transmit systems and a critical design component of any RF system. Fundamental PA design knowledge and realization expertise are highly desired and regarded skills in the RF community. With their numerous process technologies, architectures, and implementation “tricks”, the design of RF PAs may quickly become overwhelming. Moreover, the knowledge is typically acquired through years of design experience and multiple failed design attempts. This workshop jump-starts you into the world of PA design by walking you through the various aspects of RF PA design, starting from the basics and then introducing the most popular forms of advanced PA architectures. The various tutorials within the workshop will categorize the different PA design methodologies to give you a better understanding behind their motivations. Experts from industry and academia will also summarize the strengths of various process technologies, enabling you to better select processes depending on your target application. Finally, PA designers with decades of experience will provide insight into successfully implementing RF PAs, including practical design aspects (“tricks of the trade”), accounting for PA memory and thermal effects (the big “gotcha”), and effectively simulating PA designs to closely predict performance. This workshop will provide design insights not obtained from textbook reading, thus benefiting those who are new to the RF PA design field and seasoned warriors who would like a rapid refresher.

*Speakers:*

1. “Introduction to the Workshop”, **Jennifer Kitchen<sup>1</sup>**, **Debopriyo Chowdhury<sup>2</sup>**,  
*<sup>1</sup>Arizona State University, <sup>2</sup>Broadcom*
2. “Foundations of RF Power Amplifiers”, **Joseph Staudinger**, *NXP Semiconductors*
3. “Comparison of Efficiency Enhancement Techniques for RF PAs”, **Matthew Heins**,  
*University of Texas at Dallas*
4. “Digital Power Amplifiers and Transmitters Based on RF Digital-to-Analog Converters”,  
**Sangmin Yoo**, *Samsung*
5. “Envelope Tracking Systems for RF PA Efficiency Enhancement”, **Peter Asbeck**,  
*University of California, San Diego*
6. “The Promise of Load Modulation and Doherty Power Amplifiers”, **Hua Wang**, *ETH Zürich*
7. “CMOS vs SOI vs GaAs — What is the Best Technology for RF and mm-Wave PA Design?”,  
**Ali M. Darwish**, *Army Research Laboratory*
8. “Practical Challenges in Integrated CMOS Power Amplifier Design”, **Ali Afsahi**,  
*Broadcom*
9. “Concluding Remarks”, **Jennifer Kitchen<sup>1</sup>**, **Debopriyo Chowdhury<sup>2</sup>**, *<sup>1</sup>Arizona State University, <sup>2</sup>Broadcom*

**WSH (full-day): 08:00–17:20**

## **Integration of 6G Systems from BB to Antenna for 6G Phased Arrays**

*Sponsor:*     **RFIC**

*Organizers:* **Gernot Hueber**, *United Micro Technology*  
**Shahriar Shahramian**, *Nokia Bell Labs*

**Abstract:** Wireless networks have enabled socio-economic growth worldwide and are expected to further advance to foster new applications such as autonomous vehicles, virtual/augmented-reality, and smart cities. Due to limitations of further growth in capacity in the sub-6GHz spectrum, mm-wave and sub-THz frequencies are gaining an important role in the emerging 6G and the communication-on-the-move applications. In 6G, RF/mm-wave/sub-THz front-ends have challenges on bandwidth, power consumption, antenna coupling, array integration, etc. We examine the integration technologies and packaging challenges. 6G covering from sub-10GHz to high frequency as well the complexity of systems is increasing, which demands implementations in the right technology (CMOS, SiGe, ...) and integration of chipsets heterogeneously from basedband, transceiver to the antenna. The heterogeneous integration will be important with the multitude of frequency bands covered, e.g. 7–14GHz bands up to frequencies >100GHz.

*Speakers:*

1. “The Challenges of Integration in 6G Transceiver Systems”, **Gernot Hueber<sup>1</sup>**, **Shahriar Shahramian<sup>2</sup>**, <sup>1</sup>*United Micro Technology*, <sup>2</sup>*Nokia Bell Labs*
2. “Toward 6G: From New Hardware Design to Wireless Semantic and Goal-Oriented Communication Paradigms”, **Emilio Calvanese-Strinati**, *CEA-Leti*
3. “6G from System Architectures Multi-Band Transceivers and Integration”, **Harish Viswanathan**, *Nokia Bell Labs*
4. “THz CMOS Phased Array Transceiver for 6G”, **Kenichi Okada**, *Tokyo Tech*
5. “Advances in Packaging and Integration for 6G Phased Array Transceiver Systems”, **Hsin-Chia Lu**, *National Taiwan University*
6. “Architectures, Algorithms, and Vertical Integration for Advanced Beamforming in Next Generation 5G and 6G Systems”, **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*
7. “Architectures, Technology Partitioning, and Challenges for 6G Beamformers”, **Giuseppe Gramegna**, *imec*
8. “Techniques for MIMO and Extreme Data-Rates at mm-Wave/Sub-THz”, **Harish Krishnaswamy**, *Columbia University*

**WSI (full-day): 08:00–17:20**  
**mm-Wave Integrated Radars: Opportunities and Challenges**

*Sponsor:*     **RFIC**

*Organizers:* **Yahya Tousi**, *University of Minnesota*  
                  **Vito Giannini**, *Ubnder*

**Abstract:** The unique sensing capabilities of mm-wave radars bolstered by modern nano-scale silicon technology and advanced image processing has created the opportunity for integrated radar technology to create substantially improved image perception at a considerably lower size and cost compared to the radars of the 20th century. There is a growing effort in both academia and industry to bring this technology to fruition. In this workshop, we overview the existing opportunities in this field and the challenges that need to be overcome in order to standardize and commercialize integrated radar technology. The workshop brings together a complementary mix of top academic and industry speakers with a breadth of expertise and experience in this field ranging from the fundamental aspects of circuit design, system integration to sensor fusion, product design and testing.

*Speakers:*

1. “Introduction to the mm-Wave Radar Workshop”, **Yahya Tousi**, *University of Minnesota*
2. “Automotive Radar — Applications and Technology Trends”, **Juergen Hasch**, *Robert Bosch*
3. “Imaging Radars at Scale — From Automotive to Security Applications”, **Sherif Ahmed**, *Stanford University*
4. “High-Performance and Low-Power mm-Wave Radar Systems: Requirements and Challenges”, **Krishnanshu Dandu**, *Texas Instruments*
5. “Phased-Array-based Real-Time 3D Radar for AI-Based Event Classification”, **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*
6. “A Digital-Perception Radar Platform for Automotive Safety”, **James Maligeorgos**, *Ubnder*
7. “140GHz Automotive Radar — Sense and Nonsense”, **Ilja Ocket**, *imec*
8. “THz and mm-Wave High-Resolution Imaging and Radar Sensing for Low-Power and Short-Range Applications”, **Omeed Momeni**, *University of California, Davis*
9. “Soli: Radar for Intelligent Human-Computer Interactions”, **Jaime Lien**, *Google*

**WSJ (full-day): 08:00–17:20**  
**mm-Wave and Sub-THz PA Design for**  
**Next-Gen Wireless and Sensing Applications**

*Sponsor:*     **RFIC/IMS**

*Organizers:* **Steven Callender**, *Intel*  
                  **Sungwon Chung**, *Neuralink*

**Abstract:** There is no silver bullet power amplifier (PA) design that provides a one-size-fits-all solution for next-gen communication and sensing systems due to the diversity of applications and their associated PA specs (eg output power, linearity, bandwidth, and back-off efficiency). The goal of this workshop is to explore leading mm-wave and sub-THz applications and the associated PA specs for these systems. The applications of focus are massive MIMO and large-scale phased-arrays, sub-orbital satellite communication (SATCOM), and mm-wave radar. A balanced mix of both industry and academic perspectives will be provided, offering both a high-level familiarization of the application and associated specifications, along with deeper technical dives into PA design techniques in modern process nodes.

*Speakers:*

1. “Design of D-Band PAs in Bulk-CMOS and FinFET”, **Patrick Reynaert**, *KU Leuven*
2. “Generating “Efficient” D-Band Power Using Nanoscale CMOS Technology”, **Ali M. Niknejad**, *University of California, Berkeley*
3. “Reliable mm-Wave and Sub-THz PA Design”, **Jefy Jayamon**, *Qualcomm*
4. “Power Amplifiers for Large-Scale SATCOM Phased Arrays”, **Kaushik Dasgupta**, *Amazon*
5. “GaN and GaAs Power Amplifier Design for Arrays”, **Taylor Barton**, *University of Colorado Boulder*
6. “High-Efficiency Silicon PAs for mm-Wave Radar Sensors”, **Tolga Dinc**, **Krishnanshu Dandu**, **Swaminathan Sankaran**, **Brian Ginsburg**, *Texas Instruments*

**WSK (full-day): 08:00–17:20**  
**To 100Gb/s and Beyond: High-Data-Rate Interconnect Technologies,**  
**Who Will Win at Which Scenario?**

*Sponsor:*     **RFIC**

*Organizers:* **Jane Gu**, *University of California, Davis*  
                  **Wooram Lee**, *Penn State University*

**Abstract:** Interconnect bottlenecks have been a long-standing grand challenge over decades, caused by the increasing gap between exponentially growing data generation and transmission demand, and slowly-increasing supporting data bandwidth supply. Both Electrical Interconnect (EI) and Optical Interconnect (OI) have been investigated extensively to try to combat the challenge, however, both of them face their own inherent constraints. The newly emerging sub-THz/THz Interconnect (TI) aims to complement the existing EI and OI to close the interconnect gap. This workshop plans to bring experts from different domains, OI, EI, and emerging TI, to discuss the challenges, opportunities and best use scenarios of each interconnect scheme.

*Speakers:*

1. “Analog and Digital Optical Interconnects”, **Vladimir Stojanovic**, *University of California, Berkeley*
2. “High-Density, Low-Power Optical Communications for AI, Data Center, and More”, **Jonathan Proesel**, *Nubis Communications*
3. “Silicon Photonics-Based Optical I/O for Next-Gen XPU”, **Ganesh Balamurugan**, *Intel*
4. “Waveguide Interconnects — D/F-Band Systems for >100Gbps Medium Reach Links”, **Thomas W. Brown**, *Intel*
5. “High-Speed Short-Reach Interconnects Using Dielectric Waveguide”, **Hyeon-Min Bae**, *KAIST*
6. “Going Beyond 100Gbps with Polymer Microwave Fibers”, **Patrick Reynaert**, *KU Leuven*
7. “A Path to 200+Gb/s Transceiver Design for Electrical Interconnects”, **Jihwan Kim**, *Intel*
8. “Next-Generation Electrical Interconnects: Chips and Chiplets”, **Tod Dickson**, *IBM T.J. Watson Research Center*

**WSL (full-day): 08:00–17:20**  
**State-of-the-Art mm-Wave GaN Transistor and MMIC Technologies  
and Future Perspective**

*Sponsor:*     **IMS/RFIC**

*Organizers:* **Farid Medjdoub**, *IEMN (UMR 8520)*  
                  **Keisuke Shinohara**, *Teledyne Scientific & Imaging*

**Abstract:** Owing to superior electrical and thermal properties of GaN-on-SiC material systems, tremendous progress has been made on GaN-based transistor and MMIC technologies. Advanced heterostructure material designs, epitaxial growth techniques, and transistor scaling processes enabled GaN MMICs to extend their applications from microwave to mm-wave frequencies (up to W-band). Next-generation RF systems require high efficiency and high linearity for more complex modulation schemes to support very high data-rates. The traditional trade-off among efficiency, linearity, and power density imposes performance limitations on GaN MMICs, which become more pronounced at mm-wave frequencies. In this workshop, world-leading experts will discuss the present status, challenges, and future perspective of mm-wave GaN transistor and MMIC technologies, covering emerging materials and devices, device modeling, thermal management, reliability, and circuit designs.

*Speakers:*

1. “N-Polar GaN Devices for Efficiency and Linearity”, **Matthew Guidry**, *Umesh Mishra*, *University of California, Santa Barbara*
2. “High-Efficiency High-Robustness mm-Wave AlN/GaN Transistors”, **Farid Medjdoub**, *IEMN (UMR 8520)*
3. “Progress in Highly Linear and Efficient mm-Wave GaN HEMTs and MMICs”, **Jeong-sun Moon**, *HRL Laboratories*
4. “Polarization-Engineered III-N mm-Wave Transistors for Linearity, Efficiency, and Reconfigurability”, **Patrick Fay**, *University of Notre Dame*
5. “Broadband mm-Wave GaN MMICs: Technology Aspects and Design Examples”, **Fabian Thome**, *Fraunhofer IAF*
6. “GaN Transistor Reliability Drivers — Temperature and Electric Fields”, **Martin Kuball**, *University of Bristol*
7. “The Interplay Between Deep Level Effects and Reliability in Deep Submicron-Gate GaN HEMTs for RF Applications”, **Enrico Zanoni**, *Università di Padova*
8. “N-Polar GaN HEMT Technology for mm-Wave Amplifiers using Commercial 4-inch Wafer Process Facilities”, **Kozo Makiyama**, *Sumitomo Electric*
9. “ScAlN/GaN Heterostructure Field Effect Transistors for Ultra-High-Power and Wide-Band MMICs”, **Eduardo Chumbes**, *Raytheon*
10. “GaN Transistor Designs for mm-Wave Applications”, **Keisuke Shinohara**, *Teledyne Scientific & Imaging*

**WSA (half-day): 13:30–17:20**  
**Recent Advances in**  
**Ultra-Low-Power Wireless Communication Technology**

*Sponsor:*     **RFIC**

*Organizers:* **Sai-Wang Rocco Tam**, *NXP Semiconductors*

**Yao-Hong Liu**, *imec*

**Oren Eliezer**, *Samsung*

**Minyoung Song**, *imec*

**Abstract:** Ultra-Low-Power (ULP) wireless communication technology provides many unique features over conventional wireless communication such as high energy efficiency, low cost, small form factor, large scale deployments, reconfigurability and simple architecture. This workshop will bring together experts from academia and industry to highlight recent works and applications in this exciting technology. In the first topic, we are going to review the industry impacts on the most successful and large-scale commercialization using ULP wireless communication technologies such as RFID and Near-Field Communication (NFC). After that, we are going to shift our focus to recent research advances in using RF backscattering techniques in Reconfigurable Intelligent Surface (RIS) and WLAN/BT connectivity solutions. In the last topic of this workshop, we will discuss recent advances from medical, industrial and academic fields in biomedical implants with technologies such as co-optimizing antenna and RFIC to miniaturize radio module volume. Unconventional wireless propagation methods are also introduced, such as body channel communication, Magnetoelectric, ultrasound, etc.

*Speakers:*

1. “Recent Circuit and System Architecture Design Advances in RFID/NFC Products”, **Peter Thüringer**, *NXP Semiconductors*
2. “Recent Advances in Reconfigurable Intelligent Surfaces (RIS) and Backscatter Communication”, **Manos Tentzeris**, *Georgia Tech*
3. “Enabling Low-Power yet Standards Compatible Wireless Communication via Wake-Up Receivers and Backscatter Circuits”, **Patrick Mercier**, *University of California, San Diego*
4. “Circuit Techniques for Wirelessly Powered Sensors and Actuators”, **Aydin Babakhani**, *University of California, Los Angeles*
5. “Magnetoelectric Power and Data Transfers to Millimetric Bioelectronic Implants”, **Kaiyuan Yang**, *Rice University*



**WSE (half-day): 13:30–17:20**  
**FDSOI CMOS Energy Efficient 5G and IoT Design Techniques and  
Related Technology**

*Sponsor:*     **RFIC**

*Organizers:* **Wanghua Wu**, *Samsung*  
**Andreia Cathelin**, *STMicroelectronics*

**Abstract:** Thanks to the extended body biasing feature, FDSOI process has enabled new system and circuit design techniques to drastically improve the RF and mm-wave system performance. Tremendous industry collaboration efforts have committed to bring up the FDSOI to higher volumes of production to serve the wireless, IoT, and automotive market in the near future. This workshop includes an overview introductory presentation followed by 4 talks on FDSOI technology and its industry design examples for RF and mm-wave applications. The introduction provides the overview on FDSOI technology and its benefits for analog/RF/mm-wave circuit design, focusing on a technology perspective. The following three talks demonstrate RF and mm-wave system design examples using FDSOI technology, for 5G infrastructure and user terminal as well as for ULP IoT. The last talk reveals the advanced FDSOI process design roadmap and what is expected in the near future.

*Speakers:*

1. “Benefits of FD-SOI Technology for Analog/RF/mm-Wave Circuits”, **Andreia Cathelin**, *STMicroelectronics*
2. “5G FR2 UE Phased Array Transceiver Solution Using 28nm CMOS FD-SOI”, **Xiaohua Yu**, *Samsung*
3. “Ultra-Low-Power IoT Frequency Synthesis Solutions Based on FD-SOI Technology”, **Yann Deval<sup>1</sup>**, **David Gaidioz<sup>2</sup>**, **Andres Mauricio Asprilla Valdes<sup>2</sup>**, **Denis Michael Flores Pazos<sup>2</sup>**, **Andreia Cathelin<sup>2</sup>**, <sup>1</sup>*IMS (UMR 5218)*, <sup>2</sup>*STMicroelectronics*
4. “mm-Wave Front-End Circuits for 5G and 6G Applications Using FD-SOI”, **Yang Zhang**, *imec*
5. “22FDX Platform and Features Optimized for Demanding RF Applications Ranging from WiFi Connectivity and mm-Wave Cellular to Auto Radar”, **Andreas Knorr**, **Tianbing Chen**, **Shafi Syed**, **Randy Wolf**, **Zhixing Zhao**, **Mingcheng Chang**, **Steffen Lehmann**, **Peter Javorka**, **Shih Ni Ong**, **Amit Kumar Sahoo**, **Jen Shuang Wong**, **Wai Heng Chow**, **Kok Wai Johnny Chew**, **Nicholas Comfoltey**, **Farzad Michael David Inanlou**, **Stephen Moss**, **Julio Costa**, *GlobalFoundries*

**WSO (half-day): 13:30–17:20**  
**Advanced Wafer-Level Heterogeneous Integration and Packaging for  
mm-Wave 5G and 6G Applications**

*Sponsor:*     **IMS/RFIC**

*Organizers:* **Kamal Samanta**, *Sony*  
                  **Kevin Xiaoxiong Gu**, *Metawave*

**Abstract:** This workshop will cover various recently developed technologies and the state-of-the-art performance in wafer-level integration and packaging technologies and manufacturing techniques with challenges and possible future directions and solutions. In particular, it will highlight the latest advances in the areas such as embedded wafer-level ball grid array (eWLB) technology for system integration with high Q interconnects and passives in thin-film Re-Distribution Layers (RDL), wafer-level heterogeneous integration of different substrates, BiCMOS embedded TSVs, sub-THz on-chip antenna integration, innovative Fan-Out technologies for wafer-level package, RF IPD, and FOSiP, and embedding various chips within the silicon Metal-Embedded Chip/Chiplet Assembly. Further, the workshop will present the practical realization of highly integrated systems, including 60GHz and 77GHz eWLB transceiver modules with integrated antennas, 3D wafer-level packaging for mm-wave and sub-mm-wave space systems, and hetero-integration technology solutions to enable a full 2D array of phased array systems above 120GHz.

*Speakers:*

1. “Developments in Wafer-Level Packaging for mm-Wave Communication and Radar System”, **Maciej Wojnowski**, **Klaus Pressel**, *Infineon Technologies*
2. “Advanced Packaging and Heterogeneous Integration Technologies for mm-Wave and THz Applications”, **Mehmet Kaynak**, *IHP*
3. “Fan-Out Packages Enabling Pivotal mm-Wave Performance”, **CP Hung**, *ASE Group*
4. “Metal-Embedded Chip/Chiplet Assembly (MECA) Platform for High-Frequency RF Subsystems”, **Souheil Nadri**, *HRL Laboratories*
5. “Wafer-Level Packaging for High Frequency Applications at Northrop Grumman Space Systems”, **Matthew Laurent**, *Northrop Grumman*

## **Social Events/Guest Program**

**SUNDAY, 11 June 2023**

**RFIC Welcoming Reception: 19:30–21:00**

RFIC 2023 starts with a welcome event on Sunday for all attendees, which will be hosted at the San Diego Convention Center in the Sails Pavilion immediately following the RFIC 2023 Plenary Session.

**MONDAY, 12 June 2023**

**IMS Welcome Event: 19:00–21:00**

IMS 2023 starts with a welcome event on Monday for all attendees, which will be hosted at the San Diego Convention Center in the Sails Pavilion immediately following the IMS 2023 Plenary Session.

**MONDAY, 12 June 2023 – THURSDAY, 15 June 2023**

**Young Professionals' Lounge**

Young Professionals' Lounge will be located in the Sails Pavilion of the San Diego Convention Center from Monday, 12 June 2023 through Thursday, 15 June 2023. Students can hang out, play games, network, and meet & greet the speakers of various student related sessions.

**Guest Lounge**

The Guest Lounge will be open to all registered guests Monday, 12 June 2023 through Thursday, 15 June 2023. Light refreshments will be provided for all registered guests.

**TUESDAY, 13 June 2023**

**RFIC Student/Industry ChipChat**

**“The 3 Things to Start Your Career with a Bang”**

**17:00–19:00**

Come and join the special event customized by and for RFIC 2023 students and the RF industry!

**HAM Radio Social Event: 18:00–20:00**

All radio amateurs and other interested IMS participants are cordially invited to the event. There will be a complimentary buffet with an array of hot and cold appetizers as well as drinks. Held at the The Pointe, Hilton San Diego Hotel.

**Women in Microwaves Networking Event: 18:30–21:00**

The Women in Microwaves Networking Event will be held at the Hilton San Diego Bayfront Hotel.

**Young Professionals Networking Reception: 19:00–21:00**

The Young Professionals Networking Reception will be held at the Hilton San Diego Bayfront Hotel. Please refer to the conference website for detailed information on the panel sessions and activities.

## **Social Events/Guest Program continued...**

**WEDNESDAY, 14 June 2023**

### **Industry-Hosted Cocktail Reception: 17:00–18:00**

The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

### **Awards Banquet: 18:30–20:00**

The MTT-S Awards Banquet will be hosted at the Hilton Bayfront Hotel and will feature exciting entertainment.

## Conference Hotel Accommodations

Hotel	Rate	Distance
Hilton Bayfront (HQ)	\$309	0.1
Andaz	\$279	0.7
Courtyard by Marriott San Diego Downtown	\$299	0.9
Courtyard San Diego Gaslamp/Convention Center	\$289	0.2
Embassy Suites Downtown	\$269	0.4
Hard Rock San Diego	\$309	0.1
Hilton San Diego Gaslamp Quarter	\$299	0.1
Hotel Indigo	\$274	0.5
Manchester Grand Hyatt San Diego	\$275	0.2
Moxy San Diego Downtown/Gaslamp Quarter	\$269	0.7
Omni San Diego	\$289	0.1
Residence Inn by Marriott San Diego Gaslamp	\$259	0.2
San Diego Marriott Gaslamp Quarter	\$299	0.2
Solamar San Diego Hotel	\$279	0.2
The Bristol	\$199	0.9
The Guild Hotel San Diego	\$275	0.9
The Westgate Hotel	\$289	0.9
US Grant Hotel	\$279	0.9
Westin San Diego Bayview	\$309	0.9
Westin San Diego Gaslamp	\$259	0.8
Wyndham San Diego	\$229	1.3

The conference rates, shown in USD, are subject to applicable state and local taxes. The conference rates are available for the dates of three days prior to and three days following the main convention dates, based on availability.

The distance shown in miles is the distance from the conference venue.

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**2023 RFIC Symposium**  
San Diego, California, USA  
11–13 June 2023



**RFIC PROGRAM**