2022 IEEE Radio Frequency Integrated Circuits Symposium

Denver, Colorado, USA 19–21 June 2022





Colorado Convention Center and Hyatt Regency Denver

Sponsored by

IEEE Microwave Theory and Techniques Society IEEE Electron Devices Society and IEEE Solid-State Circuits Society









RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 19 June 2022 Colorado Convention Center & Hyatt Regency Denver

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held at the Colorado Convention Center (CCC) and the Hyatt Regency Denver (Hyatt).

17:30–19:00, Plenary Session, CCC Four Seasons Ballroom: The evening begins with the Student Paper Awards, Industry Paper Awards, and Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Dr. Curtis Ling, CTO of MaxLinear, USA, and Professor Sorin Voinigescu, IEEE Fellow, University of Toronto, Canada.

19:00–21:00, RFIC Symposium Reception and Showcase, Hyatt Centennial Ballroom: Immediately following the Plenary Session is the RFIC Symposium Reception. Food and drinks will be provided while you connect with old friends, make new acquaintances and catch up on the latest developments in the field.

The RFIC Symposium Showcase is held concurrently with the reception and will feature our industry paper awards finalists, student paper awards finalists and the Systems & Applications Forum. The selected authors will be present to highlight their innovative work, summarized in poster format, and some will also show a live demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss the microwave week's opening event. Please see <u>https://rfic-ieee.org/</u> for more details.

The RFIC Symposium is made possible through the generous support of our corporate sponsors:



	Mon 20 June Tue 21 June	07:00-19:00	07:00-08:00						08:00–09:40 13:30–15:10 15:40–17:00)-13:30	10:10-11:55
									$\begin{array}{c} 08:00-09:40\\ 10:10-11:50\\ 13:30-15:10\\ 15:40-17:00 \end{array}$	12:00	
	Sun 19 June	07:00-18:00		08:00-17:00	11:45-13:30	11:45-13:15	17:30–19:00	19:00-21:00			
	Sat 18 June	08:00-18:00									
	Location	CCC Lobby A	CCC Four Seasons 1	CCC 102–113, 201–203, 205–207, 401–404, 501–504, 605–607, 702–706, 708–712	CCC Lobby C	CCC 601–603	CCC Four Seasons Ballroom	Hyatt Centennial Ballroom	CCC 1A–1F, 4A–4C (Mon) CCC 1A–1F (Tue)	CCC 2C-3C (Mon) CCC 4A-4C (Tue)	CCC 1A-1C
	Event	Registration	Speakers' Breakfast	Workshops	Workshops Lunch	Technical Lecture	Plenary Session	Reception and Symposium Showcase	Technical Sessions	Panel Sessions	Student Forums

RFIC Symposium Schedule (18–22 June 2022)

CCC: Colorado Convention Center, Hyatt: Hyatt Regency Denver



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Welcome Message from Chairs

On behalf of the Executive and Steering Committee, we would like to invite you to join us for the 2022 *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*. The RFIC Symposium is the premier IC conference focused exclusively on the latest advances in RF, millimeter-wave, and high-frequency IC technologies and designs. The Symposium, combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition, forms the "IMS Week", the largest RF and microwave technical meeting of the year. As the world is recovering from the unprecedented COVID-19 pandemic, we are organizing the Symposium as an in-person event. I am sure many of us are missing the face-to-face and personal interaction with authors and presenters as well as the social networking and technical discussions with other colleagues that define what the experience of attending a conference is all about.

The RFIC Symposium is taking place at the Colorado Convention Center, in Denver, CO starting on Sunday, 19 June 2022 and lasting through Tuesday, 21 June 2022. The event starts with a workshop program on Sunday. The RFIC 2022 Plenary Session is held on Sunday night, followed by a welcome reception and the Symposium Showcase. The RFIC technical sessions will be held on Monday and Tuesday in parallel tracks. Finally, the IMS technical exhibition will be held on Tuesday, Wednesday, and Thursday.

The 2022 RFIC Symposium will feature a rich and diverse educational program, including a technical lecture, and 13 workshops. The technical lecture is intended for students, junior, as well as seasoned engineers who are interested in the subject, with this year's lecture entitled *"Fundamentals of Noise and Understanding its Effects on RFICs"* by Prof. Asad Abidi, of the University of California, Los Angeles. The Technical Lecture and Workshops are scheduled on Sunday, 19 June 2022. Workshops cover a wide range of advanced topics in RF and mmWave circuits & Systems design, including power amplifiers, 5G/6G technologies and systems, THz, imaging radars, bio circuits, optical systems and much more.

The RFIC Plenary Session will be held on Sunday at 17:30, featuring two prominent speakers from both industry and academia. Dr. Curtis Ling, CTO of MaxLinear, USA, will share his vision for the future of RFIC in his talk "The Future of RFIC is Digital," providing a historical perspective. The talk examines the evolution and current state of communication systems-on-chips, highlighting the role of digitally enabled analog, and then speculates about where this might take us. Additionally, Professor Sorin Voinigescu, a Fellow of the IEEE and a Professor at University of Toronto, Canada, will deliver his vision on breaking the speed limits of RFIC in his talk "RFICs into the Roaring 20's: Hot and Cold," giving a look ahead to the challenges and research problems RFIC designers will have to address through the end of the decade, addressing the power/speed limitations of future circuits and providing possible solutions to the future extremely high-data rate circuits. The RFIC Symposium Sunday program concludes with the "Symposium Showcase," featuring the best student and industry papers, as well as the Systems and Applications Forum, all taking place following our Plenary and at the same place where the reception is held. The Systems and Applications Forum is where authors will demonstrate their work in a lab-like manner. This year we opened participation to all authors who opt to demonstrate their work, in addition to those presenting novel system solutions to known RFIC problems. Additionally, in 2022 we continue with an expanded scope that includes emerging technologies in RF, such as quantum computing, optoelectronics, MEMs, hardware security, and machine learning.

Twelve RFIC technical sessions will be held on Monday, and six more are planned on Tuesday. Our sessions will include topics spanning from sub-6GHz cellular and connectivity wireless systems-on-chip and low-power radios to mmWave/THz phased arrays, power amplifiers, Phase-locked loops, and front-end circuits.

This year, we have two outstanding panels to enrich interaction and discussions amongst attendees. The first technical panel is joined with IMS and it is scheduled for Tuesday, 21 June 2022. Panelists will discuss the topic of *"The Race to the Next-G — Ride the mmWave or Wave Goodbye!"*, debating whether mmWave is the right technology for 5G/6G and perhaps leading to THz, or the fundamentals will limit its use in favor of the more traditional sub-10GHz bands. The second panel is non-technical, and is scheduled on Monday, 20 June 2022. It discusses a controversial topic of *"Industry vs. Academia: Who is Leading Whom?"*. There has been a clear paradigm shift in which we start to see more and more professors taking leave to start companies, while people from the industry are invited to teach classes in universities. In addition, state of the art deep sub-micron CMOS technologies such as 7nm and 5nm are inaccessible to academia due to cost and security concerns, resulting in industry being now leading the state of the art technologies as compared to academia and research. We are confident you will enjoy participating in these two controversial and exciting panels. Lunch boxes will be available for registered participants to purchase.

RFIC 2022 and IMS Week have many opportunities for students. New in 2022, we will have two handcrafted student events scheduled on Tuesday, 21 June 2022. The first event is called Student Industry CHIPS Forum, in which students can meet industry experts and learn the exciting technology trends in the field. The other event is called Student Entrepreneurship Forum, in which students can learn from successful entrepreneurs the art of founding successful RFIC startups. In addition, RFIC will once again conduct a contest to select the top student papers from the symposium. These top papers will be featured at our Sunday Symposium Showcase. Furthermore, all RFIC authors who are students and young professionals (YP) will have the opportunity to apply for and participate in the Three-Minute Thesis (3MT®) program. Students can also hangout in the Young Professionals' Lounge at the Four Season Foyer for networking, playing games and also enjoy a bonus casual interaction with the speakers of the Student Forums.

On behalf of the RFIC Steering, Executive and Technical Committees, we welcome you to join us at the 2022 RFIC Symposium! Please visit the RFIC 2022 website (<u>https://rfic-ieee.org/</u>) for more details and updates.





Donald Y.C. Lie TPC Chair Texas Tech University

Osama Shana'a General Chair MediaTek



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RFIC 2022 Schedule Colorado Convention Center & Hyatt Regency Denver

Saturday, 18 June 2022

08:00-18:00 Registration — Colorado Convention Center (CCC) Lobby A

Sunday, 19 June 2022

- 07:00–18:00 Registration CCC Lobby A
- 07:00–08:00 Speakers' Breakfast CCC Four Seasons 1
- 08:00–17:00 Workshops CCC 102–113, 201–203, 205–207, 401–404, 501–504, 605–607, 702–706, 708–712
- 11:45–13:30 Workshops Lunch CCC Lobby C
- 11:45–13:15 Technical Lecture CCC 601–603: Fundamentals of Noise, and Understanding its Effects on RFICs
- 17:30–19:00 RFIC Plenary CCC Four Seasons Ballroom
- 19:00-21:00 Welcoming Reception Featuring Symposium Showcase Hyatt Centennial Ballroom

Monday, 20 June 2022

- 07:00–19:00 Registration CCC Lobby A
- 07:00-08:00 Speakers' Breakfast --- CCC Four Seasons 1
- 08:00–09:40 RMo1A CCC 1A–1C: mm-Wave Transmitters and Receivers for Communication and 5G Applications RMo1B — CCC 1D–1F: Cryogenic and Advanced Front-End Circuits

RMo1C — CCC 4A–4C: Emerging Applications of RFICs in Quantum, Biomedical and Communication Systems

- 09:40–10:10 Coffee Break CCC Grand Concourse
- 10:10–11:50 RMo2A CCC 1A–1C: Multi-Gigabit Transceivers and Modules for Point-to-Point and Emerging Applications

RMo2B — CCC 1D–1F: Power Switches, Amplifiers and Power Dividers for mm-Wave and Sub-THz Applications

RMo2C — CCC 4A-4C: RF and mm-Wave Transmitters

- 12:00–13:30 RFIC Panel Session CCC 2C–3C: Industry vs. Academia: Who is Leading Whom?
- 13:30–15:10 RMo3A CCC 1A–1C: mm-Wave and Sub-THz Circuits and Systems for Radar Sensing and Metrology
 - RMo3B CCC 1D–1F: Mixed-Signal Building Blocks for Next-Generation Systems
 - RMo3C CCC 4A–4C: Frequency Generation Techniques for 5G and IoT
- 15:10–15:40 Coffee Break CCC Grand Concourse
- 15:40–17:00 RMo4A CCC 1A–1C: Power Amplifiers for 100+ GHz Applications RMo4B — CCC 1D–1F: Switch Technology, CMOS Reliability, and ESD RMo4C — CCC 4A–4C: RF, mm-Wave and Sub-THz VCOs

Tuesday, 21 June 2022

- 07:00–19:00 Registration CCC Lobby A
- 07:00–08:00 Speakers' Breakfast CCC Four Seasons 1
- 08:00-09:40 RTu1A --- CCC 1A-1C: mm-Wave and Wide Band Low-Noise CMOS Amplifiers
- RTu1B CCC 1D–1F: Efficiency Enhancement Techniques for Power Amplifiers
- 09:40–10:10 Coffee Break CCC Exhibit Hall
- 10:10–11:55 Student Forums CCC 1A–1C
- 12:00–13:30 RFIC/IMS Joint Panel Session CCC 4A–4C: Race to the Next G Ride the mmWave or Wave Goodbye!
- 13:30–15:10 RTu3A CCC 1A–1C: Circuits and Techniques for Full Duplex Transceivers RTu3B — CCC 1D–1F: mm-Wave/THz Devices and BIST/Calibration, and Circuits for Emerging Applications
- 15:10–15:40 Coffee Break CCC Exhibit Hall
- 15:40–17:00 RTu4A CCC 1A–1C: Emerging Wireless Communications RTu4B — CCC 1D–1F: Building Blocks for Next Generation Frequency Synthesis

RFIC Plenary, Reception, and Symposium Showcase Sunday Evening, 19 June 2022

17:30–19:00 RFIC Plenary Colorado Convention Center, Four Seasons Ballroom Chair: Osama Shana'a, MediaTek Co-Chair: Donald Y.C. Lie, Texas Tech University

- 17:30 Welcome Message from General Chair and TPC Chairs Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
- 18:00 *The Future of RFIC is Digital* Curtis Ling, MaxLinear
- 18:30 *RFICs into the Roaring 20's: Hot and Cold* Sorin P. Voinigescu, University of Toronto

19:00–21:00 RFIC Welcoming Reception Featuring Symposium Showcase Hyatt Regency Denver, Centennial Ballroom

The RFIC Interactive Reception starts immediately after the Plenary Session and will highlight the Student Paper Awards finalists, the Industry Paper Awards finalists, and the Systems and Applications Forum in an engaging social and technical evening event with food and drinks. Authors of these showcase papers will present their innovative work, summarized in poster format. Some showcase papers will also offer live demonstrations. You will not want to miss the RFIC Reception! This event is supported by the RFIC Symposium corporate sponsors.

RFIC Plenary Speaker 1



Dr. Curtis Ling Chief Technology Officer MaxLinear

The Future of RFIC is Digital

Abstract: The successful integration of high-performance communication systems in monolithic silicon over the past twenty years is the result of digital circuits becoming an integral part of the analog front end. An important focus of "digital + analog" chip design has been on circuit impairment suppression, which is to say, making analog circuits behave more ideally. Two important examples are the proliferation of direct conversion receivers in high performance applications (to the point of becoming almost passé); and linearization techniques integrated within transceiver signal paths. What will happen as technology scaling continues to feed digital performance without proportional improvements in RF? This talk will briefly examine the evolution and current state of communication systems-on-chips, highlighting the role of digitally-enabled analog in current state of the art; then explore ways in which digital + analog front ends might become increasingly relevant to systems design and network architecture.

About Dr. Curtis Ling

Curtis Ling, Ph.D. is a co-founder of MaxLinear and has served as Chief Technical Officer since April 2006. From March 2004 to July 2006, Dr. Ling served as Chief Financial Officer, and from September 2003 to March 2004, as a co-founder, he consulted for MaxLinear. From July 1999 to July 2003, Dr. Ling served as a principal engineer at Silicon Wave, Inc. From August 1993 to May 1999, Dr. Ling served as a professor at the Hong Kong University of Science and Technology. Dr. Ling received a B.S. in Electrical Engineering from the California Institute of Technology and an M.S. and Ph.D. in Electrical Engineering from the University of Michigan, Ann Arbor.

RFIC Plenary Speaker 2



Prof. Sorin P. Voinigescu Stanley Ho Chair of Microelectronics, Director of the VLSI Research Group, Professor of Electrical and Computer Engineering, University of Toronto

RFICs into the Roaring 20's: Hot and Cold

Abstract: In this talk, I will look ahead to the challenges and research problems RFIC designers will have to address through the end of the decade. With the end of III-V and silicon-based transistor performance scaling in sight, the push for higher operation frequency, bandwidth, data rate, and dynamic range will continue unabated for the main economic drivers in our field: radio, radar sensors, and for the fiberoptic infrastructure that enables all of them. With little fanfare, the baseband of fiberoptic systems is now approaching 100 GHz, higher than 5G and automotive radar carrier frequencies, with over 200 GS/s sampling rate required for ADCs and DACs. Adding AI elements to all these applications may lead us to the "metaverse", but the power consumption of each RFIC function will have to be drastically reduced if we do not wish to melt this "universe". The good news is that the high frequency performance of all transistor technologies improves by ~30% in the cold down to 70 Kelvin and remains excellent at 2 Kelvin. This will open niche markets for RFICs in space and quantum computing which are likely to grow rapidly. Classical computing, data centers, and AI will also greatly benefit from 77 Kelvin operation, improving speed and reducing the power consumption of the classical computation function. I will wrap up with examples of representative RFICs for all these applications and of the research problems that still need solutions.

About Prof. Sorin P. Voinigescu

Sorin P. Voinigescu is a Professor in the Electrical and Computer Engineering Department at the University of Toronto where he holds the Stanley Ho Chair in Microelectronics and is the Director of the VLSI Research Group. He is an IEEE Fellow and an expert on millimetre-wave, 100+Gbaud integrated circuits and atomic-scale semiconductor device technologies and has an established research and development track record in industry (Nortel, Quake Technologies, Peraso Technologies). He obtained his PhD degree in Electrical and Computer Engineering from the University of Toronto in 1994 and his M.Sc. Degree in Electronics and Telecommunications from the Polytechnical Institute of Bucharest in 1984.

The Student Paper Awards Finalists

Chair: Hua Wang, ETH Zürich Co-Chair: Gernot Hueber, Silicon Austria Labs

The RFIC Symposium's Student Paper Award is devised to both encourage student paper submissions to the conference as well as give the authors of the finalists' papers a chance to promote their research work with the conference attendees after the plenary session during reception time. A total of eleven outstanding student paper finalists were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of ten TPC judges have selected the top three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top-three Student Papers will be announced during the RFIC Plenary Session on 19 June 2022 in Denver. Each winner will receive an honorarium and a plaque. This year's Student Paper Awards finalists are (in no particular order):

A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45dB Blocker Rejection Ce Yang, Shiyu Su, Mike Shuo-Wei Chen University of Southern California, USA RMo1A-1

A Wireless Network of 8.8mm3 Bio-Implants Featuring Adaptive Magnetoelectric Power and Multi-Access Bidirectional Telemetry Zhanghao Yu, Wei Wang, Joshua C. Chen, Zhiyu Chen, Yan He, Amanda Singer, Jacob T. Robinson, Kaiyuan Yang Rice University, USA RMo1C-2

Multi-Beam, Scalable 28GHz Relay Array with Frequency and Spatial Division Multiple Access Using Passive, High-Order N-Path Filters Parham P. Khial, Samir Nooshabadi, Austin Fikes, Ali Hajimiri Caltech, USA RMo1C-4

A DC-to-18GHz SP10T RF Switch Using Symmetrically-Routed Series-TL-Shunt and Reconfigurable Single-Pole Network Topologies Presenting 1.1-to-3.2dB IL in 0.15μm GaAs pHEMT Zhaowu Wang, Zhenyu Wang, Tao Yang, Yong Wang UESTC, China RMo2B-1

A Sub-THz CMOS Molecular Clock with 20ppt Stability at 10,000s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration Mina Kim¹, Cheng Wang¹, Lin Yi², Hae-Seung Lee¹, Ruonan Han¹ ¹MIT, USA, ²Jet Propulsion Laboratory, USA RMo3A-1

- A 2MHz 4–48V VIN Flying-Capacitor Based Floating-Ground GaN DC-DC Converter with Real-Time Inductor Peak-Current Detection and 6µs Load Transient Response Weizhong Chen¹, Chang Yang¹, Lei Chen², Ping Gui¹ ¹Southern Methodist University, USA, ²Texas Instruments, USA RMo3B-5
- A 21.8–41.6GHz Fast-Locking Sub-Sampling PLL with Dead Zone Automatic Controller Achieving 62.7fs Jitter and -250.3dB FoM
 Wen Chen¹, Yiyang Shu¹, Huizhen Jenny Qian¹, Jun Yin², Pui-In Mak², Xiang Gao³, Xun Luo¹
 ¹UESTC, China, ²University of Macau, China, ³Zhejiang University, China RMo3C-2

A 38GHz Deep Back-Off Efficiency Enhancement PA with Three-Way Doberty Network Synthesis Achieving 11.3dBm Average Output Power and 14.7% Average Efficiency for 5G NR OFDM Xiaohan Zhang¹, Sensen Li², Daquan Huang², Taiyun Chi¹ ¹Rice University, USA, ²Samsung, USA

RTu1B-1

An Integrated Reconfigurable SAW-Less Quadrature Balanced N-Path Transceiver for Frequency-Division and Half Duplex Wireless Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen Technion, Israel RTu3A-1

 Fully Integrated Ultra-Wideband Differential Circulator Based on Sequentially Switched Delay Line in 28nm FDSOI CMOS
Jun Hwang, Byung-Wook Min Yonsei University, Korea RTu3A-4

E-Band CMOS Built-In Self-Test Circuit Capable of Testing Active Antenna Impedance and Complex Channel Response Seung-Uk Choi, Kyunghwan Kim, Kangseop Lee, Seunghoon Lee, Ho-Jin Song POSTECH, Korea RTu3B-2

<u>Student Paper Contest Eligibility</u>: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

The Industry Paper Awards Finalists

Chair: Gernot Hueber, Silicon Austria Labs Co-Chair: Hua Wang, ETH Zürich

The RFIC Industry paper awards highlight eight outstanding industry papers which are listed below. These papers received nominations for this recognition from the TPC sub-committees and godparents in a double-blind review. From these top eight papers, a two-stage double-blind review process was conducted with a committee of eight judges selected from the TPC that did not have conflict of interest. Finally, the Best Paper Chair and other key Steering Committee members finalize the top three winners after rigorous reviews and discussions. The top three winners will be announced during the RFIC Plenary Session on 19 June 2022. Each winner will receive a plaque and will be recognized in an upcoming Microwave Magazine article. This year's Industry Paper Awards finalists are (in no particular order):

A Linear High-Power Reconfigurable SOI-CMOS Front-End Module for WI-FI 6/6E Applications CEA-Leti, France

D. Parat, A. Serhan, P. Reynier, R. Mourot, A. Giry RM01B-5

- An All-Silicon E-Band Backhaul-on-Glass Frequency Division Duplex Module with >24dBm PSAT & 8dB NF Nokia Bell Labs, USA Shahriar Shahramian, Michael Holyoak, Mike Zierdt, Joe Weiner, Amit Singh, Yves Baeyens RMo2A-1
- A 0.2–2GHz Time-Interleaved Multi-Stage Switched-Capacitor Delay Element Achieving 448.6ns Delay and 330ns/mm2 Area Efficiency Sandia National Laboratories, USA Travis Forbes, Benjamin Magstadt, Jesse Moody, Andrew Suchanek, Spencer Nelson RMo3B-1
- DC to 12+GHz, +30dBm OIP3, 7.2dB Noise Figure Active Balun in 130nm BiCMOS for RF Sampling Multi-Gbps Data Converters Texas Instruments, USA Siraj Akhtar, Gerd Schuppener, Tolga Dinc, Baher Haroun, Swaminathan Sankaran RMo3B-2
- An F-Band Power Amplifier with Skip-Layer Via Achieving 23.8% PAE in FinFET Technology Intel, USA Qiang Yu, Jeffrey Garrett, Seahee Hwangbo, Georgios Dogiamis, Said Rami RMo4A-2
- A 2Gb/s 9.9pJ/b Sub-10GHz Wireless Transceiver for Reconfigurable FDD Wireless Networks and Short-Range Multicast Applications

¹Intel, USA, ²Intel, Mexico Renzhi Liu¹, Asma Beevi K. T.¹, Richard Dorrance¹, Timothy Cox¹, Rinkle Jain¹, Tolga Acikalin¹, Zhen Zhou¹, Tae-Young Yang¹, Johanny Escobar-Pelaez², Shuhei Yamada¹, Kenneth Foust¹, Brent Carlton¹ RTu3A-3 802.11ab Transmitter with -55dBr at ±3MHz and -58dBr at ±20MHz ACLR and 60dB 2nd-Order Harmonic Rejection for 470MHz ~ 790MHz TV White Space Band Devices Newracom, USA Seong-Sik Myoung, Jonghoon Park, Chang Hun Song, Ryun Woo Kim, Jaeyoung Ryu, Jeongki Choi, Hoai-Nam Nguyen, Seungyun Lee, Ilyong Jung, Jong-Han Lim, Sok Kyu Lee RTu4A-1

Class-C BAW Oscillator Achieving a Close-In FOM of 206.5dB at 1kHz with Optimal Tuning for Narrowband Wireless Systems Texas Instruments, USA

Bichoy Bahr, Danielle Griffith, Ali Kiaei, Thomas Tsai, Ryan Smith, Baher Haroun RTu4B-1

<u>Industry Paper Contest Eligibility</u>: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must present the paper at the symposium.

RFIC Reception and Symposium Showcase Featuring System & Application Demo Forum and Best Student/Industry Paper Showcase

Chair: Oren Eliezer, Ambiq Co-Chair: Hua Wang, ETH Zürich Co-Chair: Gernot Hueber, Silicon Austria Labs

The RFIC Interactive Reception, supported by the RFIC Symposium corporate sponsors, starts immediately after the Plenary Session and will highlight the Student and Industry Paper Awards finalists in an engaging social and technical evening event with food and drinks. Furthermore, additional authors, both from academia and from industry, who chose to showcase/demo their work will also be present. Twenty authors in total will present their innovative work on large monitors (in place of posters) and some will also offer live demonstrations. Make sure to attend this event, where you will be able to network and to plan on selected paper presentations that you will want to attend during the two days that follow.

Student Paper Awards Finalists' Showcase/Demonstrations

A Mil	<i>llimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter</i> <i>Achieving >45dB Blocker Rejection</i> Ce Yang, Shiyu Su, Mike Shuo-Wei Chen University of Southern California, USA RMo1A-1
A Win	reless Network of 8.8mm3 Bio-Implants Featuring Adaptive Magnetoelectric Power and Multi-Access Bidirectional Telemetry Zhanghao Yu, Wei Wang, Joshua C. Chen, Zhiyu Chen, Yan He, Amanda Singer, Jacob T. Robinson, Kaiyuan Yang Rice University, USA RMo1C-2
Mult	<i>i-Beam, Scalable 28GHz Relay Array with Frequency and Spatial Division Multiple Access Using Passive, High-Order N-Path Filters</i> Parham P. Khial, Samir Nooshabadi, Austin Fikes, Ali Hajimiri Caltech, USA RMo1C-4
A DC	-to-18GHz SP10T RF Switch Using Symmetrically-Routed Series-TL-Shunt and Reconfigurable Single-Pole Network Topologies Presenting 1.1-to-3.2dB IL in 0.15μm GaAs pHEMT Zhaowu Wang, Zhenyu Wang, Tao Yang, Yong Wang UESTC, China RMo2B-1

A Sub-THz CMOS Molecular Clock with 20ppt Stability at 10,000s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration Mina Kim¹, Cheng Wang¹, Lin Yi², Hae-Seung Lee¹, Ruonan Han¹ ¹MIT, USA, ²Jet Propulsion Laboratory, USA RMo3A-1

Sunday, 19 June 2022

19:00-21:00

Hyatt Centennial Ballroom

- A 2MHz 4–48V VIN Flying-Capacitor Based Floating-Ground GaN DC-DC Converter with Real-Time Inductor Peak-Current Detection and 6µs Load Transient Response
 Weizhong Chen¹, Chang Yang¹, Lei Chen², Ping Gui¹
 ¹Southern Methodist University, USA, ²Texas Instruments, USA RMo3B-5
- A 38GHz Deep Back-Off Efficiency Enhancement PA with Three-Way Doberty Network Synthesis Achieving 11.3dBm Average Output Power and 14.7% Average Efficiency for 5G NR OFDM Vischan Zhang, Songen Li², Damon Hugon², Tairan Chil

Xiaohan Zhang¹, Sensen Li², Daquan Huang², Taiyun Chi¹ ¹Rice University, USA, ²Samsung, USA RTu1B-1

An Integrated Reconfigurable SAW-Less Quadrature Balanced N-Path Transceiver for Frequency-Division and Half Duplex Wireless Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen Technion, Israel

RTu3A-1

Fully Integrated Ultra-Wideband Differential Circulator Based on Sequentially Switched Delay Line in 28nm FDSOI CMOS

Jun Hwang, Byung-Wook Min Yonsei University, Korea RTu3A-4

E-Band CMOS Built-In Self-Test Circuit Capable of Testing Active Antenna Impedance and Complex Channel Response Seung-Uk Choi, Kyunghwan Kim, Kangseop Lee, Seunghoon Lee, Ho-Jin Song POSTECH, Korea RTu3B-2

Industry Paper Awards Finalists' Showcase/Demonstrations

- A Linear High-Power Reconfigurable SOI-CMOS Front-End Module for WI-FI 6/6E Applications CEA-Leti, France D. Parat, A. Serhan, P. Reynier, R. Mourot, A. Giry RMo1B-5
- An All-Silicon E-Band Backbaul-on-Glass Frequency Division Duplex Module with >24dBm PSAT & 8dB NF Nokia Bell Labs, USA Shahriar Shahramian, Michael Holyoak, Mike Zierdt, Joe Weiner, Amit Singh, Yves Baeyens RMo2A-1
 - A 2Gb/s 9.9pJ/b Sub-10GHz Wireless Transceiver for Reconfigurable FDD Wireless Networks and Short-Range Multicast Applications ¹Intel, USA, ²Intel, Mexico Renzhi Liu¹, Asma Beevi K. T.¹, Richard Dorrance¹, Timothy Cox¹, Rinkle Jain¹, Tolga Acikalin¹, Zhen Zhou¹,

Tae-Young Yang¹, Johanny Escobar-Pelaez², Shuhei Yamada¹, Kenneth Foust¹, Brent Carlton¹ RTu3A-3

- A 0.2–2GHz Time-Interleaved Multi-Stage Switched-Capacitor Delay Element Achieving 448.6ns Delay and 330ns/mm2 Area Efficiency Sandia National Laboratories, USA Travis Forbes, Benjamin Magstadt, Jesse Moody, Andrew Suchanek, Spencer Nelson RMo3B-1
- DC to 12+GHz, +30dBm OIP3, 7.2dB Noise Figure Active Balun in 130nm BiCMOS for RF Sampling Multi-Gbps Data Converters Texas Instruments, USA Siraj Akhtar, Gerd Schuppener, Tolga Dinc, Baher Haroun, Swaminathan Sankaran RMo3B-2
- 802.11ab Transmitter with -55dBr at ±3MHz and -58dBr at ±20MHz ACLR and 60dB 2nd-Order Harmonic Rejection for 470MHz ~ 790MHz TV White Space Band Devices Newracom, USA Seong-Sik Myoung, Jonghoon Park, Chang Hun Song, Ryun Woo Kim, Jaeyoung Ryu, Jeongki Choi, Hoai-Nam Nguyen, Seungyun Lee, Ilyong Jung, Jong-Han Lim, Sok Kyu Lee RTu4A-1
 - An F-Band Power Amplifier with Skip-Layer Via Achieving 23.8% PAE in FinFET Technology Intel, USA

Qiang Yu, Jeffrey Garrett, Seahee Hwangbo, Georgios Dogiamis, Said RamiRMo4A-2

Class-C BAW Oscillator Achieving a Close-In FOM of 206.5dB at 1kHz with Optimal Tuning for Narrowband Wireless Systems Texas Instruments, USA

Bichoy Bahr, Danielle Griffith, Ali Kiaei, Thomas Tsai, Ryan Smith, Baher Haroun RTU4B-1

Systems and Applications Forum Showcase/Demonstrations

- Miniaturized Wirelessly Powered and Controlled Implants for Vagus Nerve Stimulation University of California, Los Angeles, USA Iman Habibagahi, Jaeeun Jang, Aydin Babakhani RMo1C-3
 - A 56.32Gb/s 16-QAM D-Band Wireless Link Using RX-TX Systems-in-Package with Integrated Multi-LO Generators in 45nm RFSOI CEA-Leti, France Abdelaziz Hamani, Francesco Foglia Manzillo, Alexandre Siligaris, Nicolas Cassiau, Frederic Hameau, Fabrice Chaix, Cedric Dehos, Antonio Clemente, José Luis Gonzalez-Jimenez RMo2A-5

RFIC Panel Session

Monday, 20 June 2022 12:00–13:30 Colorado Convention Center 2C–3C

Panel Sessions Chair: Mona Hella, Rensselaer Polytechnic Institute

Industry vs. Academia: Who is Leading Whom?

Pane	l Organizers and Moderators:
	Hossein Hashemi, University of Southern California
	Oren Eliezer, Ambiq

Panelists: Andreia Cathelin, STMicroelectronics Vadim Issakov, Technische Universität Braunschweig Waleed Khalil, The Ohio State University Ali Niknejad, University of California, Berkeley Joy Laskar, Maja Systems Stefano Pellerano, Intel

Abstract: This panel debates the roles of academia and industry in shaping the future of RFIC design. Given the increased complexity of modern RF integrated systems and the need for well trained RFIC engineers, the panel raises the question of who should lead RFIC research . If the industry is to take the lead, what is the role of universities and who should pay for training graduate students? Should academics move to other research domains? What should be done to prevent them from being lured away from universities and into financially rewarding industry careers? Are there fundamental RFIC research challenges that academics can still tackle for the next generation RF systems given the increasing complexities in design and fabrication of advanced RFICs?

The panel, formed of industry experts, university professors and those who crossed the line between academic and industry careers, will debate past, current and future RFIC research, education, and funding models with the audience's participation.

RFIC/IMS Joint Panel Session

Tuesday, 21 June 2022 12:00–13:30 Colorado Convention Center 4A–4C

Panel Sessions Chairs RFIC: Mona Hella, Rensselaer Polytechnic Institute IMS: Jasmin Grosinger, Technische Universität Graz Alan Brannon, CACI International

Race to the Next G - Ride the mmWave or Wave Goodbye!

Panel Organizers and Moderators: François Rivet, University of Bordeaux Aida Vera Lopez, Intel

Panelists: Khurram Muhammad, Samsung Shariar Shahramian, Nokia Bell Labs Emilio Calvanese, CEA-Leti John Strange, MediaTek Omar Bakr, Tarana Wireless Mike Noonen, MixComm Reza Arefi, Intel

Abstract: A Millimeter-Wave (mmW) 5G promises high capacity and low latency by tapping into the wide bandwidth available in the Ka-band. Although there are practical limitations when using such band for non-line-of-sight communication as well as difficulty in realizing energy-efficient and cost-effective circuitry, mobile operators and technology companies have been making considerable investments in developing and deploying mmW equipment, while few continue to bid on the C-band and are willing to pay tens of billions for a 160MHz slice in it.

Is now a good time to pause and reevaluate or is the global deployment of 5G mmW networks inevitable? What has the user experience with 5G networks been so far and what are the expectations for 6G and beyond? Do mmW mobile communications make engineering and economic sense and should we push for even higher bands (THz) in the next G?

This panel of international experts from various industry sectors and academia will discuss the technical practicality and economics of 5G mmW deployment, and assess the potential for use of even higher frequency bands (D-band and above) in next generation communications.

RFIC Student Forums Student Industry CHIPS Forum

Tuesday, 21 June 2022 10:10–11:00 Colorado Convention Center 1A–1C

Organizer: Jennifer Kitchen, Arizona State University

The snowball effect of the COVID-19 pandemic has led to an alarming global shortage in integrated circuits and severe disruptions in the production of goods that rely on semiconductor supply chains. On the other hand, we have witnessed radically increasing public attention and government/industry investments on semiconductor technologies, such as the CHIPS for America Act. While the semiconductor industry may envision an explosive growth in the next decade, the semiconductor tech industry leaders are struggling to attract and retain talent.

In this student forum prominent industry leaders will present the new technology trends in the semiconductor industry and their visions on the RFIC industry and its exciting future ahead. The purpose of this student forum is to introduce to graduate students and senior undergrads the possibilities in the RFIC industry and its potential to impact our lives.

Panelists: Alessandro Piovaccari, Università di Bologna Gary Xu, Samsung Research America Jeremy Dunworth, Qualcomm Andreia Cathelin, STMicroelectronics Shahriar Shahramian, Nokia Bell Labs Nadine Collaert, imec

RFIC Student Forums Student Entrepreneurship Forum

Tuesday, 21 June 2022 11:05–11:55 Colorado Convention Center 1A–1C

Organizer: Vadim Issakov, Technische Universität Braunschweig

Startup companies emerging from cutting-edge academic research have always been an integral component of the semiconductor industry and its continuous growth. However, there is lack of education on entrepreneurship and what it takes to establish a successful semiconductor startup company.

In this student forum entrepreneurs in the RFIC community will discuss the opportunities and challenges in RFIC based entrepreneurship and will share their personal experiences.

Panelists: Arun Natarajan, MixComm Bogdan Staszewski, Equal 1 Patrick Chiang, PhotonIC Technologies Yang Xu, InnoPhase Wouter Steyaert, Tusk IC

RFIC Technical Lecture

Sunday, 19 June 2022 11:45–13:15 Colorado Convention Center 601–603 Chair: Mohyee Mikhemar, Broadcom

Fundamentals of Noise, and Understanding its Effects on RFICs

Speaker: Asad A. Abidi, Professor, University of California, Los Angeles, USA



About Professor Asad A. Abidi

Abstract: Even circuit designers who are experienced with low noise design can find it difficult to explain how noise is quantified and analyzed. I will explain the formal methods of quantifying noise and illustrate their use in the design of a variety of common RF circuits. For linear time-invariant circuits such as small-signal amplifiers, noise transfer functions play a key role. For time-varying circuits such as passive mixers and LC oscillators, noise is in many cases injected in discrete time. Methods for the design continue to evolve towards greater simplicity, and I will present some of them. There is seldom a noise optimum in these circuits. It is usually a tradeoff, as I will show, between noise, large-signal linearity, and power dissipation.

Asad A. Abidi received the B.Sc. degree (Hons.) from Imperial College London, London, U.K., in 1976, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Berkeley, CA, USA, in 1978 and 1981, respectively. From 1981 to 1984, he was with Bell Laboratories, Murray Hill, NJ, USA, as a Member of the Technical Staff with the Advanced LSI Development Laboratory. Since 1985, he has been with the Department of Electrical Engineering, University of California, Los Angeles, CA, USA, where he is currently a Distinguished Chancellor's Professor. He also holds the Abdus Salam Chair at the Lahore University of Management Sciences (LUMS), Lahore, Pakistan. His research interests include fundamentals of circuit design, RF CMOS circuits, high-speed analog circuits, and data conversion.

Professor Abidi is a life fellow of the IEEE. He has been elected as a member of the U.S. National Academy of Engineering and a fellow of The World Academy of Sciences (TWAS). He received the IEEE Millennium Medal, the 1988 TRW Award for Innovative Teaching, the 1997 IEEE Donald G. Fink Award, the 2007 Lockheed-Martin Award for Excellence in Teaching, and the 2008 IEEE Solid-State Circuit Society's Donald O. Pederson Award. He was a co-recipient of the 2012 Best Paper Award in the IEEE Journal of Solid-State Circuits. He was named one of the top ten contributors to the ISSCC in its first 50 and 60 years. The University of California, Berkeley recognized him as a Distinguished EECS Alumnus in 2015. He was the Editor-in-Chief of the IEEE Journal of Solid-State Circuits from 1992 to 1995.

Monday, 20 June 2022 08:00–09:40 1A-1C

Session RMo1A: mm-Wave Transmitters and Receivers for Communication and 5G Applications

Chair: Hossein Hashemi, University of Southern California, USA Co-Chair: Jeyanandh Paramesh, Carnegie Mellon University, USA

RMo1A-1

A Millimeter-Wave Mixer-First Receiver with Non-Uniform Time-Approximation Filter Achieving >45dB Blocker Rejection

Ce Yang, Shiyu Su, Mike Shuo-Wei Chen; University of Southern California, USA

Abstract: This paper presents a non-uniform (NU) time-approximation filter (TAF) technique for a wireless receiver to reject unwanted blockers spectrally. The proposed NU-TAF leverages the alias-spreading property of NU sampling (NUS) and a TAF that approximates an FIR filter response in the time domain, achieving an overall flexible filter response with a higher attenuation factor. The filter response can be readily reconfigured by changing the NU sequence and/or the TAF waveform without adjusting the passive component value. Additionally, a quad-switch integrator is proposed to significantly reduce power consumption by sharing the current among the Gm cells. A proof-of-concept millimeter-wave receiver is implemented in 28nm CMOS. Thanks to the NU-TAF, the receiver prototype achieves >45dB blocker rejection with a 33.7-GHz carrier frequency. The EVM measures -30.9dB using a 100-MSymbol/s 64QAM signal in the presence of a 10dBc out-of-band blocker.

RMo1A-2

A 28GHz/39GHz Dual-Band Four-Element MIMO RX with Beamspace Multiplexing at IF in 65nm CMOS

Robin Garg¹, Paul Dania¹, Gaurav Sharma¹, Armagan Dascurcu², Soumya Gupta¹, Harish Krishnaswamy², Arun Natarajan¹; ¹Oregon State University, USA, ²Columbia University, USA **Abstract:** Dense-aperture mm-wave MIMO RX front-ends will require simplified IF interfaces, particularly when multiple 5G NR bands must be supported. The first dual-band 28 GHz and 39 GHz MIMO RX front-end with beam-space frequency-domain multiplexing (FDM) is presented that enables concurrent amplitude/phase weighted signal combining across four elements and 28 GHz/39 GHz bands. The FDM scheme places the four beam-space outputs at four different IF frequencies. The IC includes local multi-phase LO generation in each element, consumes 516mW (32.3 mW/beam/ element) and occupies 14mm² in 65-nm CMOS.

RMo1A-3

A Millimeter-Wave Front-End for FD/FDD Transceivers Featuring an Embedded PA and an N-Path Filter Based Circulator Receiver

Masoud Pashaeifar, Leo C.N. de Vreede, Morteza S. Alavi; Technische Universiteit Delft, The Netherlands

Abstract: This work presents an ultra-compact single-antenna FD/FDD transceivers front-end. It comprises a nonreciprocal circulator, RX, and an integrated power amplifier (PA). In the proposed circulator, we devise a ring quarter-wave transmission line topology with adjusted characteristic impedances to improve TX-to-antenna insertion loss and TX-to-RX isolation. Besides, an AND-gate switching-based N-path filter is proposed to realize the circulator's nonreciprocal gyrator while acting as a mixer-first RX. Owing to the ultra-compact N-path filter structure, the circulator occupies only 0.38mm² core area. Over a 27.1-to-31.1GHz band, the realized front-end offers >20dB TX-to-RX isolation while its measured TX-to-antenna insertion loss is $1.7 \sim 2.2$ dB. The RX path tolerates the PA's blocker signal, achieving 5dBm in-band and 13dBm out-of-band B_{LdB}. Moreover, the PA delivers 15.15dBm peak output power with 33% drain efficiency. Our front-end prototype occupies only 0.7mm², including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits.

RMo1A-4

A Ka-Band Dual Circularly Polarized CMOS Transmitter with Adaptive Scan Impedance Tuner and Active XPD Calibration Technique for Satellite Terminal

Dongwon You, Yun Wang, Xi Fu, Hans Herdian, Xiaolin Wang, Ashbir Fadila, Hojun Lee, Michihiro Ide, Sena Kato, Zheng Li, Jian Pang, Atsushi Shirane, Kenichi Okada; Tokyo Tech, Japan **Abstract:** An adaptive scan impedance tuner for varying impedance of array antenna along with the beam scan and calibration circuits for deteriorated cross-polarization are proposed for the low earth orbit (LEO) satellite terminal for earth observation application. With the proposed load tuner, TX power efficiency is improved to 11.7% from 6.5% at a VSWR=1:3 load condition where the same load point as the 50° scan angle. Furthermore, 18.1 dB and 16.4 dB of the cross-polarization discrimination (XPD) is recovered for the right-handed circular polarization calibration circuit with the modulated signal. Accordingly, the error vector magnitudes (EVM) are also improved by 12.2 dB and 14.8dB at the RHCP and the LHCP, respectively. To the best of the authors' knowledge, the proposed TX is the first reported work with the dual circular polarization transmitting mode measurement results in Ka-band for satellites.

RMo1A-5

A 8–30GHz Passive Harmonic Rejection Mixer with 8GHz Instantaneous IF Bandwidth in 45RFSOI

Amr Ahmed, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This work presents a passive harmonic rejection mixer which employs resistive scaling to maintain high linearity and to achieve 3rd and 5th harmonic rejection. The 8-phase 50% duty-cycle clocks are generated using polyphase filters without any clock dividers, and isolation between the 4 mixers is achieved using a Wilkinson network in the RF path. This enables the mixer to operate at mm-wave frequencies with wide instantaneous bandwidth, and greatly reduces the LO power consumption due to the much lower operating frequency of the LO network. The mixer is fabricated in the GlobalFoundries CMOS 45-RFSOI process and has a measured conversion loss of 12 dB with a 3-dB bandwidth of 8–30 GHz, and an IF instantaneous bandwidth of up to 8 GHz. The measured harmonic rejection ratio (HRR) at the 2nd, 3rd and 5th harmonics is better than 27 dBc across the entire bandwidth. An input P1dB of 4.2–7 dBm is achieved at 8–30 GHz due to the passive architecture. Application areas are in high linearity high-IF mm-wave 5G systems and wideband receivers.

Monday, 20 June 2022 08:00–09:40 1D-1F B: Cryogenic and Advanced From

Session RMo1B: Cryogenic and Advanced Front-End Circuits Chair: Emanuel Cohen, Technion, Israel Co-Chair: Ramesh Harjani, University of Minnesota, USA

RMo1B-1

A 4.2–9.2GHz Cryogenic Transformer Feedback Low Noise Amplifier with 4.5K Noise Temperature and Noise-Power Matching in 22nm CMOS FDSOI

Boce Lin¹, Hamdi Mani², Phil Marsh³, Richard Al Hadi⁴, Hua Wang¹; ¹Georgia Tech, USA, ²CryoElec, USA, ³Carbonics, USA, ⁴Alcatera, USA

Abstract: This paper presents a compact broadband cryogenic low noise amplifier (LNA) with simultaneous noise and power matching with transformer-based feedback. The LNA is composed of an input impedance transforming network and three-stage amplifiers to achieve simultaneous broadband low-noise and power matching. The first stage is a cascode amplifier with a drain source-coupled transformer. The second stage is a current-reuse broadband amplifier, and the third stage is an inductive-peaking cascode common-source amplifier. The LNA is packaged in a custom chassis and measured at 300K and 16K. At 300K probing measurement, the LNA achieves minimum noise Fig. of 1.42dB and S₁₁ < -10dB from 3.6–8.2 GHz with 34dB–35.9dB gain. The overall group delay is less than 0.3ns and IIP₃ is \geq -6dBm across the frequency range. At 16K, the LNA achieves a minimum noise Fig. (NF) of 0.065dB and NF < 0.3dB from 4.2–9.2 GHz with 31.4dB–34.7dB gain.

RMo1B-2

A 2.57mW 5.9-8.4GHz Cryogenic FinFET LNA for Qubit Readout

Jean-Olivier Plouchart, Dereje Yilma, John Timmerwilke, Sudipto Chakraborty, Kevin Tien, Alberto Valdes-Garcia, Daniel Friedman; IBM, USA

Abstract: A 5.9–8.4GHz LNA intended for use at cryogenic temperatures was implemented in a 14nm FinFET CMOS technology. At 4.1 K, peak LNA gain of 13.4dB is measured at 7.1GHz, with a 3dB bandwidth of 2.5GHz and power consumption of 2.1mW. Also, at 4.1K, measured noise figure from 6 to 8GHz is 0.53–0.57dB and the measured noise temperature is 37.6–41K; power consumption in this set of measurements was 2.57mW.

RMo1B-3

A Mixer-First Receiver Frontend with Resistive-Feedback Baseband Achieving 200MHz IF Bandwidth in 65nm CMOS

Benqing Guo¹, Haishi Wang¹, Yao Wang², Ke Li¹, Lei Li³, Wanting Zhou³; ¹CUIT, China, ²Zhengzhou University, China, ³UESTC, China

Abstract: A mixer-first receiver frontend with resistive-feedback baseband is proposed. The baseband combination of G_m and transimpedance amplifier (TIA) is designed to cover a wide frequency range for high data rate applications. The N-path filtering at the RF side and enhanced filtering at the BB side inhibit out-of-band blocker interferences. The receiver is fabricated in a 65 nm CMOS. Measurement results display an NF of 2.3 dB and a conversion gain of 33.5 dB at 2 GHz f_{LO} . The inband and out-of-band IIP3 are -7.5 dBm and 19 dBm respectively. The receiver core draws 34 mW in the signal path and occupies an active area of 0.31 mm².

RMo1B-4

A Feedback-Based N-Path Receiver with Reduced Input-Node Harmonic Response

Venkata S. Rayudu¹, Ki Yong Kim¹, David Z. Pan¹, Ranjit Gharpurey²; ¹University of Texas at Austin, USA, ²Independent Researcher, USA

Abstract: A downconversion receiver employing a switch-based N-path filter with reduced input harmonic response and harmonic translation from around the 3rd and the 5th LO harmonics is presented. The N-path filter employs 8 paths, and is embedded inside a harmonic-selective negative feedback loop. A pulse-width-modulated LO (PWM-LO) is used in the feedback upconverter to reduce the noise injected around the LO fundamental at the input of the N-path downconverter. The architecture is verified in a 65-nm CMOS technology. Approximately 15–18 dB reduction in the 3f_{LO} harmonic response, and 8–10 dB enhancement in harmonic-blocker 3-dB compression is observed in measurement. The use of a PWM-LO, instead of a rectangular clock in the upconverter, improves noise figure by nearly 4 dB.

RMo1B-5

A Linear High-Power Reconfigurable SOI-CMOS Front-End Module for WI-FI 6/6E Applications

D. Parat, A. Serhan, P. Reynier, R. Mourot, A. Giry; CEA-Leti, France

Abstract: This paper presents a high-power monolithic SOI-CMOS Front End-Module (FEM) supporting Wi-Fi 6/6E signals at 2.4GHz. The FEM includes an SP4T antenna switch, a power amplifier (PA), a low noise amplifier (LNA) with bypass mode, and a digital controller. The RX path achieves 15dB of power gain with less than 1.8dB of noise figure (NF) with 10mW of power consumption. The TX path delivers 33.4dBm of saturated output power (P_{sat}) with 51.7% of peak PAE and 28.5dB of power gain. Without DPD, the reconfigurable TX path achieves state-of-the art performance with 23.4/20dBm of linear output power (P_{out}) for an EVM of -35.1/-43.9dB and an operating current of 282/254mA for 802.11ac/ax MCS9/MCS11 40MHz signals.

Monday, 20 June 2022 08:00–09:40 4A-4C

Session RMo1C: Emerging Applications of RFICs in Quantum, Biomedical and Communication Systems Chair: Raja Pullela, MaxLinear, USA Co-Chair: Yao-Hong Liu, imec, The Netherlands

RMo1C-1

An Integrated Quantum Spin Control System in 180nm CMOS

Kaisarbek Omirzakhov, Mohamad Hossein Idjadi, Tzu-Yung Huang, S. Alexander Breitweiser, David A. Hopper, Lee C. Bassett, Firooz Aflatouni; University of Pennsylvania, USA

Abstract: Solid-state electron spins are key building blocks for emerging applications in quantum information science, including quantum computers, quantum communication links, and quantum sensors. However, solid-state spins are controlled using complex microwave pulse sequences, which are typically generated using benchtop electrical instruments. Integration of the required electronics will enable realization of a scalable low-power and compact optically addressable quantum system. Here, we report an integrated reconfigurable quantum control system, which is used to perform Rabi and Ramsey oscillation measurements for an NV center in diamond. The 180nm CMOS chip, fabricated within a footprint of 3.02mm², consumes 80 mW of power, and is capable of generating a tunable microwave signal from 1.6 GHz to 2.6 GHz modulated with a sequence of up to 4098 reconfigurable pulses with a pulse width adjustable from 10ns to 42ms and a pulse-to-pulse delay adjustable between 18 ns to 42m, at a resolution of 2.5 ns.

RMo1C-2

A Wireless Network of 8.8mm³ Bio-Implants Featuring Adaptive Magnetoelectric Power and Multi-Access Bidirectional Telemetry

Zhanghao Yu, Wei Wang, Joshua C. Chen, Zhiyu Chen, Yan He, Amanda Singer, Jacob T. Robinson, Kaiyuan Yang; Rice University, USA

Abstract: This paper presents a hardware platform for wireless mm-sized bio-implant networks, exploiting adaptive magnetoelectric power transfer and novel schemes for efficient bidirectional multi-access communication. The closed-loop power control mitigates power delivery fluctuations caused by distance and alignment change and avoids redundant power of the external transceiver. The system also enables simultaneous power and time-domain modulated downlink data with a 5% peak power transfer efficiency and a 62.3-kbps maximum data rate at 340-kHz carrier frequency; multi-access uplink of all the implants enabled by individually programmed IF with a 40-kbps maximum data rate at 31-MHz carrier frequency; and more than 6-cm distance between the implant and the external TRX.

RMo1C-3

Miniaturized Wirelessly Powered and Controlled Implants for Vagus Nerve Stimulation

Iman Habibagahi, Jaeeun Jang, Aydin Babakhani; University of California, Los Angeles, USA

Abstract: Multisite stimulation has shown enhanced clinical outcomes in different biomedical applications. This work presents a novel System on Chip (SoC) solution that enables up to 16 implantable stimulators to be powered and controlled using a single transmitter. The implants can be powered at 40.68MHz industrial, scientific and medical (ISM) band up to 80mm in air. Each implant can tolerate up to 70° misalignment between the Tx and Rx coil, and they provide two channels for constant voltage stimulation. The frequency, voltage, and pulse width are sent wirelessly using pulse width modulated amplitude shift keying (PWM-ASK) to each chip. The performance of implantable devices was verified by bilateral *in vivo* (pig) vagus nerve stimulation (VNS) and invitro measurements. The implant has a diameter of 14mm and weighs 80mg.

RMo1C-4

Multi-Beam, Scalable 28GHz Relay Array with Frequency and Spatial Division Multiple Access Using Passive, High-Order N-Path Filters

Parham P. Khial, Samir Nooshabadi, Austin Fikes, Ali Hajimiri; Caltech, USA

Abstract: A 28 GHz scalable relay array that independently re-routes multiple beamformed datachannels in different frequency bands is presented, allowing for frequency and spatial division multiple access. The array is implemented at the element-level with a 65 nm CMOS RFIC that has two transmit-and-receive branches. Each transmit-and-receive branch provides phase delay, true time delay, and amplitude control for up to 3 frequency channels independently and simultaneously. The baseband signal chain is enabled by a dual function N-path filter architecture that is passive and inductorless yet provides high-order filtering with complex roll-off and performs phase shifting. The resulting array consists of a 2-chip, 4-branch prototype that independently steers 3 frequency multiplexed incident data beams into different spatial directions, with true time delay control in each beam. A radiative measurement shows the router supporting a simultaneous throughput of 625 Mb/s 32-QAM data across 3 frequency channels that are independently spatially steered.

Monday, 20 June 2022 10:10–11:50 1A-1C

Session RMo2A: Multi-Gigabit Transceivers and Modules for Point-to-Point and Emerging Applications

Chair: Hongtao Xu, Fudan University, China Co-Chair: Qun Jane Gu, University of California, Davis, USA

RMo2A-1

An All-Silicon E-Band Backhaul-on-Glass Frequency Division Duplex Module with >24dBm PSAT & 8dB NF

Shahriar Shahramian, Michael Holyoak, Mike Zierdt, Joe Weiner, Amit Singh, Yves Baeyens; Nokia Bell Labs, USA

Abstract: E-band Backhaul-on-Glass Frequency Division Duplex (FDD) modules combining SiGe BiCMOS transceivers (TRX) and power amplifiers (PA) with glass-integrated RF splitting/combining and diplexing are presented. The TRX ICs operate at 71–76 GHz (Low-Band) and 81–86 GHz (High-Band). The TX PSAT and RX NF of the FDD modules on average measure 24dBm and 8dB across the two operating bands. Each FDD module supports TX constellations up to 1024-QAM (<2% EVM at 15dBm output) and data rates up to 24Gb/s (64-QAM at 20dBm output). Complete FDD measurements mimicking distances from 2km to 20km demonstrate bidirectional constellations up to 256-QAM and data-rates up to 24Gb/s.

RMo2A-2

Active Tunable Millimeter-Wave Reflective Surface Across 57–64GHz for Blockage Mitigation and Physical Layer Security

Suresh Venkatesh¹, Hooman Saeidi¹, Xuyang Lu², Kaushik Sengupta¹; ¹Princeton University, USA, ²UM-SJTU Joint Institute, China

Abstract: Millimeter-wave wireless networks allow for spatial multiplexing and high throughput. However, they are critically susceptible to blockages, channel propagation variations, and fading. To incorporate resilience in such networks, a class of reconfigurable surfaces realized with reflect-arrays have shown theoretical promise in reconfiguring the channel on demand, creating programmable non-line-of-sight (NLOS) paths, and providing a scalable solution compared to densification of base stations and access points. In this paper, we present a scalable approach towards realizing active surfaces with the ability to simultaneously receive, amplify, beamform, and re-transmit to the intended receiver (Rx) in a secure fashion. We demonstrate with the proof-of-concept 2D and 1D arrays realized with custom silicon ICs in a 65-nm CMOS process while the reception and retransmission is achieved through off-chip packaged dual-feed probe-fed patch antenna. Each chip incorporates two independent transceiver (TxRx) chains, with two-stage LNA and a 5-bit controlled 360° IQ phase shifter, collectively providing controllable gain of up to 15.2dB, P_{sat} of 4.2dBm at 60GHz, noise figure \approx 5–6dB, and supporting up to 20Gbps with 32-QAM constellation. With packaged 1D and 2D arrays, we demonstrate \pm 45° beamforming capability for various Tx positions closing links where simple reflective surfaces tend to fail. In addition, with spatio-temporal control over the surface, we also demonstrate physical layer security.

RMo2A-3

A 60GHz Phased Array Transceiver Chipset in 45nm RF SOI Featuring Channel Aggregation Using HRM-Based Frequency Interleaving

Armagan Dascurcu¹, Sohail Ahasan¹, Ali Binaie¹, Kuei Jih Lu², Arun Natarajan², Harish Krishnaswamy¹; ¹Columbia University, USA, ²Oregon State University, USA

Abstract: Channel aggregation at mm-wave enables extremely high data rates, but necessitates high-speed data converters. This paper presents an alternative approach leveraging HRM-based frequency interleaving (FI), which relaxes the requirements on the data converters, reducing their power consumption and cost. The implemented 45nm RF SOI chipset includes 4-element 60GHz phased-array RX and TX chips, and 4-channel TX and RX baseband (BB) FI channelizer chips, which channelize 8GHz of bandwidth (BW) over 59–67 GHz into 4 channels. Measured link results indicate that the BB FI channelizers and 60GHz phased array ICs together achieve sufficient SNDR in each channel to support 16-QAM and 64-QAM modulations over wide bandwidths, enabling wireless links at 32Gbps and beyond.

RMo2A-4

A 17Gb/s 10.7pJ/b 4FSK Transceiver System for Point to Point Communication in 65nm CMOS

Hamidreza Afzal, Cheng Li, Omeed Momeni; University of California, Davis, USA

Abstract: This paper presents a novel 145–185 GHz transceiver (TRX) with 4 frequency-shift keying (4FSK) modulation. The proposed non-coherent 4FSK design removes the need for separate modulator and demodulator blocks reducing the power consumption and complexity. The proposed TX generates four different RF frequencies based on the two parallel streams of binary input data, and the RX employs a slot power divider to divide the 4FSK RF signal into two paths, where the 4FSK RF signal is demodulated and data is recovered by enveloped detectors and digital buffers. Both the transmitter and receiver are fabricated in a 65 nm CMOS technology with a total core area of 0.6 mm². The TRX architecture achieves 17 Gb/s over 18 cm link distance while consuming only 182 mW power.

RMo2A-5

A 56.32Gb/s 16-QAM D-Band Wireless Link Using RX-TX Systems-in-Package with Integrated Multi-LO Generators in 45nm RFSOI

Abdelaziz Hamani, Francesco Foglia Manzillo, Alexandre Siligaris, Nicolas Cassiau, Frederic Hameau, Fabrice Chaix, Cedric Dehos, Antonio Clemente, José Luis Gonzalez-Jimenez; CEA-Leti, France

Abstract: This paper presents an energy-efficient wideband D-band wireless link using receiver (RX) and transmitter (TX) modules based on a channel-bonding scheme. The modules include RX and TX integrated circuits (ICs) fabricated in 45nm CMOS RFSOI technology. They are mounted on low-cost multi-layer printed circuit boards (PCBs) and connected to patch antennas. The RX and TX ICs are composed of two down-conversion and up-conversion chains, respectively, operating over contiguous sub-bands around 147.96 GHz. The required multiple millimeter-wave local oscillator signals (LOs) are generated on-chip. The presented wireless system achieves a data rate of 56.32 Gb/s by using 16 QAM modulation over 8 radiofrequency (RF) channels, with a competitive energy consumption (RX+TX) of 18 pJ/bit, including the LOs generation circuitry.

Monday, 20 June 2022 10:10-11:50 1D-1F

Session RMo2B: Power Switches, Amplifiers and Power Dividers for mm-Wave and Sub-THz Applications

Chair: Alyssa Apsel, Cornell University, USA Co-Chair: Domine Leenaerts, NXP Semiconductors, The Netherlands

RMo2B-1

A DC-to-18GHz SP10T RF Switch Using Symmetrically-Routed Series-TL-Shunt and Reconfigurable Single-Pole Network Topologies Presenting 1.1-to-3.2dB IL in 0.15 μ m GaAs pHEMT

Zhaowu Wang, Zhenyu Wang, Tao Yang, Yong Wang; UESTC, China

Abstract: As a rule of thumb, the number of throws, bandwidth (BW), and insertion losses (IL) limit each other in a single switch circuit. This paper proposes three topologies, i.e. symmetrically-routed structure, series-transmission-line-shunt unit, and reconfigurable matching network, to breakthrough these limits. Demonstrations show this work attains a single-pole ten-throw (SP10T) switch and achieves an impressive BW from DC-to-18 GHz with a favourable IL performance (1.1–3.2 dB) compared to prior arts. RF input power for 1-dB compression is 21.2 dBm, and isolation is higher than 24 dB.

RMo2B-2

A DC-120GHz SPDT Switch Based on 22nm FD-SOI SLVT NFETs with Substrate Isolation Rings Towards Increased Shunt Impedance

M. Rack, L. Nyssens, Q. Courte, D. Lederer, J.-P. Raskin; Université catholique de Louvain, Belgium **Abstract:** A DC–120 GHz SPDT switch is proposed using GlobalFoundries' 22FDX SIVT devices with improved substrate isolation rings. For mm-wave switch applications, 22FDX offers BFMOAT devices that include substrate isolation zones *beneath* them to reduce high-frequency shunt loss, though, compared to SIVT devices, this sacrifices the back-gate functionality, resulting in higher R_{on}C_{off}. This paper proposes and analyses substrate isolation zones implemented in ring-shapes *around* SIVT-FETs to reduce parasitic shunt admittance while preserving the back-gate. The resulting effective device boasts a low R_{on}C_{off} metric (thanks to an SIVT-FET core with back-gate) and simultaneously achieves high substrate impedance to the reference ground node (similar performance as BFMOAT-FETs). From such devices, a full SPDT switch was fabricated and characterized up to 130 GHz. Having less than 2.4 dB insertion loss and better than 22 dB isolation from DC to 120 GHz, it outperforms analogous SPDT modules implemented using conventional SIVT or BFMOAT FETs.
RMo2B-3

Analysis and Design of Dual-Peak G_{max}-Core CMOS Amplifier in D-Band Embedding a T-Shaped Network

Jiseul Kim, Chan-Gyu Choi, Kangseop Lee, Kyunghwan Kim, Seung-Uk Choi, Ho-Jin Song; POSTECH, Korea

Abstract: In order to overcome the performance limitation of CMOS technology at high frequencies above 100 GHz, the concept of maximum achievable gain (G_{max}) with an embedding network has been investigated. In this work, a novel G_{max} -core embedding a T-shaped gain-boosting network that provides two G_{max} -peaks is analyzed and demonstrated in the D-band with a 28-nm FD-SOI CMOS process. With the proposed topology, one can design the peak G_{max} frequencies and in/output impedances simultaneously as desired for high gain and broadband operation. The fabricated amplifier offers a peak small-signal gain and bandwidth of 14.5 dB and 26 GHz, respectively, with power consumption of 21.6 mW in 117–143 GHz.

RMo2B-4

280.2/309.2GHz, 18.2/9.3dB Gain, 1.48/1.4dB Gain-per-mW, 3-Stage Amplifiers in 65nm CMOS Adopting Double-Embedded-G_{max}-Core

Byeonghun Yun¹, Dae-Woong Park², Chan-Gyu Choi³, Ho-Jin Song³, Sang-Gug Lee¹; ¹KAIST, Korea, ²Kumoh National Institute of Technology, Korea, ³POSTECH, Korea

Abstract: This paper reports a sub-THz high-gain amplifier design technique which is more flexible and suitable for performance optimization based on a double-embedded- G_{max} -core. The double-embedded- G_{max} -core is implemented by adopting an additional linear, lossless, and reciprocal (LLR) network that satisfies the G_{max} -condition ($Y_{2Y}/Y_{12}=-G_{max}$) on to an N-stage pseudo- G_{max} -cores where each stage satisfies the stability factor $k_i=1$ and phase delay of $2m\pi/N$. Implemented in a 65nm CMOS, the three-stage 280.2 and 309.2 GHz amplifiers achieve power gains of 18.2 and 9.3 dB and gain-per-mW of 1.48 and 1.4 dB/mW, respectively.

RMo2B-5

4-Way 0.031mm² Switchable Bidirectional Power Divider for 5G mm-Wave Beamformers

Aniello Franzese¹, Renato Negra², Andrea Malignaggi¹; ¹IHP, Germany, ²RWTH Aachen University, Germany

Abstract: This paper presents a miniaturized bidirectional power divider (PD) which incorporates the function of a single-pole-double-throw (SPDT) switch in addition to its regular operation. Therefore, the new component can be used as a transmitting/receiving (TRx) switch. With the proposed solution, several PDs are removed, and the SPDT is integrated, thereby saving area and reducing the overall insertion loss (IL) in phased antenna arrays. Moreover, due to its compact size and simplified routing strategy, the design is also suitable whenever many TRx elements are required, i.e., especially for 5G mm-wave beamformers. A 4-way prototype has been fabricated in a 130-nm SiGe BiCMOS technology to validate the concept and occupies an effective area of 180×170 μ m². Measurements results show an IL of 3.1 dB at 28 GHz and isolation higher than 19 dB. In addition, phase and amplitude errors are lower than 3° and 0.2 dB, respectively. In conclusion, a device that integrates the functionalities of SPDTs and PDs is reported without increasing area occupation compared to state-of-the-art PDs and, therefore, paving the way for compact, costeffective beamformer chips.

Monday, 20 June 2022 10:10–11:50 4A-4C Session RMo2C: RF and mm-Wave Transmitters Chair: Debopriyo Chowdhury, Broadcom, USA

Co-Chair: Margaret Szymanowski, Crane Aerospace & Electronics, USA

RMo2C-1 A 4-to-9GHz IEEE 802.15.4z-Compliant UWB Digital Transmitter with Reconfigurable Pulse-Shaping in 28nm CMOS

Hua Chen¹, Zhenqi Chen², Rongde Ou², Run Chen², Zhaohui Wu¹, Bin Li¹; ¹SCUT, China, ²NewRadio Technology, China

Abstract: This paper presents an IEEE 802.15.4z standard-compliant UWB digital transmitter that features reconfigurable pulse-shaping. The proposed UWB pulse-shaping technique exploits programmable delay lines to achieve high spectrum efficiency and significant sidelobe suppression. An on-chip broadband matching network with a second-harmonic trap is implemented to protect the digital power amplifier (DPA) realized by thin-gate transistors. Implemented in a 28nm CMOS process with a supply voltage of 0.9V, the prototype chip can operate from 4 to 9 GHz at various pulse repetition rates (PRF) from 1 to 249.6 MHz with programmable signal bandwidths (500 ~ 1331 MHz). The measured transmitted waveform meets with IEEE 802.15.4z standard, and its spectrum efficiency is up to 59%. The output power is highly programmable with a peak value of 14.5 dBm.

RMo2C-2

A 23GHz RF-Beamforming Transmitter with >15.5dBm P_{sat} and >21.7% Peak Efficiency for Inter-Satellite Communications

Kaijie Ding, Dusan Milosevic, Vojkan Vidojkovic, Rainier van Dommele, Mark Bentum, Peter Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents a 23GHz RF-beamforming transmitter (TX) for inter-satellite communications. By combining a variable gain amplifier (VGA), a phase shifter (PS), and a four-inductor-coupling differential quadrature-signal (IQ) generator, a power-efficient design with high compactness is demonstrated. The chip is fabricated in a 130nm SiGe BiCMOS technology. It achieves a measured saturated output power (P_{sat}) of >15.5dBm and a peak TX efficiency of >21.7%, with 2.09° RMS phase error and >29.3dB maximum power gain. The realized mm-wave TX supports 64-QAM with a 900Mbps data rate, the Error Vector Magnitude (EVM) of 4.98% (-26.06dB), the Adjacent Channel Power Ratio (ACPR) of -30.1dBc, and TX efficiency of 8.52% are measured at 9.2dBm output power. The core area of this TX is 0.9mm × 0.23mm.

RMo2C-3

A Quadrature-Rotation Phased-Array Transmitter with 15-Bit Phase Tuning and 0/3/6/9/12/15-dB PBOs Efficiency Enhancement

Jie Zhou, Huizhen Jenny Qian, Bingzheng Yang, Xun Luo; UESTC, China

Abstract: In this paper, a 4-element digital-modulated phased-array transmitter (TX) based on quadrature switched/ floated-capacitor power amplifiers (SFCPAs) and reconfigurable switched-capacitor tuning lines (RSCTLs) is proposed. Phase shifting in each element is achieved by hybrid coarse and fine phase-tuning techniques. The SFCPAs with quadrature rotation is presented for coarse phase tuning, while the RSCTLs is used for fine phase tuning. To improve the efficiency at deep power back-off (PBO) peaks, a 4-to-1 reconfigurable transformer is introduced in the SFCPAs. Meanwhile, a 1-by-4 active power divider is utilized for isolation improvement among each elements. The proposed phased-array TX is implemented in conventional 40-nm CMOS technology. The fabricated phased-array TX features 28.4dBm peak output power and 37.9% peak system efficiency. In addition, it supports 0/3/6/9/12/15-dB PBOs efficiency enhancement and 15-bit phase-tuning resolution.

RMo2C-4

An E-Band CMOS Direct Conversion IQ Transmitter for Radar and Communication Applications

Seunghoon Lee¹, Kyunghwan Kim¹, Kangseop Lee¹, Sungmin Cho¹, Seung-Uk Choi¹, Jayol Lee², Bontae Koo², Ho-Jin Song¹; ¹POSTECH, Korea, ²ETRI, Korea

Abstract: This paper presents an E-band direct conversion IQ transmitter (TX) with IQ calibration for joint radar-communications system. To generate high-quality digitally modulated signal and frequency-modulated continuous-wave (FMCW) radar chirp signal, I/Q calibration capability is integrated in the TX with a miniaturized hybrid coupler and variable capacitors. The measured image rejection ratio and LO feedthrough suppression, which are critical for both communication and FMCW signal generation, are better than 36 and 23 dB, respectively, in the range of 74–83 GHz. The TX successfully generates not only a 24-Gb/s 16-QAM modulated signal but also a FMCW modulated signal with 1 GHz bandwidth. Moreover, as the LO frequency is tuned from around 74 GHz to 83 GHz, 16-QAM with EVM around -22 dB is measured. The output P1dB and conversion gain of the TX are 9.8 dBm and 12 dB, respectively.

Monday, 20 June 2022 13:30–15:10

1**A-1C**

Session RMo3A: mm-Wave and Sub-THz Circuits and Systems for Radar Sensing and Metrology

Chair: Vito Giannini, Uhnder, USA

Co-Chair: Vadim Issakov, Technische Universität Braunschweig, Germany

RMo3A-1

A Sub-THz CMOS Molecular Clock with 20ppt Stability at 10,000s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration

Mina Kim¹, Cheng Wang¹, Lin Yi², Hae-Seung Lee¹, Ruonan Han¹; ¹MIT, USA, ²Jet Propulsion Laboratory, USA

Abstract: This paper presents a dual-loop chip-scale molecular clock (CSMC), which enhances the Allan Deviation performance by combining high signal-to-noise ratio of using fundamental mode and long-term stability of using higher order modes in derivative molecular absorption spectroscopy. In addition, digital frequency-error integration is adopted in the frequency-locked loop to provide an infinite open-loop DC gain, which fully suppresses any frequency drift caused by the temperature-sensitive crystal oscillator. This new generation CSMC is implemented in 65-nm CMOS, and achieves 20 ppt (part-per-trillion) Allan Deviation at 10,000 s averaging time with 71-mW power consumption.

RMo3A-2

A Small-Area, Low-Power 76–81GHz HBT-Based Differential Power Detector for Built-In Self-Test in Automotive Radar Applications

Yannick Wenger¹, Herman Jalli Ng², Falk Korndörfer³, Bernd Meinerzhagen¹, Vadim Issakov¹;

¹Technische Universität Braunschweig, Germany, ²Hochschule Karlsruhe, Germany, ³IHP, Germany **Abstract:** This paper presents a differential power detector for automotive radar applications based on the nonlinearity of a SiGe HBT. Compared to other commonly used detectors, this architecture achieves true measurement of the differential-mode power by applying the differential input signal over the base-emitter diodes of complementary bipolar transistors. A competitive dynamic range of 30 dB is reached. Because of its low power consumption of only 0:5 mW and small active area of 0:005 mm², the detector is well-suited for built-in self-test applications. To the authors' best knowledge this is the only true differential power detector in the 76 GHz to 81 GHz automotive radar band. Measurements over the complete automotive temperature range and the detector's sensitivity to process variation are reported.

RMo3A-3

A Compact 28nm FD-SOI CMOS 76–81GHz Automotive Band Receiver Path with Accurate 0.2° Phase Control Resolution

Antoine Le Ravallec¹, Patrice Garcia¹, João Carlos Azevedo Gonçalves¹, Loïc Vincent², Jean-Marc Duchamp³, Philippe Benech³; ¹STMicroelectronics, France, ²CIME Nanotech, France, ³G2Elab (UMR 5269), France

Abstract: This paper presents a 76–81 GHz receiver path for automotive radar applications in 28nm FD-SOI CMOS technology. It introduces a new accurate phase control using MOS varactors. The proposed solution implemented in the front-end low noise amplifier (LNA) allows a phase control of maximum 22° with a 0.2° resolution for minimum degradation of the LNA and the receiver performances. The receiver contains a two-stage LNA with 5.5 dB noise figure (NF), a passive mixer, a local oscillator (LO) driver and a baseband (BB) amplifier. The receiver exhibits input compression points (ICP1dB) of -25.2 dBm and -12.6 dBm with and without BB amplifier, respectively. The active area of the receiver path is only 0.057 mm² for a total power consumption of 41.7 mW.

RMo3A-4

An E-Band Phase Modulated Pulse Radar SoC with an Analog Correlator

Wen Zhou, Yahya Tousi; University of Minnesota, USA

Abstract: This paper presents a bi-static integrated pulse radar in the E-band based on a digitally modulated transmitter and an analog processing receiver module. The proposed frontend correlator operates at 1Gbps and uses a 1.5-bit sampler to compress the sensing data, enabling a low-speed and energy-efficient digital backend while delivering a high range resolution. The TSMC 65nm chip prototype has a 1.5mm×1.3mm area and consumes a total of 407mW with only 38mW corresponding to the analog baseband and digital backend. Over-the-air measurements at the 66GHz carrier frequency indicate the measured distance from the correlator output has an RMS error of 11.6cm and the integral non-linearity is less than 10cm across the entire target range, demonstrating the state-of-the-art range resolution with superior energy efficiency.

RMo3A-5

A 29-to-36GHz 4TX/4RX Dual-Stream Phased-Array Joint Radar-Communication CMOS Transceiver Supporting Centimeter-Level 2D Imaging and 64-QAM OTA Wireless Link

Fuyuan Zhao¹, Wei Deng¹, Rui Wu², Haikun Jia¹, Qixiu Wu¹, Jihao Xin², Zhiyuan Zeng², Yanlei Li², Zhihua Wang³, Baoyong Chi¹, ¹Tsinghua University, China, ²CAS, China, ³RITS, China

Abstract: This paper introduces a Ka-band 4-channel dual-stream phased-array joint radarcommunication transceiver for the future radar-communication integrated wireless system. In order to enhance the signal to noise and distortion ratio in low input signal region and reduce the chip area, a current-flopping bi-directional active mixer is proposed. A variable-transmission-line-based phase shifter with tilting structure is introduced to achieve wide-band phase shifting and mitigate the in-band loss fluctuation. The proposed transceiver is designed and implemented in a 65nm CMOS technology. The chip area is 16.2 mm². The measured TX peak saturated output power is 19.9 dBm and the output 1 dB compression point is 17.4 dBm. The measured RX minimum noise figure is 4.8 dB. System measurement results indicates that the proposed transceiver supports real-time centimeter-level 2D imaging and 400-Msym/s 64-QAM over-the-air (OTA) wireless link.

Monday, 20 June 2022

13:30-15:10

1**D-**1F

Session RMo3B: Mixed-Signal Building Blocks for Next-Generation Systems

Chair: Subhanshu Gupta, Washington State University, USA Co-Chair: Bahar Jalali Farahani, Cisco, USA

RMo3B-1

A 0.2–2GHz Time-Interleaved Multi-Stage Switched-Capacitor Delay Element Achieving 448.6ns Delay and 330ns/mm² Area Efficiency

Travis Forbes, Benjamin Magstadt, Jesse Moody, Andrew Suchanek, Spencer Nelson; Sandia National Laboratories, USA

Abstract: A 0.2–2 GHz digitally programmable RF delay element based on a time-interleaved multi-stage switched-capacitor (TIMS-SC) approach is presented. The proposed approach enables hundreds of ns of broadband RF delay by employing sample time expansion in multiple stages of switched-capacitor storage elements. The delay element was implemented in a 45 nm SOI CMOS process and achieves a 2.55–448.6 ns programmable delay range with <0.12% delay variation across 1.8 GHz of bandwidth at maximum delay, 2.42 ns programmable delay steps, and 330 ns/mm² area efficiency. The device achieves 24 dB gain, 7.1 dB noise figure, and consumes 80 mW from a 1 V supply with an active area of 1.36 mm².

RMo3B-2

DC to 12+GHz, +30dBm OIP3, 7.2dB Noise Figure Active Balun in 130nm BiCMOS for RF Sampling Multi-Gbps Data Converters

Siraj Akhtar, Gerd Schuppener, Tolga Dinc, Baher Haroun, Swaminathan Sankaran; Texas Instruments, USA

Abstract: An active balun using dual stage feedback and distributed feedforward distortion cancellation for use as a driver amplifier for wideband RF sampling ADCs is presented. With a gain of 16.5dB and HD2 of 60dBc while delivering 3dBm (100 Ω), the DC coupled balun achieves a linear-bandwidth of >12GHz holding OIP3>27dBm and NF<8dB, and small-signal bandwidth of 18GHz with <±0.5dB amplitude and <±2.5° phase imbalance. Cascaded balun + ADC measurements demonstrate no linearity limitation, while allowing for 19.5dB lower input signal. Occupying 1mm² in a 130nm BiCMOS process, the device consumes 100mA from 5V in a 2×2mm² flip chip QFN package.

RMo3B-3

An 11GS/s 2×10b 20–26GHz Modulator Using Segmented Non-Linear RF-DACs and Non-Overlapping LO Signals

Victor Åberg¹, Christian Fager¹, Rui Hou², Lars Svensson¹; ¹Chalmers University of Technology, Sweden, ²Ericsson Research, Sweden **Abstract:** We present a Cartesian I/Q modulator based on dual 10-bit RF-DACs. Non-overlapping LO signals and a segmented RF-DAC architecture with scaled bit currents contribute to good linearity and allow low-complexity DPD. Unit-cell flip-flops with a balanced clock distribution enable a high sample rate. Drive slope control for data switches reduce out-of-band emissions. Implemented in 22nm FDSOI CMOS, the modulator operates up to 26GHz with a maximum sample rate of 11 GS/s. The modulator is used to demonstrate transmission of a 64QAM signal at 13.2 Gb/s, a 256QAM signal at 7.33 Gb/s, and an OFDM signal comprising four aggregated 400-MHz 64QAM channels at an EVM of 6.43%. The results demonstrate the potential of the proposed modulator architecture for realization of ultra wideband transmitters for high performance mm-wave systems.

RMo3B-4

A 345 μ W 1GHz Process and Temperature Invariant Constant Slope-and-Swing Ramp-Based 7-Bit Phase Interpolator for True-Time-Delay Spatial Signal Processors

Soumen Mohapatra, Chung-Ching Lin, Mohammad Chahardori, Erfan Ghaderi, Md Aminul Hoque, Subhanshu Gupta, Deukhyoun Heo; Washington State University, USA

Abstract: In the baseband time delay (TD) elements used for delay compensation in discrete-time beamformers, phase interpolator (PI) plays a crucial role as the resolution of the PI defines the delay resolution of the TD. In this paper, we present a process and temperature invariant high-resolution and highly linear low-power PI. The proposed PI uses current integration which generates an adaptable constant slope-and-swing ramp signal to achieve low power. By switched-capacitor bias generation, the PI linearity is enhanced with 0.2 LSB DNL and 0.3 LSB INL, respectively. The 7-bit PI is realized in 65nm CMOS technology can generate the full range delay with a resolution of 8psec with the input of 1GHz. The PI consumes a power of 345µW and occupies an active area of 0.021mm².

RMo3B-5

A 2MHz 4–48V V_{IN} Flying-Capacitor Based Floating-Ground GaN DC-DC Converter with Real-Time Inductor Peak-Current Detection and 6μ s Load Transient Response

Weizhong Chen¹, Chang Yang¹, Lei Chen², Ping Gui¹; ¹Southern Methodist University, USA, ²Texas Instruments, USA

Abstract: This paper presents a 2MHz 4V-to-48V VIN, GaN-based buck-boost converter with optimized buck-boost mode, enhanced safe protection, and fast transient response for automotive Advanced Driving Assistant Systems (ADAS). A flying-capacitor-based floating-ground topology is proposed first time to solve the issue associated with extremely short on time, improve power efficiency in the buck-boost region and provide real-time detection and management of the inductor peak current. This floating-ground technique helps alleviate the problem of efficiency drop in the four-switch buck-boost topology and ensures converter/load safety. An indirect current sensor is also proposed, which allows for sensing the inductor current change in the buck-boost mode without using any bulky sensing resistors and achieves 6µs fast transient response with 100mv-undershoot/80mV-overshoot for 1A load current change. This converter achieves a maximum efficiency of 92% which is comparable to the state-of-the-art buck-boost schemes.

Monday, 20 June 2022 13:30-15:10 4A-4C

Session RMo3C: Frequency Generation Techniques for 5G and IoT Chair: Wanghua Wu, Samsung, USA Co-Chair: Andreia Cathelin, STMicroelectronics, France

RMo3C-1

Open-Source Fully-Synthesizable ADPLL for a Bluetooth Low-Energy Transmitter in 12nm FinFET Technology

Kyumin Kwon, Omar Abdelatty, David D. Wentzloff; University of Michigan, USA

Abstract: In this work, we present an open-source fully-synthesizable fractional-N ADPLL designed for a Bluetooth Low-Energy (BLE) transmitter (TX). A highly automated design flow is used to lower the barrier for new developers and to reduce porting cost. In the PLL, a novel two-step TDC (TSTDC) is proposed, which is amenable to P&R, and uses an embedded TDC (EMBTDC) and vernier delay-line TDC (DLTDC) as coarse and fine TDCs, respectively. This combination reduces the required DLTDC input time range by $5\times$ and is used to measure and compensate the P&R induced non-linearity of the EMBTDC. The PLL is fabricated in 12-nm FinFET and demonstrated in a BLE-TX. BLE transmissions satisfy the standard requirements thanks to the reduced fractional spurs by abovementioned techniques. In a standalone PLL mode, the TSTDC reduced fractional spurs by 6.8 dB compared to an EMBTDC alone, and the proposed LUT-based calibration further reduced spurs by 7.5 dB in near-integer operation. The PLL supports frequency range of 1.8-2.7GHz and consumes 3.91mW at 2.4006 GHz, with a 40MHz reference, occupying area of 0.063mm².

RMo3C-2

A 21.8–41.6GHz Fast-Locking Sub-Sampling PLL with Dead Zone Automatic Controller Achieving 62.7fs Jitter and -250.3dB FoM

Wen Chen¹, Yiyang Shu¹, Huizhen Jenny Qian¹, Jun Yin², Pui-In Mak², Xiang Gao³, Xun Luo¹; ¹UESTC, China, ²University of Macau, China, ³Zhejiang University, China

Abstract: In this paper, a wideband fast-locking millimeter-wave (mmW) sub-sampling PLL (SSPLL) with low jitter is proposed. A quadrature sub-sampling phase detector (QSSPD)-based dead zone automatic controller (DZAC) is introduced to automatically switch on the frequency-locked loop (FLL) for fast-locking. Here, the long locking time caused by the dead zone of FLL is eliminated. The mmW quad-mode oscillator is integrated in the SSPLL to achieve the low jitter within a wide frequency range. The proposed SSPLL is fabricated in a 40-nm CMOS technology. Measurements exhibit a frequency tuning range of 62.5% from 21.8 to 41.6GHz. The SSPLL achieves a 62.7 to 79.1fs rms jitter within the frequency tuning range. Besides, the typical power consumption is 23.6mW, leading to a PLL FOM of -248.3 to -250.3dB. Meanwhile, the proposed SSPLL achieves more than $8.9 \times$ locking time improvement. The PLL occupies a core area of 0.18mm².

RMo3C-3 A 59fs-rms 35GHz PLL with FoM of -241dB in 0.18 μ m BiCMOS/SiGe Technology

Rajath Bindiganavile, Asif Wahid, Jacob Atkinson, Armin Tajalli; University of Utah, USA

Abstract: A wideband and ultra low-noise Phase-Locked Loop (PLL) circuit is designed and implemented in a 0.18 μ m BiCMOS/SiGe technology to operate at a nominal frequency of 35.68 GHz. Incorporating a multi-phase phase frequency detector along with a high frequency reference signal, the bandwidth of the PLL was maximized to reduce the phase noise and jitter contribution of the forward path loop components within the frequency band of interest. A multi-phase phase comparator also relaxes the constraints imposed by the sampling nature of the PLL, allowing for a more convenient performance optimization with reduced jitter peaking and more optimal loop characteristics. The PLL was measured to have a Phase Noise of -113.3 dBc/Hz at an offset frequency of 1 MHz, and a total integrated jitter of 59 fs-rms integrated from 1 kHz to 100 MHz, consuming 194.6 mW with a jitter-power FoM -241.6 dB. The power dissipation of the proposed PLL is lower than implementations in similar technology nodes, while obviously higher than designs made in advanced CMOS/FinFET technologies. The PLL has been designed in BiCMOS/SiGe 0.18 μ m, aiming to be integrated together with power amplifiers in a 3D structure targeted for the next generation 5G systems.

RMo3C-4

A 14GHz-Band Harmonic Tuned Low-Power Low-Phase-Noise VCO IC with a Novel Bias Feedback Circuit in 40nm CMOS SOI

Mengchu Fang, Toshihiko Yoshimasu; Waseda University, Japan

Abstract: In this paper, a harmonic tuned low-power low-phase-noise VCO IC with a novel bias feedback circuit is proposed. The transformer-based LC tank providing high impedance at the second and third harmonics is used to improve the phase noise performance. In addition, a novel feedback circuit is designed to suppress the gate-to-source voltage of the core transistors under their threshold voltage at the steady state while guaranteeing the robust start-up of the oscillation. The novel feedback circuit that requires no dc power supply can operate with an extremely small additional dc power consumption. The proposed VCO IC is designed, fabricated, and fully evaluated on-wafer in 40-nm CMOS SOI process. The proposed VCO IC has exhibited a measured best phase noise of -131.8 dBc/Hz at 10-MHz offset from the oscillation frequency of 14.94 GHz under a dc power consumption of only 1.4 mW.

RMo3C-5

A 5G 65nm PD-SOI CMOS 23.2-to-28.8GHz Low-Jitter Quadrature-Coupled Injection-Locked Digitally-Controlled Oscillator

Romane Dumont¹, Magali De Matos², Andreia Cathelin¹, Yann Deval²; ¹STMicroelectronics, France, ²IMS (UMR 5218), France

Abstract: A low-phase-noise mm-W low-power quadrature differentially injection-locked digitallycontrolled oscillator (QILDCO) is presented. This work adopts a differential injection to enable a trade-off between phase noise performance and power consumption. Switched-capacitor banks and active devices are integrated inside the inductor loop to reduce the active area. The total active area is 0.109 mm² including harmonic extractors and buffers (excluding I/O pads). The proposed oscillator is supporting two 5G mm-W bands below 30 GHz with a tuning range of 21.3%. The prototype has been implemented in 65-nm Partially-Depleted SOI (PD-SOI) CMOS process. It achieves best stateof-the-art jitter of 25.6 fs while consuming 22 mW from a 1 V supply voltage.

Monday, 20 June 2022 15:40–17:00 1A-1C Session RMo4A: Power Amplifiers for 100+ GHz Applications

Chair: Jennifer Kitchen, Arizona State University, USA Co-Chair: Steven Callender, Intel, USA

RMo4A-1

A 22nm FD-SOI CMOS 2-Way D-Band Power Amplifier Achieving PAE of 7.7% at 9.6dBm OP1dB and 3.1% at 6dB Back-Off by Leveraging Adaptive Back-Gate Bias Technique

Elham Rahimi¹, Farhad Bozorgi², Gernot Hueber³; ¹Keysight Technologies, Germany, ²Barkhausen Institut, Germany, ³Silicon Austria Labs, Austria

Abstract: This work presents a 2-way 3-stage D-band Power Amplifier (PA) in 22nm FD-SOI technology. A dynamic 3-stage bias scaling technique is proposed for this PA. It is based on leveraging the back-gate terminal in CMOS FD-SOI technology to optimize the power consumption of each stage adaptive to the input power of the PA, and hence improve its overall PAE in the linear range, i.e. at OP1dB and power back-off. The PA has been fabricated on a die with the core area of 0.16mm². Small signal and large signal characteristics of the PA chip have been measured. At 1V supply voltage and frequency of 135GHz, it provides 14.2dB power gain with 20GHz and 52GHz 3-dB and 6-dB bandwidth, respectively. Measurement results show this PA achieves 7.7% and 3.1% PAE at 9.6 dBm OP1dB and 6dB back-off that features >1.5× and >2× improvement, respectively, compared to the state-of-the-art D-band PAs in CMOS technologies.

RMo4A-2

An F-Band Power Amplifier with Skip-Layer Via Achieving 23.8% PAE in FinFET Technology

Qiang Yu, Jeffrey Garrett, Seahee Hwangbo, Georgios Dogiamis, Said Rami; Intel, USA

Abstract: This paper presents an F-band power amplifier (PA) designed using novel back-endof-line (BEOL) in Intel 16 technology. In the PA transistor array, skip-layer vias which directly connect transistor to thick metal layers are used to reduce parasitics from BEOL and improve the PA performance. This 2-stage PA shows excellent peak PAE and gain per stage. At 110GHz, the measured P_{sat} peak PAE, linear power gain, and OP1dB are 11.8dBm, 23.8%, 17.1dB, and 9.2dBm, respectively. The core area of the PA is 0.023mm², enabling compact integration into phased array or waveguide based transceivers. To the authors' knowledge, this is the first circuit demonstration using skip-layer via that operates beyond 100GHz.

RMo4A-3

A 97–107GHz Triple-Stacked-FET Power Amplifier with 23.7dB Peak Gain, 15.1dBm P_{sar} , and 18.6% PAE_{MAX} in 28nm FD-SOI CMOS

Kyunghwan Kim, Kangseop Lee, Seung-Uk Choi, Jiseul Kim, Chan-Gyu Choi, Ho-Jin Song; POSTECH, Korea

Abstract: A 97–107 GHz power amplifier (PA) based on a stacked-FET topology is presented. In a triple-stacked-FET structure, stacking efficiency is analyzed using four combinations of series or shunt inductors for compensating phase of impedances between stack nodes, and optimal inductances are chosen. Phase-compensation inductors are implemented by considering a finite quality factor with the tradeoff between layout size and stacking efficiency. A layout of a transistor cell is customized to reduce gate resistance. The triple-stacked-FET PA provides peak P_{SAT} and PAE_{MAX} of 15.1 dBm and 18.6%, respectively. The presented PA achieves the highest power density and efficiency compared to state-of-the-art CMOS PAs in F-band.

RMo4A-4

A 124–152GHz >15dBm P_{sat} 28nm CMOS PA Using Chebyshev Artificial-Transmission-Line-Based Matching for Wideband Power Splitting and Combining

Jincheng Zhang¹, Tianxiang Wu¹, Yong Chen², Junyan Ren¹, Shunli Ma¹; ¹Fudan University, China, ²University of Macau, China

Abstract: This paper presents a 124–152 GHz power amplifier (PA) with >15 dBm saturation output power (P_{sat}) in a 28-nm CMOS process. Low-coupling transformer-based fourth-order matching networks are used to extend the bandwidth (BW) with low insertion loss and compact area. A four-way Chebyshev-type artificial-transmission-line-based power combiner is proposed to further improve the output power without sacrificing BW. The measurement results show that this PA can achieve a peak gain of 22.6 dB with 28 GHz 3-dB BW. The in-band P_{sat} is >15 dBm with a maximum output power of 16.2 dBm at 135 GHz. The total area of the chip is 0.66×0.73 mm².

Monday, 20 June 2022 15:40–17:00 1D-1F 3: Switch Technology, CMOS Relia

Session RMo4B: Switch Technology, CMOS Reliability, and ESD Chair: Alvin Joseph, GlobalFoundries, USA Co-Chair: Edward Preisler, Tower Semiconductor, USA

RMo4B-1

Advanced 200mm RF SOI Technology Exhibiting 78fs $R_{_{ON}} \times C_{_{OFF}}$ and 3.7V Breakdown Voltage Targeting Sub 6GHz 5G FEM

F. Gianesello, A. Fleury, F. Julien, J. Dura, S. Monfray, S. Dhar, C.A. Legrand, J. Amouroux, B. Gros, L. Welter, C. Charbuillet, P. Cathelin, E. Canderle, N. Vulliet, E. Escolier, L. Antunes, E. Granger, P. Fornara, C. Rivero, G. Bertrand, P. Chevalier, A. Regnier, D. Gloria; STMicroelectronics, France **Abstract:** RF Front End Modules (FEMs) are currently achieved using a variety of technologies. However, since integration drives wireless business in order to achieve the appropriate cost and form factor, CMOS Silicon-on-insulator (SOI) has been adopted 10 years ago and is now the dominant technology for RF switches in RF FEMs for cell phones and WiFi [1]. While current performances available on RF SOI technology have been exceeding what was feasible using GaAs one, new cellular system requirements ask even more stringent performances and consequently RF SOI technology must continue to improve. In this paper, we review and discuss the optimization of an advanced 200 mm RF SOI technology achieving $R_{on} \times C_{ofF}$ of 78 fs with a breakdown voltage of 3.7 V.

RMo4B-2

Superior Reliability and Low Self-Heating of a 45nm CMOS 39GHz Power Amplifier for 5G mmWave Applications

P. Srinivasan, S. Syed, J.A. Sundaram, S. Moss, S. Jain, P. Colestock, N. Cahoon, A. Bandyopadhyay, F. Guarin, B. Min, M. Gall; GlobalFoundries, USA

Abstract: A 5G new-radio (NR) 2-stack differential 39 GHz Power Amplifier (PA) designed with ADNFETs in 45RFSOI technology is used to showcase superior CW and 5G performance and excellent reliability. Measured CW linear gain of ~12 dB, ~18 dBm Psat with PAE of 35.1% is seen while 5G QPSK results show Plin ~13dBm@-22dB EVM and ~17dBm@-19dB ACPR at 1.7V VDD back-off conditions. Time domain waveforms followed by RF reliability characterization show that off-state Hot Carrier Injection (HCI) is a key fail mechanism under matched-Z load and VSWR. Key RF degradation metrics from long term RF stress show Δ Pout, Δ Gain < 0.5dBm and Δ PAE < 1% meeting overall 10yr lifetime criteria. Self-heating characterization show ~6 C increase at 1.6V/160mW dissipated power demonstrating excellent thermal stability. From 5G aging measurements and model sims, good model-hardware correlation is seen where gain degradation < 0.5 dB at 10y demonstrating overall superior performance and excellent reliability of the PA for 5G mmWave applications.

RMo4B-3

Impact of Non-Conducting RF and DC Hot Carrier Stresses on FinFET Reliability for RF Power Amplifiers

X. Ding¹, G. Niu¹, H. Zhang², W. Wang², K. Imura², F. Dai¹, ¹Auburn University, USA, ²MaxLinear, USA **Abstract:** Impact of non-conducting RF and DC stresses on transistor I-V and RF characteristics are investigated experimentally on a production 14/16-nm FinFET technology for the first time, for high voltage devices commonly used in RF PAs. The degradation is shown to be non-quasi static (NQS), and does not permit the use of DC stress to predict device lifetime under RF stress. Further modeling shows that these FinFETs provide enough margins against non-conducting RF stress for intended PA application.

RMo4B-4

Device for Protecting High Frequency and High Data Rate Interface Applications in FinFET Process Technologies

Srivatsan Parthasarathy, Ray Shumovich, Javier Salcedo, Roxann Broughton-Blanchard, J.-J. Hajjar; Analog Devices, USA

Abstract: The relatively poor ESD robustness of many RF ports is a direct result of the performance degradation introduced by traditional ESD diodes. The later limits the amount of ESD protection that can be tolerated in RF applications. This paper introduces a ground-referenced low capacitance and highly linear Silicon Controlled Rectifiers (SCR) topology designed in 16nm CMOS FinFET process technology. The device presented in this work is employed to protect RF ports with asymmetrical signal swings in the range of +3.0V/-1.0V operating to 20 GHz with a 3rd order linearity specification requirement of -75dBc or greater.

Monday, 20 June 2022 15:40-17:00 4A-4C

Session RMo4C: RF, mm-Wave and Sub-THz VCOs Chair: Teerachot Siriburanon, University College Dublin, Ireland Co-Chair: Howard C. Luong, HKUST, China

RMo4C-1

An 8.2–10.2GHz Digitally Controlled Oscillator in 28nm CMOS Using Constantly-Conducting NMOS Biased Switchable Capacitor

Lantao Wang¹, Jonas Meier¹, Johannes Bastl¹, Tim Lauber¹, Andreas Köllmann², Ulrich Möhlmann², Michael Hanhart¹, Alexander Meyer¹, Christopher Nardi¹, Ralf Wunderlich¹, Stefan Heinen¹; ¹RWTH Aachen University, Germany, ²NXP Semiconductors, Germany

Abstract: This paper presents an 8.2–10.2GHz digitally controlled oscillator (DCO) in a 28 nm technology. The proposed DCO utilizes a switchable capacitor (SC) structure with a constantly conducting NMOS pair, featuring an SC bank with unitary cells arranged in a matrix. With the unitary weighted capacitor bank, the DCO demonstrates an inherently monotonic tuning with a range of 24.3%. The finest tuning resolution is 17 kHz thanks to the customized fringe capacitor. The DCO shows a phase noise of -115.1 dBc/Hz at 1MHz offset from 9 GHz carrier frequency with 13mW power consumption, achieving a -183 dBc/Hz FOM and -190.6 dBc/Hz FOM_r.

RMo4C-2

A 14.5–17.9GHz Harmonically-Coupled Quad-Core P-N Class-B DCO with -117.3dBc/Hz Phase Noise at 1MHz Offset in 28nm CMOS

Ioanna Apostolina, Danilo Manstretta; Università di Pavia, Italy

Abstract: In this paper, a CMOS quad-core DCO with class-B operation and transformer-based tail coupling is investigated to achieve ultra-low phase noise in the K_u band. The design uses an averaging approach to minimize systematic frequency step errors arising in DCOs with large tuning capacitor arrays due to signal unequal distribution. A proof-of-concept prototype has been developed in 28-nm CMOS technology. The DCO achieves a phase noise of -117.3 dBc/Hz at 1 MHz offset from the 15.35 GHz carrier frequency, a figure of merit (FoM) of -187.6 dBc/Hz, and a tuning range of 20.3% with a frequency resolution of 10MHz and less than ± 240 kHz error.

RMo4C-3

A Compact CMOS 76–82GHz Super-Harmonic VCO with 189dBc/Hz FoM Operating Based on Harmonic-Assisted ISF Manipulation

Behnam Moradi, Xuyang Liu, Michael M. Green, Hamidreza Aghasi; University of California, Irvine, USA

Abstract: A compact super-harmonic voltage-controlled oscillator (VCO) for mm-wave radar applications employing a novel distributed structure operating at a center frequency of 78.9 GHz is presented. An state-of-the-art phase-noise performance is achieved by leveraging the strong presence of second harmonic at the output. This new VCO structure operates based on the minimization of the thermal noise contribution for fundamental signal and thus, improves the phase noise. The VCO is fabricated in 65nm Bulk CMOS technology and attains a measured phase-noise of -109.82 dBc/Hz at 1 MHz offset frequency, corresponding to a figure-of-merit of 189dBc/Hz. The VCO also demonstrates 7% of frequency tuning, 4.6% efficiency, and -0.6 dBm peak output power. To the best of our knowledge, this is the highest reported FOM for a super-harmonic CMOS oscillator operating at this frequency band.

RMo4C-4

Sub-THz Switch-Less Reconfigurable Triple-/Push-Push Dual-Band VCO for 6G Communication

Seongwoog Oh, Jinhyun Kim, Jungsuek Oh; Seoul National University, Korea

Abstract: This work presents a novel switch-less reconfigurable triple-/push-push dual-band VCO topology and design methods for a W-band metal-oxide-semiconductor (CMOS) voltage-controlled oscillator (VCO). A clover-shaped inductor with a three-port connection and single frequency multiplied output port configuration provides switch-less mode changes between triple-push and push-push operation. This topology is demonstrated in a W-band VCO by controlling three cores with a measured phase noise of -109.17 dBc/Hz at a 10-MHz offset of a 105.3 GHz carrier. The measured center frequency of each band is 91.04 GHz and 102.33 GHz with a tuning range of 10.4% and 14.1%, respectively. The proposed VCO with independent core on/off state control enables low parasitic switch-less frequency band shift resulting in a superior tuning range compared to those of conventional dual-/single-band VCOs. The effectiveness of this approach is demonstrated through fabrication in a 28-nm CMOS process, with the best FOM_x being -174.4 dBc/Hz in this case.

Tuesday, 21 June 2022 08:00–09:40 1A-1C Session RTu1A: mm-Wave and Wide Band Low-Noise CMOS Amplifiers

Chair: Hao Gao, Silicon Austria Labs, Austria Co-Chair: Marcus Granger-Jones, Qorvo, USA

RTu1A-1

28GHz Compact LNAs with 1.9dB NF Using Folded Three-Coil Transformer and Dual-Feedforward Techniques in 65nm CMOS

Xiangrong Huang¹, Haikun Jia¹, Wei Deng¹, Zhihua Wang², Baoyong Chi¹, ¹Tsinghua University, China, ²RITS, China

Abstract: This article presents two Ka-band low-noise amplifiers (LNA) for millimeter-wave (mmwave) phased-arrays. The folded three-coil transformer and EM dual-feedforward techniques are proposed to improve the LNA's noise performance and reduce the chip area. The first two-stage single-ended LNA, consisting of a common-gate (CG) input stage and a common-source (CS) output stage, achieves 1.9 dB minimum noise figure (NF), 16.7 dB peak gain, 4.3 GHz 3-dB bandwidth (BW) from 25.6 to 29.9 GHz, and -12 dBm input 1-dB gain-compression-point (IP1dB) with 13.2 mW Pdc. The second LNA employs the current-reuse topology, which reduces the power consumption to 3.6 mW at the cost of a 0.6 dB NF degradation. The proposed LNAs have been fabricated in 65nm CMOS process. The two LNAs have the same 200 μ m \times 300 μ m core chip area.

RTu1A-2

22–33GHz CMOS LNA Using Coupled-TL Feedback and Self-Body Forward-Bias for 28GHz 5G System

Yo-Sheng Lin, Kai-Siang Lan; National Chi Nan University, Taiwan

Abstract: We report a 22–33 GHz low-noise amplifier (LNA) with low power dissipation (P_p), low noise-figure (NF) and small group-delay (GD) variation in 90 nm CMOS for 28 GHz 5G system. Current-reused and body self-forward-bias (BSFB) techniques are used for low P_p . Compact quarter-wavelength (λ /4) spiral transmission-line (TL) in conjunction with a large bypass capacitor is used for gate-bias and simultaneous drainbias and current-source. Coupled-TL feedback and BSFB techniques are used for gain and NF enhancement in the condition of the same P_p . The LNA dissipates 12.2 mW and achieves decent S_{21} of 16 dB, 3 dB bandwidth (f_{3dB}) of 11 GHz (22–33 GHz), minimum NF (NF_{min}) of 2.5 dB, average NF (NF_{avg}) of 3.1 dB and GD variation of ±6 ps for 22–33 GHz, and figure-of-merit (FOM) of 91.7 GHz. Furthermore, the LNA occupies 0.406 mm² chip area, and attains decent input third-order intercept point (IIP3) of -3 dBm at 28 GHz. The NF and FOM are one of the best performances ever demonstrated for Ka-band CMOS LNAs with f_{3dB} wider than 5 GHz and P_p lower than 14 mW.

RTu1A-3

A Capacitor Assisting Triple-Winding Transformer Low-Noise Amplifier with 0.8–1.5dB NF 6–12GHz BW ±0.75dB Ripple in 130nm SOI CMOS

Tenghao Zou¹, Hao Xu¹, Yizhuo Wang¹, Weitian Liu¹, Tingting Han², Zengqi Wang³, Nan Li³, Mi Tian², Weiqiang Zhu², Na Yan¹; ¹Fudan University, China, ²CASIC IT Academy, China, ³Archiwave Microelectronics, China

Abstract: This paper presents a novel capacitor assisting triple-winding transformer (CTTF) low noise amplifier (LNA) with ultra-low noise figure (NF) and a flat passband gain in 130nm SOI CMOS process. The assisting capacitor in the triple-winding transformer expands the design space by enabling independent control of the coupling strength between each two inductors. The negative resistor enhanced by the assisting capacitor boosts the transformer gain that not only suppresses the noise from the second stage, but also leads to a wider passband by compensating the gain droop from the active transistors. Through two-stage simultaneous noise and power matching, the LNA provides a remarkable 0.8–1.5 dB NF, <-14dB S11, <-8dB S22, -11.8dBm IP_{1dB} and 21.8–23.3dB power gain across the 6–12GHz passband with \pm 0.75dB ripple while drawing 20mA from a 3.3V supply. It reports the lowest NF so far.

RTu1A-4

An LNA with Input Power Match from 6.1 to 38.6GHz, the Noise-Figure Minimum of 1.9dB, and Employing Back Gate for Matching

Mohammad Radpour, Leonid Belostotski; University of Calgary, Canada

Abstract: This paper proposes using the back-gate terminal of an FDSOI transistor for input power matching. This concept is experimentally demonstrated with a 22-nm FDSOI low-noise amplifier (LNA). Thanks to the real part of the back-gate impedance, the LNA $|S_{11}| < -10$ -dB bandwidth extends from 6.1 to 38.6 GHz. In addition, applying input to both the front- and back-gate terminals, as well as employing a current-reuse configuration, increases the effective transconductance of the LNA first stage, thereby increasing its gain and lowering its input-referred noise. As a result, the LNA is able to achieve 12.2 ± 3.4 dB of gain, -13dBm of IP1dB, and a noise-figure minimum of 1.9 dB while consuming 7.8 mW of power and occupying 0.03-mm² of active area.

Tuesday, 21 June 2022 08:00-09:40

1**D-**1**F**

Session RTu1B: Efficiency Enhancement Techniques for Power Amplifiers

Chair: SungWon Chung, Neuralink, USA Co-Chair: Alexandre Giry, CEA-Leti, France

RTu1B-1

A 38GHz Deep Back-Off Efficiency Enhancement PA with Three-Way Doherty Network Synthesis Achieving 11.3dBm Average Output Power and 14.7% Average Efficiency for 5G NR OFDM

Xiaohan Zhang¹, Sensen Li², Daquan Huang², Taiyun Chi¹; ¹Rice University, USA, ²Samsung, USA **Abstract:** We propose a mmWave three-way Doherty output network synthesis methodology that can realize close-to-ideal dual-peaking Doherty active load modulation while absorbing the device parasitic capacitance. Following this methodology, we present a 38GHz PA prototype, achieving 13.7% / 11.0% PAE at 9.5dB / 11.5dB back-off, which are the highest among reported silicon PAs operating at 30GHz and above. Tested under 1-CC and 2-CC 5G NR FR2 64-QAM OFDM signals in the Band n260, the PA demonstrates state-of-the-art average output power (11.3dBm) and average efficiency (14.7%).

RTu1B-2

A Polar Doherty SCPA with 4.4° AM-PM Distortion Using On-Chip Self-Calibration Supporting 64-/256-/1024-QAM

Hongxin Tang, Huizhen Jenny Qian, Bingzheng Yang, Tianyi Wang, Xun Luo; UESTC, China **Abstract:** In this paper, an efficient switched-capacitor power amplifier (SCPA) with high linearity using on-chip self-calibration technique is proposed. The inherent AM-PM distortion in digital power amplifier (DPA) is decreased by the proposed self-calibration technique without any pre-distortion. Meanwhile, to improve the modulation bandwidth, a storage capacitor array (SCA) is introduced to decrease the settle-time of the calibration loop for transition among various baseband signals. The proposed polar Doherty SCPA is implemented in conventional 40-nm CMOS technology. It operates in 1.4–2.8 GHz with peak output power of 28.9 dBm, peak drain efficiency (DE) of 43.9%, peak system efficiency (SE) of 37.2%, and AM-PM distortion of 4.4° at 1.8 GHz. It supports 100 MHz 64-QAM signal (i.e., 22.6 dBm average output power, 4.87% EVM, and 33.9% average DE) and 10 MHz 1024-QAM signal (i.e., 21.3 dBm average output power, 1.77% EVM, and 32.1% average DE) without any pre-distortion.

RTu1B-3

A Compact Single Transformer Footprint Hybrid Current-Voltage Digital Doherty Power Amplifier

Jeongseok Lee, Doohwan Jung, David Munzer, Hua Wang; Georgia Tech, USA

Abstract: This paper presents a fully integrated single footprint hybrid current-voltage mode digital Doherty power amplifier (PA). A prototype PA is implemented in a 45nm CMOS SOI process. The proposed PA design provides enhanced linearity through adaptive biasing-based AM-PM distortion mitigation of the current mode digital PA and AM-PM cancelation through hybrid current/voltage mode Doherty-based power combining. It achieves 21.7dBm peak output power (P_{sat}) at 1.2GHz and 37.6% drain efficiency (DE) at 1.4GHz. The proposed digital Doherty PA demonstrates $1.2 \times /1.22 \times$ PBO efficiency enhancement, compared to the ideal class-B at 3/6 dB PBO at 1.2GHz. The measured error vector magnitude (EVM) of 64-QAM/20MHz is -23dB with 22.8% average DE without DPD. This is the first demonstration of hybrid current-voltage mode Doherty power combining on a single footprint transformer over a broad bandwidth (BW).

RTu1B-4

An Eight-Core Class-G Switched-Capacitor Power Amplifier with Eight Power Backoff Efficiency Peaks

Bo Qiao, Ajmal V. Kayyil, David J. Allstot; Oregon State University, USA

Abstract: An eight-core class-G polar switched-capacitor power amplifier (SCPA) is described that uses an eight-way digitally-scalable transformer (DST) and a new pseudo-differential class-G switch. Employing both supply and load modulation, eight seamless efficiency peaks are realized at 0 dB, 2.5, 6, 8.5, 12, 14.5, 18 and 24 dB power backoff levels by minimizing the dynamic switching loss in the capacitor array. A prototype chip was designed and fabricated in a 65nm CMOS process. It achieves peak output power and drain efficiency (DE) values of 27.2 dBm and 35.5%, respectively, at a carrier frequency of 2.42 GHz. Compared to a normalized class-B power amplifier, the measured DE is increased by \sim 3.3× which corresponds to a 70% power saving. For a single-carrier 64 QAM signal with a 1 MHz bandwidth, the measured average output power and DE are 20.0 dBm and 23.1%, respectively, with an error vector magnitude (EVM) of -28.6 dB.

Tuesday, 21 June 2022 13:30–15:10 1A-1C

Session RTu3A: Circuits and Techniques for Full Duplex Transceivers Chair: Roxann Broughton-Blanchard, Analog Devices, USA Co-Chair: Mohyee Mikhemar, Broadcom, USA

RTu3A-1

An Integrated Reconfigurable SAW-Less Quadrature Balanced N-Path Transceiver for Frequency-Division and Half Duplex Wireless

Erez Zolkov, Nimrod Ginzberg, Emanuel Cohen; Technion, Israel

Abstract: In this work, we propose a fully integrated transceiver for frequency-division and half duplex wireless operation based on a quadrature balanced N-path mixer-first architecture. The quadrature balanced N-path transceiver (QBNT) comprises a quadrature hybrid and two identical mixer-first receivers (MFRXs), presenting a short circuit and 50 ohms matching in the transceiver (TX) and receiver (RX) bands, respectively. The TX power reflects at the MFRXs' interface and adds up in-phase at the antenna, while the RX signal from the antenna is reconstructed in phase in digital baseband, with the TX noise cancelled at RX regardless of antenna voltage standing wave ratio. QBNT equations and design considerations are shown. An integrated QBNT prototype was fabricated in TSMC 65nm CMOS process as a proof of concept, occupying an active area of 2.96 mm². The QBNT operates at the frequency range between 0.75–2 GHz with a TX-RX offset above 200 MHz. It achieves RX noise figure (NF) of 2.8–5.8 dB, RXB1dB of 18 dBm, TX-ANT OIP3 of 27.3 dBm and 29.5 dBm in FDD and half duplex (HD) modes, respectively. The RX and TX (at OP1dB) consume DC power of 82–130 mW and 254 mW, respectively.

RTu3A-2

A 0.5–4GHz Full-Duplex Receiver with Multi-Domain Self-Interference Cancellation Using Capacitor Stacking Based Second-Order Delay Cells in RF Canceller

Chuangguo Wang, Wei Li, Fan Chen, Wen Zuo, Yunyou Pu, Hongtao Xu; Fudan University, China **Abstract:** Nanosecond-scale on-chip delay is critical for integrated wideband self-interference cancellation (SIC) in full-duplex (FD) system, especially for radio frequency (RF) domain SIC. In this paper, we presented a FD receiver with multi-domain SIC using capacitor stacking based second-order delay cell in the RF canceller which breaks the trade-off between delay, loss, size and noise. A prototype is fabricated in 65nm CMOS process. The FD receiver can operate in 0.5–4GHz with gain of 29–32dB. At 2GHz local oscillator (LO) frequency, the RF canceller can achieve delay of 2–8ns while consuming 10mW. The baseband (BB) canceller can achieve delay of 9–15ns while consuming 4.4mW. These large nanosecond-scale delays ensure more than 34dB SIC over 20MHz modulated signal bandwidth in case of applying a commercial circulator (isolation of 23–26dB). In FD mode, the RF and BB cancellers degrade the receiver noise figure (NF) by 0.9dB and 0.4dB, respectively. The receiver power handling is improved by 11.5dB. The active chip area is only 0.4mm².

RTu3A-3

A 2Gb/s 9.9pJ/b Sub-10GHz Wireless Transceiver for Reconfigurable FDD Wireless Networks and Short-Range Multicast Applications

Renzhi Liu¹, Asma Beevi K. T.¹, Richard Dorrance¹, Timothy Cox¹, Rinkle Jain¹, Tolga Acikalin¹, Zhen Zhou¹, Tae-Young Yang¹, Johanny Escobar-Pelaez², Shuhei Yamada¹, Kenneth Foust¹, Brent Carlton¹; ¹Intel, USA, ²Intel, Mexico

Abstract: This paper presents a sub-10GHz wireless transceiver for short-range multicast applications in a reconfigurable FDD wireless network. The transceiver adopts a digital-process-friendly architecture and can deliver up to 2Gb/s data rate in a 500MHz channel bandwidth with 19.8mW power consumption and 9.9pJ/b energy efficiency. Being a coherent transceiver, it outputs -5.5dBm power, achieves -67.5dBm sensitivity at 1Gb/s and 1dB de-sensitization during FDD operation while tolerating -26dBm close-in Wi-Fi blockers.

RTu3A-4

Fully Integrated Ultra-Wideband Differential Circulator Based on Sequentially Switched Delay Line in 28nm FDSOI CMOS

Jun Hwang, Byung-Wook Min; Yonsei University, Korea

Abstract: In this paper, a non-magnetic circulator, which realizes non-reciprocal signal flows by sequentially switching delay lines, is presented in 28-nm fully depleted silicon-on-insulator (FDSOI) CMOS process. The proposed circulator is designed differentially to increase power handling capability and bandwidth. The bandwidth of insertion loss and isolation can be extended by latticely coupled inductors used in the differential synthetic delay lines. The characteristic impedance of the delay lines is determined by considering the channel resistance of CMOS transistor. The measured insertion losses of transmitter (TX) to antenna (ANT) and ANT to receiver (RX) are 2.5 dB and 2.6 dB, respectively. TX to RX isolation is >20 dB up to 7 GHz. The measured TX input power 1 dB compression point is 4.7 dBm at 3.5 GHz. The chip size of the differential circulator is 1.33×0.72 mm², which is as small as a single ended version, thanks to the coupled inductors.

RTu3A-5

A C-Band Commutated-LC-Negative-R Delay Circuit with Harmonic Power Recycling Achieving 1.5ns Delay, 1.4GHz BW, and 6dB IL

Shuxin Ming, Rakibul Islam, Jin Zhou; University of Illinois at Urbana-Champaign, USA

Abstract: This work presents a commutated-LC-negative-R delay circuit for broadband signal processing at RF. It introduces negative resistance to compensate inductor loss in a commutated-LC broadband delay circuit, and unveils a new capability of time-varying RF circuits that we call *harmonic power recycling*. For a time-invariant circuit or an N-path filter circuit, its desired passband consists of only one harmonic. Hence, energies at all other harmonics provided by the broadband negative resistance are wasted. In contrast, a commutated-LC broadband delay circuit has multiple harmonics across its passband, recycling the wasted RF energies from the negative resistance. This *harmonic power recycling* results in improved noise figure and low dc power in addition to reduced insertion loss (IL). A proof-of-concept CMOS delay line is implemented, achieving 1.5-ns delay, 1.4-GHz instantaneous bandwidth (BW), and 6-dB IL at the C band.

Tuesday, 21 June 2022 13:30–15:10 1D-1F

Session RTu3B: mm-Wave/THz Devices and BIST/Calibration, and Circuits for Emerging Applications

Chair: Mona Hella, Rensselaer Polytechnic Institute, USA Co-Chair: Fabio Sebastiano, Technische Universiteit Delft, The Netherlands

RTu3B-1

LNFET Device with 325/475GHz $f_{\rm T}/f_{\rm MAX}$ and 0.47dB $NF_{\rm MIN}$ at 20GHz for SATCOM Applications in 45nm PDSOI CMOS

S.V. Khokale¹, T. Ethirajan¹, H.K. Kakara², B. Humphrey¹, K. Shanbhag¹, V. Vanukuru², V. Jain¹, S. Jain¹; ¹GlobalFoundries, USA, ²GlobalFoundries, India

Abstract: An experimental low noise FET (LNFET) device is presented in this paper with f_{T}/f_{MAX} of 325/475GHz. To authors' knowledge, this is the highest reported f_{MAX} for a CMOS device. The device was demonstrated on a 45nm partially depleted Silicon on insulator (PDSOI) CMOS wafer for low noise amplifier (LNA) design. The device has been developed for Ku/K/Ka-band applications in SATCOM (satellite communications) RF transceiver. It shows ~0.26 / 0.47 / 0.60 dB NF_{MIN} and ~20.1 / 17.8 / 16.6 dB MSG at 12 / 20 / 26 GHz respectively. LNA reference circuits at 12GHz and 20GHz were designed using this device with an inductively degenerated source cascode. Measured data from the circuits show NF of ~0.82dB at 12GHz and ~1.23dB at 20GHz with 15.2dB and 12.3dB gain respectively. Measured NF is the lowest amongst recent silicon-based designs in these frequency bands.

RTu3B-2

E-Band CMOS Built-In Self-Test Circuit Capable of Testing Active Antenna Impedance and Complex Channel Response

Seung-Uk Choi, Kyunghwan Kim, Kangseop Lee, Seunghoon Lee, Ho-Jin Song; POSTECH, Korea **Abstract:** A novel built-in self-test (BIST) circuit is presented. The proposed BIST enables the testing of active antenna impedance and the VSWR resilient channel response. The technique is achieved simply by extracting the complex voltages at two nodes on a short-distance transmission line. For efficient implementation, a single-pole double-throw RF switch is used for sharing the signal detector, and the required switch on-off ratio is analyzed mathematically based on detection accuracy. The proposed BIST was experimentally verified with a test chip fabricated with a 40-nm bulk CMOS process. The measured magnitude and phase rms errors for the complex forward waves are less than 1.1dB and 2.5°, respectively, within 82–86GHz. In the impedance estimation test, Γ magnitude and phase rms errors are less than 0.1 and 17°, respectively, within 76–86GHz.

RTu3B-3

Millimeter-Wave VNA Calibration Using a CMOS Transmission Line with Distributed Switches

Jun-Chau Chien; National Taiwan University, Taiwan

Abstract: This paper presents a single-element VNA electronic calibration (E-Cal) technique implemented in CMOS technology. The structure employs a transmission line (t-line) loaded with twenty distributed switches whose impedance states can be independently modulated during S-parameter measurements. An algorithm that leverages the implementation concepts from the one-port *offset-shorts* and the two-port *Line-Reflect-Reflect-Match (LRRM)* calibrations and takes advantage of the loading periodicity and the structure layout symmetry is developed. The calibration method is justified using a 65-nm CMOS test chip and the measurement results are compared with on-chip one-tier TRL calibration using both passive and active devices up to 67 GHz.

RTu3B-4

Multi-Tone Frequency Generator for Gate-Based Readout of Spin Qubits

Mathilde Ouvrier-Buffet, Alexandre Siligaris, José Luis Gonzalez-Jimenez; CEA-Leti, France

Abstract: This paper presents a multi-tone frequency generator in the sub-10 GHz range. The implemented circuit allows to reduce the number of interconnections between the control electronics and the quantum processor layer during reflectometry readout of spin qubits. The circuit is fabricated in a 45nm CMOS SOI technology. It is able to generate a multi-tone signal spaced by 500 MHz with 2.3 dB power ripple between the tones. It achieves phase noise performances between -107 dBc/Hz and -112 dBc/Hz @1 MHz offset according the considered tones. The complete system presents a consumption of 84.4 mW for an area of 0.27 mm².

RTu3B-5

A Dual-Antenna, 263GHz Energy Harvester in CMOS for Ultra-Miniaturized Platforms with 13.6% RF-to-DC Conversion Efficiency at -8dBm Input Power

Muhammad Ibrahim Wasiq Khan, Eunseok Lee, Nathan M. Monroe, Anantha P. Chandrakasan, Ruonan Han; MIT, USA

Abstract: This paper reports a CMOS energy harvester, which operates at so far the highest reported frequency (263 GHz) in order to realize wireless powering of ultra-miniaturized platforms. To maximize the THz-to-DC conversion efficiency, η , at low available radiation power, the harvester not only utilizes a high-speed 22-nm FinFET transistor but also achieves the optimal operating conditions of the device. In specific, the circuit enables self-gate biasing; and through a dual-antenna topology, it drives the transistor drain and gate terminals with both optimal voltage phase difference and power ratio simultaneously and precisely. With a low input power of -8 dBm, the harvester achieves 13.6% measured conversion efficiency and delivers 22 μ W to a 1-k Ω load. Without relying on any external component, the harvester chip occupies an area of 0.61×0.93 mm².

Tuesday, 21 June 2022 15:40–17:00 1A-1C

Session RTu4A: Emerging Wireless Communications Chair: David D. Wentzloff, University of Michigan, USA Co-Chair: Arun Paidimarri, IBM T.J. Watson Research Center, USA

RTu4A-1

802.11ah Transmitter with -55dBr at \pm 3MHz and -58dBr at \pm 20MHz ACLR and 60dB 2nd-Order Harmonic Rejection for 470MHz ~ 790MHz TV White Space Band Devices

Seong-Sik Myoung, Jonghoon Park, Chang Hun Song, Ryun Woo Kim, Jaeyoung Ryu, Jeongki Choi, Hoai-Nam Nguyen, Seungyun Lee, Ilyong Jung, Jong-Han Lim, Sok Kyu Lee; Newracom, USA **Abstract:** A novel 802.11ah transmitter for TV white space (TVWS) band devices is presented. To realize the transmitter meeting the stringent FCC and ETSI TVWS device emission limits for the adjacent channels and FCC restricted bands, a low noise and high linear class-AB voltage-to-current converter (V21) as the mixer driver and a 2nd-order harmonic notch filter with the frequency tracking capability on the power amplifier (PA) load are newly proposed. The designed transmitter is implemented in a 40nm CMOS process as a part of the TVWS band 802.11ah connectivity System-on-Chip (SoC), and the measured results with the 802.11ah CBW4 signal show -55dBr and -58dBr Adjacent Channel Leakage Ratio (ACLR) at \pm 3MHz and \pm 20MHz frequency offset, respectively, and 60dB 2nd harmonic rejection for 470MHz ~ 790MHz TVWS bands. This transmitter is the first SoC level transmitter meeting the FCC and ETSI ACLR requirements.

RTu4A-2

A 915MHz 19 $\!\mu\text{W}$ Blocker-Enhanced Wake-Up Receiver with Frequency-Hopping Two-Tone Modulation Achieving 53dB Tolerance to In-Band Interference

Heyu Ren¹, Dawei Ye¹, Binbin Chen¹, Xu Jin¹, Wenjun Gong¹, Rongjin Xu¹, C.-J. Richard Shi²; ¹Fudan University, China, ²University of Washington, USA

Abstract: A 915MHz ultra-low-power blocker-enhanced wake-up receiver (BE-WuRx) is presented in a 65nm CMOS process. Employing the proposed frequency-hopping two-tone modulation (FH-TTM), the BE-WuRx can dynamically convert the in-band blocker power to data power, and achieves a -63.6dBm sensitivity without blocker and a -90dBm enhanced sensitivity with a -25dBm CW interferer, while just consuming 19 μ W. With the -63.6dBm sensitivity, the BE-WuRx performs 53dB tolerance to the in-band blocker, exhibiting 14dB improvement compared to the case that FH-TTM is off. The wake-up latency is 6.4ms for a quiet channel and 6.4 to 64ms for a congested channel.

RTu4A-3

A 320µW Receiver with -58dB SIR Leveraging a Time-Varying N-Path Filter

Milad Moosavifar, Yaswanth K. Cherivirala, David D. Wentzloff; University of Michigan, USA **Abstract:** This paper presents a 900MHz ultra-low-power (ULP) receiver (RX) with -88dBm sensitivity and up to -58dB Signal-to-Interference Ratio (SIR) for the Internet of Things (IoT) applications. The receiver utilizes chirped On-Off-Keying (OOK) modulation for data reception. We proposed a mixer-first receiver leveraging a chirped Miller N-path filter, to achieve low-power operation while ensuring strong in-band and out-of-band interference rejection as well as sufficient RX sensitivity. A novel 4-phase chirped Miller N-path filter, using a high quality factor time-varying narrowband frequency response, is introduced in this work to facilitate bandpass filtering of the wideband chirp-OOK modulated signal, that results in enhanced RX interference tolerance. The RX chip is designed and fabricated in a CMOS 65nm technology and consumes 320µW at 5kb/s datarate, while achieving -88dBm sensitivity at 10⁻³ Bit-Error-Rate (BER).

RTu4A-4

A 26-to-33GHz Time-Modulated Spectral-Spatial Mapping MIMO Receiver Array with Concurrent Steerable Multi-Beams Using Only One Beamformer and One Single-Wire Interface

Tzu-Yuan Huang, Boce Lin, Naga Sasikanth Mannem, Hua Wang; Georgia Tech, USA

Abstract: This work proposes a wideband 26–33GHz MIMO receiver (RX) array that leverages timemodulation operation to achieve concurrent steerable Multi-Beam MIMOs (MB-MIMO) using only one set of array beamformer. The time-modulation enables spectral-spatial mapping that maps the multi-beam information to a single-wire interface. A proof-of-concept 26–33GHz time-modulated RX array with MB-MIMOs is implemented in 45nm CMOS RF SOI. The proposed RX demonstrates S11 < -10 dB across 24~32 GHz and its maximum conversion gain of 28dB with a 3dB-bandwidth of 26 to 33 GHz. The measured NF is 5.78 dB at 28 GHz with RX input-referred IP_{1dB} of -38dBm. Also, this proposed RX is supported with wideband-16/64QAM single carrier modulations.

Tuesday, 21 June 2022 15:40–17:00 1D-1F Session RTu4B: Building Blocks for Next Generation Frequency Synthesis

Chair: Joseph D. Cali, Raytheon, USA Co-Chair: Ehsan Afshari, University of Michigan, USA

RTu4B-1

Class-C BAW Oscillator Achieving a Close-In FOM of 206.5dB at 1kHz with Optimal Tuning for Narrowband Wireless Systems

Bichoy Bahr, Danielle Griffith, Ali Kiaei, Thomas Tsai, Ryan Smith, Baher Haroun; Texas Instruments, USA

Abstract: This paper presents a low-power, low-phase noise class-C Bulk Acoustic Wave (BAW) oscillator. It achieves a FOM of -206.5 dB at 1 kHz offset, enabling low-power, crystal-less SoC implementation for multiple wireless standards. A reference oscillator module for SoC integration is presented with a corresponding optimal tuning procedure for best phase noise performance. Power efficient class-C operation, reduced device count, and amplitude trimming, allow for 3 dB FOM and FOM_o improvement over state-of-the-art GHz MEMS-based oscillators.

RTu4B-2

A 5.1dBm 127–162GHz Frequency Sextupler with Broadband Compensated Transformer-Based Baluns in 22nm FD-SOI CMOS

Shuyang Li¹, Wenhua Chen¹, Xingcun Li¹, Yunfan Wang², ¹Tsinghua University, China, ²University of Michigan, USA

Abstract: This paper presents a D-band frequency sextupler in 22nm FD-SOI CMOS. It consists of a differential frequency tripler followed by a push-push frequency doubler for six times frequency multiplication, and several differential amplifiers for enhanced conversion gain and output power. A broadband balance-compensation method is proposed for transformer-based baluns to realize wideband conversion between single-ended and balanced signals. The measured peak output power and peak efficiency are 5.1dBm and 8.49% at 145.5 GHz, respectively. The fabricated frequency sextupler features a 3-dB output power bandwidth from 127 to 162 GHz and low DC power consumption less than 50mW from 0.8V power supply.

RTu4B-3

A Digital-to-Time Converter Based on Crystal Oscillator Waveform Achieving 86fs Jitter in 22nm FD-SOI CMOS

Xi Chen¹, Teerachot Siriburanon¹, Zhongzheng Wang², Jianglin Du¹, Yizhe Hu¹, Anding Zhu¹, R. Bogdan Staszewski¹; ¹University College Dublin, Ireland, ²MCCI, Ireland

Abstract: In this paper, we propose a digital-to-time conversion (DTC) technique operating entirely in the sinusoidal waveform voltage domain of a crystal oscillator (XO) before the signal's final slicing into the time-domain of the programmably delayed clock, with a deterministic predistortion to further improve the linearity. Precise timing delay is obtained by simply adjusting the dc offset of the signal. The technique merges the functionality of DTC with XO generation, thus drastically reducing the power consumption, while offering wide range with fine resolution, low noise and high linearity. Fabricated in 22-nm FD-SOI CMOS, the prototype of XO+DTC consumes only 0.52mW while achieving a 546 ps range with fine resolution of 266 fs. The rms jitter is only 86.6 fs at a frequency of 100 MHz.

RTu4B-4

Highly Accurate Frequency Quadrupler Based LO Phase Shifter Achieving 0.29° RMS Phase Error for Wideband E-Band Beamforming Receiver

Kangseop Lee¹, Chan-Gyu Choi¹, Kyunghwan Kim¹, Seunghoon Lee¹, Seung-Uk Choi¹, Jayol Lee², Bontae Koo², Ho-Jin Song¹; ¹POSTECH, Korea, ²ETRI, Korea

Abstract: Despite several advantages in terms of linearity and operating bandwidth, LO phaseshifting is not widely used in beamforming transceivers due to the difficulty in realizing fine phase resolution. Regarding the use of a ×M frequency multiplier, the phase resolution at f_{L0} /M should be much higher than that desired at f_{L0} . Here, we propose a frequency multiplier based LO phaseshifting technique that does not reduce the phase resolution after the frequency multiplication. At the cost of a few phase states out of 2ⁿ, the phase resolution at f_{L0} /M can be retained after the frequency multiplier. For experimental evaluation, the proposed scheme was implemented in an E-band beamforming receiver. Because the proposed scheme is suitable for fine resolution and broadband transceivers at millimeter-wave frequencies, the bandwidth of the receiver reaches as high as 23 GHz at 77 GHz with phase resolution and rms phase error of 2.835° and 0.29°, respectively.

RFIC Workshops

Sunday, 19 June 2022

Workshops are offered on Sunday 19 June 2022 at the Colorado Convention Center. Please see handout on Sunday in the registration area and from volunteers throughout the meeting floors to confirm room location.

WSA (full day): 08:00–17:00 Large-Scale Antenna Arrays: Circuits, Architectures, and Algorithms

Sponsor: RFIC/IMS

Organizers: Subhanshu Gupta, Washington State University Renyuan Wang, BAE Systems Gernot Hueber, Silicon Austria Labs

Abstract: Wireless networks have fueled socio-economic growth worldwide and are expected to further advance to enable new applications such as autonomous vehicles, virtual/augmented-reality, and smart cities. Due to shortage of sub-6GHz spectrum, mm-wave frequencies play an important role in the emerging 6G and the communication-on-the-move applications. Given that the propagation loss in the lower mm-wave band needs to be compensated by antenna array gain and densification of base stations with cell radius as small as a hundred meters, radio chipsets need to be power and cost efficient. To make radio chipsets power and cost efficient, state-of-the-art mm-wave-net transceivers are designed with phased antenna array (PAA). As a consequence, signal processing techniques and network protocols for mm-wave-nets are designed under constraints of PAA architectures. Future generations of mm-wave-nets will operate in the upper mm-wave frequency band where more than 10GHz bandwidth can be used to meet the ever-increasing demands. Their realization will demand addressing a completely new set of challenges including wider bandwidths, larger antenna array size, and higher cell density. These new system requirements demand fundamental rethinking of radio architectures, signal processing and networking protocols. Major breakthroughs are thus required in radio front-end architectures to enable coherent combining of wideband mm-wave spectrum, as most commonly adopted PAA-based radios face many challenges in achieving fast beam training, interference suppression, and wideband data communication. Through this workshop, we will look at the fundamental issue of coherent signal combination at these large scales from sub-GHz to sub-THz enabled by a diverse group of speakers with expertise spanning circuits, architecture, algorithms, and applications. The coherent combination will bring out true-time-delay array architectures including recent developments in wideband delay compensation methods with large range-to-resolution ratios. The delay compensation at different points of the receiver chain including RF, baseband, and digital will empower not only traditional wireless communications but also spatial signal processing for direction finding and interference suppression.

- 1. "Key Developments in Low-Cost, Wide-Beam Scanning Phased Arrays for Mobile Airborne Communications", **Julio Navarro**, *Boeing*
- 2. "A Phased Array Perspective on the Importance of True Digital Time Delay for Wide Bandwidth Systems", **Andrew Rogers**, *Northrop Grumman*

- 3. "Wideband mm-Wave Beam Training with True-Time-Delay Array Architectures", **Danijela Cabric**, *University of California, Los Angeles*
- 4. "Overview of TTD from Electrical Optical to Acoustic Domain", **Hossein Hashemi**, *University of Southern California*
- 5. "Wideband Digital True-Time-Delay Compensation Techniques for Digital Arrays", **Michael P. Flynn**, *University of Michigan*
- 6. "Beamforming for Large, Wideband Phased Arrays: Advanced True-Time Delay and Associated Digital Control Implementations", **Alberto Valdes-Garcia**, *IBM*
- 7. "Circuits and Architectures for Multi-Gb/s mm-Wave and sub-THz Wireless Transceivers in FinFET CMOS", **Stefano Pellerano**, *Intel*
- 8. "Front-End Architectures for 100Gbps and More at sub-THz Frequencies", **Jose-Luis** Gonzalez-Jimenez, *CEA-Leti*

WSD (Full day): 08:00–17:00 Micro and Nano Technology Challenges to Address 6G Key Performance Indicators

Sponsor: RFIC/IMS

Organizers: Didier Belot, CEA-Leti Wolfgang Heinrich, FBH

Abstract: Telecom communities are beginning to prepare the next generation of mobile telecom, the 6G, and present KPIs going to the Tbps, 300GHz carrier frequency, space multiplexing, spectrum agility, dense Massive MIMO, wide bands, and so forth. Serving these challenges, microelectronics communities must re-think their medium term roadmap: what role can CMOS processes play? Is SiGe HBT a good answer to these KPIs? Do we need more exotic technologies such as III-V HBT or HEMT? How to do Heterogeneous Integrations, in a 3D approach? How to integrate antennas and passives?

- 1. "Toward 6G: From New Hardware Design to Wireless Semantic and Goal-Oriented Communication Paradigms", **Emilio Calvanese Strinati**, *CEA-Leti*
- 2. "Technology Challenges for 6G", Nadine Collaert, Piet Wambacq, imec
- 3. "Advanced 200mm and 300mm RF SOI and BiCMOS Technologies Targeting 5G and Beyond (6G) RF Front-End Module SOC", **Frederic Gianesello**, *STMicroelectronics*
- 4. "SiGe HBT for mm-Wave and THz Applications", Mohamed Hussein Eissa, IHP
- 5. "2.5D and 3D Integrations for mm-Wave and THz Applications", **Tanja Braun**, *Fraunhofer IZM*
- 6. "FinFET CMOS for mm-Wave Applications", Stefano Pellerano, Said Rami, Intel
- 7. "InP HBT for mm-Wave and THz Applications", **Wolfgang Heinrich**, *FBH*
- 8. "100nm to 40nm GaN-on-Si for mm-Wave Application", **Remy Leblanc**, *OMMIC*

- 9. "InGaAs mHEMTs: Technology and Circuit Aspects for mm-Wave and THz Applications", **Fabian Thome**, *Fraunhofer IAF*
- 10. "A Technology-Design Roadmap Addressing 300GHz Connectivity", **Baudouin Martineau**, *CEA-Leti*

WSE (full day): 08:00–17:00 Wideband and High Efficiency mm-Wave CMOS PA Design for 5G and Beyond

Sponsor: RFIC/IMS

Organizers: Steven Callender, Intel Sungwon Chung, Neuralink

Abstract: The Power Amplifier (PA) continues to be a critical building block in mm-wave communication systems, often dictating the overall system efficiency and can thereby impose constraints on system deployment (eg max phased-array size due to thermal constraints). As such, many publications focus on efficiency enhancement techniques for mm-wave power amplifiers. However, when used in systems targeting "5G and Beyond" applications, transceiver bandwidths must be suitable to meet the high data-rate specifications, and hence, maximum PA efficiency cannot be blindly pursued. Instead, efficiency enhancement techniques must be explored in close consideration of their implications on bandwidth which is what this workshop aims to explore more deeply. The goal of this workshop is three-fold: 1) familiarize the audience with PA specifications required for next-gen applications, 2) review well-known (and emerging) efficiency enhancement techniques for mm-wave PAs with perspectives on attainable bandwidth, and 3) discuss techniques to enhance bandwidth while maintaining adequate efficiency required for practical systems. The workshop features talks which will highlight PA specifications for two of the forefront "5G and Beyond" applications — radar and large-scale phased-arrays — covering the 20–100+ GHz, along with reference designs suitable for such applications. In addition, there will be discussions on design methodologies for maximizing bandwidth while optimizing efficiency in the context of mm-wave and sub-THz linear amplifiers and mm-wave Doherty amplifiers. Lastly, an emerging efficiency enhancement technique, the sub-harmonic switching amplifier, will also be presented.

- "Broadband, Back-Off Efficient, and VSWR Resilient mm-Wave PA Architectures Across 30–100+ GHz in CMOS/SiGe/InP", Kaushik Sengupta, Zheng Liu, Princeton University
- "Design of mm-Wave Power Amplifiers for Radar Applications in CMOS and SiGe HBT Technologies", Vadim Issakov¹, Vincent Lammert², Sascha Breun³, ¹Technische Universität Braunschweig, ²Infineon Technologies, ³FAU Erlangen-Nürnberg
- "mm-Wave CMOS Power Amplifiers for 5G Base Station Applications", Hyun-Chul Park, Jooseok Lee, Joonho Jung, Seungjae Baek, Taewan Kim, Sung-Gi Yang, Samsung
- 4. "mm-Wave CMOS PAs for 5G Handsets", Sherif Shakib, Jeremy Dunworth, Vladimir Aparin, *Qualcomm*

- "High Efficiency D-Band Multi-Way Power Combined Amplifiers in 45nm CMOS RFSOI", Siwei Li, Gabriel M. Rebeiz, University of California, San Diego
- 6. "Broadband mm-Wave PA Design in Advanced FinFET CMOS", Steven Callender, Ritesh Bhat, Intel
- 7. "mm-Wave Doherty PA with Bandwidth Enhancement Techniques for 5G and Beyond", **Fei Wang**, *Georgia Tech*
- 8. "Subharmonic Switching 5G PAs for Efficiency Enhancement", Aoyang Zhang, *Harvard University*

WSF (full day): 08:00–17:00 Emerging Low-Temperature/Cryogenic Microwave Techniques and Technologies for Quantum Information Processing

Sponsor: RFIC/IMS

Organizers: Alirio Boaventura, NIST Michael Hamilton, Auburn University

Abstract: Quantum computers hold the promise to perform certain complex calculations that are not solvable even with today's most powerful supercomputers. But despite the significant progress made in the last decade in the science and engineering of quantum computation systems, several challenges remain to be overcome before quantum computation can become practically usable. A key challenge relates to system scalability — fault-tolerant quantum computation will likely require thousands or millions of quantum bits (qubits), far beyond the capacity of current prototypes. Today's most prominent candidate for implementing large-scale systems, the superconducting qubit platform, operates in the microwave regime and is controlled and readout via conventional microwave electronics operating at room temperature. While the current room temperature control and readout approach works for small-scale experiments, it is not scalable to thousands or millions of gubits. The engineering challenges of realizing practical large-scale systems present quantum microwave engineers with new opportunities in microwave modeling, design, and characterization of cryogenic semiconductor and superconductor devices, circuits, and systems. This workshop will address emerging techniques and technologies for quantum information processing including lowtemperature measurements and calibrations, cryogenic packaging and interconnects, monolithic semiconductor-based quantum processors, and quantum-classical interfaces based on cryogenic CMOS and Josephson superconductive electronics.

- 1. "Cryo-CMOS Systems and Circuits for Large-Scale Quantum Computers", **Fabio** Sebastiano, *Technische Universiteit Delft*
- 2. "Packaging and Interconnect Challenges for Cryogenic and Quantum Systems", Michael Hamilton, *Auburn University*
- 3. "Josephson Junction Based Control Electronics for Superconducting Qubits", Adam Sirois, *NIST*
- 4. "Cryogenic Microwave Measurement and Characterization Approaches for Communications and Quantum Information", **Alirio Boaventura**, *NIST*

- 5. "Towards Automated Microwave Measurements and Calibrations at Millikelvin Temperatures", **Rich Chamberlin, Elyse McEntee Wei**, *NIST*
- 6. "Application of a VNA for Measurement of Superconducting Microwave Resonators", **Suren Singh**, *Keysight Technologies*
- 7. "Developing S-Parameter Measurement Setups for Characterizing Superconducting Qubit Circuits at mK Temperatures", **Manoj Stanley, Nick Ridler**, *NPL*
- 8. "Towards Millions of Qubits in a Quantum SoC", **Robert Bogdan Staszewski¹**, **Imran Bashir²**, **Elena Blokhina¹**, ¹University College Dublin, ²Equal1 Labs

WSG (full day): 08:00–17:00 mm-Wave Design Challenges and Solutions for 6G Wireless Communications

Sponsor: RFIC

Organizers: Hsieh-Hung Hsieh, TSMC Tim LaRocca, Northrop Grumman Qun Jane Gu, University of California, Davis

Abstract: With recent 5G deployment underway, the focus of wireless research is shifting toward 6G, which is expected to have a peak data rate of 1Tb/s and air latency less than 100 microseconds, 50 times the peak data rate and one-tenth the latency of 5G. To achieve Tb/s transmissions in 6G, it is inevitable to utilize the frequency band over 100GHz or sub-THz due to enormous amount of available bandwidth. However, the use of such high frequency bands results in more design challenges of RF circuits including output power, noise, linearity, signal conversion, and high-quality signal source for 6G communications and sensing. In addition, the optimal phased array architecture needs to be carefully analyzed such that the compact and energy-efficient system package can be attained. Moreover, to compensate for the severe mm-wave or sub-THz path loss, a large number of phased array is required to enhance EIRP and SNR while appropriate designs are necessary to establish reliable wireless links and ensure the array performance. Failure in any of these will prevent us from moving forward regarding the development of 6G. In this workshop, the main theme to be discussed concentrates on mm-wave design challenges and solutions for 6G wireless communications, especially targeting RF circuits. The workshop starts with an overview of mm-wave 6G to illustrate the whole picture to the audience. Afterwards, the RF design challenges based on silicon technologies to realize 6G systems are paid more attention while the innovative design techniques are provided such that the advantages of low cost and high-level integration in silicon can be still obtained. For in-depth exploration, being a critical building block in RF front-ends, mm-wave and sub-THz PA is specially under discussion to investigate the design bottlenecks as well as technology limitations, and the potential solutions and technology directions are presented. Besides RF designs, the analysis of phased-array architecture suitable for 6G applications is mentioned while the analog and digital beamforming structures are compared. In this workshop, to overcome the hurdles arising from silicon technologies, a new silicon-compatible III-V technology is introduced to facilitate 6G RF front-end designs. This workshop also covers the mm-wave and sub-THz communication and sensing systems from the top-down perspective for the comprehensive demonstration of 6G realization.

Speakers:

- 1. "Overview of mm-Wave 6G: Opportunities and Challenges", Gary Xu, Samsung
- 2. "Energy-Efficiency in Power Amplifiers and Transmitters for Digital Beamforming Arrays Above 100GHz", **James F. Buckwalter**, *University of California, Santa Barbara*
- 3. "Practical Approaches to Industrializing Near-THz Communication Systems", **Shahriar** Shahramian, *Nokia Bell Labs*
- 4. "mm-Wave RF Transceiver Designs Over 100GHz for 6G Wireless Communications", Kenichi Okada, *Tokyo Tech*
- 5. "mm-Wave PA Design Challenges and Solutions for 6G Applications", **Hua Wang**, *ETH Zürich*
- 6. "Next-Generation Phased Arrays for 6G mm-Wave Wireless Communications", Amr Ahmed, Siwei Li, Gabriel M. Rebeiz, University of California, San Diego
- 7. "Joint 3D Sensing and Communication at mm-Wave", Arun Paidimarri, *IBM T.J. Watson Research Center*
- 8. "Heterogeneous III-V/CMOS Technologies for Beyond-5G and 6G Solutions to RF Front-End Circuits", **Nadine Collaert**, *imec*

WSH (full day): 08:00–17:00 mm-Wave and THz Systems for Near-Field Imaging, Spectroscopy and Radar Sensing Applications

Sponsor: RFIC

Organizers: Vadim Issakov, Technische Universität Braunschweig Omeed Momeni, University of California, Davis

Abstract: The amount of sensing applications at mm-wave frequencies is continuously growing. Most of the applications can be addressed by classical radar techniques, but not all. Additional types of novel energy efficient sensing concepts for near-field imaging arrays and spectroscopy are being investigated. This full-day workshop covers near-field sensing and advanced state of the art radar techniques at mm-wave and THz frequencies. The intention is to showcase the unique applications and innovative concepts for sensing different materials and parameters including vital signs, small motions and distances, permittivity, humidity and gas density, and biomolecules using mm-wave to THz frequencies. The first half of the workshop will focus on various solutions for mm-wave and THz imaging and spectroscopy. For example, real-time THz super-resolution near-field imaging will be discussed, as well as transceivers at THz for gas spectroscopy. Advantages and disadvantages of various sensing approaches will be discussed. In the second half, we will discuss the latest trends and future directions in mm-wave radar systems. We will focus specifically on novel mm-wave radar modulation schemes, advanced system and circuit realizations. The emphasis is on digital radar modulation techniques, such as OFDM, PMCW, spread-spectrum, and their advantages or disadvantages versus classical FMCW radar realizations. The main idea of the workshop is to give an overview on mm-wave and THz sensing concepts and show the future directions for the advanced mm-wave radar radar transceivers.

Speakers:

- 1. "Towards High-Angular-Resolution Radar Imaging at Sub-THz", Ruonan Han, MIT
- 2. "An Integrated-Circuit Approach to THz Bio-Medical Applications", **Ullrich R. Pfeiffer**, *Bergische Universität Wuppertal*
- "RFIC Design Challenges Dealing with mm-Wave Massive MIMO Radars", Nadav Mazor, Pär Svalänge, Vayyar Imaging
- 4. "Fully Integrated FMCW Radars: Devices to Systems", **Ehsan Afshari**, *University of Michigan*
- 5. "Advanced Digital Modulation Schemes for mm-Wave Radar Systems", **Thomas Zwick**, *KTT*
- 6. "Highly-Integrated PMCW and FMCW Radar Systems on Chip in CMOS", **Ilja Ocket**, *imec*
- 7. "System-Level Considerations on mm-Wave Radar for Proximity Sensing", **Vincent** Lammert, Matteo Bassi, *Infineon Technologies*

WSI (full day): 08:00–17:00 Advanced Interference Mitigation in Integrated Wireless Transceivers

Sponsor: RFIC

Organizers: Alyosha Molnar, Cornell University Harish Krishnaswamy, Columbia University Jin Zhou, University of Illinois at Urbana-Champaign

Abstract: Modern transceivers often rely on many discrete components, such as SAW and BAW filters and duplexers, to protect them from interference. The number of these discrete front-end components is expected to grow further as more bands are made available at RF and mm-wave frequencies, limiting the system cost, form factor and flexibility. Also, while integrated self-interference cancellation has been demonstrated, many challenges remain at the antenna interface and scaling to phased-array and MIMO transceivers. In this workshop, experts from academic and industry will present the state-of-the-art interference mitigation approaches that can be applied to integrated wireless transceivers. Finally, the workshop will conclude with an interactive panel discussion about the potential and limitations of integrated interference mitigation.

- 1. "Introduction to RF and mm-Wave Interference Mitigation (Past Work and Future Directions)", Alyosha Molnar, *Cornell University*
- 2. "Multi-Blocker-Tolerant Passive MIMO Receivers", **Ramesh Harjani**, *University of Minnesota*
- 3. "Passive-Mixer-First Acoustic-Filtering Superheterodyne RF Front-Ends", **Jin Zhou**, *University of Illinois at Urbana-Champaign*
- 4. "Integrated Non-Reciprocal Components: Design, Applications and Future Directions", Aravind Nagulu, *Washington University in St. Louis*
- 5. "Multi-Antenna Full-Duplex Receivers", Mahmood Dastjerdi, MixComm
- 6. "Transceiver Techniques for FDD and Full-Duplex Wireless", **Emanuel Cohen**, *Technion*
- 7. "Time-Approximation Filter for Direct RF Transmitter", **Shiyu Su, Shuo-Wei Chen**, *University of Southern California*
- 8. "Mitigation of Reciprocal Mixing Caused by Phase Noise and Spurs in Wideband RF Receivers", **Hao Wu**, *Broadcom*

WSJ (full day): 08:00–17:00 System Design Considerations for Advanced Radios

Sponsor: RFIC

Organizers: Travis Forbes, Sandia National Laboratories Raja Pullela, MaxLinear Oren Eliezer, Ambiq

Abstract: This workshop will walk you through the steps involved in designing today's complex radios for applications such as infrastructure cellular, Wi-Fi or mm-wave beam forming arrays from a systems perspective. The workshop caters to students, as well as experienced engineers in the industry, with background in RF systems, circuit design or standards, who are interested in expanding the scope of their knowledge beyond the narrow design tasks they may be exposed to. Attendees will learn how system specifications are derived, how we partition design between RF/ Analog/Mixed-signal and digital sections to achieve the most optimum solution in terms of size, power, external BOM. You will hear from speakers who are experts in their areas: a mix from industry and academia. Standards related specification and product level requirements that drive architecture or topology choices will be presented. Using Wi-Fi 802.11be emerging standard as an example, we will outline the salient features and how they compare with previous generations. We will address design considerations imposed by the new standard requirements, with particular focus on RF. Presentations focused on base station cellular transceivers will illustrate the differences between narrow-band (mixer-based) and Direct Sampling/Synthesis approaches. Using microwave and mmwave point to point communication systems, we will go over design aspects such as line-up analysis to arrive at block level specifications. We will present transmit/receive circuit/system challenges in large-scale arrays, followed by approaches towards realizing scalable, digital-intensive large-scale arrays. Design advances in critical building blocks, such as blocker tolerant receivers and ADPLLs will also be discussed. We will present built-in self-calibration techniques and built-in mitigation of self-interference, leading to reduced production testing costs and high production yields. Calibration techniques to overcome impairments such as IQ error or LO offset calibration and Digital Pre-Distortion (DPD) for linearization of power amplifiers will be discussed.

Speakers:

- 1. "Design Considerations for Radios for Cellular Infrastructure", **David McLaurin**, *Analog Devices*
- 2. "Wireless Point to Point Communication System Design Considerations", **Vamsi Paidi**, *MaxLinear*

- 3. "Design Considerations for Direct RF Sampling and Synthesis Wideband Radios", **Gabriele Manganaro**, *MediaTek*
- 4. "All-Digital Phase-Locked Loops (ADPLL) Architectures and Implementations", **Teerachot Siriburanon**, *University College Dublin*
- 5. "Design Considerations for Next-Generation Wi-Fi Standards", **Sigurd Schelstraete**, *MaxLinear*
- 6. "Beamforming and MIMO Transceivers for Communication and Radar Systems", **Arun** Natarajan, *Oregon State University*
- 7. "Receiver Design Techniques to Maintain Sensitivity in the Presence of Large Blockers", **Travis Forbes**, *Sandia National Laboratories*
- 8. "Design for Manufacturability in High-Volume Extensively Digital RF Transceivers", **Oren Eliezer**, *Ambiq*

WSK (half day): 08:00–12:00 Toward Tbps Optical and Wireline Transceivers: A Tutorial for RFIC Designers

Sponsor: RFIC/IMS

Organizers: Bahar Jalali Farahani, Cisco Mahdi Parvizi, Cisco

Abstract: According to the latest report by Global Market Insights Inc. the market valuation of optical communication and networking will cross \$30 billion by 2027. The significant revenue comes from the emerging technologies such as IoT (Internet of things), machine-to-machine networks, AI, cloud-based services, and web-based applications. Several innovations are underway to enhance the wireline and optical transceiver designs so that they can serve the increase in demand and future generations of applications.

Speakers:

- 1. "Market Forces and Network Evolution", Martin Zirngibl, MACOM
- 2. "Advancements in High-Speed Packaging", **Clint Schow**, *University of California, Santa Barbara*
- 3. "Architecting Wireline Transceivers for Beyond 1Tbps Applications", **Tony Chan Carusone**, *University of Toronto*
- 4. "Coherent vs PAM-4 Optics in the Data Center", Alexander Rylyakov, Nokia
- 5. "Towards Tb/s Coherent Silicon Photonic Links", **Sudip Shekhar**, University of British Columbia

WSL (half day): 13:30–17:00 Wireless Proximity Communication

Sponsor: RFIC/IMS

Organizers: Rocco Tam, NXP Semiconductors Yao-Hong Liu, imec

Abstract: Wireless proximity communication provides many unique features over conventional wireless communication such as ultra-high data rate, superior data privacy, energy efficiency, mechanical reliability, precision ranging and bandwidth density. However, those unique features always come with many design trade-offs in system complexity, effective communication distance, energy efficiency and system robustness. In this workshop, we are going to go over several wireless proximity communication techniques such as Mid-Field powering and communication for bio-medical implants, impulse ultra-wide-band and mm-wave. The first and second workshops will introduce the applications in latest UWB standard (IEEE 802.15.4z), and the design trade off in commercial UWB SoC system and circuit design. The third workshop will focus on Mid-Field technology offers advantages such as significantly smaller, implanted deeper, implant complexity, patient complication and post-surgical pain. The last work workshop presents the overview of solid-state-based mm-wave wireless interconnects from fundamental research to commercialization.

Speakers:

- 1. "Energy-Efficient IEEE 802.15.4z IR-UWB Transceiver Design", **Minyoung Song**, *Holst Centre*
- 2. "Ultra-Wide Band Technology, New Era, New Use Cases", **Babak Vakili-Amini**, *NXP* Semiconductors
- 3. "Mid-Field Technology for Biomedical Neuromodulation Implantable System", Alexander Yeh, *NeuSpera Medical*
- 4. "mm-Wave Contactless Connectors: From Fundamental Research to Commercialization", **Yanghyo Kim**, *Stevens Institute of Technology*

WSM (half day): 08:00–12:00 Recent Developments in Sub-6GHz PAs and Front-End Modules

Sponsor: RFIC/IMS

Organizers: Alexandre Giry, CEA-Leti Jennifer Kitchen, Arizona State University

Abstract: Increasing demand for high data rates, reduced latency, and increased device density are driving the development of 5G wireless systems. 5G spectrum is presently covering sub-7GHz (FR1) and mm-wave bands (FR2, FR3,...). This workshop will bring together experts from academia and industry to highlight recent works and performance trends related to 5G-FR1 Power Amplifiers (PAs)

and Front-End Modules (FEMs). Multiband and high linearity requirements, along with the need for higher power and reduced power consumption, make the design of 5G-FR1 PA and FEM highly challenging and critical to overall system performance. Recent trends in Doherty, class F/F-1, multi-stage PAs, and Envelope Tracking PA architectures will be highlighted and insights into different design techniques and integration technologies (CMOS, SOI, GaN) will be presented as pathways to enable the integration of future PAs and FEMs. An introduction to emerging heterogeneous technologies combining high-power GaN with CMOS will also provide the attendees with new directions for next-generation PA design and integration.

Speakers:

- 1. "Power Amplifier Circuit Design Techniques for 4/5G Mobile Phone Terminals", **Satoshi Tanaka**, *Murata Manufacturing*
- 2. "An Overview of Envelope Tracking PAs and Hybrid Supply Modulators in CMOS Technologies", **Jennifer Kitchen**, *Arizona State University*
- 3. "Hybrid Architectures and Technologies for Load-Modulated Power Amplifiers", **Ayssar Serhan**, *CEA-Leti*
- 4. "Heterogeneous GaN and RFSOI Technology: Device and Circuits", **Gregory U'Ren**, *X-FAB*
- 5. "RF Power Amplifier Architectures to Support Cellular Infrastructure for 5G and Beyond", **Joseph Staudinger, Maruf Ahmed**, *NXP Semiconductors*

WSN (half day): 13:30–17:00 Digitally Intensive PAs and Transmitters for RF Communication

Sponsor: RFIC

Organizers: Xun Luo, UESTC Debopriyo Chowdhury, Broadcom

Abstract: The power amplifiers (PA) and transmitters are the last door in the RF front-end for both the digital and analog kingdoms, one which greatly affects the quality of service (QoS) of the wireless link for modern RF communication, such as 5G, IoT, and beyond. Due to the multi-function trends nowadays, this workshop will showcase the digitally intensive PAs and transmitters, which attract much attention due to their highly reconfigurable nature and rapid development that is on pace with the decreasing scale of CMOS technology. In the first talk, with the aim to powering the next generation of wireless communication, from RF to mm-wave, a series of switched capacitor power amplifiers are discussed. Then, CMOS digital power amplifier and transmitter for efficient signal amplification and beam steering are introduced in the second talk. Next, in the third talk, the all digital transmitter with GaN switching mode power amplifiers with high power efficiency is discussed. Later, digital polar transmitter for impulse-radio ultrawide band communication is introduced in the fourth talk. Finally, the high-performance digital-to-analog converter design towards a digital transmitter is discussed in the fifth talk.

Speakers:

- 1. "Switched Capacitor Power Amplifiers: Powering the Next Generation of Wireless Communication, from RF to mm-Wave", **Jeffrey Walling**, *Virginia Tech*
- 2. "All Digital Transmitter with GaN Switching Mode Power Amplifiers", Rui Ma, MERL
- 3. "CMOS Digital Power Amplifier and Transmitter for Efficient Signal Amplification and Beam Steering", **Huizhen Jenny Qian**, *UESTC*
- 4. "Digitally Intensive Power Amplifier Based Transmitter for Ultra-Low Power RF Communication", **Minyoung Song**, *Holst Centre*
- 5. "High-Performance Digital-to-Analog Converter Design Towards A Digital Transmitter", Mike Shuo-Wei Chen, University of Southern California

WSO (half day): 08:00–12:00 Human Body Communications

Sponsor: RFIC

Organizers: Antoine Frappé, University of Lille François Rivet, University of Bordeaux Fred Lee, Twenty/Twenty Therapeutics

Abstract: The human body is a new playground for wireless communications to connect health devices or open new services related to information exchange or security. It faces many constraints such as power consumption, quality of service, reliability, and of course being compatible with the human body. The last decade has seen several innovations that exploit the body as a medium to propagate the information efficiently. This workshop proposes a state-of-the-art of up-to-date research on the topic. It starts with an overview of body area networks and pioneering research on communications and power delivery through the body. It is followed by recent developments on broadband human-body communication transceivers for wearable health monitoring. Then, surface-wave capacitive body-coupled communications are introduced and challenges for upper layers and synchronization of nodes are addressed. Finally, intra-body communications using ultrasounds are explored to complete the scope of this workshop.

Speakers:

- 1. "Body Area Network Connecting and Powering Things Together Around the Human Body", **Jerald Yoo**, *NUS*
- 2. "Secure and Efficient Internet of Bodies Using Body as a 'Wire'", **Shreyas Sen**, *Purdue University*
- 3. "Capacitive Body-Coupled Communications and Heartbeat-Based MAC Protocol for the Human Intranet", **Guillaume Tochou**, *STMicroelectronics*
- 4. "How About Other Waves for Intra Body Communication? Ultrasound Maybe?", **Wim Dehaene**, *KU Leuven*

Social Events/Guest Program

SUNDAY, 19 June 2022

RFIC Welcoming Reception: 19:30–21:00

RFIC2022 starts with a welcome event on Sunday for all attendees, which will be hosted at the Hyatt Regency Denver Hotel immediately following the RFIC2022 Plenary Session.

MONDAY, 20 June 2022

IMS Welcome Event: 19:00-21:00

IMS2022 starts with a welcome event on Monday for all attendees, which will be hosted at the Denver Performing Arts Complex in the Sculpture Park and Galleria immediately following the IMS2022 Plenary Session.

MONDAY, 20 June 2022 – THURSDAY, 23 June 2022

Young Professionals' Lounge

RFIC2022 will host Young Professionals' Lounge at the Colorado Convention Center Four Season Foyer. Students can hang out, play games, network, and also meet & greet the speakers of the student forums after the Tuesday lunch panel.

Guest Lounge: 07:00-13:00

Located at the Hyatt Regency Denver Hotel. Light refreshments will be provided for all registered guests.

TUESDAY, 21 June 2022

Networking Reception: 19:00–21:00

The Young Professionals are planning a Lounge Area at the Colorado Convention Center dedicated to Young Professionals where they will hold multiple panel sessions and activities throughout the week. The Young Professionals Networking Reception will be held at the ViewHouse Eatery. Please refer to the conference website for detailed information on the panel sessions and activities.

WEDNESDAY, 22 June 2022

Industry-Hosted Cocktail Reception: 17:00-18:00

The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

Women in Microwaves Panel Session and Networking Event: 18:00–21:00

The Women in Microwaves Panel Session and Networking Event will be held at the Denver Performing Arts Complex in Chambers Grant Salon in the Opera House.

Awards Banquet: 18:30-20:00

The MTT-S Awards Banquet will be hosted at the Hyatt Regency Denver Hotel and will feature exciting entertainment.

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