



# 2020 IEEE Radio Frequency Integrated Circuits Symposium

Virtual Event  
4–6 August 2020



## PROGRAM

*Sponsored by*

IEEE Microwave Theory and Techniques Society  
IEEE Electron Devices Society  
and  
IEEE Solid-State Circuits Society



# RFIC Virtual Event

4–6 August 2020

**Tuesday 4 August 2020, 09:00–13:00 PDT:** Three Minute Thesis (3MT)

**Tuesday 4 August 2020, 16:00–17:30 PDT:** The Plenary Session begins with the Student Paper Awards, Industry Paper Awards, and Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Dr. Thomas Byunghak Cho (Corporate Executive Vice President of the System LSI Business at Samsung Electronics) and Prof. Ali Hajimiri (Bren Professor of Electrical Engineering and Medical Engineering at Caltech).

All Pre-Recorded Technical Sessions will be available immediately following the Plenary Session.

**Wednesday 5 August 2020, 11:30–13:00 PDT:** Joint IMS/RFIC Panel Session

**Wednesday 5 August 2020, 13:00–17:00 PDT:** 5G Summit

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## Welcome Message from Chairs

We invite you to join us in the 2020 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held as a virtual symposium beginning on 4 August 2020. The RFIC Symposium is the premier IC conference focused exclusively on the latest advances in RF, mm-wave and high-frequency analog/mixed-signal IC technologies and designs. The Symposium, combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition, form “Microwave Week”, the largest worldwide RF/microwave technical meeting of the year.

While we are regrettably unable to gather in person due to the COVID-19 pandemic, the RFIC and our IMS and ARFTG partners, with support from our organizers and sponsors, have worked tirelessly to build a world-class virtual platform through which we hope to provide a rewarding and engaging experience. A single registration will allow attendees to access all Microwave Week content, including RFIC, IMS, ARFTG, the 5G Summit, a virtual exhibition, panel sessions, and more. This registration is free to all members of the IEEE Microwave Theory and Technique Society (MTTS). All Microwave Week content will be available on-line beginning on 4 August 2020 and lasting through 30 September 2020.

The 2020 RFIC Symposium will begin on Tuesday, 4 August 2020, with the RFIC Plenary Session. This session will be streamed live, beginning at 16:00 PDT, and will then be made available afterwards on demand. The Session will feature two visionary talks by our distinguished plenary speakers. Dr. Thomas Cho, Executive Vice President, Infrastructure & Design Technology Center, System LSI Business, at Samsung Electronics, will share his vision for the future of RFIC in his talk “Is the Third Wave Coming in CMOS RF?”, providing a historical perspective and analyzing in depth the diverse challenges and opportunities looking ahead in RF integrated circuits and systems technology. Prof. Ali Hajimiri, Bren Professor of Electrical Engineering and Medical Engineering, California Inst. of Technology (Caltech), will deliver his vision on integrating RFIC with flexible electronics in his talk “The Flexible Future of RF”, giving a perspective on a breadth of new applications ranging from wearable RF fabric to instantly deployable communication networks to wireless power transfer systems, to enable a truly wireless ecosystem of the future.

Our technical program continues with presentations of 95 papers organized within 21 technical sessions. These pre-recorded video presentations will be available to attendees on demand from 4 August 2020 through 30 September 2020, allowing attendees to digest all that our symposium has to offer. Our papers feature cutting-edge research on power amplifiers, phased arrays, advanced transceivers, imagers and radars, synthesizers and VCOs, IoT, RF and mm-wave front ends, semiconductors, and RF systems and applications. As part of this, we also plan to feature our top student-authored papers and top industry-authored papers.

For those attendees looking to understand the latest breakthroughs in 5G technology, two special 5G focus sessions have been organized at RFIC along with special 5G sessions at IMS and the 5G Summit. The 5G Summit will feature talks from some of the world’s leading experts in 5G systems and technologies, discussing topics such as the evolution of front-ends, silicon technology differentiation, application and deployment challenges of the 5G network, and perspectives from fabless semiconductor companies. This 5G Summit will be live streamed on Wednesday, 5 August 2020 at 13:00 PDT and then made available on demand.

A joint RFIC/IMS live-streamed panel session is scheduled for Wednesday, 5 August 2020 at 11:30 PDT. This panel will feature speakers discussing the important topic of “Who Needs RF When We Can Digitize at the Antenna Interface?”. This topic is sure to interest both experts and newcomers alike.

Finally, as students of today will be our leaders for tomorrow, the RFIC 2020, in partnership with IMS, offers opportunities for students to enhance their career growth and educational experiences. These include the RFIC student paper contest and the Three-Minute Thesis (3MT<sup>®</sup>) program.

Behind the scenes, the steering committee has implemented important changes for RFIC 2020 in an effort to introduce new research content and chart a path of growth for our symposium. In addition to the Emerging Circuits area introduced in RFIC 2019, the symposium has expanded its scope to System and Applications. This includes papers and presentations on systems and applications in 5G, radar, imaging, terahertz, biomedical, security, IoT, and optoelectronic areas. Two sessions will feature papers from this new area and we expect many more in future years.

On behalf of the RFIC Steering, Executive and Technical Committees, we welcome you to join us at the 2020 RFIC Symposium! Please visit the RFIC 2020 website (<https://rfic-ieee.org/>) for more details and updates.



**Waleed Khalil**  
General Chair  
The Ohio State University



**Brian Floyd**  
TPC Chair  
North Carolina State University



**Osama Shana'a**  
TPC Co-Chair  
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Wanghua Wu, *Samsung*  
Haolu Xie, *Transa Semiconductor*  
Hongtao Xu, *Fudan University*

# Plenary Session

**Tuesday, 4 August 2020**

**16:00–17:30 PDT**

**General Chair: Waleed Khalil, The Ohio State University**

**TPC Chair: Brian Floyd, North Carolina State University**

**TPC Co-Chair: Osama Shana'a, MediaTek**

- 16:00 Welcome Message from General Chair, TPC Chair, and TPC Co-Chair  
Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
- 16:30 *Is the Third Wave Coming in CMOS RF?*  
Dr. Thomas Byunghak Cho  
Corporate Executive Vice President of the System LSI Business at Samsung Electronics
- 17:00 *The Flexible Future of RF*  
Prof. Ali Hajimiri  
Bren Professor of Electrical Engineering and Medical Engineering at Caltech





## Plenary Speaker 1

**Dr. Thomas Byunghak Cho**  
**Corporate Executive Vice President**  
**System LSI Business**  
**Device Solutions Division**  
**Samsung Electronics**

### *Is the Third Wave Coming in CMOS RF?*

**Abstract:** In the late 90's, academia's active research on CMOS RF, combined with the industry's increasing need for compact and low-cost mobile devices, had triggered a succession of waves in CMOS RF, making the rapid deployment and widespread commercialization of CMOS RFICs. Of course, there were many technical challenges and concerns in using CMOS for RF for the first time, such as substrate noise, lack of good RF models, etc. However, they weren't big enough to stop those waves. In fact, CMOS scaling for digital and increasing digital signal processing capabilities added extra momentum to the waves. As a result, CMOS RF has played a key role in enabling many generations of modern solutions for a variety of wireless applications such as Cellular, WiFi, BT, GPS, IoT, etc.

Now, we are in 2020. The market is still hot. It demands even more mobile performance than before. New applications such as 5G, Automotive, AR/VR, etc. are on the rise. However, for RFIC designers, the situation is even more challenging than before. RF performance gain from scaling has slowed down. Sub-6GHz spectrum is quite busy and crowded, pushing new standards to higher frequency. Low power consumption is ever important. In this complex situation, several questions arise. Is the third wave coming in CMOS RF? If so, what are the winds that will create the new wave? Is the wave big enough to enable new applications? In this talk, we will briefly go over the past two decades of CMOS RF history and examine these questions to gain insights into the future.

### **About Dr. Thomas Byunghak Cho**

Dr. Thomas Cho is a Corporate Executive Vice President of the System LSI Business in Samsung Electronics' Device Solutions Division, responsible for centralized development of SOC design/verification platform and various core IP/ICs including RF, analog, mixed-signal, and multimedia. Prior to his current role, he served as Senior Vice President from 2016 to 2018 and as Vice President from 2012 to 2015, managing the development of cellular and connectivity RFICs and data converters for several generations of the Exynos modem platforms. Prior to joining Samsung Electronics in 2012, he was with several different Silicon Valley companies, including Marvell, Intel, and Level One Communications, and led the development of numerous CMOS RF/Analog/Mixed-signal ICs for both wireless and wireline communication applications.

Dr. Cho earned his B.S. degree from the University of California at Los Angeles, and M.S. and Ph.D. degrees from the University of California at Berkeley, all in electrical engineering. He holds over 40 patents in RF/Analog/Mixed-signal circuit/system design and has authored and co-authored over 50 conference and journal papers.



## Plenary Speaker 2

**Prof. Ali Hajimiri**  
**Bren Professor of**  
**Electrical Engineering & Medical Engineering**  
**Caltech**

### *The Flexible Future of RF*

**Abstract:** Over the last quarter of a century, RF and mm-wave CMOS integrated circuits have gone from the realm of exotic research to becoming the only realistic way to implement almost all commercial communication and sensing systems. The ability to reliably integrate a large number of active and passive components operating at RF and mm-wave frequencies continues to enable an unlimited number of new applications and design approaches previously not practical or economical. Wireless power transfer at a distance is an example of an emerging third prong of novel use cases for RF and mm-waves integrated circuits.

Despite these major advances, such RF and microwave systems remain relatively small, static, and rigid, thereby limiting their ability to be used in many novel applications ranging from wearable fabric, to easily deployable large-scale arrays in various environments. Such systems can provide significant additional utilization of the unprecedented IC fabrication capacity of the silicon foundries and enable yet another wave of new domains of use.

Flexible lightweight collapsible active electromagnetic surfaces enabled by an array of CMOS RFICs with the dynamic ability to compensate and correct for mechanical changes in the real time can open the door to a breadth of new applications from RF active fabric for clothing to communication and wireless power transfer systems that can be rapidly deployed on the ground and in space to enable a truly wireless ecosystem of the future.

### **About Prof. Ali Hajimiri**

Prof. Ali Hajimiri is the Bren Professor of Electrical Engineering and Medical Engineering at California Institute of Technology (Caltech), where he has served as a faculty member since 1998. He has had several appointments in the industry and has co-founded several start-ups companies in the field of RFIC, such as Axiom Microdevices Inc., whose fully-integrated CMOS PA has shipped around 400,000,000 units, and was acquired by Skyworks Inc.

Prof. Hajimiri has authored and coauthored more than 200 refereed journal and conference technical articles. He has been granted more than 100 U.S. patents and has many more pending applications.

Prof. Hajimiri is a Fellow of National Academy of Inventors (NAI). Prof. Hajimiri was selected to the TR35 top innovator's list. He is also a Fellow of IEEE and has served as a Distinguished Lecturer of the IEEE Solid-State and Microwave Societies. He won the Feynman Prize for Excellence in Teaching, Caltech's most prestigious teaching honor. He was a co-recipient of the IEEE Journal of Solid-State Circuits Best Paper Award, the International Solid-State Circuits Conference (ISSCC) Jack Kilby Outstanding Paper Award, a co-recipient of RFIC best paper award, a two-time co-recipient of CICC best paper award.

**Tuesday, 4 August 2020**

**17:00–17:30 PDT**

# The Industry Showcase

Chair: Fred Lee, Verily Life Sciences

The RFIC Industry Showcase highlights ten outstanding industry papers, which are listed below. These papers received nominations for this recognition from the TPC sub-committees, and possess among the highest normalized scores from the double-blind review process. From these top ten papers, a committee of eleven TPC judges, also in a double-blind fashion, have selected the top three Industry Papers after rigorous reviews and discussions. The top three will be announced during the RFIC Virtual Plenary Session on 4 August 2020, and each winner will receive a plaque. This year's Industry Paper Award finalists are:

## *3D Imaging Using mmWave 5G Signals*

IBM T.J. Watson Research Center, USA

Junfeng Guan, Arun Paidimarri, Alberto Valdes-Garcia, Bodhisatwa Sadhu

RMo3A-1

## *Spatio-Temporal Filtering: Precise Beam Control Using Fast Beam Switching*

IBM T.J. Watson Research Center, USA

Arun Paidimarri, Bodhisatwa Sadhu

RMo4A-2

## *A 77GHz 8RX3TX Transceiver for 250m Long Range Automotive Radar in 40nm CMOS Technology*

DENSO, Japan

Tatsunori Usugi, Tomotoshi Murakami, Yoshiyuki Utagawa, Shuya Kishimoto, Masato Kohtani, Ikuma Ando, Kazuhiro Matsunaga, Chihiro Arai, Tomoyuki Arai, Shinji Yamaura

RMo1B-2

## *A 1.2V, 5.5GHz Low-Noise Amplifier with 60dB On-Chip Selectivity for Uplink Carrier Aggregation and 1.3dB NF*

Infineon Technologies, Austria

Daniel Schrögendorfer, Thomas Leitner

RTu2C-2

## *A D-Band Radio-on-Glass Module for Spectrally-Efficient and Low-Cost Wireless Backhaul*

Nokia Bell Labs, USA

Amit Singh, Mustafa Sayginer, Michael J. Holyoak, Joseph Weiner, John Kimionis, Mohamed Elkhoully, Yves Baeyens, Shahriar Shahramian

RMo2B-3

## *Fully Autonomous System-on-Board with Complex Permittivity Sensors and 60GHz Transmitter for Biomedical Implant Applications*

<sup>1</sup>Infineon Technologies, Germany, <sup>2</sup>eesy-IC, Germany

V. Issakov<sup>1</sup>, C. Heine<sup>1</sup>, V. Lammert<sup>1</sup>, J. Stoegmueller<sup>1</sup>, M. Meindl<sup>2</sup>, U. Stubenrauch<sup>1</sup>, C. Geissler<sup>1</sup>

RMo3A-4

## *High Resolution CMOS IR-UWB Radar for Non-Contact Human Vital Signs Detection*

GRIT Custom-IC, Korea

Sang Gyun Kim, In Chang Ko, Seung Hwan Jung

RMo1B-3

*Parasitic Model to Describe Breakdown in Stacked-FET SOI Switches*

<sup>1</sup>Qorvo, USA, <sup>2</sup>University of Dayton, USA

Kathleen Muhonen<sup>1</sup>, Scott Parker<sup>1</sup>, Kaushik Annam<sup>2</sup>

RMo2D-3

*77GHz CMOS Built-In Self-Test with 72dB C/N and Less Than 1ppm Frequency Tolerance for a Multi-Channel Radar Application*

DENSO, Japan

Masato Kohtani, Tomotoshi Murakami, Yoshiyuki Utagawa, Tomoyuki Arai, Shinji Yamaura

RMo1B-5

*A Reconfigurable SOI CMOS Doherty Power Amplifier Module for Broadband LTE High-Power User Equipment Applications*

<sup>1</sup>CEA-Leti, France, <sup>2</sup>Huawei Technologies, Belgium

A. Serhan<sup>1</sup>, D. Parat<sup>1</sup>, P. Reynier<sup>1</sup>, M. Pezzin<sup>1</sup>, R. Mourot<sup>1</sup>, F. Chaix<sup>1</sup>, R. Berro<sup>1</sup>, P. Indirayanti<sup>2</sup>, C. De Ranter<sup>2</sup>, K. Han<sup>2</sup>, M. Borremans<sup>2</sup>, E. Mercier<sup>1</sup>, A. Giry<sup>1</sup>

RMo2A-2

Industry Paper Contest Eligibility: The first author must have an affiliation from industry. The first author must also be the lead author of the paper and must submit a pre-recorded technical presentation to be shown during the virtual conference.

# The Student Paper Awards Finalists

Chair: Donald Y.C. Lie, Texas Tech University

The RFIC Symposium's Student Paper Award is devised to both encourage student paper submissions to the conference as well as give the authors of the finalists' papers a chance to promote their research work with the conference attendees after the plenary session during reception time. A total of thirteen outstanding student paper finalists were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of ten TPC judges have selected the top-three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top-three Student Papers will be announced during the RFIC Virtual Plenary Session on 4 August 2020. Each winner will receive an honorarium and a plaque. This year's Student Paper Award finalists are:

*Ultra Compact, Ultra Wideband, DC-1GHz CMOS Circulator Based on Quasi-Electrostatic Wave Propagation in Commutated Switched Capacitor Networks*

Aravind Nagulu<sup>1</sup>, Mykhailo Tymchenko<sup>2</sup>, Andrea Alù<sup>2</sup>, Harish Krishnaswamy<sup>1</sup>

<sup>1</sup>Columbia University, USA, <sup>2</sup>University of Texas at Austin, USA

RM01C-5

*A 66.97pJ/Bit, 0.0413mm<sup>2</sup> Self-Aligned PLL-Calibrated Harmonic-Injection-Locked TX with >62dBc Spur Suppression for IoT Applications*

Chung-Ching Lin, Huan Hu, Subhanshu Gupta

Washington State University, USA

RTu2A-1

*A Scalable 60GHz 4-Element MIMO Transmitter with a Frequency-Domain-Multiplexing Single-Wire Interface and Harmonic-Rejection-Based De-Multiplexing*

Ali Binaie<sup>1</sup>, Sohail Ahasan<sup>1</sup>, Armagan Dascurcu<sup>1</sup>, Mahmood Baraani Dastjerdi<sup>1</sup>, Robin Garg<sup>2</sup>, Manoj Johnson<sup>2</sup>, Arman Galioglu<sup>1</sup>, Arun Natarajan<sup>2</sup>, Harish Krishnaswamy<sup>1</sup>

<sup>1</sup>Columbia University, USA, <sup>2</sup>Oregon State University, USA

RM03B-3

*A SiGe Millimeter-Wave Front-End for Remote Sensing and Imaging*

Milad Frounchi, John D. Cressler

Georgia Tech, USA

RM04B-3

*A 1.5–3GHz Quadrature Balanced Switched-Capacitor CMOS Transmitter for Full Duplex and Half Duplex Wireless Systems*

Nimrod Ginzberg<sup>1</sup>, Dror Regev<sup>2</sup>, Emanuel Cohen<sup>1</sup>

<sup>1</sup>Technion, Israel, <sup>2</sup>Toga Networks, Israel

RM02C-1

*A Dual-Mode V-Band 2/4-Way Non-Uniform Power-Combining PA with +17.9-dBm  $P_{sat}$  and 26.5-% PAE in 16-nm FinFET CMOS*

Kun-Da Chu<sup>1</sup>, Steven Callender<sup>2</sup>, Yanjie Wang<sup>3</sup>, Jacques C. Rudell<sup>1</sup>, Stefano Pellerano<sup>2</sup>, Christopher Hull<sup>2</sup>

<sup>1</sup>University of Washington, USA, <sup>2</sup>Intel, USA, <sup>3</sup>USA

RM03C-1

*A DC to 43-GHz SPST Switch with Minimum 50-dB Isolation and +19.6-dBm Large-Signal Power Handling in 45-nm SOI-CMOS*

Ayman Eltaliawy<sup>1</sup>, John R. Long<sup>1</sup>, Ned Cahoon<sup>2</sup>

<sup>1</sup>University of Waterloo, Canada, <sup>2</sup>GLOBALFOUNDRIES, USA

RMo1D-2

*A Wideband True-Time-Delay Phase Shifter with 100% Fractional Bandwidth Using 28nm CMOS*

Minjae Jung, Hong-Jib Yoon, Byung-Wook Min

Yonsei University, Korea

RMo1D-1

*A 16-Element Fully Integrated 28GHz Digital Beamformer with In-Package 4×4 Patch Antenna Array and 64 Continuous-Time Band-Pass Delta-Sigma Sub-ADCs*

Rundao Lu, Christine Weston, Daniel Weyer, Fred Buhler, Michael P. Flynn

University of Michigan, USA

RTu2B-1

*A Dual-Core 8–17GHz LC VCO with Enhanced Tuning Switch-Less Tertiary Winding and 208.8dBc/Hz Peak FoM<sub>r</sub> in 22nm FDSOI*

Omar El-Aassar, Gabriel M. Rebeiz

University of California, San Diego, USA

RMo4C-4

*A 7.4dBm EIRP, 20.2% DC-EIRP Efficiency 148GHz Coupled Loop Oscillator with Multi-Feed Antenna in 22nm FD-SOI*

Muhammad Waleed Mansha, Mona Hella

Rensselaer Polytechnic Institute, USA

RTu1A-5

*Characterization of Partially Overlapped Inductors for Compact Layout Design in 130nm RFCMOS and 22nm FinFET Processes*

Xuanyi Dong, Andreas Weisshaar

Oregon State University, USA

RMo2D-2

*A Hybrid-Integrated Artificial Mechanoreceptor in 180nm CMOS*

Han Hao, Lin Du, Andrew G. Richardson, Timothy H. Lucas, Mark G. Allen,

Jan Van der Spiegel, Firooz Aflatouni

University of Pennsylvania, USA

RMo3A-3

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper.

## IMS/RFIC 2020 Joint Panel Session

Wednesday, 5 August 2020

11:30–13:00 PDT

IMS2020 Panel/Rump Sessions Chairs:

Fred Schindler, Independent Consultant, USA

John Wood, Wolfspeed, USA

RFIC2020 Panel Sessions Chair: Andre Hanke, Intel, USA

### Who Needs RF When We Can Digitize at the Antenna Interface?

*Panel Organizer and Moderator:*

**Lawrence Kushner**, *Raytheon Technologies, USA*

*Panelists:* **Timothy M. Hancock**, *DARPA Microelectronics Technology Office, USA*

**Gabriel M. Rebeiz**, *University of California, San Diego, USA*

**Craig Hornbuckle**, *Jarret Technologies, USA*

**Jacques C. Rudell**, *University of Washington, USA*

**Harold Pratt**, *Raytheon Technologies, USA*

**Boris Murmann**, *Stanford University, USA*

**Abstract:** With the advent of GS/s data converters driven by Moore's law and advances in converter architectures, it is now possible to digitize directly at RF. The question is, should we? On the one hand, eliminating mixers, filters, amplifiers, and local oscillators reduces RF complexity and allows more flexible, multi-function designs. On the other hand, do we really want to digitize the entire spectrum from DC to daylight and process 10's of GS/s of data if the information BW we care about is orders of magnitude lower? In the context of phased arrays, element-level digital beamforming allows simultaneous beams with different beamwidths and pointing angles, but may be more susceptible than analog-beam-formed arrays to interferers since spatial filtering occurs after the analog-to-digital conversion. What is the right approach? Our distinguished panel will debate the pros and cons of competing system architectures and the audience will be engaged to judge who is right.

# 5G Summit

Wednesday, 5 August 2020

13:00–17:00 PDT

IMS2020 5G Summit Chair & Co-Chair:

Walid Y. Ali-Ahmad, Samsung, USA

Timothy LaRocca, Northrop Grumman, USA

**Abstract:** The technologies and systems for 5G are now pushing for commercial deployment with focus on Stand Alone (SA) networks, mass market for 5G devices, and global adoption of mmWave in premium devices and for small cell enhancement and fixed wireless access (FWA). Furthermore and looking beyond 5G, technology research and development needs to focus on MIMO enhancement, V2X and IoT evolution, integration of 5G with Non-Terrestrial Network, and new FR3 & FR4 spectrum development. To bring all this into focus, the IEEE Microwave Theory and Techniques Society (MTT-S) is organizing a 5G Summit during the 2020 MTT-S International Microwave Symposium (IMS2020) Virtual Event with speakers at the leadership level from different companies and industries to discuss 5G related topics, including foundries, standards, mobile networks, MIMO and millimeter-wave systems, RFIC, and RFFE. As part of the IEEE Comsoc 5G Summit series (details at <http://www.5GSummit.org>), this summit will provide a platform for leaders, innovators, and researchers from both industrial and academic communities to collaborate and exchange ideas regarding 5G and beyond 5G technologies.

## *Speakers:*

1. “Differentiated End to End Silicon Solutions for the New 5G Reality”, **Bami Bastani**, *GLOBALFOUNDRIES*
2. “5G — Evolution or Revolution”, **James Chen**, *MediaTek*
3. “The Myths and Facts of O-RAN Whitebox”, **Chih-Lin I**, *China Mobile*
4. “RF Front-End Evolution from 4G to 5G”, **David Pehlke**, *Skyworks Solutions*
5. “Sub-6GHz and mm-Wave RFICs for 5G Wireless Infrastructure RF Front Ends”, **Naveen Yanduru**, *Renesas Electronics*
6. “A Fabless Perspective on 5G Phased Arrays, from Devices to Network Capacity”, **Curtis Ling**, *MaxLinear*
7. “The 5G Quest: System, Deployment & Application Challenges”, **Shahriar Shahramian**, *Nokia Bell Labs*
8. “FR 1,2,3,4,...PA and FEM Technology Approaches for 5G and Beyond”, **Michael Peeters**, *imec*



## Session RMo1A: High Spectral Purity Phase-Locked Loops

Chair: Fa Foster Dai, Auburn University, USA

Co-Chair: Joseph D. Cali, BAE Systems, USA

### RMo1A-1

#### A 23.6–38.3GHz Low-Noise PLL with Digital Ring Oscillator and Multi-Ratio Injection-Locked Dividers for Millimeter-Wave Sensing

Yan Zhang<sup>1</sup>, Yan Zhao<sup>1</sup>, Rulin Huang<sup>1</sup>, Chia-Jen Liang<sup>2</sup>, Ching-Wen Chiang<sup>2</sup>, Yen-Cheng Kuan<sup>2</sup>, Mau-Chung Frank Chang<sup>1</sup>; <sup>1</sup>University of California, Los Angeles, USA, <sup>2</sup>National Chiao Tung University, Taiwan

**Abstract:** This paper presents a 23.6–38.3GHz cascaded PLL with quadrature phases designed and prototyped in 28nm CMOS. Unlike conventional approaches, no on-chip inductor is used for millimeter-wave frequency generation. Instead, a simple inverter-based ring oscillator, with scaled copies of itself and explicit mixers, forms a unique VCO-and-multi-ratio-injection-locked-frequency-divider subsystem suitable for ultra-wide frequency synthesis. The prototype achieves comparable noise performance to its LC-VCO-based counterparts for similar applications. The phase noise is better than -96dBc/Hz at 1MHz offset across the entire range with power consumption less than 35mW. This PLL is intended for integrated wide-band sensing applications at Ka- and W-bands (with an additional frequency tripler).

### RMo1A-2

#### A 1Mb/s 2.86% EVM GFSK Modulator Based on $\Delta\Sigma$ BB-DPLL Without Background Digital Calibration

Yuguang Liu, Woogeun Rhee, Zhihua Wang; Tsinghua University, China

**Abstract:** This paper presents a two-point modulation architecture based on the  $\Delta\Sigma$  bang-bang digital PLL (BB-DPLL) that does not rely on high-resolution digital-to-time converter (DTC) to avoid long digital calibration time for wireless systems. Multiple techniques are integrated to improve in-band noise performance and overcome DCO nonlinearity. In the proposed two-point modulator, FIR-filtered 1b high-pass modulation overcomes the nonlinearity of a digitally-controlled oscillator (DCO), while low-pass modulation achieving good linearity with a 1b time-to-digital converter (TDC) having high reference frequency. To mitigate in-band noise degradation in the  $\Delta\Sigma$  BB-DPLL, a third-order  $\Delta\Sigma$  modulator with a 1b output, a 4b hybrid DTC using a 3b delay line and a 1b phase-interpolated frequency divider, and a  $\Delta\Sigma$  BB-DPLL with high reference frequency are employed. A prototype 1.8GHz 1Mb/s GFSK modulator implemented in 65nm CMOS achieves the in-band phase noise of -94dBc/Hz and the EVM performance of 2.86%, while consuming 5.3mW from a 1V supply.

### **RMo1A-3**

#### **A 2.0–2.9GHz Digital Ring-Based Injection-Locked Clock Multiplier Using a Self-Alignment Frequency Tracking Loop for Reference Spur Reduction**

Rongjin Xu<sup>1</sup>, Dawei Ye<sup>1</sup>, Liangjian Lyu<sup>1</sup>, C.-J. Richard Shi<sup>2</sup>; <sup>1</sup>Fudan University, China, <sup>2</sup>University of Washington, USA

**Abstract:** This paper presents a 2.0–2.9 GHz digital ring-based injection-locked clock multiplier (ILCM) in a 65 nm CMOS process. A self-alignment frequency tracking loop (SA-FTL) with background delay calibration is proposed to improve the accuracy of injection timing. Since the frequency mismatch of the free-running oscillator and the target frequency is minimized without delay error, the reference spur is reduced to -55.6 dBc, exhibiting 15.9 dB improvement comparing to the case that the SA-FTL is off. The proposed ILCM achieves 545 fs RMS jitter at 2.5 GHz output frequency with a power consumption of 3.1 mW, achieving the FoM of 240.3 dB.

### **RMo1A-4**

#### **A 10-to-12GHz 5mW Charge-Sampling PLL Achieving 50fsec RMS Jitter, -258.9dB FOM and -65dBc Reference Spur**

Jiang Gong<sup>1</sup>, Fabio Sebastiano<sup>1</sup>, Edoardo Charbon<sup>2</sup>, Masoud Babaie<sup>1</sup>; <sup>1</sup>Technische Universiteit Delft, The Netherlands, <sup>2</sup>EPFL, Switzerland

**Abstract:** This paper presents a charge-sampling PLL (CSPLL), that demonstrates the best reported jitter-power FOM of -258.9 dB thanks to its high phase-detection gain and to the removal of the power-hungry buffer driving the phase detector. It also achieves -65 dBc of reference spur by both minimizing the modulated capacitance seen by the VCO tank and reducing the duty cycle of the sampling clock. Without requiring any RF dividers, a 50  $\mu$ W frequency tracking loop is also introduced to robustly lock the CSPLL to a 100MHz reference. Fabricated in 40-nm CMOS, the 0.13mm<sup>2</sup> CSPLL achieves an RMS jitter of 50 fsec at 11.4GHz while consuming 5mW.

## Session RMo1B: Microwave and Millimeter-Wave Radar Systems

Chair: Ed Balboni, Analog Devices, USA

Co-Chair: Duane Howard, Jet Propulsion Laboratory, USA

### RMo1B-1

#### Low Power Low Phase Noise 60GHz Multichannel Transceiver in 28nm CMOS for Radar Applications

Johannes Rimmelspacher<sup>1</sup>, Radu Ciocoveanu<sup>1</sup>, Giovanni Steffan<sup>2</sup>, Matteo Bassi<sup>2</sup>, V. Issakov<sup>1</sup>;

<sup>1</sup>Infineon Technologies, Germany, <sup>2</sup>Infineon Technologies, Austria

**Abstract:** This paper presents a highly integrated 60 GHz transceiver for FMCW radar applications realized in a 28 nm bulk CMOS technology. The chip provides two transmit (TX) and three receive (RX) channels. The 60 GHz local oscillator (LO) distribution is fed with the frequency-multiplied signal of the integrated low phase noise 15 GHz voltage-controlled oscillator (VCO). Realized in 28 nm technology node, the proposed chip is able to generate chirp signals over a continuous 57–64 GHz frequency-tuning-range. The phase noise is  $< -93$  dBc/Hz @ 1 MHz offset. The measured peak phase noise performance is  $-99$  dBc/Hz @ 1 MHz offset for a 55.5 GHz carrier frequency. The single TX/RX DC power consumptions are 63 mW and 39 mW, respectively. The total DC power dissipation is 478 mW.

### RMo1B-2

#### A 77GHz 8RX3TX Transceiver for 250m Long Range Automotive Radar in 40nm CMOS Technology

Tatsunori Usugi, Tomotoshi Murakami, Yoshiyuki Utagawa, Shuya Kishimoto, Masato Kohtani, Ikuma Ando, Kazuhiro Matsunaga, Chihiro Arai, Tomoyuki Arai, Shinji Yamaura; DENSO, Japan

**Abstract:** This paper presents a fully integrated 77 GHz transceiver for long range automotive radar with a  $2 \times 8$  time-division-multiplexing multi-input multi-output (TDM-MIMO) technique in 40 nm CMOS technology. The MMIC integrates an 8-channel receiver (RX), a 3-channel transmitter (TX), a phase locked loop (PLL), a TX power detector and a power calibration loop, an SRAM, an eFuse, a temperature compensation calibration loop with look up table (LUT) and a temperature sensor, a serial peripheral interface (SPI), and a MIMO control logic. The RX shows noise figure (NF) of 8.7 dB and input-referred 1 dB compression point (IP1dB) of  $-7.4$  dBm. The RX with the worst condition shows NF of 14 dB and IP1dB of  $-10$  dBm. The TX shows output power of 14.1 dBm and phase noise of  $-116$  dBc/Hz at 12.5 MHz offset frequency. The radar module demonstrates the detection range of 250 m.

## **RMo1B-3**

### **High Resolution CMOS IR-UWB Radar for Non-Contact Human Vital Signs Detection**

Sang Gyun Kim, In Chang Ko, Seung Hwan Jung; GRIT Custom-IC, Korea

**Abstract:** This paper presents an impulse radio ultra-wideband radar transceiver chip for monitoring human vital signs, featuring a spectrum adjustable transmitter and equivalent time sampling based receiver. The radar receiver samples the echo signal at 20.48 GS/s, which corresponds to a 7.4 mm range resolution using high-speed track and hold sampler. The received pulses are added up to increase the SNR of the receiver. With the proposed pseudo 16-bit DAC, an embedded DC-offset cancellation circuit can improve the dynamic range of the receiver according to the gain of integrator. Respiration and heartbeat of humans were detected by the proposed UWB radar transceiver, while consuming 55.2 mW from 1.2 V power supply. The radar transceiver chip was implemented in a 130 nm CMOS technology occupying chip area of 5.04 mm<sup>2</sup>.

## **RMo1B-4**

### **A 62mW 60GHz FMCW Radar in 28nm CMOS**

Sehoon Park, Anirudh Kankuppe, Pratap Renukaswamy, Davide Guermandi, Akshay Visweswaran, Juan C. Garcia, Siddhartha Sinha, Piet Wambacq, Jan Craninckx; imec, Belgium

**Abstract:** A 56–66GHz FMCW radar transceiver achieves 17% fractional RF bandwidth with a dynamic tuning technique on matching networks that tracks the frequency chirp. A novel frequency tripler architecture is proposed that uses harmonic combination to enhance efficiency and output power. The transmitter (TX) output power of 8.1dBm and the receiver (RX) NF of 12.8dB support a detection range up to 15m with a 20MHz IF bandwidth. Continuous power consumption is only 62mW, which can be heavily duty-cycled thanks to a 1μs start-up time.

## **RMo1B-5**

### **77GHz CMOS Built-In Self-Test with 72dB C/N and Less Than 1ppm Frequency Tolerance for a Multi-Channel Radar Application**

Masato Kohtani, Tomotoshi Murakami, Yoshiyuki Utagawa, Tomoyuki Arai, Shinji Yamaura; DENSO, Japan

**Abstract:** A built-in self-test (BIST) system with 72 dB C/N and less than 1 ppm frequency tolerance of down-converted BIST tone for a multi-channel radar application is presented. The BIST consists of a frequency doubler, an up-conversion mixer, a variable gain amplifier, a phase shifter, 8-way splitter and an RF GSG PAD coupler for BIST signal distribution. The proposed up-conversion mixer can operate from 76 to 77 GHz, mixing with arbitrary offset frequencies from 600 kHz to 42.7 MHz generated by a fully-synchronized PLL. The proposed mixer can cope with a through mode for testability and flexibility improvements as well. Measured relative phase among all of 8 channels were less than 2 degrees from -25°C to 150°C through on-chip 12-bit ADCs. The proposed BIST was fabricated in a 40 nm CMOS process and assembled with a wafer level chip sized package (WLCSP).

## Session RMo1C: Circulators and Full-Duplex Transceivers

Chair: François Rivet, University of Bordeaux, France

Co-Chair: Magnus Wiklund, Qualcomm, USA

### RMo1C-1

#### RFIC Inductorless, Widely-Tunable N-Path Shekel Circulators Based on Harmonic Engineering

Negar Reiskarimian, Mohammad Khorshidian, Harish Krishnaswamy; Columbia University, USA

**Abstract:** Recently demonstrated non-magnetic circulators rely on the interference between an LPTV non-reciprocal gyrator and reciprocal transmission-line circuits, which limits their form factor and compromises the tunability of N-path circuits. In this paper, a new class of non-magnetic inductorless widely-tunable non-reciprocal circulators based on harmonic engineering is introduced. LPTV circuits rely on modulating the input signals with a square-wave clock waveform that can contain multiple harmonics. The harmonic engineering concept controls the response to various harmonics of the clock signal, the superposition of which results in the desired functionality. Two prototype N-path Shekel circulators have been implemented in 65nm CMOS. The first prototype, operating in the large-RC-regime can be reconfigured for operation across 0.1–1.1 GHz, with losses ranging from 2.4–3.4 dB. It has a form factor of  $\lambda^2/2,000,000$  at 500 MHz, with a power consumption of 9.6 mW. The second prototype operates in the low-RC-regime with a tuning range of 0.28–1.15 GHz and a loss of 2.3–3.3 dB, and achieves more than 20 dB isolation across a 233 MHz BW (38%) within a  $\lambda^2/1,500,000$  form factor at 600 MHz.

### RMo1C-2

#### A Full-Duplex Receiver Leveraging Multiphase Switched-Capacitor-Delay Based Multi-Domain FIR Filter Cancelers

Aravind Nagulu, Aditya Gaonkar, Sohail Ahasan, Tingjun Chen, Gil Zussman, Harish Krishnaswamy; Columbia University, USA

**Abstract:** Wideband self-interference cancellation (SIC) in full-duplex (FD) radios requires the achievement of large delays to accurately emulate the SI channel. However, compact, power-efficient, low-loss/noise nanosecond-scale delays are extremely challenging to achieve on silicon. Passive LC-based approaches are area intensive, whereas active approaches are power hungry and noisy. In this work, we presented a technique which leverages switched-capacitor circuits with multiphase clocking to obtain large on-chip delays with low area and power consumption. This technique is demonstrated in a FD receiver with time-interleaved switched-capacitor-based delay cells in RF and BB domains. The FD receiver is implemented in a standard 65nm CMOS process and operates from 100MHz–1GHz with gain tunability of 15–38dB, noise figure of 5.4dB, and power consumption of 31mW. The canceler delay cells have delays ranging from 0.2ns–1.1ns in the RF domain, and 10ns–75ns in the BB domain, while consuming 25.5mW and 6.5mW respectively. These large tunable delays perform FIR-filtering based cancellation, enabling 30–35dB integrated SI cancellation over 20MHz on top of an off-the-shelf ferrite circulator when terminated by a dipole antenna (isolation of 22dB), and can handle TX power of up to +9dBm. Under SIC, the RF and BB cancellers degrade the RX noise figure by 1.1dB and 0.8dB respectively.

## **RMo1C-3**

### **A 3.4–4.6GHz In-Band Full-Duplex Front-End in CMOS Using a Bi-Directional Frequency Converter**

Xiang Yi<sup>1</sup>, Jinchun Wang<sup>1</sup>, Cheng Wang<sup>1</sup>, Kenneth E. Kolodziej<sup>2</sup>, Ruonan Han<sup>1</sup>; <sup>1</sup>MIT, USA, <sup>2</sup>MIT Lincoln Laboratory, USA

**Abstract:** Magnetic-free circulators using phase nonreciprocity of spatial-temporal modulated structures have enabled in-band full-duplex systems on CMOS chips. In this paper, we present an alternative and simple integrated circuit scheme based on a bi-directional frequency converter, which not only realizes nonreciprocal signal flow for in-band full-duplex systems but also improves the isolation performance by completely eliminating any chip-level TX-to-RX coupling. These functions are implemented through a direction/frequency-independent single-sideband down-conversion process, which well splits the on-chip TX and RX frequencies. That principle also leads to extension of isolation bandwidth and integrated receiver down-mixing function. Implemented in a 65-nm bulk CMOS technology, a circuit prototype operates from 3.4 to 4.6 GHz (30% fractional bandwidth) and achieves >25.5-dB measured TX-RX isolation. The measured TX-ANT and ANT-RX insertion loss are 3.0 and 3.2 dB, respectively, and the TX-ANT and ANT-RX IIP<sub>3</sub> are 29.5 and 27.6 dBm, respectively. This full-duplex front-end component occupies 0.27mm<sup>2</sup> area and has 48 mW of power consumption.

## **RMo1C-4**

### **A Self-Interference-Tolerant, Multipath Rake Receiver with More Than 40-dB Rejection and 9-dB SNR Multipath Gain in a Fading Channel**

Ahmed Hamza, Cameron Hill, Hussam AlShammary, James Buckwalter; University of California, Santa Barbara, USA

**Abstract:** This paper presents a 3-finger rake receiver (RX) that exploits multipath characteristics in PN-modulated received signals to improve the signal-to-noise ratio (SNR) in full-duplex (FD) links. Orthogonality between PN codes allows up to 41.2 dB of TX self-interference (TX-SI) rejection and autocorrelation between delayed versions of received PN code improves the SNR by 9 dB. The receiver is implemented in 45-nm SOI CMOS and is tunable from 0.4 to 1.4 GHz with 30.5 dB of gain and an in-band/out-of-band baseband IIP<sub>3</sub> of -6.5/14.2 dBm while consuming 45.8 mW per finger.

## RMo1C-5

### Ultra Compact, Ultra Wideband, DC-1GHz CMOS Circulator Based on Quasi-Electrostatic Wave Propagation in Commutated Switched Capacitor Networks

Aravind Nagulu<sup>1</sup>, Mykhailo Tymchenko<sup>2</sup>, Andrea Alù<sup>2</sup>, Harish Krishnaswamy<sup>1</sup>; <sup>1</sup>Columbia University, USA, <sup>2</sup>University of Texas at Austin, USA

**Abstract:** Recent research has revealed the possibility to achieve non-magnetic non-reciprocity using time-variance. However, prior CMOS-based circulators rely on the interference between non-reciprocal switched-capacitor/transmission-line gyrators and reciprocal transmission-line rings, which increases form factor and restricts frequency tunability and bandwidth. On the other hand, recent works on quasi-electrostatic wave propagation in switched-capacitor media have demonstrated a new regime in multipath switched-capacitor network operation that enables an ultra-broadband, ultra-compact reciprocal/non-reciprocal true-time-delay element. In this work, we apply synthetic rotation across this quasi-electrostatic medium to realize an ultra-broadband N-port circulator with ultra-compact form-factor. This new architecture is showcased in a wideband 3-port circulator implemented in a standard 65nm CMOS process. This circulator exhibits symmetric performance across all 3 ports and DC-1GHz operation for a modulation frequency of 500MHz. The measured transmission losses range between 3.1–4.3dB, matching is <-15dB, isolation is >18dB and NF is consistent with the insertion loss. This device occupies an area of 0.19mm<sup>2</sup> ( $\lambda_{center}^2/1.9 \times 10^6$ ), representing about 100–1000× higher miniaturization compared to the prior art.

## **Session RMo1D: Switches and Delay Elements for Receiver Front-Ends**

**Chair: Danilo Manstretta, Università di Pavia, Italy**

**Co-Chair: Domine M.W. Leenaerts, NXP Semiconductors, The Netherlands**

### **RMo1D-1**

#### **A Wideband True-Time-Delay Phase Shifter with 100% Fractional Bandwidth Using 28nm CMOS**

Minjae Jung, Hong-Jib Yoon, Byung-Wook Min; Yonsei University, Korea

**Abstract:** A fully integrated passive true-time-delay (TTD) phase shifter is presented for a wideband phased array antenna using 28-nm CMOS technology. By using a delay-compensation technique, a linear phase characteristic is achieved within a wide frequency range over 8–24 GHz. A combined bridged-tee network (BTN) delay cell is proposed to accomplish the delay compensation with the most significant bit (MSB) at 29.6 ps and the least significant bit (LSB) at 7.4 ps, which are 45° and 180° at 16 GHz, respectively. The measured insertion loss is in the range of 7.8–12 dB with an RMS gain error less than 1.4 dB from 8 GHz to 24 GHz. In addition, the measured RMS TTD phase and delay errors are less than 1.6 ps and 1.5°, respectively, within 8–24 GHz. The chip size of the proposed TTD phase shifter is 0.48 mm<sup>2</sup>.

### **RMo1D-2**

#### **A DC to 43-GHz SPST Switch with Minimum 50-dB Isolation and +19.6-dBm Large-Signal Power Handling in 45-nm SOI-CMOS**

Ayman Eltaliawy<sup>1</sup>, John R. Long<sup>1</sup>, Ned Cahoon<sup>2</sup>; <sup>1</sup>University of Waterloo, Canada,

<sup>2</sup>GLOBALFOUNDRIES, USA

**Abstract:** A fully-differential, single-pole single-throw (SPST) switch capable of high isolation in broadband CMOS transceivers is described. The SPST switch realizes > 50-dB isolation across DC to 43GHz while maintaining an insertion loss (IL) < 3dB. RF input power for -1dB compression (IP<sub>1dB</sub>) of the IL is +19.6dBm and the input third-order intercept point is +30.4dBm (both for differential inputs at 20GHz). The prototype is fabricated in 45-nm RF-SOI CMOS technology and has an active area of 0.0058mm<sup>2</sup>.

### **RMo1D-3**

#### **DC-40GHz SPDTs in 22nm FD-SOI and Back-Gate Impact Study**

Martin Rack<sup>1</sup>, Lucas Nyssens<sup>1</sup>, Sidina Wane<sup>2</sup>, Damienne Bajon<sup>2</sup>, Jean-Pierre Raskin<sup>1</sup>; <sup>1</sup>Université catholique de Louvain, Belgium, <sup>2</sup>eV-Technologies, France

**Abstract:** In this paper, ultra-wideband SPDTs fabricated in the 22 nm FD-SOI process from GLOBALFOUNDRIES are presented. Three SPDT modules were implemented, each using a different type of millimeter-wave NFET, namely a conventional-well regular-V<sub>t</sub> (RVT) device, a flipped-well super-low-V<sub>t</sub> (SLVT) device and a specially treated device without back-gate well contact for decreased substrate parasitics (BFMOAT device). It is shown that using the back-gate achieves lower losses, higher isolation and better linearity for the RVT and SLVT based switches, while the reduced parasitic BFMOAT switch shows better performance at the high-end of the mm-wave spectrum.



## RMo1D-4

### A 100W, UHF to S-Band RF Switch in the Super-Lattice Castellated Field Effect Transistor (SLCFET) 3S Process

John J. Hug, Justin Parke, Vanu Kapoor; Northrop Grumman, USA

**Abstract:** High power RF switches were designed in the Super-Lattice Castellated Field Effect Transistor (SLCFET) 3S process. The design goals were low ON-state insertion loss (0.25 dB for UHF-band, 1 dB for S-band), high OFF-state isolation from the RF input (65 dB for UHF-band, 40 dB for S-band), high operating power (100 W pulsed RF through S-band), and a high switch failure power (200 W pulsed RF, 100 W CW through S-band). We used an RF stacking approach in the design in order to allow for voltage swings that exceed the drain-gate breakdown voltage of the process. Measurements performed on switches that were fabricated indicate that all of the goals were met, and demonstrate that a reliable SLCFET process would offer advantages over many existing GaN HEMT processes in RF switching applications.

## Session RMo2A: Reconfigurable RF Front-End Blocks

Chair: Magnus Wiklund, Qualcomm, USA

Co-Chair: François Rivet, University of Bordeaux, France

### RMo2A-1

#### A Context-Aware Reconfigurable Transmitter with 2.24pJ/Bit, 802.15.6 NB-HBC and 4.93pJ/Bit, 400.9MHz MedRadio Modes with 33.6% Transmit Efficiency

Baibhab Chatterjee, Abhishek Srivastava, Dong-Hyun Seo, David Yang, Shreyas Sen; Purdue University, USA

**Abstract:** The emerging Narrowband Human Body Communication (NB-HBC) technology, as well as MedRadio communication in the 400 MHz band promise better energy efficiencies than traditional Bluetooth Low Energy for wireless body area networks (WBAN) due to lower channel losses and lower frequencies, respectively. Although HBC offers less than 10pJ/bit energy efficiencies, it strictly demands both the transmitter and receiver to be on the body. Traditional MedRadio enables data transfer even when either devices are not on the body, but consumes orders of magnitude more energy than HBC, primarily due to large power consumption in LO generation. In this work, for the first time, we demonstrate a Context-aware, Reconfigurable transmitter (COR-Tx) consisting sub-3pJ/bit HBC and sub-5pJ/bit MedRadio modes (both state-of-the-art), while supporting opportunistic switching between the two modes depending on the location of the receiver (on-body/off-body) for achieving optimum system-level energy with seamless communication. For 10 Mbps data rate, the HBC mode achieves an energy efficiency of 2.24pJ/bit, while the MedRadio mode achieves 4.93pJ/bit using a shared LO generation scheme that utilizes direct-modulated edge combination (EC) for minimizing energy consumption. The energy-efficiency improvement over the state-of-the-art is  $\sim 2.1\times$  for HBC and  $\sim 90\times$  for MedRadio.

### RMo2A-2

#### A Reconfigurable SOI CMOS Doherty Power Amplifier Module for Broadband LTE High-Power User Equipment Applications

A. Serhan<sup>1</sup>, D. Parat<sup>1</sup>, P. Reynier<sup>1</sup>, M. Pezzin<sup>1</sup>, R. Mouro<sup>1</sup>, F. Chaix<sup>1</sup>, R. Berro<sup>1</sup>, P. Indirayanti<sup>2</sup>, C. De Ranter<sup>2</sup>, K. Han<sup>2</sup>, M. Borremans<sup>2</sup>, E. Mercier<sup>1</sup>, A. Giry<sup>1</sup>; <sup>1</sup>CEA-Leti, France, <sup>2</sup>Huawei Technologies, Belgium

**Abstract:** A reconfigurable broadband Doherty PA module for LTE HPUE (High Power User Equipment) applications is presented, which is the first to be based on an SOI-CMOS PA without predistortion and supply modulation. The PA die ( $1.3\times 1.7\text{mm}^2$ ) is fabricated in a 130nm SOI-CMOS process and assembled, using flip-chip, on a  $3.2\times 3.7\text{mm}^2$  laminate package. From 1.9GHz to 2.7GHz, the PA provides 28dBm of output power ( $P_{\text{out}}$ ) under 3.4V supply voltage (Vdd), with a PAE higher than 35% and an E-UTRA ACLR lower than -35dBc when using a 10MHz-50RB QPSK LTE uplink signal, without predistortion. At 2.3GHz, the proposed PA achieves 43.5% of PAE and -39.6dBc of ACLR at 28dBm of  $P_{\text{out}}$ . When operating at Vdd=5V (HPUE mode), the PA reaches a saturated power of 4W with a maximum PAE of 57% and delivers a  $P_{\text{out}}$  of 31dBm with 42.6% of PAE and -35.7dBc of ACLR using a 20MHz-100RB QPSK LTE signal.

## RMo2A-3

### A 4-Element 7.5–9GHz Phased Array Receiver with 8 Simultaneously Reconfigurable Beams in 65nm CMOS Technology

Nayu Li<sup>1</sup>, Min Li<sup>1</sup>, Shaogang Wang<sup>1</sup>, Zijiang Zhang<sup>1</sup>, Huiyan Gao<sup>1</sup>, Yen-Cheng Kuan<sup>2</sup>, Xiaopeng Yu<sup>1</sup>, Zhiwei Xu<sup>1</sup>, <sup>1</sup>Zhejiang University, China, <sup>2</sup>National Chiao Tung University, Taiwan

**Abstract:** This paper presents a 4-element 7.5–9 GHz phased array receiver with 1–8 concurrent beams in a 65-nm CMOS technology. All the elements are fully-connected to each output beam using 32 phase shifters and 8 active combiners. The current-starving gm-based phase shifter with 6-bit phase resolution achieves  $<2^\circ$  RMS phase error and  $<0.3$  dB RMS gain error. The receiver demonstrates 20 dB gain, 3.6 dB noise figure (NF) and -19 dBm input 1-dB gain compression point (IP1dB) in 7.5–9 GHz band for each element. The chip occupies  $5.42 \times 3.62$  mm<sup>2</sup> area excluding pads and consumes 860 mW, equivalent to 27 mW per element per beam. To our knowledge, the receiver achieves the maximum number of simultaneously reconfigurable beams with the lowest power consumption per element per beam in RF phase shifting and combining receiver chips.

## RMo2A-4

### A 29-mW 26.88-GHz Non-Uniform Sub-Sampling Receiver Front-End Enabling Spectral Alias Spreading

Ce Yang, Mostafa Ayesh, Aoyang Zhang, Tzu-Fan Wu, Mike Shuo-Wei Chen; University of Southern California, USA

**Abstract:** This paper introduces a non-uniform sub-sampling (NUSS) technique to relax the analog anti-aliasing filter design for mm-Wave receiver applications. By applying pre-designed periodic perturbation to the sub-sampling time instants, the unwanted spectral aliases, i.e., the integer multiples of the sampling frequency other than the carrier frequency, are spread out; hence undesired blocker aliasing at specific bands is significantly reduced. The NUSS technique effectively creates frequency notches during the sampling process that can be reconfigured simply by changing the NU perturbation sequence. A proof-of-concept NUSS receiver front-end is implemented in 28nm CMOS with 26.88GHz carrier frequency. Through spectral alias spreading, NUSS technique achieves 33dB alias rejection with 29mW power dissipation, which effectively creates notch filtering during sampling. The measured EVM is -25dB using a 200MHz 64QAM modulated signal in the presence of a 0dBc blocker.

## Session RMo2B: Millimeter-Wave Circuits in D and E Band for High Data-Rate Wireless Links

Chair: Pierre Busson, STMicroelectronics, USA

Co-Chair: Kenichi Okada, Tokyo Institute of Technology, Japan

### RMo2B-1

#### D-Band Phased-Array TX and RX Front Ends Utilizing Radio-on-Glass Technology

Mohamed Elkhoully, Michael J. Holyoak, David Hendry, Mike Zierdt, Amit Singh, Mustafa Sayginer, Shahriar Shahramian, Yves Baeyens; Nokia Bell Labs, USA

**Abstract:** This paper reports wide-band TX and RX phased-array front ends for D-band (130–170 GHz), implemented in 0.13  $\mu\text{m}$  SiGe BiCMOS process with  $f_{\text{r}}/f_{\text{max}}$  of 300/500 GHz. The TX front end consists of a wide-band vector-modulator phase shifter followed by a PA. The TX yields an output  $P_{\text{dB}}$  of 10 dBm and a total gain of 16 dB. The RX consists of an LNA, wide-band vector-modulator and a buffer stage. It exhibits a gain of 22 dB and a noise figure of 10 dB. A glass interposer is designed with 8 flip-chip TX/RX front ends and an integrated  $8 \times 16$  slot antenna array, forming a radio-on-glass (RoG) D-band phased-array module.

### RMo2B-2

#### A 71–76/81–86GHz, E-Band, 16-Element Phased-Array Transceiver Module with Image Selection Architecture for Low EVM Variation

Najme Ebrahimi<sup>1</sup>, Kamal Sarabandi<sup>1</sup>, James Buckwalter<sup>2</sup>, <sup>1</sup>University of Michigan, USA, <sup>2</sup>University of California, Santa Barbara, USA

**Abstract:** A 4-element, compact bidirectional phased-array transceiver die covers the full E-band (71–76 & 81–86GHz) and is tiled on PCB to demonstrate a 16-element antenna array. A Weaver image-selection architecture reduces the  $\text{LO}_{\text{RF}}$  tuning range to 3 GHz (4% FBW) while covering the 10 GHz band (20% FBW). The bidirectional architecture is proposed in a scalable array with a shared image-selection IF mixer. The  $2 \times 2$  transceiver die is implemented in a 90-nm SiGe BiCMOS process and assembled on PCB with a compact differential aperture-coupled feed network for LO and IF distribution with low amplitude and phase mismatch between multiple chips input/output. The proposed 16-element array steers over a  $\pm 30^\circ$  range and demonstrates 30-dBm EIRP and 32-dB RX conversion gain with 1.5 GHz modulation bandwidth for 64 QAM (9 Gb/s) and 2 GHz for 16 QAM with  $\pm 2$  dB EVM variation over the entire E-band under same calibration states. The power consumption is 250 mW for TX mode and 160 mW for RX mode at each element.

### RMo2B-3

#### A D-Band Radio-on-Glass Module for Spectrally-Efficient and Low-Cost Wireless Backhaul

Amit Singh, Mustafa Sayginer, Michael J. Holyoak, Joseph Weiner, John Kimionis, Mohamed Elkhoully, Yves Baeyens, Shahriar Shahramian; Nokia Bell Labs, USA

**Abstract:** D-Band Radio-on-Glass (RoG) modules combining two highly integrated SiGe BiCMOS transceivers (TRX) with a record low-loss glass interposer technology are presented. The ICs operate

at 115–155 GHz (Low-Band) and 135–170 GHz (High-Band). In this frequency range, a transmitter  $P_{\text{sat}}$  up to 13 dBm and an average receiver NF of 8.5 dB is achieved. The integrated module supports TX constellations up to 512-QAM (2.2% EVM at 2 dBm output, 145 GHz) and data-rates up to 42 Gb/s (128-QAM). Measurements mimicking a 250-meter wireless-link demonstrate a maximum data-rate of 36 Gb/s using 64-QAM. The RoG modules represent the first low-cost and highly integrated solution for spectrally efficient backhaul systems in D-Band.

## RMo2B-4

### A 134–149GHz IF Beamforming Phased-Array Receiver Channel with 6.4–7.5dB NF Using CMOS 45nm RFSOI

Siwei Li, Gabriel M. Rebeiz; University of California, San Diego, USA

**Abstract:** This paper presents a 140 GHz IF beamforming phased-array receive channel with low noise performance in 45nm RFSOI process. The proposed high-IF (9–14 GHz) beamforming architecture realizes the lower loss and power consumption compared with RF and LO beamforming at 140 GHz, while rejecting the noise contribution from the image without external filtering. In this design, a fully-differential low-noise amplifier (LNA) is followed by an active double-balanced mixer and an IF beamformer, consisting of a variable gain amplifier (VGA) and a vector modulator (VM). A  $\times 6$  on-chip multiplier is used to generate the 126–138 GHz local oscillator. The receiver consumes 133 mW with a measured peak gain and average NF of 26.5 dB and 7 dB, respectively (NF 6.4–7.5 dB at 134–149 GHz). The measured input P1dB is  $-30 \pm 1$  dBm at 139–142 GHz. To our knowledge, this work presents the first phased-array beamformer receive channel with the lowest NF in the 140 GHz band.

## RMo2B-5

### A Fully Integrated 32Gbps 2×2 LoS MIMO Wireless Link with UWB Analog Processing for Point-to-Point Backhaul Applications

Mahmoud Sawaby<sup>1</sup>, Baptiste Grave<sup>1</sup>, Clement Jany<sup>1</sup>, Cheng Chen<sup>1</sup>, Siavash Kananian<sup>1</sup>, Pierino Calascibetta<sup>2</sup>, Frederic Giancesello<sup>2</sup>, Amin Arbabian<sup>1</sup>; <sup>1</sup>Stanford University, USA, <sup>2</sup>STMicroelectronics, France

**Abstract:** In this paper, we demonstrate a proof-of-concept 130 GHz wireless 2×2 line-of-sight (LoS) multi-input multi-output (MIMO) transceiver using fully packaged transmit and receive arrays and scalable analog baseband processing. The link utilizes the Rayleigh criterion to transmit independent wireless streams over a LoS channel. The transmitter (TX) and receiver (RX) chips are fully packaged with integrated mm-wave antennas. The two-element QPSK TX array consumes 432 mW, while the entire four-channel QPSK MIMO RX consumes 630 mW and supports four concurrent 130 GHz mm-wave channels with a simulated passband bandwidth of 20 GHz. Wireless measurements demonstrate 32 Gbps QPSK transmission over 40 cm, allowing for a link efficiency of 83 pJ/bit/m and an energy efficiency of 33 pJ/bit. Scaling the system from the two channels measured here to the four channels supported by the RX chip will double the data rate as well as the range reported.

## Session RMo2C: Digital Power Amplifiers

Chair: Jeffrey Walling, Qualcomm, USA

Co-Chair: Justin (ChiaHsin) Wu, Amlogic, Taiwan

### RMo2C-1

#### A 1.5–3GHz Quadrature Balanced Switched-Capacitor CMOS Transmitter for Full Duplex and Half Duplex Wireless Systems

Nimrod Ginzberg<sup>1</sup>, Dror Regev<sup>2</sup>, Emanuel Cohen<sup>1</sup>; <sup>1</sup>Technion, Israel, <sup>2</sup>Toga Networks, Israel

**Abstract:** This work proposes a reconfigurable multi-mode digital transmitter based on quadrature balanced switched-capacitor power amplifiers (QB-SCPA), supporting both full duplex (FD) and half duplex (HD) operation. The QB-SCPA architecture provides built-in passive transmit-receive isolation along with an embedded and wideband self-interference cancellation (SIC) signal injection mechanism. In addition, it allows for phase noise suppression at the RX through clock sharing and exhibits excellent TX and RX linearity. In FD mode, we demonstrate >72 dB of total TX-RX isolation over a BW larger than 1 GHz at 21 dBm peak TX power with 17.4% system PAE. In HD<sub>TX</sub> mode, the system achieves 23 dBm peak TX power with 26.5% PAE.

### RMo2C-2

#### A 65nm CMOS Switched-Capacitor Carrier Aggregation Transmitter

Nimrod Ginzberg, Emanuel Cohen; Technion, Israel

**Abstract:** This paper presents a new carrier aggregation transmitter architecture with high linearity performance based on series post-PA combining of two switched-capacitor power amplifiers (SCPA), each operating at a different carrier frequency. Linear operation is achieved through the low and digital code word independent output impedance of the SCPA, resulting in low nonlinear interaction between the SCPAs comprising the transmitter. The transmitter operates around the center frequency of 2.4 GHz with a 3 dB bandwidth of 600 MHz and achieves 18.5% peak PAE at a maximum output power of 19 dBm. Carrier to third-order intermodulation distortion product is >40 dBc at 9 dB power backoff within a carrier spacing range larger than 250 MHz. The chip was fabricated in TSMC's 65 nm CMOS, and it occupies an area of 1.6 mm<sup>2</sup>.

## RMo2C-3

### A Differential Digital 4-Way Doherty Power Amplifier with 48% Peak Drain Efficiency for Low Power Applications

Jay Sheth, Steven M. Bowers; University of Virginia, USA

**Abstract:** This paper presents a differential digital 4-way Doherty power amplifier (PA) for low-power applications that achieves high efficiency in deep power back-off (PBO) without supply switching. The PA uses compact input and output matching networks through consolidation of various elements. A proof-of-concept PA was implemented in a 65 nm general purpose CMOS process, and it achieves a peak output stage drain efficiency (DE) of 48% at 4.75 GHz with 7.3 dBm output power ( $P_{out}$ ). Also, it achieves peak PBO enhancements at 5.25 GHz with a DE of 42% at 0 dB PBO and 20% at 12.8 dB PBO. This corresponds to 2.2 $\times$  improvement compared to normalized class B PA. The PA achieves an error vector magnitude (EVM) of -20 dB for a 1 Msym/s 16 QAM baseband signal with an average  $P_{out}$  of 2.9 dBm and DE of 34% at 5.25 GHz.

## RMo2C-4

### 1.2–3.6GHz 32.67dBm 4096-QAM Digital PA Using Reconfigurable Power Combining Transformer for Wireless Communication

Bingzheng Yang, Huizhen Jenny Qian, Tianyi Wang, Xun Luo; UESTC, China

**Abstract:** This paper presents a 1.2–3.6 GHz 32.67 dBm 4096-QAM CMOS digital power amplifier (DPA) with peak power added efficiency (PAE) of 35.5%. The reconfigurable power combining transformer with controllable impedance is introduced to achieve enhanced bandwidth. Meanwhile, the L-C circuit is utilized to suppress the 3<sup>rd</sup>-harmonic and improve output power of fundamental signal. Besides, the 12-bit power digital-to-analog (power-DAC) with low LO leakage and large dynamic range is introduced to support high order modulation signals. The proposed wideband watt-level DPA is implemented in conventional 40-nm CMOS technology. It supports 50 MHz 256-QAM signal with 22.76 dBm average output power, 2.67% EVM, -30.67 dBc ACLR, and 1 MHz 4096-QAM signal with 24.08 dBm average output power, 0.67% EVM, -50.15 dBc ACLR, which is promising candidate for wireless communication.

## RMo2C-5

### A Quadrature Digital Power Amplifier with Hybrid Doherty and Impedance Boosting for Efficiency Enhancement in Complex Domain

Huizhen Jenny Qian<sup>1</sup>, Bingzheng Yang<sup>1</sup>, Jie Zhou<sup>1</sup>, Hongtao Xu<sup>2</sup>, Xun Luo<sup>1</sup>; <sup>1</sup>UESTC, China, <sup>2</sup>Fudan University, China

**Abstract:** In this paper, a quadrature digital PA with hybrid Doherty and impedance boosting (HDIB) is proposed using reconfigurable transformer for PBO efficiency enhancement in complex domain. With the HDIB tracking the optimum load-impedance for different PBOs in wideband, efficiency peaking at 3/6/9/12/15dB PBO is provided from 2.3–3.4GHz without any supply switching or PA short-switches. The fabricated 40-nm CMOS digital PA achieves 24.2dBm peak  $P_{out}$  with 38.5% drain efficiency (DE), and -32.3dB EVM for 10MHz 256QAM signals with average DE of 24.6%.

## Session RMo2D: Novel RF Devices and Modeling Approaches

Chair: Edward Preisler, Tower Semiconductor, USA

Co-Chair: Hsieh-Hung Hsieh, TSMC, Taiwan

### RMo2D-1

#### W-Band Noise Characterization with Back-Gate Effects for Advanced 22nm FDSOI mm-Wave MOSFETs

Q.H. Le<sup>1</sup>, D.K. Huynh<sup>1</sup>, D. Wang<sup>1</sup>, Z. Zhao<sup>2</sup>, S. Lehmann<sup>2</sup>, T. Kämpfe<sup>1</sup>, M. Rudolph<sup>3</sup>; <sup>1</sup>Fraunhofer IPMS, Germany, <sup>2</sup>GLOBALFOUNDRIES, Germany, <sup>3</sup>Brandenburgische Technische Universität, Germany

**Abstract:** This paper presents the W-band noise performance of the 22nm FDSOI CMOS technology. In detail, the mm-wave thin-oxide MOSFETs is characterized comprehensively in term of device geometries using the tuner-based noise measurement approach. To aid the noise analysis and extraction, the following study adopts an accurate small-signal equivalent circuit model validated well with bias-dependence up to 110 GHz. The effects of back-gate bias to the overall noise performance are also addressed in this work. The test devices exhibit low noise figure in the full W-band 75–110 GHz. Besides,  $NF_{min}$  of 2.8 dB and 3.6 dB is recorded at 94 GHz respectively for the n- and p-FETs with 18nm gate-length ( $N_f = 32$ ,  $W_f = 1.0 \mu m$ ). The result of this study indicates the comparable performance of the 22nm FDSOI technology to other candidates for W-band applications.

### RMo2D-2

#### Characterization of Partially Overlapped Inductors for Compact Layout Design in 130nm RFCMOS and 22nm FinFET Processes

Xuanyi Dong, Andreas Weisshaar; Oregon State University, USA

**Abstract:** Based on the principle of magnetic flux cancellation, partially overlapped spiral inductors can achieve nearly zero magnetic coupling with ultra-compact footprint. This paper presents a study of the characteristics of partially overlapped spiral inductor configurations fabricated in 130nm RFCMOS and 22nm FinFET processes. The viability of the compact inductor layout with controlled very low magnetic coupling is demonstrated by on-wafer measurement and full-wave simulations. Negligible degradation in isolation due to metal fill is observed for both processes, demonstrating the feasibility of the compact layout design methodology even at lower technology nodes with stringent metal density requirements.



## RMo2D-3

### Parasitic Model to Describe Breakdown in Stacked-FET SOI Switches

Kathleen Muhonen<sup>1</sup>, Scott Parker<sup>1</sup>, Kaushik Annam<sup>2</sup>; <sup>1</sup>Qorvo, USA, <sup>2</sup>University of Dayton, USA

**Abstract:** A simple passive capacitance model has been optimized to predict breakdown in a stacked SOI FET. Specifically, as the number of FETs in a switch increases, an equivalent increase in breakdown is not seen in hardware; instead, the breakdown performance saturates as the number of stacks in the FET increases. This phenomenon is not predicted by the FET foundry model. This work is focused on FETs for RF switches in flip chip topologies. As a result of this work, the different components that contribute to off-state capacitances were also described which is important for model development and accuracy.

## RMo2D-4

### Residual Network Based Direct Synthesis of EM Structures: A Study on One-to-One Transformers

David Munzer, Siawpeng Er, Minshuo Chen, Yan Li, Naga S. Mannem, Tuo Zhao, Hua Wang;  
Georgia Tech, USA

**Abstract:** We propose using machine learning models for the direct synthesis of on-chip electromagnetic (EM) passive structures to enable rapid or even automated designs and optimizations of RF/mm-Wave circuits. As a proof of concept, we demonstrate the direct synthesis of a 1:1 transformer on a 45nm SOI process using our proposed neural network model. Using pre-existing transformer s-parameter files and their geometric design training samples, the model predicts target geometric designs.

**Session RMo3A:**  
**RFIC Systems and Applications I: Biomedical and Radar Systems**  
**Chair: Oren Eliezer, Apogee Semiconductor, USA**  
**Co-Chair: Yao-Hong Liu, imec, The Netherlands**

**RMo3A-1**

**3D Imaging Using mmWave 5G Signals**

Junfeng Guan, Arun Paidimarri, Alberto Valdes-Garcia, Bodhisatwa Sadhu, IBM T.J. Watson Research Center, USA

**Abstract:** The ability to create and steer beams, and the availability of large bandwidths have opened up the possibility of using mmWave 5G networks for radar-like sensing applications. In this paper, we introduce a signal processing pipeline that is able to process reflected OFDM-based communications waveforms and create radar images without affecting communications protocols or data throughput. An experimental demonstration system for this concept comprising a prototype basestation transmitter and an auxiliary imaging receiver is also presented. These two components are implemented with Si-based 28-GHz, 64-element phased array transceiver modules and software-defined radios. Measurement results show 3D radar images of indoor scenes with 2° angular and 15 cm ranging resolution using 5G-like communications waveforms at 28-GHz, without any effect on communication functionality.

**RMo3A-2**

**Digitally Assisted mm-Wave FMCW Radar for High Performance**

Karthik Subburaj<sup>1</sup>, Anil Mani<sup>1</sup>, Krishnanshu Dandu<sup>2</sup>, Karan Bhatia<sup>1</sup>, Karthik Ramasubramanian<sup>1</sup>, Sriram Murali<sup>1</sup>, Rittu Sachdev<sup>1</sup>, Pankaj Gupta<sup>1</sup>, Sreekiran Samala<sup>2</sup>, Dheeraj Shetty<sup>1</sup>, Zahir Parkar<sup>1</sup>, Shankar Ram<sup>1</sup>, Vashishth Dudhia<sup>1</sup>, Daniel Breen<sup>2</sup>, Sachin Bharadwaj<sup>1</sup>, Sumeer Bhatara<sup>1</sup>, Brian Ginsburg<sup>2</sup>, <sup>1</sup>Texas Instruments, India, <sup>2</sup>Texas Instruments, USA

**Abstract:** This paper presents digital techniques to improve performance parameters of an mm-wave Frequency Modulated Continuous Wave (FMCW) radar front end. It proposes calibration techniques to: a) reduce a complex (IQ) baseband receiver's (RX) quadrature mismatch (IQMM) and a beamforming transmitter's (TX) phase shifter inaccuracies, b) reduce RX analog baseband mismatches, and c) reduce effect of multiplicative noise arising from strong TX-RX external coupling / reflections from radar-casing. Benefits are demonstrated with measurements from a 45nm CMOS 77GHz band radar SoC.

## RMo3A-3

### A Hybrid-Integrated Artificial Mechanoreceptor in 180nm CMOS

Han Hao, Lin Du, Andrew G. Richardson, Timothy H. Lucas, Mark G. Allen, Jan Van der Spiegel, Firooz Aflatouni; University of Pennsylvania, USA

**Abstract:** A low-power wireless chip for an implantable tactile sensor system is presented. The reported ASIC utilizes the low-loss magnetic human body communication channel for both wireless powering and data transfer. The chip is hybrid-integrated with an in-house fabricated MEMS capacitive force sensor to form an implantable artificial mechanoreceptor (IAM). An on-chip correlated double sampling capacitance-to-time converter consumes  $3.9\mu\text{W}$  from a 1.2V on-chip regulated supply and achieves a resolution of 22.8fF over an input capacitance range of 100pF, while occupying an area of only  $0.04\text{mm}^2$ . A wireless power management feedback is used to ensure robust operation for different hand gestures and under process-voltage-temperature (PVT) variations. The IAM can operate in on-off keying (OOK) or frequency-shift keying (FSK) modulation formats, where the transmitter consumes only  $15.6\mu\text{W}$  in OOK mode and is more immune to hand gesture variations in FSK mode. The  $1.62\text{mm}^2$  chip is fabricated in a standard 180nm CMOS process and consumes  $104.3\mu\text{W}$ .

## RMo3A-4

### Fully Autonomous System-on-Board with Complex Permittivity Sensors and 60GHz Transmitter for Biomedical Implant Applications

V. Issakov<sup>1</sup>, C. Heine<sup>1</sup>, V. Lammert<sup>1</sup>, J. Stoeckmueller<sup>1</sup>, M. Meindl<sup>2</sup>, U. Stubenrauch<sup>1</sup>, C. Geissler<sup>1</sup>;

<sup>1</sup>Infineon Technologies, Germany, <sup>2</sup>eesy-IC, Germany

**Abstract:** This paper presents a system on board (SoB) solution intended for fully autonomous implantable continuous monitoring of biomaterials. The proposed SoB is built around a packaged highly-integrated chip, which comprises two capacitive resonant-tank-based complex permittivity dielectric sensors operating in K-band, temperature sensor, wakeup timer, finite state machine (FSM), serial peripheral interface (SPI), ADC and a 60 GHz transmitter. Wakeup timer is used to turn on the 1.5 V power domain regularly every 8.9 min, which stays “on” only for 4.2 ms. During this time the FSM implements the fully autonomous functionality of the system by running a pre-defined sequence, performing the sensor measurements and forwarding the data to transmitter. The sensor data is read via SPI, buffered and transmitted outside of the implant as a Manchester coded BPSK sequence modulated onto a 60 GHz carrier. The chip is realized in a 130 nm BiCMOS process and packaged using a flip-chip ball-grid array technology. To save chip area, the 60 GHz antenna is realized in the redistribution layer (RDL) of the package. The SoB additionally comprises an external PLL, low-dropout regulators and external reference oscillator. The size of the SoB module is only  $18\text{mm} \times 14\text{mm}$ . It can operate up to 233 days from a small 3.7 V LiPo 95 mAh battery. The functionality is verified in measurement by monitoring the fully autonomous sequence. Next, biological materials are applied to the sensor, modulated values are transmitted and demodulated using an external 60 GHz down-converter and digital Costas loop. Finally, isopropanol-water solutions are applied in 25% concentration change steps and demodulated complex permittivity values are evaluated.

## Session RMo3B: Millimeter-Wave Transceivers and Building Blocks

Chair: Shahriar Shahramian, Nokia Bell Labs, USA

Co-Chair: Hongtao Xu, Fudan University, China

### RMo3B-1

#### 60GHz Variable Gain & Linearity Enhancement LNA in 65nm CMOS

David Bierbuesse, Renato Negra; RWTH Aachen University, Germany

**Abstract:** This paper reports on the design of a 60 GHz low-noise amplifier (LNA) with a linear and power efficient gain tuning mechanism in a 65 nm CMOS process. The transformer-based (TF) matching topology enables a compact LNA design which requires a total chip area of 0.26 mm<sup>2</sup> including all probing pads. The designed LNA has a maximum gain of 25 dB with a 3-dB bandwidth of 8 GHz and a minimum measured noise figure (NF) of 4.8 dB. By means of the proposed gain tuning concept, a tuning range of 17 dB with an input referred 1-dB compression point,  $P_{1dB}$ , of -7 dBm can be achieved. The power consumption is adapted to the LNA gain and ranges from 26 mW to 47 mW.

### RMo3B-2

#### A 64-QAM 45-GHz SiGe Transceiver for IEEE 802.11aj

Peigen Zhou<sup>1</sup>, Jixin Chen<sup>1</sup>, Pinpin Yan<sup>1</sup>, Hao Gao<sup>2</sup>, Debin Hou<sup>1</sup>, Jiayang Yu<sup>1</sup>, Jiarui Hu<sup>1</sup>, Chen Wang<sup>1</sup>, Haoyi Dong<sup>1</sup>, Long Wang<sup>1</sup>, Zhengbo Jiang<sup>1</sup>; <sup>1</sup>Southeast University, China, <sup>2</sup>Technische Universiteit Eindhoven, The Netherlands

**Abstract:** The approval of IEEE 802.11aj in 2018 enabling the indoor short range application of 45 GHz millimeter-wave (mm-wave) frequency band in China. This paper presents an IEEE 802.11aj mm-wave transceiver with printed on-board antenna, operating from 42.3 to 48.4 GHz, in a 0.13  $\mu$ m SiGe:C BiCMOS technology. The transmitter chip achieves a maximum output power of 18.7 dBm at 44 GHz and delivers an OP1dB of 14.6 to 16.4 dBm at the IEEE 802.11aj frequency band. The receiver chip achieves 3.8 to 4.1 dB noise figure (NF), -18.7 to -22 dBm input 1 dB compression point and a conversion gain better than 43.8 dB in the IEEE 802.11aj frequency band. The measured printed on-board Yagi-Uda antenna achieves 9 dBi gain. The power consumption is 478 mW and 186 mW in the transmitter and the receiver modes respectively. In the system wireless data transmission measurement, the measured TX-to-RX EVM in 64-QAM is -29 dB (3.55%) at a 1 meter distance. Compared to other state-of-arts, the transmitter's output power is the highest, and the demonstrated transceiver achieves the highest performance in the IEEE 802.11aj wireless link.

## RMo3B-3

### A Scalable 60GHz 4-Element MIMO Transmitter with a Frequency-Domain-Multiplexing Single-Wire Interface and Harmonic-Rejection-Based De-Multiplexing

Ali Binaie<sup>1</sup>, Sohail Ahasan<sup>1</sup>, Armagan Dascurcu<sup>1</sup>, Mahmood Baraani Dastjerdi<sup>1</sup>, Robin Garg<sup>2</sup>, Manoj Johnson<sup>2</sup>, Arman Galioglu<sup>1</sup>, Arun Natarajan<sup>2</sup>, Harish Krishnaswamy<sup>1</sup>; <sup>1</sup>Columbia University, USA, <sup>2</sup>Oregon State University, USA

**Abstract:** This work demonstrates a 60GHz 45nm RF-SOI 4-element scalable MIMO TX with a single-wire interface (SWI) to alleviate the challenge of supporting high data-rate I/O in a large-scale tiled MIMO mm-wave array. Frequency-domain multiplexing is used on the single wire to simultaneously support the signals of all 4 MIMO channels while breaking the trade-off between channel-to-channel isolation and single-wire bandwidth. Harmonic-rejection mixing (HRM) is used to demultiplex the 4 modulated signals simultaneously from the single-wire, each with 2GHz bandwidth (total BW of 8GHz). A novel two-stage wideband HRM achieves high channel-to-channel isolation with low power overhead. The single-wire interface can support 8GHz total IF bandwidth across the 4 channels with 30–40dB SFDR. Each TX in the array achieves 20–35dB conversion gain and 8.8–10.9dBm OP1dB while maintaining a channel-to-channel isolation >30dB. System level measurements show the ability of the MIMO chip to form multiple simultaneous independent beams carrying independent signals.

## RMo3B-4

### A Bidirectional 56–72GHz to 10.56GHz Transceiver Front-End with Integrated T/R Switches in 28-nm CMOS Technology

Wei Zhu<sup>1</sup>, Di Li<sup>1</sup>, Jiawen Wang<sup>1</sup>, Xiaohan Zhang<sup>2</sup>, Yan Wang<sup>1</sup>; <sup>1</sup>Tsinghua University, China, <sup>2</sup>Rice University, USA

**Abstract:** This paper presents a co-matched bidirectional 56–72 GHz to 10.56 GHz transceiver (TRX) front-end (FE) targeting the IEEE 802.11ad/ay standard with integrated transformer-based transmit/receive (T/R) switches. The TRX FE includes an RF FE and an IF FE. In the RF FE, the reused transformer functions as T/R switch, balun, and impedance matching networks for both LNA and PA simultaneously. The T/R switch, LNA and PA are co-matched, bandwidth and linearity enhancement techniques are utilized in the LNA and PA's inter-stage matching networks. A similar design method is also used in the IF FE. The proposed architecture is implemented in a 28-nm CMOS technology; test results prove that the insertion loss of the proposed T/R switches introduced in RF/IF FE is about 1.2 dB. It also benefits from the gain-boosting technique in RX mixer, the RX mode of the TRX FE achieves maximum conversion gain (CG) of 23.8 dB over 56–72 GHz while demonstrating a 6.1 dB minimum noise figure. The TX mode of the TRX FE achieves maximum CG of 26.2 dB over 56–72 GHz while demonstrating an 8.5 dB maximum OP1dB. The core area of the TRX FE is only 1.2 mm × 1.2 mm.

## RMo3B-5

### A 10.56Gbit/s, -27.8dB EVM Polar Transmitter at 60GHz in 28nm CMOS

Johan Nguyen<sup>1</sup>, Khaled Khalaf<sup>2</sup>, Steven Brebels<sup>1</sup>, Mithlesh Shrivastava<sup>1</sup>, Kristof Vaesen<sup>1</sup>, Piet Wambacq<sup>1</sup>;  
<sup>1</sup>imec, Belgium, <sup>2</sup>Pharrowtech, Belgium

**Abstract:** A 28 nm CMOS 60 GHz polar transmitter (TX) is presented. It can handle modulations up to 64 QAM with a baud rate up to 1.76 Gbaud. Both amplitude and phase modulation are performed on chip at a sample rate up to 5.28 GS/s. The saturated output power is 12.6 dBm and the peak drain efficiency is 26.0%. A TX data rate of 10.56 Gb/s is achieved with a DAC alias at -19.4 dBc. With a core area of 0.115 mm<sup>2</sup> this transmitter consumes 95.4 mW (without on-chip memory) from a 0.9 V supply.

## Session RMo3C: Millimeter-Wave Power Amplifiers

Chair: Patrick Reynaert, KU Leuven, Belgium

Co-Chair: Oleh Krutko, Xilinx, Ireland

### RMo3C-1

#### A Dual-Mode V-Band 2/4-Way Non-Uniform Power-Combining PA with +17.9-dBm $P_{\text{sat}}$ and 26.5-% PAE in 16-nm FinFET CMOS

Kun-Da Chu<sup>1</sup>, Steven Callender<sup>2</sup>, Yanjie Wang<sup>3</sup>, Jacques C. Rudell<sup>1</sup>, Stefano Pellerano<sup>2</sup>, Christopher Hull<sup>2</sup>; <sup>1</sup>University of Washington, USA, <sup>2</sup>Intel, USA, <sup>3</sup>Hillsboro, USA

**Abstract:** This paper presents the design of a dual-mode V-band PA with efficiency enhancement at power back-off via load modulation. The design utilizes a reconfigurable 2/4-way non-uniform power combiner to enable two discrete modes of operation — full power and back-off power. The 2-stage PA achieves a peak gain of 21.4dB with a fractional BW of 22.6% (51–64GHz). At 65GHz, the PA has a  $P_{\text{sat}}$  of +17.9dBm with an  $OP_{\text{1dB}}$  of +13.5dBm and a peak PAE of 26.5% in full-power mode. In back-off power mode, the measured  $P_{\text{sat}}$ ,  $OP_{\text{1dB}}$ , and peak PAE are +13.8dBm, +9.6dBm, and 18.4%, respectively. The PAE is enhanced by 6-% points at 4.5-dB back-off. The PA is capable of amplifying a 6-Gb/s 16-QAM modulated signal with an  $EVM_{\text{rms}}$  of -20.7dB at an average  $P_{\text{out}}$ /PAE of +13dBm/13.6%, respectively. This PA is implemented in 16-nm FinFET, occupies a core area of 0.107mm<sup>2</sup>, and operates under a 0.95-V supply.

### RMo3C-2

#### A 28-GHz Highly Efficient CMOS Power Amplifier Using a Compact Symmetrical 8-Way Parallel-Parallel Power Combiner with IMD3 Cancellation Method

Hyunjin Ahn, Ilku Nam, Ockgoo Lee; Pusan National University, Korea

**Abstract:** This paper presents a linear CMOS power amplifier (PA) for mm-wave 5G applications. A compact 8-way parallel-parallel power combiner is proposed to increase  $P_{\text{out}}$  with low loss and symmetrical phase/amplitude. The IMD3 cancellation method is presented in this work to obtain a high linear  $P_{\text{out}}$  with high PAE. The PA in 65-nm CMOS shows a 23.2dBm  $P_{\text{out}}$  with 33.5% PAE for CW signals at 28GHz. It achieves the highest linear PAE of 17.6% at an average  $P_{\text{out}}$  of 18.02dBm with -31.2dB EVM and -30dBc ACPR supporting a 256-QAM 100MSym/s signal at 28GHz.

### RMo3C-3

#### An Embedded 200GHz Power Amplifier with 9.4dBm Saturated Power and 19.5dB Gain in 65nm CMOS

Hadi Bameri, Omeed Momeni; University of California, Davis, USA

**Abstract:** This paper presents a 200 GHz power amplifier in 65 nm bulk CMOS technology aiming for maximizing the saturated power ( $P_{\text{sat}}$ ). A matched-cascode amplification cell (amp-cell) is designed to increase supply voltage and  $P_{\text{sat}}$ , while maintaining the power gain. Embedding is used around the amp-cell to boost power gain and increase total  $P_{\text{sat}}$  by overcoming matching loss. A low input impedance, balanced slot power combiner is proposed to increase  $P_{\text{sat}}$  even further. The PA is implemented using 8 cascaded embedded amp-cells and features 9.4dBm maximum  $P_{\text{sat}}$  and 6.3dBm OP1dB, and has 19.5dB power gain at 202GHz.

### RMo3C-4

#### A 130-GHz Power Amplifier in a 250-nm InP Process with 32% PAE

Kang Ning, Yihao Fang, Mark Rodwell, James Buckwalter; University of California, Santa Barbara, USA

**Abstract:** This work presents a 120- to 140-GHz 250-nm Indium Phosphide (InP) HBT power amplifier (PA) capable of delivering 15-dBm saturated output power ( $P_{\text{sat}}$ ) and 32% power added efficiency (PAE). The PA is designed using a pseudo-differential common-base (CB) stage to improve the power gain and power-added efficiency (PAE). A load-line matching design methodology is described for CB topology using a planar sub-quarter wavelength balun for low-loss power combining. The chip size is 0.4mm×0.5mm including pads. To the author's knowledge, this is a record PAE for D-band PAs using any integrated circuit process.

### RMo3C-5

#### A 160GHz High Output Power and High Efficiency Power Amplifier in a 130-nm SiGe BiCMOS Technology

Xingcun Li, Wenhua Chen, Yunfan Wang, Zhenghe Feng; Tsinghua University, China

**Abstract:** In this paper, a compact sub-terahertz low loss power combiner is proposed to realize optimal output matching and power combining, simultaneously. With the proposed technique, a 160 GHz 4-way power amplifier (PA) in a 130-nm SiGe BiCMOS technology is achieved, which exhibits a maximum power gain of 24 dB and 3-dB bandwidth of 20 GHz. Moreover, the PA achieves a saturated output power of 18 dBm and power-added efficiency (PAE) of 9.4% at 160 GHz, where the loss of pads, input and output feed lines are all included. To the best of our knowledge, it achieves the highest efficiency among the previously reported SiGe PAs above 150 GHz. The chip area of the power amplifier is only 1.02×0.82 mm<sup>2</sup>.



## **Session RMo4A: RFIC System and Applications II: Wideband Wireless Communication and Quantum Computing**

**Chair:** Renyuan Wang, BAE Systems, USA

**Co-Chair:** Rocco Tam, NXP Semiconductors, USA

### **RMo4A-1**

#### **A Flexible Control and Calibration Architecture Using RISC-V MCU for 5G Millimeter-Wave Mobile RF Transceivers**

Jungwoo Kim<sup>1</sup>, Jae Min Kim<sup>1</sup>, Sangwook Han<sup>1</sup>, Pritesh Vora<sup>2</sup>, Pranav Dayal<sup>2</sup>, Hyunggi Kim<sup>1</sup>, Jonghwan Lee<sup>1</sup>, Daeyoung Yoon<sup>1</sup>, Jeiyoun Lee<sup>1</sup>, Tienyu Chang<sup>2</sup>, Ivan Siu-Chuang Lu<sup>2</sup>, Kee-Bong Song<sup>2</sup>, Sang Won Son<sup>2</sup>, Jongwoo Lee<sup>1</sup>; <sup>1</sup>Samsung, Korea, <sup>2</sup>Samsung, USA

**Abstract:** We propose an architecture for mobile RF transceivers which integrates RISC-V micro-controller unit (MCU) to control its internal function without requiring multiple chip-to-chip control messages from the modem. The proposed architecture is utilized to perform 5G millimeter wave (mmWave) control tasks including beamforming and temperature dependent gain compensation. The control architecture including MCU and its subsystem occupies 0.258 mm<sup>2</sup> in 28-nm process, and consumes 2.61 mW at 140 MHz (18  $\mu$ W/MHz). Based on the evaluation results, our proposed architecture enables control of 5G mmWave RF transceivers.

### **RMo4A-2**

#### **Spatio-Temporal Filtering: Precise Beam Control Using Fast Beam Switching**

Arun Paidimarri, Bodhisatwa Sadhu; IBM T.J. Watson Research Center, USA

**Abstract:** This paper presents a spatio-temporal filtering approach for beamforming with phased arrays. The approach takes advantage of fast beam switching in modern Si-integrated phased arrays enabled by integrated digital circuits. The key technique involves fast switching among spatial beams created using the phased array. The resulting time-averaged beam represents a new spatial filter that might not have been feasible using the phase and gain control resolution available in the phased array. We present the underlying theory, and perform extensive system measurements on a software defined phased array radio based on state-of-the-art 28GHz phased array ICs. We demonstrate three use cases of spatio-temporal beam control in measurement: a) side lobe reduction, b) multi-armed beam formation and c) null pointing. We demonstrate how this approach can enable high precision beam control even in systems with limited phase shifter resolution and/or systems without any gain control per antenna element.

### **RMo4A-3**

#### **An Integrated True Zero-Wait-Time Dynamic Frequency Selection (DFS) Look-Ahead Scheme for WiFi-Radar System Co-Existence**

YangChuan Chen, Bing Xu, Eric Lu, Osama Shana'a; MediaTek, USA

**Abstract:** An integrated look-ahead DFS scheme relies on having a dedicated low-cost receiver that constantly scans the WiFi band for radar existence. A table of radar-occupied WiFi channels is constructed as a result. When it is time to switch channels upon radar in-channel detection, the WiFi transceiver can directly jump to an empty channel without having to sniff for 60s, as required by FCC/ETSI regulations. The scheme results in zero-wait time and zero impact to WiFi throughput. Circuit implementation relies on reusing some readily existing hardware in a 55nm CMOS  $n \times n$  MIMO WiFi transceiver to reduce die cost.

### **RMo4A-4**

#### **RF Clock Distribution System for a Scalable Quantum Processor in 22-nm FDSOI Operating at 3.8K Cryogenic Temperature**

Imran Bashir<sup>1</sup>, Dirk Leipold<sup>1</sup>, Mike Asker<sup>1</sup>, Ali Esmailiyan<sup>2</sup>, Hongying Wang<sup>2</sup>, Teerachot Siriburanon<sup>2</sup>, Panagiotis Giounanlis<sup>2</sup>, Anna Koziol<sup>2</sup>, Dennis A. Miceli<sup>2</sup>, Elena Blokhina<sup>2</sup>, R. Bogdan Staszewski<sup>2</sup>; <sup>1</sup>Equal1 Labs, USA, <sup>2</sup>University College Dublin, Ireland

**Abstract:** We present an RF clock distribution system for a fully integrated and scalable quantum processor core operating at 3.8 K. An external 2.4 GHz signal is guided from the generator to the flip-chip package IC through a cryogenic coaxial cable. The choice of coaxial cable and the clock routing design on the PCB and IC, minimizes path loss and coupling to the supplies, the I/O signals, and more importantly the sensitive quantum core. The clock integrity up to the quantum core is maintained and verified by the jitter measurement of 0.8 ps from a test port while all circuitry within the cryo-cooler operates within the thermal load specification of 1.5W.

## Session RMo4B: Millimeter-Wave and Terahertz Circuits and Systems for Sensing and Communications

Chair: Omeed Momeni, University of California, Davis, USA

Co-Chair: Ruonan Han, MIT, USA

### RMo4B-1

#### An Integrated 132–147GHz Power Source with +27dBm EIRP

Akshay Visweswaran<sup>1</sup>, Alexander Haag<sup>2</sup>, Carmine de Martino<sup>3</sup>, Karina Schneider<sup>2</sup>, Tim Maiwald<sup>4</sup>, Bastien Vignon<sup>1</sup>, Klaus Aufinger<sup>5</sup>, Marco Spirito<sup>3</sup>, Thomas Zwick<sup>2</sup>, Piet Wambacq<sup>1</sup>; <sup>1</sup>imec, Belgium, <sup>2</sup>KIT, Germany, <sup>3</sup>Technische Universiteit Delft, The Netherlands, <sup>4</sup>FAU Erlangen-Nürnberg, Germany, <sup>5</sup>Infineon Technologies, Germany

**Abstract:** We present a 132–147GHz power source based on four power amplifiers whose outputs are combined into a compact ( $0.52 \times 0.48 \text{mm}^2$  footprint) dielectric resonator antenna mounted on the chip face. The source, prototyped in  $0.13 \mu\text{m}$  SiGe BiCMOS, demonstrates an EIRP of 27dBm with a power-added efficiency of 13.8%. Individual PAs deliver a peak  $P_{\text{sat}}$  of 15dBm over a 3-dB bandwidth of 116–152GHz. Excited by shorted patches on chip, the maximum efficiency of the hybrid antenna is 80% over a 16% relative bandwidth. The EIRP and transmitted RF power are the highest reported for D-band silicon-based transmitters.

### RMo4B-2

#### A High-Speed 390GHz BPOOK Transmitter in 28nm CMOS

Carl D'heer, Patrick Reynaert; KU Leuven, Belgium

**Abstract:** This paper presents a 390 GHz transmitter in 28nm bulk CMOS employing the spectrally efficient binary-phase on-off keying (BPOOK) modulation. A novel switch-based modulator is proposed, enabling high-speed OOK, BPSK and BPOOK modulation at 130GHz. The modulated signal is amplified by a three-stage power amplifier and converted to 390 GHz by a frequency tripler. The transmitter achieves an output power of -5.4dBm at 390 GHz with a power consumption of 114mW. A maximum data rate of 28 Gb/s is achieved with BPOOK and 18 Gb/s with OOK and BPSK modulation.

### **RMo4B-3**

#### **A SiGe Millimeter-Wave Front-End for Remote Sensing and Imaging**

Milad Frounchi, John D. Cressler; Georgia Tech, USA

**Abstract:** This work presents the co-design of a millimeter-wave (mm-wave) switch with a low-noise amplifier (LNA), in which the front-end switch incorporates a transformer-based topology and serves as the LNA input matching network. This mm-wave front-end is implemented in a 0.13 $\mu$ m SiGe BiCMOS technology and achieves a peak gain of 20.1 dB, a minimum noise figure of 4.5 dB, and a mean isolation of 17 dB. The input reflection coefficient is less than -15 dB over 45–70 GHz. An avalanche noise source using a diode-configured SiGe HBT is also integrated in the front-end for two-reference on-chip calibration, which can provide up to a high excess noise ratio of 25 dB. The LNA consumes a DC power of 15 mW and occupies a chip area of 0.6 mm<sup>2</sup>. To the best of our knowledge, this is the lowest reported noise figure of an integrated switch and LNA at V-band frequencies and is the first monolithic two-reference calibrating mm-wave SiGe radiometer front-end.

### **RMo4B-4**

#### **A Fully Integrated Coherent 50–500-GHz Frequency Comb Receiver for Broadband Sensing and Imaging Applications**

Sam Razavian, Aydin Babakhani; University of California, Los Angeles, USA

**Abstract:** This paper presents a fully integrated oscillator-less frequency-comb receiver for broadband sensing, spectroscopy, and imaging in millimeter-wave and THz bands. The chip consists of a THz pulse generator block to generate the reference tones for coherent frequency comb detection. The repetition rate of the reference pulses (LO frequency comb) are tunable over a 4–10.5 GHz range, with the highest sensitivity achieved at 9 GHz. A broadband on-chip antenna with a peak directivity of 15 dBi is employed for broadband detection. The receiver, which is capable of detecting any arbitrary spectrum, is characterized from 140 GHz to 500 GHz using continuous-wave sources. Peak sensitivity of -105 dBm is achieved at 261 GHz. The chip is implemented in 130-nm SiGe BiCMOS technology and consumes only 52-mW DC power. The chip can also be used as a frequency comb radiator. Chip-to-chip dual-comb measurement is performed using two identical chips in the radiator and receiver modes, respectively up to 450 GHz.

**Session RMo4C:**  
**High-Performance Frequency-Generation Components**  
Chair: Mohyee Mikhemar, Broadcom, USA  
Co-Chair: Wanghua Wu, Samsung, USA

**RMo4C-1**

**A 0.082mm<sup>2</sup> 24.5-to-28.3GHz Multi-LC-Tank Fully-Differential VCO Using Two Separate Single-Turn Inductors and a 1D-Tuning Capacitor Achieving 189.4dBc/Hz FOM and 200±50kHz 1/f<sup>3</sup> PN Corner**

Hao Guo, Yong Chen, Pui-In Mak, Rui P. Martins; University of Macau, China

**Abstract:** This paper reports a capacitive-coupling multi-LC-tank fully-differential VCO with wideband 1/f<sup>3</sup> phase noise (PN) corner reduction. It features two separate single-turn inductors and a differential-mode 1D-tuning capacitor bank to realize high-quality-factor high-impedance resonances at the 1×-to-2× of the oscillation frequency. Prototyped in 65nm CMOS technology, the VCO occupies 0.082mm<sup>2</sup> and measures a tuning range (TR) of 24.5 to 28.3GHz. The FOM is 189.4dBc/Hz and the TR-insensitive 1/f<sup>3</sup> PN corner is 200±50kHz.

**RMo4C-2**

**A 22.4-to-40.6-GHz Multi-Ratio Injection-Locked Frequency Multiplier with 57.7-dBc Harmonic Rejection**

Jingzhi Zhang, Yu Peng, Huihua Liu, Chenxi Zhao, Yunqiu Wu, Kai Kang; UESTC, China

**Abstract:** This paper presents a multi-ratio injection-locked frequency multiplier (MR-ILFM) targeting millimeter-wave (mm-wave) multiband 5G communications. With only low-frequency narrow-bandwidth input signals required, difficulties in generating low-phase-noise mm-wave wideband signals can be solved by switching the multiplication ratio of the MR-ILFM for bandwidth extension. Issues on suppressing undesired harmonics in multi-ratio multipliers are considered, and an impulse sensitivity function (ISF) based analysis is adopted to show the superior harmonic rejection properties of injection locking. With the use of injection locking and ILFM cascading, the harmonic rejection reaches to 57.7 dBc. The proposed MR-ILFM has ×5 and ×7 multiplication ratio, and 24 switchable frequency bands for ratio switching. Fabricated in 65 nm CMOS process, the MR-ILFM consumes 10.0-mW power and can operate from 22.4 to 40.6 GHz with 4.3-to-5.8-GHz inputs.

### **RMo4C-3**

#### **A 0.35mW 70GHz Divide-by-4 TSPC Frequency Divider on 22nm FD-SOI CMOS Technology**

Zoltán Tibenszky, Corrado Carta, Frank Ellinger; Technische Universität Dresden, Germany

**Abstract:** This paper presents a divide-by-4 TSPC frequency divider operating with supply voltages from 0.4 V to 0.9 V and covering input frequency ranges from below 100 MHz to 70 GHz and beyond. The operating frequency and the required input power is adjustable through the backgate voltages of the transistors of the employed fully depleted silicon on insulator (FD-SOI) technology. When operating at 70 GHz, the divider core consumes only 393  $\mu$ A from a 0.9 V supply, which correspond to a FoM of 195 GHz/mW. To the best knowledge of the authors, the presented circuit demonstrates the highest reported operating frequency for TSPC dividers, and smallest area and lowest current consumption values among RF frequency dividers reported to date.

### **RMo4C-4**

#### **A Dual-Core 8–17GHz LC VCO with Enhanced Tuning Switch-Less Tertiary Winding and 208.8dBc/Hz Peak FoM<sub>T</sub> in 22nm FDSOI**

Omar El-Aassar, Gabriel M. Rebeiz; University of California, San Diego, USA

**Abstract:** This work presents a low phase noise wide tuning range dual-core transformer-based VCO using a switch-less tertiary magnetic coupling loop. The design employs the benefits of transformer-switching without incurring switch loss and quality factor degradation, and also the benefits of mode-switching without the parasitics from the mode-selection network. The VCO uses dual-mode operation with a constant quality factor capacitors bank and a positive feedback DC-coupled inductive-degenerated output buffer to maximize the tuning range. The VCO, implemented in 22nm FDSOI, achieves a 72% tuning at 8–17 GHz and a figure-of-merit-tuning (FoM<sub>T</sub>) of 208.8 dBc/Hz at 11 GHz. The chip operates from an 0.45 V supply with a power consumption of 17–33 mW and a core area of 0.39 mm<sup>2</sup>. To the authors knowledge, the VCO achieves the highest FoM<sub>T</sub> and lowest supply for designs over 10 GHz.

## Session RTu1A: Millimeter-Wave Signal Generation

Chair: Ehsan Afshari, University of Michigan, USA

Co-Chair: Andreia Cathelin, STMicroelectronics, France

### RTu1A-1

#### Frequency Multiplier-by-4 (Quadrupler) with 52dB Spurious-Free Dynamic Range for 152GHz to 220GHz (G-Band) in 130nm SiGe

Paul Stärke, Vincent Rieß, Corrado Carta, Frank Ellinger; Technische Universität Dresden, Germany

**Abstract:** This work presents a frequency multiplier-by-4, which uses extensive passive filtering to improve the rejection of the undesired harmonics and increase the spurious-free dynamic range (SFDR). The circuit is intended for mm-wave communication systems operating at 180 GHz and its active core consists of two push-push doubler stages and a two-stage output buffer. It achieves a bandwidth of 68 GHz, covering almost the complete G-band and exhibits an SFDR between 52 dBc and 64 dBc. The saturated output power is up to -1dBm and the corresponding maximum dc power consumption is 45mW, resulting in a dc efficiency of up to 1.8%. The final chip occupies an area of 1.3mm<sup>2</sup> and is implemented in a 130nm SiGe BiCMOS process, which offers a maximum oscillation frequency  $f_{\max}$  of 450 GHz. To the knowledge of the authors, this circuit offers the highest SFDR and one of the largest bandwidths of any fully-integrated mm-wave multiplier of factor 4 or above. The fabricated chip is also packaged into a waveguide module, which shows almost the same bandwidth and only 1 dB of additional loss at the output.

### RTu1A-2

#### A D-Band SiGe Frequency Doubler with a Harmonic Reflector Embedded in a Triaxial Balun

Sunil G. Rao, Milad Frounchi, John D. Cressler; Georgia Tech, USA

**Abstract:** This paper presents a SiGe push-push frequency doubler with a triaxial balun embedded harmonic reflector. An input triaxial balun is used to generate differential signals for the push-push core, while also providing a high quality 2nd harmonic reflector. Two frequency doublers were designed in a 90nm SiGe BiCMOS platform, both with and without an output buffer. The buffer-less design achieves a record peak output power and efficiency of 9.4dBm and 12.1% at 130 GHz, with a bandwidth of 128–140 GHz. The buffered design achieves a peak output power of 8.85dBm and 8.8% efficiency, while operating over a wider bandwidth.

### **RTu1A-3**

#### **A Multichannel Programmable High Order Frequency Multiplier for Channel Bonding and Full Duplex Transceivers at 60GHz Band**

A. Siligaris, J.L. Gonzalez-Jimenez, Clement Jany, B. Blampey, A. Boulmirat, A. Hamani, C. Dehos; CEA-Leti, France

**Abstract:** This paper describes a high order programmable frequency multiplier in the 60 GHz band. The circuit implements four chains that can address simultaneously four different frequencies of the IEEE 802.11ay standard and aims to channel bonding, full duplex, or MIMO systems. It is fabricated in a 45nm CMOS PDSOI technology. Each chain consumes 32.6mW and achieves lower than 178fsec of integrated jitter (in the band 10KHz–1.08GHz) for all synthesized frequencies.

### **RTu1A-4**

#### **A 126GHz, 22.5% Tuning, 191dBc/Hz FOMt 3rd Harmonic Extracted Class-F Oscillator for D-Band Applications in 16nm FinFET**

Bart Philippe, Patrick Reynaert; KU Leuven, Belgium

**Abstract:** This paper presents a harmonic oscillator with an extracted third harmonic from 108.7-to-120.6GHz and 127.5-to-144GHz for D-band applications. The inherent third harmonic generation of the oscillator removes the need of a high frequency divider or multiplier. The mm-wave oscillator is implemented in a deeply scaled 16nm FinFET technology achieving a 22.5% tuning range around 126GHz with a peak FoMt of 191 dBc/Hz from a 0.6V supply.

### **RTu1A-5**

#### **A 7.4dBm EIRP, 20.2% DC-EIRP Efficiency 148GHz Coupled Loop Oscillator with Multi-Feed Antenna in 22nm FD-SOI**

Muhammad Waleed Mansha, Mona Hella; Rensselaer Polytechnic Institute, USA

**Abstract:** This paper presents a 148 GHz coupled loop oscillator with multi-feed (MF) octagonal slot antenna. The MF antenna combines the output power from four single ended fundamental oscillators ( $f_o$ ) and back radiates the combined fundamental power through a silicon lens. The output power from each oscillator is ac coupled to the following stage using a phase compensation capacitor, whose value is selected to increase the oscillation frequency of the coupling loop network. The oscillator is fabricated in 22nm FD-SOI process and has a peak EIRP of 7.4 dBm and a corresponding DC-EIRP efficiency of 20.2%. To the best of the authors' knowledge, this offers over an order of magnitude improvement in DC-EIRP efficiency among 100–200 GHz VCOs reported to date.



## Session RTu1B: 5G Focus Session on Advances in Mixer-First Receivers

Chair: Ramesh Harjani, University of Minnesota, USA

Co-Chair: Harish Krishnaswamy, Columbia University, USA

### RTu1B-1

#### mm-Wave Mixer-First Receiver with Passive Elliptic Low-Pass Filter

Pingyue Song, Hossein Hashemi; University of Southern California, USA

**Abstract:** Passive mixer-first receivers have gained interest for their superior linearity, lower power consumption, and smaller footprint. Traditionally, the load of these mixers is a passive or active RC filter. This paper demonstrates a passive mixer-first receiver where the mixer load is a third-order passive elliptic filter realized using on-chip capacitors and spiral inductors so that wide bandwidth and high selectivity are concurrently achieved. The 65nm CMOS prototype covers a tunable frequency between 21 and 29 GHz and achieves 0.5 GHz instantaneous baseband bandwidth,  $>49$  dB stopband to passband rejection, an in-band ICP<sub>-1dB</sub> of -6 dBm and out-of-band B<sub>-1dB</sub>  $>3.4$  dBm.

### RTu1B-2

#### 10–35GHz Passive Mixer-First Receiver Achieving +14dBm In-Band IIP3 for Digital Beam-Forming Arrays

Sashank Krishnamurthy, Ali M. Niknejad; University of California, Berkeley, USA

**Abstract:** A 10–35GHz mixer-first receiver is proposed for use in digital beam-forming arrays. Techniques are proposed to enhance the linearity of such receivers, both at baseband and the RF mixer switches. An integrated circuit prototype is fabricated in 28nm bulk CMOS as proof of concept. The receiver achieves an in-band IIP3 of +14dBm, a gain of 15dB and a noise figure of 12.5dB.

### RTu1B-3

#### A 9–31GHz 65nm CMOS Down-Converter with $>4$ dBm OOB B1dB

Zachariah G. Boynton, Alyosha Molnar; Cornell University, USA

**Abstract:** This paper presents a frequency tunable, high dynamic range 65nm bulk CMOS downconverter operating from 9–31GHz. The design implements a topology variation of a 4 phase passive mixer which allows for sinusoidal LO drive and achieves a minimum NF of 12.5dB and out of band (OOB) blocker compression (B1dB) of -6dBm for a B1dB-NF FoM of -18.5 dB while consuming only 73mW. Should higher performance be required, a B1dB of over 4 dBm, and OOB IIP3 of 21 dBm, can be achieved using 162mW of power while maintaining noise and bandwidth performance, for a FoM of -8.5dB. To the author's knowledge this is the highest such FoM reported for a CMOS receiver in this frequency range.

## RTu1B-4

### A 2.5-to-4.5-GHz Switched-LC-Mixer-First Acoustic-Filtering RF Front-End Achieving <6dB NF, +30dBm IIP3 at 1×Bandwidth Offset

Hyungjoo Seo, Jin Zhou; University of Illinois at Urbana-Champaign, USA

**Abstract:** This paper describes an agile RF front-end that consists of an N-path switched-LC mixer in silicon followed by an acoustic filter — essentially a *mixer-first acoustic-filtering RF front-end*. The mixer frequency-translates a sharp but fixed acoustic filtering profile to a much higher and LO-defined tunable frequency while preserves input matching, high-linearity, and introduces minimal loss. In contrast to the existing N-path passive-mixer-first receivers which use active baseband filters after N-path switches, using a single acoustic filter as the N-path load is fraught with fundamental challenges. We introduce on-chip LC-tanks to suppress the acoustic filter out-of-band impedance and an all-passive recombination network to share one acoustic filtering among N paths. A front-end prototype using a CMOS switched-LC passive mixer followed by an off-the-shelf 1.6-GHz surface-acoustic-wave (SAW) filter is designed and optimized. In measurement, the RF front-end operates across 2.5-to-4.5 GHz achieving 5.5-dB NF and +29.4-dBm IIP3 at 1× bandwidth offset.

## Session RTu1C: Linearization and Efficiency Enhancement Techniques

Chair: Sungwon Chung, Neuralink, USA

Co-Chair: Margaret Szymanowski, NXP Semiconductors, USA

### RTu1C-1

#### A 1–3GHz I/Q Interleaved Direct-Digital RF Modulator as a Driver for a Common-Gate PA in 40nm CMOS

Yiyu Shen, Rob Bootsman, Morteza S. Alavi, Leo C.N. de Vreede; Technische Universiteit Delft, The Netherlands

**Abstract:** We present a 1–3 GHz,  $2 \times 13$ -bit I/Q interleaved direct-digital RF modulator (DDRM) realized in 40 nm CMOS technology as a driver for an external common-gate (CG) power amplifier (PA). The proposed digital-intensive quadrature up-converter features a pair of novel current-steering mixing DACs with an additional leakage path to boost the efficiency of the external CG PA. The realized DDRM also employs IQ-interleaving, harmonic rejection, and dynamic biasing to improve its spectral purity, in-band linearity, and system efficiency. The proposed digital up-converter prototype provides standalone more than 19.6 dBm RF peak output power. Without using any digital pre-distortion, it achieves an ACLR of -44.5 dBc and an EVM of -35 dB, when applying an 80 MHz 256 QAM signal at 2.4 GHz.

### RTu1C-2

#### A 1.3V Wideband RF-PWM Cartesian Transmitter Employing Analog Outphasing and a Switched-Capacitor Class-D Output Stage

Heechai Kang, Venkata S. Rayudu, Ki Yong Kim, Ranjit Gharpurey; University of Texas at Austin, USA

**Abstract:** A wideband RF-PWM Cartesian transmitter is introduced that employs a combination of a DLL-based outphasing modulator and a switched-capacitor quadrature class-D power amplifier. A modulator that provides outphasing signals to synthesize RF-PWM without a narrow pulse-width limitation is proposed. The Cartesian transmitter is implemented in a 65-nm CMOS process. The measured peak output power of the transmitter is 15.5 dBm with a 1.3 V supply. The design is verified with digitally-modulated signals with a bandwidth of up to 160 MHz at a carrier frequency of 2 GHz.

### RTu1C-3

#### Preserving Polar Modulated Class-E Power Amplifier Linearity Under Load Mismatch

Awani Khodkumbhe<sup>1</sup>, Maikel Huiskamp<sup>2</sup>, Ali Ghahremani<sup>2</sup>, Bram Nauta<sup>2</sup>, Anne-Johan Annema<sup>2</sup>; <sup>1</sup>BITS Pilani, India, <sup>2</sup>University of Twente, The Netherlands

**Abstract:** Power amplifiers (PAs) need digital predistortion (DPD) linearization to handle high-order complex modulation schemes in next-generation communication systems. While load variation is inevitable, DPD is generally designed considering only the nominal load impedance for PAs. This paper presents a polar class-E PA with an on-chip waveform characterizer enabling adaptive digital predistortion (ADPD) to preserve the linearity of the PA under load mismatch. The presented ADPD corrects both AM/AM and AM/PM distortions, which are prominent in the demonstrated PA,

while simultaneously correcting for slow memory effects without the need for complex memory DPD algorithms. Load-pull measurements demonstrate that target error vector magnitude (EVM) and adjacent channel power ratio (ACPR) can be maintained in a significantly larger area on the Smith chart going from 50  $\Omega$  optimized static DPD to our ADPD for a 2 GHz 1024 QAM signal with 1 MSym/s symbol rate.

## RTu1C-4

### A 28GHz Voltage-Combined Doherty Power Amplifier with a Compact Transformer-Based Output Combiner in 22nm FD-SOI

Zhiwei Zong<sup>1</sup>, Xinyan Tang<sup>1</sup>, Khaled Khalaf<sup>2</sup>, Dongyang Yan<sup>1</sup>, Giovanni Mangraviti<sup>1</sup>, Johan Nguyen<sup>1</sup>, Yao Liu<sup>1</sup>, Piet Wambacq<sup>1</sup>; <sup>1</sup>imec, Belgium, <sup>2</sup>Pharrowtech, Belgium

**Abstract:** This paper presents a Doherty power amplifier (PA) in 22nm FD-SOI for achieving high output power and high back-off efficiency for 28GHz 5G communications. The output stage of the main PA and the auxiliary PA both use a stacked-FET topology for high output power without posing a reliability issue. A dedicated transformer-based output matching network is proposed to achieve a true Doherty load modulation while maintaining a compact layout. The PA is fabricated in a 22nm FD-SOI technology with a core area of 0.2mm<sup>2</sup>. At 28GHz, the measured saturated output power ( $P_{sat}$ ), 1dB output compression point ( $P_{1dB}$ ), and peak power-added efficiency (PAE) are 22.5dBm, 21.1dBm, and 28.5%, respectively. State-of-the-art ITRS figure-of-merit (FOM) and power density are achieved. The measured 6dB power back-off (PBO) PAE is 22.1%, which results in a PBO enhancement ratio of 1.56/3.12 with respect to a class-B/class-A PA. The proposed PA can support 2.4Gb/s 64-QAM and 0.8Gb/s 256-QAM signal with a competitive average PAE.

## RTu1C-5

### A 6GHz 160MHz Bandwidth MU-MIMO Eight-Element Direct Digital Beamforming TX Utilizing FIR H-Bridge DAC

Boyi Zheng, Lu Jie, Runyu Wang, Michael P. Flynn; University of Michigan, USA

**Abstract:** This work extends the bandwidth and frequency range of digital-phase-shifting direct-digital-to-RF TX, paving the way for use in MU-MIMO wireless networking applications. A sigma-delta modulation chain enables an inherently linear 1b RF DAC. Low-loss FIR filtering suppresses sigma-delta DAC noise. An H-bridge combines current-DAC, FIR-filtering and RF up-conversion for efficiency. A 28 nm CMOS 8-element 6 GHz beamforming TX has a per-element area of 0.01 mm<sup>2</sup> and a per-element power of 47.5 mW.

**Session RTu1D:**  
**Mixed-Signal and Power Management Techniques for RF Transceivers**  
Chair: Antoine Frappé, ISEN Lille, France  
Co-Chair: Bahar Jalali Farahani, Acacia Communications, USA

**RTu1D-1**

**Fourier-Domain DAC-Based Transmitter: New Concepts Towards the Realisation of Multigigabit Wireless Transmitters**

Oner Hanay, Erkan Bayram, Stefan Müller, Mohamed Elsayed, Renato Negra; RWTH Aachen University, Germany

**Abstract:** A Fourier-Domain digital-to-analogue converter (FDDAC) based transmitter is presented for the first time. The proposed topology generates a coherent bandwidth in the GHz range exploiting the Fourier Transform concept. Thus, the DAC sampling rate is reduced by up to two orders of magnitude compared to conventional transmitters. Moreover, it provides an intrinsic spectral shaping of the digital input signal. Thus, no complex signal processing in terms of oversampling and filtering is required in order to achieve a clean transmit signal with low out-of-band emissions. The feasibility of the proposed concept is validated by designing a fully integrated prototype transmitter including signal processing in 65nm CMOS technology. It generates a single-carrier signal with a bandwidth of up to 2 GHz and a modulation order of up to 16QAM in the sub 6-GHz frequency range. The occupied chip area is 1.34mm<sup>2</sup>. The achieved EVM is -9.4 dB for a QPSK modulated signal.

**RTu1D-2**

**A 10MHz 40V  $V_{IN}$  Slope-Reconfigurable Gaussian Gate Driven GaN DC-DC Converter with 49.1dB Conducted EMI Noise Reduction at 100MHz**

Chang Yang<sup>1</sup>, Weizhong Chen<sup>1</sup>, Wei Da<sup>2</sup>, Yanli Fan<sup>2</sup>, Ping Gui<sup>1</sup>; <sup>1</sup>Southern Methodist University, USA, <sup>2</sup>Texas Instruments, USA

**Abstract:** This paper demonstrates a 10MHz 4V-to-40V  $V_{IN}$ , GaN-based buck converter with reconfigurable electromagnetic interferences (EMI) reduction techniques. A Gaussian switching scheme is first time realized on chip at the switching node to effectively reduce EMI while maintaining high power efficiency. Combined with frequency dithering scheme, the proposed method reduces EMI noise by 36.9dB and 49.1dB at 10MHz and 100MHz respectively. From 250MHz to 400MHz and from 400MHz to 500MHz, the measured peak EMI noise is reduced by 22dB and 16dB, respectively. The maximum power efficiency is 85.2%, comparable to that of the conventional gate driving schemes.

### RTu1D-3

#### A Sub-10fs FOM, 5000× Load Driving Capacity and 5mV Output Ripple Digital LDO with Dual-Mode Nonlinear Voltage Detector and Dead-Zone Charge Pump Loop

Bowen Wang, Woogeun Rhee, Zhihua Wang; Tsinghua University, China

**Abstract:** This paper describes an analog-assisted digital low dropout regulator (LDO) with dual-mode operation by employing a dual-mode nonlinear voltage detector (DNVD) and a charge pump (CP) LDO for enhanced transient performance and reduced output ripple. In the transient mode, the proposed digital LDO achieves a high loop gain, operating like a flash-ADC digital LDO with a nonlinear decoder. The loop gain of the digital LDO is further boosted by the CP LDO. In the steady mode, the CP LDO is turned off, and the digital LDO becomes a shift register (S/R) digital LDO with a voltage dead-zone for small output ripple. An exponential-ratio array (ERA) is designed to substantially increase the load driving capacity of power transistors. The proposed digital LDO implemented in 65nm CMOS achieves 8.69fs FOM with 5000× load driving capacity when the input voltage and the output voltage are 0.6V and 0.5V respectively. Thanks to the DNVD with the dead-zone operation, the output ripple is reduced from 20mV to 5mV, while achieving the quiescent current of 28.5μA in the steady mode.

### RTu1D-4

#### A 32–40GHz 7-Bit CMOS Phase Shifter with 0.38dB/1.6° RMS Magnitude/Phase Errors for Phased Array Systems

Yongjie Li<sup>1</sup>, Zongming Duan<sup>2</sup>, Wei Lv<sup>2</sup>, Dongfang Pan<sup>1</sup>, Zipeng Xie<sup>1</sup>, Yuefei Dai<sup>2</sup>, Liguo Sun<sup>1</sup>; <sup>1</sup>USTC, China, <sup>2</sup>ECRIEE, China

**Abstract:** This paper presents a 32–40GHz 7-bit programmable passive vector synthesis phase shifter in 65 nm CMOS. It mainly consists of a compact differential hybrid quadrature generator (HQG) based on folded transformer and a 12-bit binary weighted passive vector modulation (PVM) composed of two 6-bit phase invariant passive variable gain amplifiers (VGAs). Two additional inter-stage matching transformer are placed between the HQG and VGAs in order to obtain wider bandwidth and better amplitude and phase performances. The measurement results show a RMS phase error of 0.45° to 1.6° over 32–40 GHz, and 0.45° to 1.1° over 33–39 GHz, whereas covering 360° phase range at 2.8° resolution. The measured variation of insertion loss (IL) is below ±0.8dB over 32–40 GHz and below ±0.6dB over 33–39 GHz, the RMS magnitude error is less than 0.38 dB over 32–40 GHz. The power consumption is zero and the core die area is 630 μm×220 μm.

**Session RTu2A: Ultra-Low Power Transceivers**  
**Chair: Chun Huat Heng, NUS, Singapore**  
**Co-Chair: Gernot Hueber, Silicon Austria Labs, Austria**

**RTu2A-1**

**A 66.97pJ/Bit, 0.0413mm<sup>2</sup> Self-Aligned PLL-Calibrated Harmonic-Injection-Locked TX with >62dBc Spur Suppression for IoT Applications**

Chung-Ching Lin, Huan Hu, Subhanshu Gupta; Washington State University, USA

**Abstract:** Digital-intensive ultra-low-power (ULP) wireless transmitters (TX) employing harmonic injection locking suffer from large close-in reference spurs that violates the TX spectral mask. This paper presents a self-aligned type-I PLL in conjunction with harmonic injection locking to achieve significantly improved spur performance at ULP for sub-GHz IoT TXs. The on-chip type-I PLL calibrates the phase error in the ring oscillator (RO) in real time and avoid large spurs induced from the frequency deviation in the harmonic injection-locked technique through the proposed twin-T notch filter in the feedback loop. Implemented in 180nm CMOS process, the proposed frequency translating TX occupies an active area of only 0.0413mm<sup>2</sup> with -14dBm output at 915MHz. We report the lowest power consumption with 3X improved energy-efficiency while consistently achieving >62dBc spur suppression. The TX also supports OOK modulation with an average power consumption of 200.9μW only at 3Mb/s data rate achieving 66.97pJ/bit energy efficiency.

**RTu2A-2**

**A 67-μW Ultra-Low Power PVT-Robust MedRadio Transmitter**

Somok Mondal, Drew A. Hall; University of California, San Diego, USA

**Abstract:** A 400 MHz narrowband MedRadio transmitter for short-range communication is presented. A new technique for PVT-robust, calibration- and regulation-free synthesis of the RF carrier is reported based on generating poly-phasors at 50 MHz with no power overhead. This is accomplished using a passive polyphase filter directly integrated within a crystal oscillator followed by an 8× edge combiner to synthesize the RF carrier with -109 dBc/Hz phase noise at 100 kHz offset. A dual supply, inverse class-E power amplifier is implemented for high efficiency at low output power (-17.5 dBm). Open-loop operation permits aggressive duty-cycling (< 40 ns start-up time). State-of-the-art ultra-low power is reported from a prototype BPSK transmitter fabricated in 22 nm CMOS FDX when operated from a 0.4/0.2 V supply consuming 67 μW with 27% global efficiency.

## RTu2A-3

### A 400MHz/900MHz Dual-Band Ultra-Low-Power Digital Transmitter for Biomedical Applications

Zhaoyang Weng<sup>1</sup>, Hanjun Jiang<sup>1</sup>, Yanshu Guo<sup>1</sup>, Zhihua Wang<sup>2</sup>; <sup>1</sup>Tsinghua University, China, <sup>2</sup>RITS, China

**Abstract:** This paper presents a 400MHz/900MHz dual-band ultra-low-power digital transmitter with high energy efficiency for biomedical applications. Direct modulation at local oscillator and digital power amplifier is adopted to simplify the transmitter architecture. With edge combining, the dual band transmitter shares a single digital controlled ring oscillator. The 400MHz transmitter adopts 16QAM modulation scheme with the ring oscillator under injection-locked while the 900MHz transmitter adopts BFSK with open loop ring oscillator. Fabricated in 65nm CMOS, the chip occupies an area of 1.3mm<sup>2</sup>. Under 0.5V supply voltage, both band transmitters consume less than 0.6mW power while delivering -15dBm of output power and the 400MHz transmitter achieves an energy efficiency of 53pJ/bit. The measured EVM is 4.35% for 16QAM at 10Mbps and the FSK error is 5.08% at 2Mbps.

## RTu2A-4

### A mm-Scale Sensor Node with a 2.7GHz 1.3μW Transceiver Using Full-Duplex Self-Coherent Backscattering Achieving 3.5m Range

Zhen Feng, Li-Xuan Chuo, Yao Shi, Yejoong Kim, HunSeok Kim, David Blaauw; University of Michigan, USA

**Abstract:** This paper presents a 1.3 μW backscatter-based transceiver for battery-powered millimeter-scale sensor nodes. By taking advantage of the coherence of reflected dual-side bands, it attains an optimum SNR and improved interference rejection with low-power, non-coherent binary modulation. Integrated with a 2.1×4 mm planar antenna in a complete, crystal-less sensor node, it achieves a 3.5 m communication distance with a reader transmitting 31 dBm equivalent isotropic radiated power (EIRP).

## RTu2A-5

### A Fully Integrated 0.2V 802.11ba Wake-Up Receiver with -91.5dBm Sensitivity

Jaeho Im<sup>1</sup>, Jacob Breiholz<sup>2</sup>, Shuo Li<sup>2</sup>, Benton Calhoun<sup>2</sup>, David D. Wenzloff<sup>1</sup>; <sup>1</sup>University of Michigan, USA, <sup>2</sup>University of Virginia, USA

**Abstract:** A standalone, fully integrated 0.2V 578μW ultra-low voltage (ULV) 2.4GHz 802.11ba WiFi wake-up receiver (WRX) is presented. It includes a current-efficient ULV noise cancelling LNA with a high turn step-up transformer, and Q-enhanced RF gain stages for low noise figure. A  $1/3 f_{RF}$  mixer and ULV FLL are implemented to reduce current. The chip includes micro-power managers for regulating all internal voltages from a single 0.2V supply. Fabricated in 40nm CMOS, the ULV WRX achieves -91.5dBm sensitivity at 10<sup>-3</sup> BER and data-rate of 62.5kbps, while rejecting a 45dB adjacent blocker with only 0.2V supply. The WRX includes an energy-efficient 5ms startup sequence which interfaces to an external node controller over serial peripheral interface (SPI).



## Session RTu2B:

### 5G Focus Session on Millimeter-Wave Components and Systems

Chair: Tim Larocca, Northrop Grumman, USA

Co-Chair: Jane Gu, University of California, Davis, USA

#### RTu2B-1

##### A 16-Element Fully Integrated 28GHz Digital Beamformer with In-Package 4×4 Patch Antenna Array and 64 Continuous-Time Band-Pass Delta-Sigma Sub-ADCs

Rundao Lu, Christine Weston, Daniel Weyer, Fred Buhler, Michael P. Flynn; University of Michigan, USA

**Abstract:** This paper presents a fully-integrated 28GHz mm-wave digital beamformer, combined with a custom-designed 8-layer LTCC substrate 4×4 patch antenna array, for a complete 16-element single-chip mm-wave-to-digital beamforming system. 16-element digital beamforming in a single IC represents an excellent tradeoff between die size, signal loss, and I/O routing complexity. Optimum placement of the ADCs, together with the use of four 27GHz PLLs, shortens both LO and mm-wave signal routing and reduces signal loss. ADC sampling of a high (1GHz) IF enables single-phase mm-wave LO routing and moves the I/Q mixing into the digital domain. A 4× parallel band-pass ADC structure provides in-built FIR filtering for additional harmonic suppression and anti-alias filtering. Bit-stream processing takes advantage of the short bit-width outputs of the RX slices to implement digital beamforming with area and energy-efficient MUXes. The prototype 16-element beamformer generates four independent, simultaneous beams. Over-the-air measurements confirm accurate 3D beam patterns, indicate a measured overall noise figure of 7dB, and QAM-4 EVM of -18dB.

#### RTu2B-2

##### A 28GHz Front-End Module with T/R Switch Achieving 17.2dBm $P_{sat}$ , 21.5% PAE<sub>max</sub> and 3.2dB NF in 22nm FD-SOI for 5G Communication

Yao Liu<sup>1</sup>, Xinyan Tang<sup>1</sup>, Giovanni Mangraviti<sup>1</sup>, Khaled Khalaf<sup>2</sup>, Yang Zhang<sup>1</sup>, Wei-Min Wu<sup>1</sup>, Shih-Hung Chen<sup>1</sup>, Björn Debaillie<sup>1</sup>, Piet Wambacq<sup>1</sup>, <sup>1</sup>imec, Belgium, <sup>2</sup>Pharrowtech, Belgium

**Abstract:** A 28 GHz front-end module (FEM) for 5G communication is implemented in 22 nm FD-SOI technology. Competitive performance for both TX and RX modes is achieved simultaneously with robustness in TX mode and ESD protection. The key for these features is the transmit/receive (T/R) switch incorporating PA circuitry, offering high linearity and robustness in TX mode, low NF in RX mode, and ESD-protection capability. The PA output stage uses a 3-stacked-FET topology to achieve high output power. Several matching techniques are implemented to equally distribute the large output voltage swing among the three stacked FETs.  $P_{sat}$  and PAE<sub>max</sub> in TX mode are 17.2 dBm and 21.5%, respectively. NF and IIP<sub>3</sub> in RX mode are 3.2 dB and -5.4 dBm, respectively. With a 100 MHz bandwidth 256-QAM single-carrier signal the FEM achieves an EVM of -30 dB with average output power of 10.1 dBm and average PAE of 8.3%. The reliability of the FEM in TX mode is assessed, demonstrating the robustness of the FEM. The ESD measurement of the FEM shows 2 kV human-body-model (HBM) ESD protection.

### RTu2B-3

#### A 24–28GHz Power and Area Efficient 4-Element Phased-Array Transceiver Front-End with 21.1%/16.6% Transmitter Peak/OP1dB PAE Supporting 2.4Gb/s in 256-QAM for 5-G Communications

Wei Zhu<sup>1</sup>, Jiawen Wang<sup>1</sup>, Wei Lv<sup>2</sup>, Xiaohan Zhang<sup>3</sup>, Bingbing Liao<sup>2</sup>, Yanping Zhu<sup>2</sup>, Yan Wang<sup>1</sup>;

<sup>1</sup>Tsinghua University, China, <sup>2</sup>ECRIIE, China, <sup>3</sup>Rice University, USA

**Abstract:** This paper presents a 24–28 GHz 4-element phased-array transceiver (TRX) front-end (FE) for 5-G communications. A transformer-based embedded T/R switch is proposed which minimizes TX and RX losses to ensure high TX output power and power efficiency while maintaining a low noise figure (NF) and extremely compact chip area. The chip prototype is fabricated in a 65-nm CMOS process, the TX path achieves a record level measured 16.4 dBm/18.8 dBm OP1dB/Psat with 21.1%/16.6% peak/OP1dB PAE for each element (including T/R switch, off-mode LNA) while maintaining a minimum 4.4 dB NF in the RX path (including T/R switch, off-mode PA) at 28 GHz. Under the 64/256-QAM modulation, the TX path achieves a state-of-the-art average output power of 13.5/10.2 dBm per element (8.4%/3.5% TX PAE) with -30.8/-26.4 dB EVM and 27.8/30.1 dB ACLR at 28 GHz, making the proposed TRX FE can be effectively deployed in both base stations and user equipment for 5-G communications. The chip size of the 4-element TRX FE excluding I/O pads is only  $3.4 \times 1.1 \text{ mm}^2$ .

### RTu2B-4

#### A CMOS Ka-Band SATCOM Transceiver with ACI-Cancellation Enhanced Dual-Channel Low-NF Wide-Dynamic-Range RX and High-Linearity TX

Yun Wang<sup>1</sup>, Dongwon You<sup>1</sup>, Xi Fu<sup>1</sup>, Takeshi Nakamura<sup>1</sup>, Ashbir Aviat Fadila<sup>1</sup>, Teruki Someya<sup>1</sup>, Atsuhiko Kawaguchi<sup>1</sup>, Jian Pang<sup>1</sup>, Kiyoshi Yanagisawa<sup>1</sup>, Bangan Liu<sup>1</sup>, Yuncheng Zhang<sup>1</sup>, Haosheng Zhang<sup>1</sup>, Rui Wu<sup>1</sup>, Atsushi Shirane<sup>1</sup>, Shunichiro Masaki<sup>2</sup>, Daisuke Yamazaki<sup>2</sup>, Kenichi Okada<sup>1</sup>;

<sup>1</sup>Tokyo Institute of Technology, Japan, <sup>2</sup>Socionext, Japan

**Abstract:** This paper presents the first Ka-band satellite communication (SATCOM) transceiver in standard CMOS technology. The proposed Ka-band SATCOM transceiver is based on direct-conversion architecture with high-linearity TX and dual-channel multi-mode RX, which is designed for a earth ground platform communicating with Geostationary (GEO) and low Earth orbit (LEO) satellites. The dual-channel RX enables multiple duplexing modes, which are polarization duplexing and frequency duplexing. In the receiver, both the RF path and the baseband path provide variable gain for a wider dynamic range. The LNA employs dual-coupling transformer for low noise figure and wideband input matching. An adjacent channel interference (ACI) cancellation scheme is proposed to further enhance the RX dynamic range in frequency duplexing mode. In the transmitter single-turn high-quality-factor transformer is employed to realize matching network and four-way power combining. A prototype of the SATCOM transceiver is fabricated in a standard 65-nm CMOS process. Under 1.05 V supply voltage, the transmitter achieves a  $P_{\text{SAT}}$  of 19 dBm and an average output power of 10.6 dBm with 2% EVM and 42.9 dB ACPR. The dual channel receiver achieves a single-sideband NF of 5.0 dB, IIP3 of 0.2 dBm and with a 10.4 dB ACI suppression.

## RTu2B-5

### Inter-Stream Loopback Calibration for 5G Phased-Array Systems

Yuuichi Aoki, Yonghoon Kim, Yongan Hwang, Sunryoul Kim, Manh Tuan Dao, Daehyun Kang, Donggyu Minn, Heedo Kang, Hyun-Chul Park, An-Sang Ryu, Sehyug Jeon, Sung-Gi Yang; Samsung, Korea

**Abstract:** A novel built-in phased-array calibration method for multi-stream 5G transceiver is presented. A transmit signal is monitored using couplers and sent to the receiver for the other stream. Multiple antenna elements are characterized simultaneously by solving linear equations using the proposed phase matrix which suppresses the required dynamic range. It takes less than 150  $\mu$ s in loopback measurement to characterize gains and phases of 16 elements.

## Session RTu2C: Sub-6 GHz Receiver Front-End Circuits

Chair: Kamran Entesari, Texas A&M University, USA

Co-Chair: Gary Hau, Qualcomm, USA

### RTu2C-1

#### A Wide-Band RF Front-End Module for 5G mMIMO Applications

Mike Fraser, Venkata N.K. Malladi, Joseph Staudinger, Chun-Wei Chang; NXP Semiconductors, USA

**Abstract:** This paper presents a 2–5 GHz mMIMO RF front-end module that includes an RF switch followed by two stages of low-noise amplifiers (LNA). The switch and LNAs are designed in 0.25 $\mu$ m GaAs technology as two ICs, placed in a multi-chip module (MCM) and housed in a LGA package. The FEM achieves 47 dBm peak power handling in failsafe (FS)/TX mode, 1.35 dB noise figure, 31.5 dBm OIP<sub>3</sub> and 17 dBm P1dB at 3.5 GHz. It also achieves a switching speed of 230 ns when tested with a very low frequency (1 KHz) toggle signal, a typical requirement on these FEMs. The excellent switching speed is accomplished through the use of a new time-adaptive bias technique to overcome interface trap charging inherent to the GaAs substrate. The RX module achieves the lowest reported noise figure & switching time while achieving high peak power handling in the FS mode operation.

### RTu2C-2

#### A 1.2V, 5.5GHz Low-Noise Amplifier with 60dB On-Chip Selectivity for Uplink Carrier Aggregation and 1.3dB NF

Daniel Schrögenderfer, Thomas Leitner; Infineon Technologies, Austria

**Abstract:** This paper presents a low-noise amplifier (LNA) with a passive and switchable 8th-order bandstop filter to enable high on-chip selectivity for inter-band uplink carrier aggregation (UL CA) applications. It is fabricated using a 60-nm RF SOI CMOS technology. The LNA uses a broadband output stage with current reuse topology which enables a reduced in-band gain variation, high voltage gain and minimized chip area. Based on using on-chip matching and filtering elements, a noise figure (NF) of only 1.3 dB in filter off-state and 1.9 dB in filter on-state respectively, along with a high filter attenuation between 1.7 GHz and 2.7GHz to fulfill all linearity requirements for UL CA applications are achieved. All RF and DC ports are ESD-protected. The power consumption of the chip is only 6mW using a 1.2V supply voltage, which enables future RF front-end requirements.

### RTu2C-3

#### A 5–6GHz Low-Noise Amplifier with >65-dB Variable-Gain Control in 22nm FinFET CMOS Technology

Yi-Shin Yeh, Hyung-Jin Lee; Intel, USA

**Abstract:** This paper presents a 5–6 GHz fully-differential low-noise amplifier in 22-nm FinFET Low-Power CMOS technology. To achieve wide gain control, the three-stage LNA consists of a Tee-type RF attenuator and a current-steering variable-gain amplifier. Three-winding transformers are implemented for input and inter-stage matching to achieve simultaneous noise and power matching. The three-stage LNA provides 30.5-dB gain, 1.9-dB minimum noise figure, -29.2-dBm IP<sub>1dB</sub> and -19.9-dBm IIP<sub>3</sub> at 5.7 GHz, and > 65-dB gain-control range with the total DC power consumption of 39 mW at 1-V supply voltage.

## RTu2C-4

### A Wideband Variable-Gain Amplifier with a Negative Exponential Generation in 40-nm CMOS Technology

Yangtao Dong, Lingshan Kong, Chirn Chye Boon, Zhe Liu, Chenyang Li, Kaituo Yang, Ao Zhou; NTU, Singapore

**Abstract:** A wideband variable-gain amplifier (VGA) with a negative exponential generation using 40 nm CMOS technology is reported. By compensating a single-branch negative exponential generator (NEG) which features a composite of dual Taylor series, the proposed negative exponential generation further extends the dB-linear range. The measurement results show the overall VGA achieves a dB-linear range of 51 dB ( $-34 \sim 17$ dB) with a gain error less than  $\pm 1$  dB. In addition, the bandwidth is around 7 GHz under different gain settings. The core circuit draws 24.6 mA current from a 1.1 V power supply (excluding the output buffer) and occupies an active area of 0.038 mm<sup>2</sup>.

## RTu2C-5

### A 0.08mm<sup>2</sup> 1–6.2GHz Receiver Front-End with Inverter-Based Shunt-Feedback Balun-LNA

Benqing Guo<sup>1</sup>, Dario Prevedelli<sup>2</sup>, Rinaldo Castello<sup>2</sup>, Danilo Manstretta<sup>2</sup>; <sup>1</sup>Chengdu University, China, <sup>2</sup>Università di Pavia, Italy

**Abstract:** An inverter-based active feedback CMOS LNA with balun function is within a direct converter receiver. The LNA has three gain stages. The Multi-gated transistor (MGTR) technique is employed to null the third-order distortion of the last two gain stages while complementary configurations are used to compensate second-order nonlinearity in all stages. The complete direct-conversion receiver was fabricated in 28nm CMOS. Measurement results indicate that the integrated receiver provides a minimum NF of 3.4 dB, and a maximum gain of 48.2 dB from 1 to 6 GHz. The in-band and out-of-band IIP3 are -10 dBm and -4 dBm, respectively. The receiver dissipates 22.2 mW at 5 GHz LO frequency and occupies an area of 0.08 mm<sup>2</sup>.

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## NOTES

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