



2019 IEEE Radio Frequency Integrated Circuits Symposium

Boston, Massachusetts, USA

2–4 June 2019



PROGRAM

Boston Convention and Exhibition Center

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society



RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 2 June 2019

Boston Conference and Exhibition Center

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in the Boston Convention and Exhibition Center.

17:30–19:00, Plenary Session, Ballroom: The evening begins with the Student Paper Awards, Industry Paper Awards, and Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Dr. Greg Henderson, Senior Vice President, Automotive, Communications and Aerospace/Defense at Analog Devices, and Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at imec.

19:00–21:00, RFIC Symposium Reception and Showcase, Ballroom Foyer: Immediately following the Plenary Session is the RFIC Symposium Reception. Food and drinks will be provided while you connect with old friends, make new acquaintances and catch up on the latest developments in the field.

The RFIC Symposium Showcase is held concurrently with the reception and will feature our industry showcase and student paper finalists. The selected authors will be present to highlight their innovative work, summarized in poster format, and some will also show a live demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss the microwave week's opening event. Please see <https://rfic-ieee.org/> for more details.

The RFIC Symposium Reception is made possible through the generous support of our corporate sponsors:

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RFIC Symposium Schedule (1–4 June 2019)

Boston Conference and Exhibition Center

Event	Location	Sat 1 June	Sun 2 June	Mon 3 June	Tue 4 June
Registration	North Lobby	08:00–18:00	07:00–18:00	07:00–18:00	07:00–18:00
Speakers' Breakfast	Room 210AB			07:00–08:00	
Workshops & Short Courses	Rooms 150–161, 251–259B		08:00–11:45 13:30–17:15		
Workshops Lunch	Room 210AB		11:45–13:00		
Technical Lecture (includes lunch)	Room 160ABC		11:45–13:15		
Plenary Session	Ballroom		17:30–19:00		
Reception, Symposium Showcase	Ballroom Foyer		19:00–21:00		
Interactive Forum	Room 253ABC				13:30–15:10
Technical Sessions	Rooms 252AB, 254AB, 257AB			08:00–09:40 10:10–11:50	
				13:30–15:10 15:55–17:15	
Panel Sessions	Room 162AB			12:00–13:15	



Photo by Kyle Chen

TABLE OF CONTENTS

	Table of Contents	1
	Welcome Message from Chairs.....	2
	Steering Committee	4
	Support Staff.....	4
	Executive Committee.....	4
	Advisory Board	4
	Technical Program Committee.....	5
	RFIC 2019 Schedule	6
	Plenary, Reception, and Symposium Showcase.....	7
	Plenary Speakers.....	8
	The Industry Showcase.....	10
	The Student Paper Award Finalists Showcase.....	12
MONDAY	AM1 RMo1A: RF Receiver Building Blocks.....	14
	AM1 RMo1B: Advanced Devices, Characterization, and Modeling for Millimeter-Wave Applications..	16
	AM1 RMo1C: Millimeter-Wave Radar and Imaging Systems	18
	AM2 RMo2A: 5G and Millimeter-Wave Beamforming Building Blocks	21
	AM2 RMo2B: Digitally Assisted Front-Ends for Emerging Wireless Applications	24
	AM2 RMo2C: RF-Inspired Emerging Technologies and Applications.....	27
	PM1 RMo3A: Millimeter-Wave Integrated Subsystems.....	30
	PM1 RMo3B: Blocker Tolerance and Interference Cancellation	33
	PM1 RMo3C: High-Performance Energy-Efficient Oscillators and Frequency Synthesizers	35
	PM2 RMo4A: Millimeter-Wave PAs for 5G and Phased Arrays	37
	PM2 RMo4B: Receiver Circuits in CMOS-SOI Technology	39
	PM2 RMo4C: Mixed Signal Circuits for High Speed RF and Optical Transceivers.....	41
TUESDAY	AM1 RTu1E: Special Session: 5G Circuits and Systems	43
	AM1 RTu1F: Energy-Efficient Wake-Up Receivers and IoT Transceivers	46
	AM2 RTu2E: Special Session: 5G Millimeter-Wave Beamforming Systems.....	48
	AM2 RTu2F: Broadband, Reconfigurable, and Multimode PAs and Transmitters.....	50
	AM2 RTu1F: Interactive Forum.....	52
	Panel Sessions.....	56
	Technical Lecture	58
	Workshops and Short Courses	59
	Social Events/Guest Program.....	77
	Conference Venue Maps.....	78

Welcome Message from Chairs

We invite you to join us in the *2019 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, to be held in Boston, Massachusetts, on 2–4 June 2019. The RFIC Symposium is the premier IC design conference focused exclusively on the latest advances in RF, Microwave and Millimeter-Wave integrated circuit (IC) technologies and designs, as well as innovations in high-frequency analog/mixed-signal ICs. This year the conference will also extend its focus to *emerging circuit technologies related to RFIC*, such as RF circuits and systems incorporating sensors and actuators, heterogeneous and 3D ICs, silicon photonics, quantum computing ICs, hardware security and machine learning applications, wearable and implantable systems, biomedical applications and autonomous systems like automotive and drones. It is with great pleasure that we cordially invite you to participate in this global event!

The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG, and the Industry Exhibition to form the “*Microwave Week*”, the world’s largest RF/microwave technical convention of the year. The 2019 Microwave Week will be held at the Boston Convention and Exhibition Center. Attendees will have the opportunity to interact with world experts, expand their network, and leave invigorated with new ideas and a drive to innovate.

RFIC 2019 features a very exciting and comprehensive program. In the evening of Sunday, 2 June 2019, the highlight during the RFIC Reception will be the popular *Interactive Symposium Showcase*, featuring poster presentations and demos of the most innovative and highly-rated industrial and academic papers.

To promote academic submissions, all of the RFIC student paper finalists will receive complimentary RFIC registration. Students may volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complimentary conference registration, meals, T-shirts, and other benefits. *In addition, this year’s student volunteers can buy the Super-pass at a discounted rate of \$250 and get access to all the sessions of IMS, RFIC and ARFTG!* The joint RFIC/IMS PhD Student Sponsorship Initiative Program will continue to involve selected first and second-year PhD students to complete technical assignments during the conference in exchange for complimentary conference registrations, lodging and meals.

The RFIC Symposium’s educational program opens on Sunday, 2 June 2019, at 08:00 with 12 workshops covering the latest advances in a wide range of topics in RFIC technology and IC design, including power amplifiers, 5G systems, silicon photonics, quantum computing and hardware security. This year RFIC is also promoting a new educational experience for the attendees: a *Technical Lecture* comprising a 1 ½ hour interactive course delivered by a distinguished speaker during lunchtime on Sunday. For 2019, Prof. Ali Niknejad from University of California, Berkeley, will teach “*Fundamentals of mmWave IC Design in CMOS*”. Admission is included with all RFIC Sunday workshops at no added cost, but don’t forget to register early since seats will be limited to the first 250 registrants!

The RFIC Symposium’s technical program opens with the RFIC Plenary Session on Sunday evening. The highlight of the plenary are two visionary talks by our distinguished plenary speakers. Dr. Greg Henderson, Senior Vice President, Automotive, Communications and Aerospace/Defense at Analog Devices, will discuss “*The Digital Future of RFICs*”, describing how digitally-assisted-and-enabled RFICs are empowering the future of wireless sensing and communications with real world examples for applications like 5G and automotive radar. Dr. Ir. Michael Peeters, Program Director Connectivity and Humanized Technology at imec, will address the question “*Do the Networks of the Future Care About the Materials of the Past?*”, taking a look at how the latest requirements for RFIC circuit design, new network capacity, reliability and latency can drive technology choices for the next 10 years. Additionally, at the plenary, we will present our annual awards for Students and Industry.

Immediately following the plenary session, we will have the *2019 RFIC Symposium Reception and Showcase*. During this engaging social and technical evening event supported by our corporate sponsors, industry showcase and student paper finalists will highlight their work in poster presentations and demonstrations. You will not want to miss the RFIC Reception and Showcase!

On Monday and Tuesday, the RFIC Symposium continues with multiple tracks of technical paper presentation sessions on several topics covering power amplifiers, phased arrays, advanced transceivers, imagers and radars, synthesizers and VCOs, IoT, RF and millimeter-wave front ends, semiconductors and emerging technologies. Two special sessions on 5G are scheduled on Tuesday morning and complement the 5G Summit technical sessions on Tuesday afternoon. The Interactive Forum session will be held in the afternoon on Tuesday.

Two enlightening panels will be featured during lunchtimes on both days. The Monday panel session titled *“The Internet of Things (IoT) — Back to the Future, or No Future?”* will feature experts from the industry and academia debating how the future IoT market will be affected by the accelerated introduction of 5G and the developments in ‘big data’ and artificial intelligence. On Tuesday, a joint IMS/RFIC panel titled *“Will Artificial Intelligence (AI) and Machine Learning (ML) Take Away My Job as an RF/Analog Designer?”* will feature distinguished panelists from academia, DARPA, CAD/EDA, and RF industries, debating the future of RF design and how we should prepare ourselves for the inevitable developments in design tools. Please make sure to bring your engaging opinions and questions to both panel sessions!

On behalf of the RFIC Steering and Executive Committees, we welcome you to join us at the 2019 RFIC Symposium in Boston, Massachusetts! Please visit the RFIC 2019 website (<https://rfic-ieee.org/>) for more details and updates.



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Haolu Xie, *Transa Semiconductor*
Hongtao Xu, *Fudan University*

RFIC 2019 Schedule

Boston Convention and Exhibition Center

Saturday, 1 June 2019

08:00–18:00 Registration — North Lobby

Sunday, 2 June 2019

07:00–18:00 Registration — North Lobby

07:00–08:00 Speakers' Breakfast — Room 210AB

08:00–17:15 Workshops and Short Courses — Rooms 150–161, 251–259B

09:40–10:10 Coffee Break — Levels 1 & 2, East Side

11:45–13:00 Workshops Lunch — Room 210AB

11:45–13:15 Technical Lecture — Room 160ABC

15:10–15:40 Coffee Break — Levels 1 & 2, East Side

17:30–19:00 RFIC Plenary — Ballroom

19:00–21:00 RFIC Welcoming Reception Featuring RFIC Symposium Showcase — Ballroom Foyer

Monday, 3 June 2019

07:00–18:00 Registration — North Lobby

07:00–08:00 Speakers' Breakfast — Room 210AB

08:00–17:15 Workshops and Short Courses — Rooms 150–161, 251–259B

08:00–09:40 RMo1A — Room 252AB: *RF Receiver Building Blocks*

RMo1B — Room 254AB: *Advanced Devices, Characterization and Modeling for Millimeter-Wave Applications*

RMo1C — Room 257AB: *Millimeter-Wave Radar and Imaging Systems*

09:40–10:10 Coffee Break — Level 2, East Side

10:10–11:50 RMo2A — Room 252AB: *5G and Millimeter-Wave Beamforming Building Blocks*

RMo2B — Room 254AB: *Digitally Assisted Front-Ends for Emerging Wireless Applications*

RMo2C — Room 257AB: *RF-Inspired Emerging Technologies and Applications*

11:45–13:00 Workshops Lunch — Room 210AB

12:00–13:15 RFIC Panel Session — Room 162AB: *The Internet of Things (IoT) — Back to the Future, or No Future?*

13:30–15:10 RMo3A — Room 252AB: *Millimeter-Wave Integrated Subsystems*

RMo3B — Room 254AB: *Blocker Tolerance and Interference Cancellation*

RMo3C — Room 257AB: *High-Performance Energy-Efficient Oscillators and Frequency Synthesizers*

15:10–15:55 Coffee Break — Level 2, East Side

15:55–17:15 RMo4A — Room 252AB: *Millimeter-Wave PAs for 5G and Phased Arrays*

RMo4B — Room 254AB: *Receiver Circuits in CMOS-SOI Technology*

RMo4C — Room 257AB: *Mixed Signal Circuits for High Speed RF and Optical Transceivers*

Tuesday, 4 June 2019

07:00–18:00 Registration — North Lobby

07:00–08:00 Speakers' Breakfast — Room 210AB

08:00–09:40 RTu1E — Room 252AB: *Special Session: 5G Circuits and Systems*

RTu1F — Room 254AB: *Energy-Efficient Wake-Up Receivers and IoT Transceivers*

09:40–10:10 Coffee Break — Level 2, East Side

10:10–11:50 RTu2E — Room 252AB: *Special Session: 5G Millimeter-Wave Beamforming Systems*

RTu2F — Room 254AB: *Broadband, Reconfigurable, and Multimode PAs and Transmitters*

12:00–13:15 IMS/RFIC Joint Panel Session — Room 162AB: *Will Artificial Intelligence (AI) and Machine Learning (ML) Take Away my Job as an RF/Analog Designer?*

13:30–15:10 Interactive Forum — Room 253ABC

Plenary, Reception, and Symposium Showcase

Sunday Evening, 2 June 2019

Boston Convention and Exhibition Center

17:30–19:00

RFIC Plenary

Ballroom

Chair: Stefano Pellerano, Intel

Co-Chair: Waleed Khalil, The Ohio State University

- 17:30 Welcome Message from General Chair and TPC Chairs,
Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
- 18:00 *The Digital Future of RFICs*
Dr. Greg Henderson, Analog Devices
- 18:30 *Do the Networks of the Future Care About the Materials of the Past?*
Dr. Ir. Michael Peeters, imec

19:00–21:00

RFIC Welcoming Reception

Featuring Industry Showcase and Student Paper Awards Finalists

Ballroom Foyer

The RFIC Interactive Reception starts immediately after the Plenary Session and will highlight the Industry Showcase and Student Paper Awards Finalists in an engaging social and technical evening event with food and drinks. Authors of these showcase and top student papers will present their innovative work, summarized in poster format. Some industry showcase papers will also offer live demonstrations. You will not want to miss the RFIC Reception! This event is supported by the RFIC Symposium corporate sponsors.



Plenary Speaker 1

Dr. Greg Henderson
Senior Vice President
Automotive, Communications and
Aerospace & Defense
Analog Devices

The Digital Future of RFICs

Abstract: Through significant advances in RFIC technology that have shrunk form factors and price points, high complexity RF, Microwave, and Millimeter wave solutions for communications and sensing are reaching the point of ubiquity. Large, complex multi-antenna and phased array solutions that previously only government organizations could justify have become the basis of modern wireless communications and automotive radar. Cars include millimeter-wave radar technology as a standard feature and 77GHz radar is playing a critical role in the autonomous vehicle revolution. Wireless bandwidth has grown from a trickle to a torrent and high channel count, multi-antenna systems are the key enabler for 5G, whose impact is predicted to extend beyond enabling that torrent of mobile data to revolutionizing industries as varied as agriculture, automotive, healthcare, and industrial.

To date, most of the advances in RFIC technology have largely been driven by the industry moving to high volume advanced geometry CMOS processes and massive increases in system-on-chip integration of complete antenna-to-bits signal chains. Since these are not the most friendly process technologies for traditional RF and microwave circuit blocks, the advances of tomorrow need new RF signal chain and circuit block architectures that exploit the strengths of advanced CMOS processes, while mitigating the disadvantages. This talk will show how such novel architectures and circuit innovations are enabled through leverage of high-performance digital capabilities, resulting in important performance advances that in fact exceed what could be obtained from traditional “RF friendly” process technologies. The talk will show how digitally-assisted-and-enabled RFICs are enabling the future of wireless sensing and communications with real world examples for applications like 5G and automotive radar.

About Dr. Greg Henderson

Dr. Greg Henderson was appointed Senior Vice President of Analog Devices’ Automotive, Communications and Aerospace & Defense Group in 2017. Prior to this role, he served as vice president of the RF and Microwave business unit, responsible for the creation and execution of Analog Devices’ strategy for its full suite of RF and microwave products and solutions.

Dr. Henderson has served in leadership roles in the microwave, semiconductor, and wireless communications industry for more than 20 years. Most recently, Dr. Henderson served as Vice President of the RF and Microwave business units of Hittite Microwave Corporation — prior to the acquisition by Analog Devices. From 2009 to 2013, Dr. Henderson served as the director of broadband products and later as the director of product management, for the Public Safety and Professional Communications Division of Harris Corporation. Prior to Harris Corporation, Dr. Henderson held various management and R&D/product development positions at TriQuint Semiconductor, IBM, and M/A-COM.

Dr. Henderson earned a B.S. in electrical engineering from Texas Tech University and was granted a Ph.D. in electrical engineering from the Georgia Institute of Technology. He holds seven patents in wireless communications and semiconductor technologies and has published over 20 conference and journal papers.



Plenary Speaker 2

Dr. Ir. Michael Peeters
Program Director
Connectivity+Humanized Technology
imec

Do the Networks of the Future Care About the Materials of the Past?

Abstract: The traffic in today's networks, 4G, 5G, mobile or otherwise, seems to be following nicely the exponential expectations projected each year. On the one hand, this is driven by and drives further CMOS scaling for the digital processing of information; on the other hand, this has pushed communication channels to use ever wider bandwidths. Unfortunately, not only the individual endpoint throughputs are increasing, but the amount of endpoints and their capabilities is skyrocketing as well. Moreover, capacity as a KPI is being complemented by reliability and latency as use-cases branch out beyond the traditional human-centric communications and entertainment into areas such as industrial automation, AR/VR and autonomous vehicles.

This is creating a perfect storm at the interface of the analog and digital worlds, where traditional scaling does not necessarily buy you performance; physical dimensions are dictated not by atom sizes but by quarter-wavelengths of one kind or another; and speeds seem to all be converging at a point where switching frequencies venture far into the super-100GHz territory. For the first time in history, this is true for chip-to-chip, board-to-board, rack-to-rack, datacenter-to-datacenter, fiber and mobile wireless access systems.

Across the design space, this (finally!) has generated renewed interest into solution spaces that are less obvious, or were considered distinctly niche only a couple of years ago. We take a look at how we can tackle this, not only from an RFIC circuit design space, but also how new network capacity, reliability and latency requirements can drive technology choices for the next 10 years. This includes novel design and integration options for III-V, more exotic telluride and graphene approaches, but also dielectrics, ceramics and nanostructured materials.

About Dr. Ir. Michael Peeters

A passionate leader with a background in both research and strategy, Dr. Ir. Michael Peeters is Program Director Connectivity+Humanized Technology at imec. Michael has been identifying and implementing state-of-the-art technology opportunities in telecommunications through a career that spans two decades.

Both as Head of the Nokia Incubator and the Innovation Portfolio at Nokia, as well as CTO for the Wireless Division at Alcatel-Lucent, his role required him to make sense out of the uncertainty that exists when technological possibilities have to be balanced with business case realities. His team's responsibility: to see beyond the business analysis and help customers envision how emerging technologies and trends, such as 5G and AI, will impact their networks and end-user community.

Prior to his role as CTO for the Wireless Division, he was CTO for the Wireline Division. The team looked beyond the product roadmap and identified what new trends, technologies and tools were on the horizon and determined how those future opportunities fit into the Alcatel-Lucent pipeline. It was also during this period that the business commercialized VDSL2 Vectoring, an idea conceived 7 years earlier while leading the Bell Labs Access Nodes and DSL Technology department.

He has authored more than 100 peer-reviewed publications, many white papers and holds patents in the access and photonics domains. Michael earned a Ph.D. in Applied Physics and Photonics from Vrije Universiteit Brussel as well as a master's degree in Electrotechnical Engineering.

Outside of work, Michael is passionate about cooking and continues to refine the recipe for the perfect lasagna, balanced by bouts of long-distance running to offset the caloric intake inherent with such a quest.

The Industry Showcase

Chair: Domine Leenaerts, NXP Semiconductors

The RFIC Industry Showcase Session, held concurrently with the plenary reception, will highlight the 10 outstanding paper finalists listed below, submitted by authors from the industry. In this interactive session, authors will present their innovative work in poster format, and some will also show a demonstration. These 10 paper finalists were nominated by the RFIC Technical Program Committee to enter the final contest and a committee of eleven judges have selected the top three among them after rigorous reviews and discussions. The top three will be announced during the RFIC Plenary Session preceding the Industry Showcase, and each winner will receive a plaque. This year's Industry Paper Award finalists are:

An 802.11ba 495μW -92.6dBm-Sensitivity Blocker-Tolerant Wake-Up Radio Receiver Fully Integrated with Wi-Fi Transceiver

¹Intel, USA, ²Intel, Mexico

Renzhi Liu¹, Asma Beevi K.T.¹, Richard Dorrance¹, Deepak Dasalukunte¹, Mario A. Santana Lopez², Vinod Kristem¹, Shahrmaz Azizi¹, Minyoung Park¹, Brent R. Carlton¹

Reconfigurable 60-GHz Radar Transmitter SoC with Broadband Frequency Tripler in 45nm SOI CMOS

IBM T.J. Watson Research Center, USA

Wooram Lee, Tolga Dinc, Alberto Valdes-Garcia

22nm Fully-Depleted SOI High Frequency Noise Modeling up to 90GHz Enabling Ultra Low Noise Millimetre-Wave LNA Design

¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, USA, ³Research Foundation CUNY, USA

L.H.K. Chan¹, S.N. Ong¹, W.L. Oo¹, K.W.J. Chew¹, Chi Zhang², Abdellatif Bellaouar², W.H. Chow¹, T. Chen², R. Rassel², J.S. Wong¹, C.K. Lim¹, C.W.F. Wan¹, J. Kim¹, W.H. Seet¹, David L. Harames³

A 26dBm 39GHz Power Amplifier with 26.6% PAE for 5G Applications in 28nm Bulk CMOS

Intel, USA

Kaushik Dasgupta, Saeid Daneshgar, Chintan Thakkar, James Jaussi, Bryan Casper

Direct Digital Synthesizer with 14GS/s Sampling Rate Heterogeneously Integrated in InP HBT and GaN HEMT on CMOS

BAE Systems, USA

Steven Eugene Turner, Mark E. Stuenkel, Gary M. Madison, Justin A. Cartwright, Richard L. Harwood, Joseph D. Cali, Steve A. Chadwick, Michael Oh, John T. Matta, James M. Meredith, Justin M. Byrd, Lawrence J. Kushner

Excellent 22FDX Hot-Carrier Reliability for PA Applications

¹GLOBALFOUNDRIES, USA, ²GLOBALFOUNDRIES, Germany, ³GLOBALFOUNDRIES, Singapore

T. Chen¹, Chi Zhang¹, W. Arfaoui², Abdellatif Bellaouar¹, S. Embabi¹, G. Bossu², M. Siddabathula², K.W.J. Chew³, S.N. Ong³, M. Mantravadi¹, K. Barnett¹, J. Bordelon¹, R. Taylor¹, S. Janardhanan¹

A 1.04–4V, Digital-Intensive Dual-Mode BLE 5.0/IEEE 802.15.4 Transceiver SoC with Extended Range in 28nm CMOS

¹Samsung, Korea, ²Samsung, USA

Nam-Seog Kim¹, Myoung-Gyun Kim¹, Ashutosh Verma², Gyungseon Seol¹, Shinwoong Kim¹, Seokwon Lee¹, Chilun Lo¹, Jaeyeol Han¹, Ikkyun Jo¹, Chulho Kim¹, Chih-Wei Yao², Jongwoo Lee¹

A High Efficiency 39GHz CMOS Cascode Power Amplifier for 5G Applications

Samsung, Korea

Hyun-chul Park, Byungjoon Park, Yunsung Cho, Jaehong Park, Jihoon Kim, Jeong Ho Lee, Juho Son, Kyu Hwan An, Sung-Gi Yang

A Low Power Fully-Integrated 76–81GHz ADPLL for Automotive Radar Applications with 150MHz/ μ s FMCW Chirp Rate and -95dBc/Hz Phase Noise at 1MHz Offset in FDSOI

¹GLOBALFOUNDRIES, USA, ²Mantric Technology, Canada

Ahmed R. Fridi¹, Chi Zhang¹, Abdellatif Bellaouar¹, Man Tran²

X-Band NMOS and CMOS Cross-Coupled DCO's with a "Folded" Common-Mode Resonator Exhibiting 188.5dBc/Hz FoM with 29.5% Tuning Range in 16-nm CMOS FinFet

Intel, Israel

R. Levinger, D. Ben-Haim, I. Gertman, S. Bershansky, R. Levi, J. Kadry, G. Horovitz

Industry Paper Contest Eligibility: The first author must have an industry affiliation. The first author must also be the lead author of the paper and must present the paper at the symposium.

The Student Paper Award Finalists Showcase

Chair: Osama Shana'a, MediaTek

The RFIC Symposium's Student Paper Award is devised to encourage student paper submissions to the conference as well as to give the authors of the finalist papers a chance to promote their research work with the conference attendees after the plenary session during the reception time. Twelve outstanding student paper finalists were nominated this year by the RFIC Technical Program Committee to enter the final contest. A committee of eleven judges selected the top three papers after rigorous reviews and discussions. All finalists benefit from a complimentary RFIC registration. The top three Student Papers will be announced during the RFIC Plenary Session, and each winner will receive an honorarium and a plaque. This year's Student Paper Award finalists are:

A 4×4×4-mm³ Fully Integrated Sensor-to-Sensor Radio Using Carrier Frequency Interlocking IF Receiver with -94dBm Sensitivity

Li-Xuan Chuo¹, Yejoong Kim¹, Nikolaos Chiotellis¹, Makoto Yasuda², Satoru Miyoshi³, Masaru Kawaminami², Anthony Grbic¹, David Wentzloff¹, Hun-Seok Kim¹, David Blaauw¹

¹University of Michigan, USA, ²Mie Fujitsu Semiconductor, Japan, ³Fujitsu Electronics, USA

A 24–43GHz LNA with 3.1–3.7dB Noise Figure and Embedded 3-Pole Elliptic High-Pass Response for 5G Applications in 22nm FDSOI

Li Gao, Gabriel M. Rebeiz

University of California, San Diego, USA

A 77dB-SFDR Multi-Phase-Sampling 16-Element Digital Beamformer with 64 4GS/s 100MHz-BW Continuous-Time Band-Pass $\Delta\Sigma$ ADCs

Rundao Lu, Sunmin Jang, Yun Hao, Michael P. Flynn

University of Michigan, USA

A Sub-mW All-Passive RF Front End with Implicit Capacitive Stacking Achieving 13dB Gain, 5dB NF and +25dBm OOB-IIP3

Vijaya Kumar Purushothaman, Eric Klumperink, Berta Trullas Clavera, Bram Nauta

University of Twente, The Netherlands

Enhanced Passive Mixer-First Receiver Driving an Impedance with 40dB/Decade Roll-Off, Achieving +12dBm Blocker-P1dB, +33dBm IIP3 and Sub-2dB NF Degradation for a 0dBm Blocker

Sashank Krishnamurthy, Ali M. Niknejad

University of California, Berkeley, USA

A Quadrature Class-G Complex-Domain Doherty Digital Power Amplifier

Shih-Chang Hung, Si-Wook Yoo, Sang-Min Yoo

Michigan State University, USA

A Coupler-Based Differential Doberty Power Amplifier with Built-In Baluns for High mm-Wave Linear-Yet-Efficient Gbit/s Amplifications

Huy Thong Nguyen, Hua Wang
Georgia Tech, USA

A 350mV Complementary 4–5GHz VCO Based on a 4-Port Transformer Resonator with 195.8dBc/Hz Peak FOM in 22nm FDSOI

Omar El-Aassar, Gabriel M. Rebeiz
University of California, San Diego, USA

A 39GHz 64-Element Phased-Array CMOS Transceiver with Built-In Calibration for Large-Array 5G NR

Yun Wang¹, Rui Wu¹, Jian Pang¹, Dongwon You¹, Ashbir Aviat Fadila¹, Rattanan Saengchan¹, Xi Fu¹, Daiki Matsumoto¹, Takeshi Nakamura¹, Ryo Kubozoe¹, Masaru Kawabuchi¹, Bangan Liu¹, Haosheng Zhang¹, Junjun Qiu¹, Hanli Liu¹, Wei Deng¹, Naoki Oshima², Keiichi Motoi², Shinichi Hori², Kazuaki Kunihiro², Tomoya Kaneko², Atsushi Shirane¹, Kenichi Okada¹

¹Tokyo Institute of Technology, Japan, ²NEC, Japan

A 24.5–43.5GHz Compact RX with Calibration-Free 32–56dB Full-Frequency Instantaneously Wideband Image Rejection Supporting Multi-Gb/s 64-QAM/256-QAM for Multi-Band 5G Massive MIMO

Min-Yu Huang¹, Taiyun Chi², Fei Wang¹, Sensen Li¹, Tzu-Yuan Huang¹, Hua Wang¹
¹Georgia Tech, USA, ²Speedlink Technology, USA

A 51.5–64.5GHz Active Phase Shifter Using Linear Phase Control Technique with 1.4° Phase Resolution in 65-nm CMOS

Tianjun Wu, Chenxi Zhao, Huihua Liu, Yunqiu Wu, Yiming Yu, Kai Kang
UESTC, China

A 6.5-GHz Cryogenic All-Pass Filter Circulator in 40-nm CMOS for Quantum Computing Applications

Andrea Ruffino¹, Yatao Peng¹, Fabio Sebastiano², Masoud Babaie², Edoardo Charbon¹
¹EPFL, Switzerland, ²Technische Universiteit Delft, The Netherlands

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must also be the lead author of the paper and must present the paper at the Symposium.

Monday 3 June 2019

08:00–09:40

252AB

Session RMo1A: RF Receiver Building Blocks

Chair: Edmund Balboni, Analog Devices

Co-Chair: Domine Leenaerts, NXP Semiconductors

RMo1A-1 08:00

A 1.2–2.8GHz Tunable Low-Noise Amplifier with 0.8–1.6dB Noise Figure

Hao Gao, Zhe Song, Zhe Chen, Domine M.W. Leenaerts, Peter G.M. Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents a tunable wideband low-noise amplifier (LNA) covering 1.2 to 2.8 GHz and is realized in a 0.25 μm SiGe:C BiCMOS technology. The LNA covers 80% fractional bandwidth in 16 states using a dual-LC tanks input broadband noise matching technique and a switch capacitor output frequency selection network. The measured minimal noise figure (NF) is 0.8 dB at 1.4 and 1.8 GHz, and the average NF is 1.2 (± 0.4) dB from 1.2 to 2.8 GHz. The best gain is 14 dB at 2 GHz and with ± 0.5 dB flatness bandwidth covers from 1.4 GHz to 2.6 GHz. The measured input 1-dB compression point and input IP₃ are better than -8 dBm and 3.5 dBm, respectively.

RMo1A-2 08:20

A 28-GHz CMOS LNA with Stability-Enhanced G_m -Boosting Technique Using Transformers

Sunwoo Kong, Hui-Dong Lee, Seunghyun Jang, Jeehoon Park, Kwang-Seon Kim, Kwang-Chun Lee; ETRI, Korea

Abstract: In this paper, we propose a low noise amplifier (LNA) using a g_m -boosting technique with improved stability using transformers in the millimeter-wave (mm-Wave) band. The transformer composed of three inductors improves not only stability, but also gain and low-noise performance of the LNA. The conditions for stability shows that the proposed structure can guarantee good stability over a high frequency range. The chip was fabricated using the TSMC 65-nm CMOS process and it has an active chip area of 0.11 μm^2 . The fabricated LNA has a gain of 18.33 dB and a noise figure (NF) of 3.25–4.2 dB. The stability factor μ values are 9.7 and 5.2 at the source and load sides of the LNA, respectively. The 3-dB bandwidth of the LNA is 24.9–32.5 GHz and the chip consumes 17.1-mA current from a 1.2-V supply.

RMo1A-3 08:40

Ka-Band CMOS Absorptive SP4T Switch with One-Third Miniaturization

Bosung Suh, Byung-Wook Min; Yonsei University, Korea

Abstract: An Ka-band absorptive single-pole four-throw (SP4T) switch in 28-nm CMOS process is presented. By capacitive matching and loading method, only four $\lambda/6$ transmission lines (t-line) are used for the proposed switch without additional series switches. The length of the t-line used in the proposed switch is only 1/3 of that of the quarter-wave t-line based absorptive switch. To improve switch performance, low threshold-voltage transistors and source and drain of transistors are biased for power handling capability. The measured insertion loss and isolation are 3.5 dB and 20 dB at 28 GHz. Return losses of on-state and off-state ports are less than -10 dB and -16 dB from 26 GHz to 33 GHz. The measured input 1-dB compression point is more than 15 dBm. The chip area is 0.53 mm^2 and electrical size is $0.0047 \times (\lambda_g)^2$ excluding pads and internal matching circuits that is the smallest electrical size among the millimeter-wave CMOS absorptive SP4T switches.

RMo1A-4 09:00

A Compact, High-Power, 60GHz SPDT Switch Using Shunt-Series SiGe PIN Diodes

Yunyi Gong, Jeffrey W. Teng, John D. Cressler; Georgia Tech, USA

Abstract: This work describes the design of a compact, 60 GHz, SPDT switch implemented using PIN diodes in a 130 nm SiGe BiCMOS technology. The SPDT RF switch employs a novel shunt-series topology with a resistive biasing scheme to “self-reverse-bias” the off-state shunt diode, thereby improving power handling capability of the SPDT. A coupled inductor matching network is used to minimize the switch size. The proposed design achieves a minimum insertion loss of 2.0 dB, more than 26 dB of isolation, and input-referred P1dB (at 60 GHz) of 22 dBm, with a $0.20 \times 0.33 \text{ mm}^2$ footprint.

Monday 3 June 2019

08:00–09:40

254AB

**Session RMo1B: Advanced Devices, Characterization, and Modeling
for Millimeter-Wave Applications**

Chair: Alvin Joseph, GLOBALFOUNDRIES

Co-Chair: Edward Preisler, TowerJazz

RMo1B-1 08:00

**Low-Cost, High-Gain Antenna Module Integrating a CMOS Frequency
Multiplier Driver for Communications at D-Band**

Francesco Foglia Manzillo, José Luis Gonzalez-Jimenez, Antonio Clemente, Alexandre Siligaris,
Benjamin Blampey, Cedric Dehos; CEA-Leti, France

Abstract: This paper presents a compact D-band antenna module for ultrafast short-range communications. The system comprises a planar lens fed by an antenna-in-package embedding an integrated 28-nm bulk CMOS frequency multiplier. Both lens and primary source are fabricated using low-cost printed circuit board (PCB) technology. The module achieves a peak gain of 25 dBi and works between 114 GHz and 138 GHz with a gain drop lower than 3 dB. The proposed solution paves the way for low-loss and low-profile wireless systems entirely integrated in planar multilayer substrate modules.

RMo1B-2 08:20

**Scalable Analytical Model of 1.7THz Cut-Off Frequency Schottky Diodes
Integrated in 55nm BiCMOS Technology**

Vincent Gidel¹, Frédéric Giancesello¹, Pascal Chevalier¹, Grégory Avenier¹, Nicolas Guitard¹,
Victor Milon¹, Michel Buczko¹, Charles-Alex Legrand¹, Cyril Luxey², Guillaume Ducournau³;
¹STMicroelectronics, France, ²Polytech'Lab (EA 7498), France, ³IEMN (UMR 8520), France

Abstract: In this paper, an innovative Schottky diode architecture is proposed and implemented in 55 nm BiCMOS technology. A State-of-the-art 1.7 THz cut-off frequency is measured and an analytical scalable model is proposed and experimentally validated paving the way for further performance improvement. In addition, this analytical model can be integrated in a Design Kit library in order to enable sub-THz Schottky diode-based circuit designs in advanced BiCMOS.

RMo1B-3 08:40

Excellent 22FDX Hot-Carrier Reliability for PA Applications

T. Chen¹, Chi Zhang¹, W. Arfaoui², Abdellatif Bellaouar¹, S. Embabi¹, G. Bossu², M. Siddabathula², K.W.J. Chew³, S.N. Ong³, M. Mantravadi¹, K. Barnett¹, J. Bordelon¹, R. Taylor¹, S. Janardhanan¹; ¹GLOBALFOUNDRIES, USA, ²GLOBALFOUNDRIES, Germany, ³GLOBALFOUNDRIES, Singapore

Abstract: This work shows the excellent HCI (hot-carrier injection) reliability that 22FDX demonstrates for mmWave PA applications. The underlying device physics to explain this performance are also shown. Due to the fact that fully depleted SOI (FDSOI) eliminates the lateral bipolar device, the MOSFETs in 22FDX technology have an increased BVDSs when compared to a device in a partially depleted SOI (PDSOI) technology. A 2-stack PA is presented that demonstrates excellent reliability against all HCI stress. The device aging model is built based on the device stress data specific for PA applications. RelXpert is used to simulate device aging based on the model and suggests excellent PA reliability even under the worst mismatch condition.

RMo1B-4 09:00

22nm Fully-Depleted SOI High Frequency Noise Modeling up to 90GHz Enabling Ultra Low Noise Millimetre-Wave LNA Design

L.H.K. Chan¹, S.N. Ong¹, W.L. Oo¹, K.W.J. Chew¹, Chi Zhang², Abdellatif Bellaouar², W.H. Chow¹, T. Chen², R. Rassel², J.S. Wong¹, C.K. Lim¹, C.W.F. Wan¹, J. Kim¹, W.H. Seet¹, David L. Harame³; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, USA, ³Research Foundation CUNY, USA

Abstract: This paper reports the high frequency (HF) noise characterized performance and modeling on 22nm FD-SOI technology transistor (GLOBALFOUNDRIES' 22FDX technology) from 2 GHz to the maximum E-band millimetre-Wave (mmWave) frequency of 90 GHz. The measurement was performed using the Focus Microwaves noise system with different customised setups and optimised for each discrete frequency bands. The data measured from each frequency bands were subsequently combined to produce the noise spectrum covering from 2 GHz to 90 GHz, with high accuracy, good continuity and excellent correlation to the compact model. The 22FDX technology transistor demonstrated very low mmWave noise figure, which is favourable for RF and mmWave applications such as LNA.

RMo1B-5 09:20

22nm Ultra-Thin Body and Buried Oxide FDSOI RF Noise Performance

Ousmane M. Kane¹, Luca Lucci¹, Pascal Scheiblin¹, Sylvie Lepilliet², François Danneville²; ¹CEA-Leti, France, ²IEMN (UMR 8520), France

Abstract: The drastic downscaling of the transistor size along with advances in material sciences allowed the development of low power CMOS technologies with competitive RF figure of merits suitable for millimeter applications. In this context, this paper presents the RF and noise characterization (up to 110 GHz) of an advanced 22 nm UTBB FDSOI technology developed by Globalfoundries. In addition to the excellent DC performance, the technology presents promising RF characteristics. Indeed, a maximum transconductance of 1.78 S/mm and a F_{\max} of 435 GHz are achieved. The technology also offers a state-of-the-art minimum noise figure (NF_{\min}) of 0.45 dB at 20 GHz (with an associated Gain of 13 dB) for a drain current of 185 mA/mm.

Monday 3 June 2019

08:00–09:40

257AB

Session RMo1C: Millimeter-Wave Radar and Imaging Systems

Chair: Shahriar Shahramian, Nokia Bell Labs

Co-Chair: Jane Gu, University of California, Davis

RMo1C-1 08:00

A 76–81GHz FMCW Transceiver with 3-Transmit, 4-Receive Paths and 15dBm Output Power for Automotive Radars

Zongming Duan¹, Dongfang Pan¹, Bowen Wu², Yan Wang², Bingbing Liao², Dong Huang³, Yanhui Wu⁴, Daiguo Xu⁴, Hua Xu⁴, Wei Lv², Yuefei Dai², Pei Li², Yan Wang³, Fujiang Lin¹; ¹USTC, China, ²ECRIIE, China, ³Tsinghua University, China, ⁴CETC 24, China

Abstract: A fully-integrated 76–81GHz FMCW transceiver in 65-CMOS is presented for automotive radar applications. The transceiver consists of 3-transmitter, 4-receiver, FMCW synthesizer and ADC with decimation filters. The transmitter, with a TX chain including a push-push doubler, a 3-stage power amplifier employing neutralization technique and 2 power-combined topologies, shows an output power of 15dBm. The receiver, with an LNA employing a 3-stage neutralized common source (CS) with inductive degeneration, achieves a noise figure of 15dB, an input P-1dB of -20dBm, and an ENOB of 10.2-b for ADC. The double tuning modulated PLL provides FMCW waveform with -81dBc/Hz phase noise at 1MHz offset and chirp rate of 50MHz/μs. The power consumption of the entire transceiver is 1.06W.

RMo1C-2 08:20

Reconfigurable 60-GHz Radar Transmitter SoC with Broadband Frequency Tripler in 45nm SOI CMOS

Wooram Lee, Tolga Dinc, Alberto Valdes-Garcia; IBM T.J. Watson Research Center, USA

Abstract: A reconfigurable 60-GHz radar transmitter with a broadband frequency tripler is proposed to support CW/FMCW, pulse, and PMCW radar waveforms from a single front-end. The proposed IC consists of a wide-band frequency tripler, a two-stage driver, two power mixers with baseband circuitry and serial I/O circuitry. The IC measurements in CW mode operation show an output power of 12.8 dBm (average) and 14.7 dBm (peak) from 54 GHz to 67 GHz with harmonic suppression greater than 27 dB. Pulse and PMCW mode operations are also demonstrated to generate short pulses with the minimum pulse width of 25 ps corresponding to 40 GHz signal bandwidth and 10-Gb/s PRBS modulated signals, respectively. Fabricated in a 45-nm CMOS SOI process, the IC consumes 0.51 W and occupies an active area of 1.95 mm² excluding pads.

RMo1C-3 08:40

A 94GHz 2×2 Phased-Array FMCW Imaging Radar Transceiver with 11dBm Output Power and 10.5dB NF in 65nm CMOS

Dong Huang¹, Li Zhang¹, Huabing Zhu², Boshen Chen², Yang Tang², Yan Wang¹, ¹Tsinghua University, China, ²CAEP, China

Abstract: This paper presents a 94GHz 2×2 phased-array frequency-modulated continuous wave (FMCW) imaging radar transceiver. The transceiver consists of two receiving paths, two transmitting paths and a local oscillator (LO) generation path. In order to improve gain and noise performance, multi-paralleled transistors with small number-of-fingers are used to design power amplifier (PA) and low noise amplifier (LNA). A 24GHz voltage-controlled oscillator (VCO) is used to generate wideband FMCW signals, and two differential push-push cascode doublers are used to act as a quadrupler, which has a low power and high stability. Phase shifter (PS) with constant insertion loss (IL) compensation is used to achieve constant gain among different phase states. The LO path has a continuous frequency tuning range of 14GHz. The transmitter has a maximum output power of 11 dBm and 2.8dB power flatness over 14GHz bandwidth. The receiver has a conversion gain of 20dB and a noise figure (NF) of 10.5dB.

RMo1C-4 09:00

X/Ku-Band Four-Channel Transmit/Receive SiGe Phased-Array IC

Prabir Saha, Sriram Muralidharan, Jinzhou Cao, Ozan Gurbuz, Christopher Hay; Analog Devices, USA

Abstract: This paper presents a phased-array core chip integrating four transmit/receive channels and supporting circuitry on a single chip working over 8–16 GHz, covering X and Ku frequency bands. Each RX and TX channel has a VGA and a phase shifter featuring precise amplitude and phase control for RF beamforming. The phase-compensated VGA provides 16 dB of gain control range in 0.5 dB steps while limiting the corresponding phase variation to 3°. The phase shifter, based on the principles of a vector modulator, provides 360° phase control range with resolution better than 2.8°, rms phase and gain error less than 2.8° and 0.3 dB respectively. Each RX channel has more than 10 dB of gain, and the noise figure for maximum gain condition is better than 10 dB. In receive mode, input P1dB is -16 dBm per channel and in transmit mode, output P1dB is greater than 9 dBm over 8–16 GHz. Each RX and TX channel draws 65 mA and 85 mA respectively from a 3.3 V supply. The chip, fabricated in a 0.18μm SiGe BiCMOS technology, occupies 4mm × 4mm and was put in a 7mm × 7mm LGA package.

Ultra-Wideband 8–45GHz Transmitter Front-End for a Reconfigurable FMCW MIMO Radar

Mantas Sakalas, Songhui Li, Niko Joram, Paulius Sakalas, Frank Ellinger; Technische Universität Dresden, Germany

Abstract: This paper presents an ultra-wideband 8–45 GHz FMCW MIMO radar transmitter (Tx) front-end, designed in a 130 nm SiGe BiCMOS technology. Various design techniques were applied to achieve the ultra-wide bandwidth, high linearity and the output power, which is at the edge for the given technology. The measured output power at 1 dB compression point was 15–20 dBm in a frequency range of 8–45 GHz and 3 dB output power flatness of 17–20 dBm was achieved for a 9–41 GHz bandwidth. The compact design features a total active IC area of 2.72 mm² and a peak overall system PAE of 9%. The total DC power consumption was 1.45 W.

Monday 3 June 2019

10:10–11:50

252AB

Session RMo2A:

5G and Millimeter-Wave Beamforming Building Blocks

Chair: Ruonan Han, MIT

Co-Chair: Abdellatif Bellaouar, GLOBALFOUNDRIES

RMo2A-1 10:10

A 51.5–64.5GHz Active Phase Shifter Using Linear Phase Control Technique with 1.4° Phase Resolution in 65-nm CMOS

Tianjun Wu, Chenxi Zhao, Huihua Liu, Yunqiu Wu, Yiming Yu, Kai Kang; UESTC, China

Abstract: This paper presents a V-band active phase shifter using proposed linear phase control technique with 1.4° phase step in 65-nm CMOS technology. Different from conventional active phase shifter, the linear phase control technique achieves a linear relationship between output phase and control signals. It makes the control of output phase more accurate and greatly improves the phase resolution. Furthermore, a current-reuse technique is used to improve gain in mm-wave frequency. The measurement results show that the measured 3-dB bandwidth of 51.5 – 64.5 GHz is achieved. The measured RMS phase error of 8-bit phase resolution is 0.5° – 1.2° in 3-dB bandwidth and the measured RMS gain variation error is 0.17 – 0.25 dB. The measured input-referred P1dB at maximum gain phase states is -5 dBm. The chip consumes 16.9 mA from 1.2 V voltage supply and the core area of the phase shifter is 720 $\mu\text{m} \times 560 \mu\text{m}$.

RMo2A-2 10:30

Digitally-Assisted 27–33GHz Reflection-Type Phase Shifter with Enhanced Accuracy and Low IL-Variation

Jingjing Xia, Mahitab Farouk, Slim Boumaiza; University of Waterloo, Canada

Abstract: This paper presents a new millimeter-wave 360° digitally-assisted reflection-type phase shifter (DA-RTPS). It is composed of a cascade of three compact, low-loss and fully-differential transformer-based hybrid couplers with two of their ports terminated by switch-controlled capacitor banks. Each stage is configured to produce a phase change of up to 60°. An additional phase inverting stage is used to attain 360° of phase shift. The proposed DA-RTPS arrangement enabled low insertion loss (IL) variation and enhanced phase accuracy compared to single-stage RTPS-based typologies. A proof-of-concept prototype, implemented using 45nm silicon-on-insulator CMOS technology, demonstrated a 1-dB RF bandwidth spanning from 27 to 33 GHz, a low root-mean-square phase error of 0.3°, and an IL of 6.8 dB \pm 0.25dB, while covering 360° of phase shift at 5.6° resolution. Furthermore, it maintained a group delay below $\pm 12\text{ps}$ and an input 1dB compression point >7.3 dBm at all phase-shift settings between 27 and 33 GHz.

RMo2A-3 10:50

A 21 to 30-GHz Merged Digital-Controlled High Resolution Phase Shifter-Programmable Gain Amplifier with Orthogonal Phase and Gain Control for 5-G Phase Array Application

Wei Zhu¹, Wei Lv², Bingbing Liao², Yanping Zhu², Yuefei Dai², Pei Li², Lei Zhang¹, Yan Wang¹;

¹Tsinghua University, China, ²ECRIIE, China

Abstract: This paper presents a 21 to 30-GHz merged passive vector sum phase shifter (PS) and programmable gain amplifier (PGA) with sub-degree phase resolution for 5-G phased array application. In PS, a transformer-based full-differential high-order resonant coupler functions as a quadrature generator (QG) with a novel layout strategy to achieve broad bandwidth, low loss, and accurate quadrature phase within only one inductor-footprint. Compared to the conventional transformer-based fourth order resonant coupler, the proposed resonant coupler with higher order features much wider quadrature bandwidth. Two phase invariant 6-bit binary-weighted arrays of vector modulators scale the quadrature signals to achieve the desired high resolution vector phase interpolation. In PGA, a phase invariant and dB-linear gain is achieved by adopting a “fractional-bit-based” PGA design. The chip prototype is fabricated in a 65-nm CMOS process, this implementation achieves 43% fractional BW_{-3dB} (20 to 31-GHz). The phase control operates with 0.8° steps while maintaining a minimum RMS phase error of 0.42°, demonstrating the best phase accuracy when compared to state-of-the-art mm-wave PSs.

RMo2A-4 11:10

A 20–43GHz VGA with 21.5dB Gain Tuning Range and Low Phase Variation for 5G Communications in 65-nm CMOS

Tianjun Wu, Chenxi Zhao, Huihua Liu, Yunqiu Wu, Yiming Yu, Kai Kang; UESTC, China

Abstract: This paper presents a broadband variable gain amplifier (VGA) with low phase variation in 65 nm CMOS technology. The mechanism of phase variation in CMOS VGA is analyzed. According to the analysis, the feedforward paths formed by parasitic capacitive and inductive couplings are one of the main factors that result in phase variation in CMOS VGA. In order to achieve low phase variation, a parasitic capacitor elimination technique is proposed to remove the feedforward path formed by gate-drain parasitic capacitor. Besides, an isolation enhancement layout technique is proposed to minimize the inductive coupling and parasitic capacitors in the layout of the variable gain stage. As results, the measured phase variation is 0.2° – 2° in 18 GHz – 37 GHz and 0.2° – 5.4° in 18 GHz – 45 GHz when the gain variation range is 21.5 dB. The measured peak gain is 14.5 dB with 3-dB bandwidth of 20 GHz – 43 GHz. The gain ripple in 3-dB bandwidth is < 2.5 dB. The noise figure and input-referred P1dB are 5.5 dB and -16.5 dBm in the maximum gain state, respectively. The chip consumes 30.8 mW from 1.1 V voltage supply and the core area is 370 μm × 930 μm.

A 26-GHz Vector Modulator in 130-nm SiGe BiCMOS Achieving Monotonic 10-b Phase Resolution without Calibration

Ilker Kalyoncu¹, Abdurrahman Burak¹, Mehmet Kaynak², Yasar Gurbuz¹; ¹Sabanci University, Turkey, ²IHP, Germany

Abstract: This paper presents a high-resolution (10-b) vector-modulator (VM) phase shifter (PS) in 130-nm SiGe BiCMOS targeting 5G applications at 26 GHz. It employs a Gilbert-cell RF core, the tail current of which is controlled by an 8-b low-power current-steering DAC and 2-b I/Q sign switches. The DAC includes an on-chip PTAT current reference with process compensation capabilities. A 2-stage RC polyphase filter (PPF) is used to generate the quadrature signals. Without any calibration or correction of PS control signals, the measured results demonstrate completely monotonic 2^{10} phase states, covering the full 0–360° range without any dead zones or overlapping phase states. The worst case (maximum) phase difference between any adjacent states is 0.65°. The VM exhibits an average insertion loss of 0.5 dB at 26 GHz with a 3-dB BW of 8 GHz, an rms amplitude error of 0.2 dB, IP_{1dB} of 2 dBm, and 23 mW dc power dissipation. Potential applications are in RF beamforming and RF self-interference cancellation.

Monday 3 June 2019

10:10–11:50

254AB

Session RMo2B:

Digitally Assisted Front-Ends for Emerging Wireless Applications

Chair: Debopriyo Chowdhury, Broadcom

Co-Chair: Oren Eliezer, PHAZR

RMo2B-1 10:10

A 20–32GHz Digital Quadrature Transmitter with Notched-Matching and Mode-Switch Topology for 5G Wireless and Backhaul

Huizhen Jenny Qian, Yiyang Shu, Jie Zhou, Xun Luo; UESTC, China

Abstract: In this paper, a mm-wave wideband digital quadrature transmitter with improved efficiency for the 5G wireless and backhaul communication is presented. A novel synthesized notched-matching network is proposed to decrease the impedance mismatch from the interconnection of power digital-to-analog converter (power-DAC) cells operating at mm-wave bands. The performance is further optimized at the low- and high-bands by mode-switch of the quadrature signal generator, interstage matching of sign map, and power-DAC output-matching, simultaneously. Based on the mechanisms mentioned above, a 2×10 -bit digital quadrature transmitter operating at 20–32GHz is implemented and fabricated using a conventional 28-nm CMOS technology, which exhibits the saturated output power of 19.02dBm, 34.4% maximum drain efficiency, and maximum system efficiency of 22.1%, respectively. Such mm-wave transmitter can support 64QAM modulation signals with 3Gb/s data-rate, -28.9dB EVM, 9.96dBm output power, and -33.6dBc ACPR.

RMo2B-2 10:30

A Wideband Digital Polar Transmitter with Integrated Capacitor-DAC-Based Constant-Envelope Digital-to-Phase Converter

Tong Li, Liang Xiong, Yun Yin, Yangzi Liu, Hao Min, Na Yan, Hongtao Xu; Fudan University, China

Abstract: This paper presents a wideband digital polar transmitter (DPTX) with integrated capacitor-DAC-based constant-envelope digital-to-phase converter (DPC). The switched-capacitor DAC topology is adopted to improve the linearity. The harmonic rejection and cell-reused techniques are employed to reject the 3rd/5th-order harmonics and reduce the power consumption, respectively. The measurement results of DPC demonstrate the maximum INL and DNL of 1 and 0.8 degrees with the power consumption of 12.7mW@1.5GHz. The DPTX obtains the peak output power of 20.1dBm with 23.7% system efficiency and wideband frequency coverage over 1.2–2.5GHz with only 0.7dB power variation. When amplifying a 10MHz 64QAM LTE signal at 1.5GHz, it achieves -28.6dB EVM and 15.2% system efficiency at 15.0dBm average output power.

RMo2B-3 10:50

A 5GHz to 6GHz CMOS Transmitter for Full-Duplex Wireless with Wideband Digital Cancellation

Nimrod Ginzberg¹, Dror Regev², Genadiy Tsodik², Shimi Shilo², Doron Ezri², Emanuel Cohen¹;

¹Technion, Israel, ²Toga Networks, Israel

Abstract: This paper presents a quadrature balanced transmitter, assisted by a digital equalization and predistortion self-interference cancellation technique for Full-Duplex wireless applications. An analysis of design trade-offs between low receiver (Rx) loss and high transmitter (Tx) efficiency is laid out and demonstrated on a 5GHz to 6GHz class AB power amplifier implemented in 180nm CMOS. Wideband cancellation of >48dB and >57dB at 20dBm and 10dBm Tx output power, respectively, is measured in CW. Cancellation of >30dB for an actual 160MHz 802.11ac OFDM packet around a carrier frequency of 5.2GHz together with EVM of -33dB is demonstrated. Measured Tx power added efficiency (PAE) for concurrent Tx-SIC operation is 35% and 6.4% at peak and RMS (10dB backoff) power, respectively. Rx loss is lower than 1.6dB at RMS Tx power within the signal frequency band.

RMo2B-4 11:10

A Sub-mW All-Passive RF Front End with Implicit Capacitive Stacking Achieving 13dB Gain, 5dB NF and +25dBm OOB-IIP3

Vijaya Kumar Purushothaman, Eric Klumperink, Berta Trullas Clavera, Bram Nauta; University of Twente, The Netherlands

Abstract: This paper presents a sub-mW mixer-first RF front-end that exploits a novel capacitive stacking technique in an altered bottom-plate N-path filter/mixer to achieve passive voltage gain and high-linearity at low noise figure. Capacitive stacking is realized implicitly by reading out the voltage from the bottom-plate of N-path capacitors instead of their top-plate, which provides a $2\times$ gain at the read-out capacitors. Additional passive voltage gain is achieved using impedance upconversion while improving the out-of-band linearity performance of small switches. With no other active circuitry, only clock generation circuits determine the total power consumption of this RF front-end. A prototype is fabricated in GF22nm FDSOI technology. Operating at $f_{LO} = 1$ GHz, the prototype achieves a voltage gain of 13 dB, 5 dB Noise Figure and +25/+66dBm Out-of-band IIP3/IIP2 at 160MHz offset while consuming only 600 μ W of power from a 0.8V supply.

A 0.3-to-1.3GHz Multi-Branch Receiver with Modulated Mixer Clocks for Concurrent Dual-Carrier Reception and Rapid Compressive-Sampling Spectrum Scanning

Guoxiang Han, Tanbir Haque, Matthew Bajor, John Wright, Peter R. Kinget; Columbia University, USA

Abstract: A flexible RF receiver is introduced that uniquely uses CW-modulated clocks for the down-conversion mixers in its mixer-first and low-noise transconductance branches, thereby enabling tuned matching and reception concurrently at two RF carriers. Turning off the modulation reverts the receiver back to single-carrier operation, whereas using PN sequences to modulate the mixer clocks enables rapid, wideband compressive-sampling spectrum scanning. All three functions are accomplished within a single unified architecture. A prototype of the multi-branch modulated-mixer-clock receiver was developed in 65nm CMOS and operates from 0.3 to 1.3GHz. For single-carrier reception, the receiver delivers 15MHz RF bandwidth, 42dB conversion gain, 3.3dB NF, +3.3dBm B1dB, and +12.2dBm OB-IIP3. Concurrent dual-carrier reception at 500MHz and 900MHz offers -8.4dBm B1dB and <6dB NF. In rapid CS spectrum scanning mode, the receiver achieves 66dB dynamic range with -75dBm sensitivity over a 630MHz RF span within 0.71 μ s and consumes 18.5nJ per detected signal.

Monday 3 June 2019

10:10–11:50

257AB

Session RMo2C: RF-Inspired Emerging Technologies and Applications

Chair: Fabio Sebastiano, Technische Universiteit Delft

Co-Chair: Renyuan (Ryan) Wang, BAE Systems

RMo2C-1 10:10

A 0.5–20GHz RF Silicon Photonic Receiver with 120 dB•Hz^{2/3} SFDR Using Broadband Distributed IM3 Injection Linearization

Navid Hosseinzadeh, Aditya Jain, Kang Ning, Roger Helkey, James F. Buckwalter; University of California, Santa Barbara, USA

Abstract: Radio-over-fiber (RoF) supports microwave and millimeter-wave communication with remote antenna heads. However, RoF links suffer from low spur-free dynamic range (SFDR) due to the low gain and high nonlinearity of silicon photonic (SiP) Mach-Zehnder modulators (MZM). This work demonstrates the first distributed silicon-germanium (SiGe) HBT LNA co-designed for linearization of a broadband SiP-based RoF link. The SiGe LNA features a distributed LNA intermodulation (IM) injection scheme that is inherently wideband, improving IIP3 over a 10 GHz range. The assembled SiGe LNA and SiP MZM prototype demonstrates an SFDR as high as 120dB•Hz^{2/3} at 9 GHz, a 19 dB improvement over previous SiP RoF links.

RMo2C-2 10:30

A 65nm CMOS Continuous-Time Electro-Optic PLL (CT-EOPLL) with Image and Harmonic Spur Suppression for LIDAR

Ali Binaie, Sohail Ahasan, Harish Krishnaswamy; Columbia University, USA

Abstract: An integrated continuous-time electro-optic phase-locked loop (CT-EOPLL) is presented that features image and harmonic spur suppression, and is used in a frequency-modulated continuous-wave (FMCW) LIDAR. The proposed EOPLL has its loop bandwidth equal to its reference frequency, which enables it to relax the trade-off between chirp bandwidth and Mach-Zehnder (MZ) delay and consequently reduce the area and loss associated with the silicon-photonic delay implementation by 10×. Image and harmonic spurs are rejected through single-sideband (SSB) and harmonic-reject (HR) mixing techniques. This EO-PLL is integrated in 65nm CMOS technology, suppresses the highest spur by more than 25dB, and is used in a LIDAR system that can detect an object at ranges exceeding 3.3 meters with an RMS depth precision of 558μm at 2m distance and 9.4mm depth resolution.

RMo2C-3 10:50

A 6.5-GHz Cryogenic All-Pass Filter Circulator in 40-nm CMOS for Quantum Computing Applications

Andrea Ruffino¹, Yatao Peng¹, Fabio Sebastiano², Masoud Babaie², Edoardo Charbon¹; ¹EPFL, Switzerland, ²Technische Universiteit Delft, The Netherlands

Abstract: Cryogenic solid-state quantum processors require classical control and readout electronics; to achieve compactness and scalability, cryogenic integrated circuits have been recently proposed for this goal. Circulators are widely used in readout circuits, however they are typically discrete bulky devices, thus preventing miniaturization. To address this issue, we propose a fully integrated 40-nm CMOS 6.5-GHz circulator operating from 300K to 4.2 K. At 300 K, it achieves a 2.2-dB insertion loss, an 18-dB isolation, and a 2.4-dB noise figure over the 1-dB bandwidth from 5.6GHz to 7.4 GHz, with a core power of only 2.5mW. This improves to 2.1mW core power at 4.2 K, while showing 1.3-dB insertion loss and 17-dB isolation over the 1-dB bandwidth from 5.8 GHz to 7.6 GHz. The circuit achieves a record-low core power and a 1.6× wider fractional bandwidth than the state-of-the-art, thus allowing its use for multiple channels in power-constrained cryogenic refrigerators. These advances are enabled by a fully-passive architecture based on LC all-pass filters, allowing the use of a lower clock frequency than in prior art.

RMo2C-4 11:10

Design Considerations for Spin Readout Amplifiers in Monolithically Integrated Semiconductor Quantum Processors

M.J. Gong¹, U. Alakusu¹, S. Bonen¹, M.S. Dadash¹, Luca Lucci², H. Jia³, L.E. Gutierrez³, W.T. Chen³, D.R. Daughton⁴, G.C. Adam⁵, S. Iordănescu⁵, M. Pășteanu⁵, N. Messaoudi⁶, David L. Harame², A. Müller⁵, R.R. Mansour³, S.P. Voinigescu¹; ¹University of Toronto, Canada, ²GLOBALFOUNDRIES, Germany, ³University of Waterloo, Canada, ⁴Lake Shore Cryotronics, USA, ⁵IMT Bucharest, Romania, ⁶Keysight Technologies, Canada

Abstract: The high frequency performance of all active and passive devices in a production 22nm FDSOI CMOS technology was measured up to 40 GHz over temperature down to 3.3 Kelvin, targeting applications in cryogenic and quantum computing ICs. It was found that the quality factor of the passives and the f_T and f_{MAX} of both p- and n-MOSFETs improved at 3.3 K. More importantly for circuit design, the peak- f_T and peak- f_{MAX} current densities, and the MOM capacitor and polysilicon resistor values show no variance with temperature. This information and the measured I-V characteristics of electron and hole single- and double-quantum dot structures, measured at 2 K and representative of qubits, were used to design monolithically integrated double quantum dots with readout transimpedance amplifiers output matched to 50 Ω . Transimpedance gain, S_{21} , and bandwidth of 108 dB Ω , 19 dB, and 7.5 GHz, respectively, were measured at 300 K with only 4.5 mW power consumption and $S_{22} < -10$ dB up to 60 GHz.

Direct Digital Synthesizer with 14GS/s Sampling Rate Heterogeneously Integrated in InP HBT and GaN HEMT on CMOS

Steven Eugene Turner, Mark E. Stuenkel, Gary M. Madison, Justin A. Cartwright, Richard L. Harwood, Joseph D. Cali, Steve A. Chadwick, Michael Oh, John T. Matta, James M. Meredith, Justin M. Byrd, Lawrence J. Kushner; BAE Systems, USA

Abstract: A 14 GS/s direct digital synthesizer (DDS) heterogeneously integrated with InP and GaN on CMOS is presented. The DDS includes over 6 million 45 nm CMOS FETs, 2151 InP HBTs, 2 GaN HEMTs, and 9930 heterogeneous interconnects, making it the most complex heterogeneously integrated mixed-signal circuit reported to date. By heterogeneously integrating multiple technologies, a high output power of 6.9 dBm is achieved while maintaining better than 37 dBc Nyquist SFDR and 8.7 W power consumption — performance currently unachievable with state-of-the-art single-technology approaches.

Monday 3 June 2019

13:30–15:10

252AB

Session RMo3A: Millimeter-Wave Integrated Subsystems

Chair: Pierre Busson, STMicroelectronics

Co-Chair: Mona Hella, Rensselaer Polytechnic Institute

RMo3A-1 13:30

A 1V 54–64GHz 4-Channel Phased-Array Receiver in 45nm RFSOI with 3.6/5.1dB NF and -23dBm IP1dB at 28/37mW Per-Channel

Hyunchul Chung, Qian Ma, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a low-power, low-noise, high-linearity 4-channel phased-array receiver in 45 nm RFSOI process. An architecture employing an active low-noise balun, a 180° active phase-shifter, and 11/22/45/90° passive phase-shifters results in optimal performance between noise figure and power consumption. The phased-array front-end channel consumes 28 mW from a 1 V supply, with a measured gain and NF of 14 dB and 3.6 dB at 59 GHz, respectively (NF 3.6–4 dB at 57–64 GHz). The four front-end receive channels are followed by a high-linearity down-conversion mixer and an IF amplifier. The chip is flipped and placed on a low-cost printed circuit board (PCB) with matching network for connectorized measurement. The measured electronic gain of the phased array receiver is 20–21 dB with a 3-dB bandwidth of 54–64 GHz and NF of 5.1–5.4 dB at 57–64 GHz, with a system IP1dB of -23 dBm at 150 mW dc power. To author's knowledge, this work achieves the lowest NF and highest dynamic range with <40 mW Pdc/channel at 60 GHz band and enables the construction of a large arrays (256–1024 elements) with low power consumption.

RMo3A-2 13:50

A Fully Integrated 60GHz 10Gb/s QPSK Transceiver with Digital Transmitter and T/R Switch in 65nm CMOS

Zheng Song, Jianfu Lin, Yutian Li, Jialiang Ye, Ruichang Ma, Baoyong Chi; Tsinghua University, China

Abstract: A fully integrated 60 GHz 10 Gb/s QPSK transceiver (TRX) with digital transmitter and T/R switch in 65nm CMOS is presented. The TRX consists of a direct-conversion receiver, a digital transmitter with on-chip QPSK modulator and a quadrature local-oscillation (LO) signals generation network with 20 GHz integer-N phase-locked loop (PLL) frequency synthesizer. A T/R switch is also integrated to interface with the antenna. RF bandwidth of the TRX is expanded to ~10GHz by using the magnetically coupled resonator based matching network. The QPSK modulation is directly realized in the I/Q digital power amplifier, which simplifies the transmitter

complexity and reduces the power consumption. A 20 GHz integer-N PLL and a quadrature injection-locked frequency tripler (QILFT) are integrated on-chip to generate 60 GHz quadrature LO signals. The QILFT utilizes in-phase coupling technique to improve the LO I/Q matching and phase noise performance. The receiver achieves 7.1 dB noise figure and 25–47 dB dynamic gain range. The LO phase noise measured at the transmitter output is -93 dBc/Hz at 1-MHz offset from 60 GHz carrier. The measured error vector magnitude (EVM) of the transmitter is -23.9 dB for 10 Gb/s QPSK signals at 7 dBm output power. The EVM of the Over-the-Air (OTA) modulation-demodulation system is -16.3 dB for 10 Gb/s QPSK signals.

RMo3A-3 14:10

A 60GHz Polarization-Duplex TX/RX Front-End with Dual-Pol Antenna-IC Co-Integration in SiGe BiCMOS

Yao Liu, Arun Natarajan; Oregon State University, USA

Abstract: In this work, a 60 GHz simultaneous transmit and receive (STAR) TRX front-end with co-integrated antennas to achieve efficient polarization-duplex mm-wave front-end is presented. The proposed antenna approach provides broadside radiation through the substrate and is compatible with low-res silicon substrates. On-chip slot structures are driven by PAs with antenna power combining for increased output power and efficiency. The orthogonal-polarization feeds provide >40 dB simulated isolation between TX and RX around 60 GHz. Subsequent TX self-interference cancellation (SIC) at the LNA output is achieved with part of the TX signal coupled to a cancellation path, includes a reflection-type attenuator (RTA) and reflection-type phase shifter (RTPS) that provides >20 dB gain variation and full 360° variable phase shift. Overall, total average SIC >40 dB is achieved for 1.07GHz RF bandwidth at 60 GHz in the presence of a reflector.

RMo3A-4 14:30

A 180-GHz Super-Regenerative Oscillator with up to 58dB Gain for Efficient Phase Recovery

Hatem Ghaleb¹, Christian Carlowitz², David Fritsche¹, Corrado Carta¹, Frank Ellinger¹; ¹Technische Universität Dresden, Germany, ²FAU Erlangen-Nürnberg, Germany

Abstract: This paper reports on the design of a 180-GHz super-regenerative oscillator in a 130nm SiGe BiCMOS technology. The oscillator has a tuning range of 6.5%, an output power of 0.5 dBm, and occupies an area of 0.72 mm². When operated with a periodic quench signal, the circuit requires a minimum input power of -58 dBm for a phase coherent output, and can be switched at a rate up to 10 GHz. The circuit has a dc power consumption of 8.8 mW, and a maximum regenerative gain of 58 dB. QPSK and 8-PSK modulation up to 3 Gbit/s have been demonstrated at an energy efficiency of 2.9 pJ/bit. To the best knowledge of the authors, this work is the fastest reported phase-sampling super-regenerative oscillator to date.

A Broadband Direct Conversion Transmitter/Receiver at D-Band Using CMOS 22nm FDSOI

Ali A. Farid, Arda Simsek, Ahmed S.H. Ahmed, Mark J.W. Rodwell; University of California, Santa Barbara, USA

Abstract: This paper presents a broadband transmitter and receiver at D-band (from 123 to 146GHz) using 22nm FDSOI technology. The direct conversion receiver is implemented with a wideband fully differential LNA at the front end, using a cross coupled pair with capacitive neutralization, followed by a linear double balanced passive mixer and broadband pseudo-differential transimpedance amplifier. The direct conversion transmitter starts with an active double balanced Gilbert cell, followed by a driver amplifier. A 9:1 frequency multiplier circuit realized by two successive tripler stages provides the on-chip 135GHz Local Oscillator (LO) signal for both the Tx and Rx chains. The receiver conversion gain is 27dB with a 20GHz 3-dB bandwidth, and the P1-dB is -30dBm. The transmitter saturated output power is 2.8 dBm. Tx and Rx chains consume 196mW and 198mW respectively from a supply voltage of 0.8V.

Monday 3 June 2019

13:30–15:10

254AB

Session RMo3B: Blocker Tolerance and Interference Cancellation

Chair: Leon van den Oever, Qualcomm

Co-Chair: Andre Hanke, Intel

RMo3B-1 13:30

Enhanced Passive Mixer-First Receiver Driving an Impedance with 40dB/Decade Roll-Off, Achieving +12dBm Blocker-P1dB, +33dBm IIP3 and Sub-2dB NF Degradation for a 0dBm Blocker

Sashank Krishnamurthy, Ali M. Niknejad; University of California, Berkeley, USA

Abstract: A “second order” passive mixer-first receiver is proposed to improve channel selectivity, linearity and noise figure in the presence of out-of-band blockers, by presenting an impedance which rolls off at 40dB/decade as the load to an N-path filter. The synthesis of this impedance is described in a step-by-step manner starting from the required impedance transfer function to its actual circuit realization. An integrated circuit prototype was fabricated in 28nm bulk CMOS as proof of concept. The receiver, capable of broadband operation from 0.2–2GHz, achieves an out-of-band IIP3 of +33dBm and a blocker P1dB of +12dBm. Additionally, it achieves a NF of 4.4dB with less than 2dB degradation in NF for a 0dBm blocker.

RMo3B-2 13:50

A Code-Domain RF Signal Processing Front-End for Simultaneous Transmit and Receive with 49.5dB Self-Interference Rejection, 12.1dBm Receive Compression, and 34.3dBm Transmit Compression

Hussam AlShammary, Cameron W. Hill, Ahmed Hamza, James F. Buckwalter; University of California, Santa Barbara, USA

Abstract: This paper demonstrates a code-domain transceiver that incorporates a transmit (TX) modulator and receive (RX) RF signal correlator. We propose a transmission gate switch with 12.1-dBm/23.1-dBm P1dB/IIP3 for both RF correlation and filtering and rejects TX self-interference by 49.5 dB. An integrate-and-dump N-path filter improves rejection by 8 dB. The RX power consumption is 18 mW at 1 GHz. The TX modulator operates to RF power levels up to 34.3 dBm and consumes less than 40 mW for 300 Megachip-per-second (Mc/s). Over the air testing demonstrates synchronization with Barker codes.

RMo3B-3 14:10

A CMOS 0.5–2.5GHz Full-Duplex MIMO Receiver with Self-Adaptive and Power-Scalable RF/Analog Wideband Interference Cancellation

Yuhe Cao, Jin Zhou; University of Illinois at Urbana-Champaign, USA

Abstract: A 65nm CMOS 0.5–2.5GHz full-duplex (FD) MIMO receiver (RX) with self-adaptive ≥ 24 dB RF/analog interference cancellation across 20MHz BW is presented. An LMS adaptive circuitry is co-designed with and partially embedded in a wideband RF/analog interference canceller and a gain-boosted mixer-first RX. With the adaptive circuitry fully integrated and consuming 14mW, the cancellers adapt themselves to an unknown channel in 1 μ s. The FD MIMO RX is also power-scalable — when used as a digital beamformer, the NF-power scalability of the FD RX enables a nearly constant canceller DC power per element, despite a quadratic increase of cancellers.

RMo3B-4 14:30

A 0.5-to-3.5GHz Self-Interference-Canceling Receiver for In-Band Full-Duplex Wireless

Ali Ershadi, Kamran Entesari; Texas A&M University, USA

Abstract: This paper proposes an in-band full-duplex self-interference canceling receiver that achieves transmitter leakage cancellation by scaling the in-phase and quadrature components of TX replica, and injecting the approximated leakage to the RX interface. More than 35 dB cancellation is measured for modulated TX samples. The receiver structure is 8-phase passive-mixer-first with high linearity and on-chip sharp rejection of out-of-band blockers. The receiver has an IB-IIP3 of 6 dBm at 1 MHz offset from 2 GHz carrier, and OB-IIP3 of 27 dBm. The NF at 5 MHz baseband frequency is 3.3 dB at TDD mode. At FD mode, i.e., RX and TX are operating simultaneously at the same frequency band, only 2–2.5 dB noise degradation is observed. The NF reaches 5.3 dB in FD mode. As a proof of concept prototype is fabricated and measured in 65 nm CMOS. The system is functional from 500 MHz to 3.5 GHz.

RMo3B-5 14:50

A Baseband-Matching-Resistor Noise-Canceling Receiver Architecture to Increase In-Band Linearity Achieving 175MHz TIA Bandwidth with a 3-Stage Inverter-Only OpAmp

Anoop Narayan Bhat¹, Ronan van der Zee¹, Salvatore Finocchiaro², Francesco Dantoni³, Bram Nauta¹; ¹University of Twente, The Netherlands, ²Texas Instruments, USA, ³Texas Instruments, Italy

Abstract: In this paper we propose a baseband noise-canceling receiver architecture to increase in-band linearity. Key feature of the architecture is that all active circuits are in baseband, including the LNTA. The receiver targets high IF bandwidths, enabled by a TIA composed of an OpAmp using only inverters. The receiver is fabricated in 22nm FDSOI CMOS. Measured results show an in-band IIP3 of > 9 dBm for an IF bandwidth of 175MHz with sub-5dB NF across 1–6GHz I.O.

Monday 3 June 2019

13:30–15:10

257AB

Session RMo3C: High-Performance Energy-Efficient Oscillators and Frequency Synthesizers

Chair: Wanghua Wu, Samsung

Co-Chair: Piero Andreani, Lund University

RMo3C-1 13:30

A 350mV Complementary 4–5GHz VCO Based on a 4-Port Transformer Resonator with 195.8dBc/Hz Peak FOM in 22nm FDSOI

Omar El-Aassar, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents an ultra-low voltage and power complementary VCO topology based on a 4-port transformer resonator. The design benefits from the high current efficiency of a CMOS topology and the low phase noise and supply voltage of the NMOS/PMOS-only structure without sacrificing reliability. A 4-port transformer resonator is used to provide two differential-mode (DM) and two common-mode (CM) harmonic impedances for lower phase noise, voltage supply, and sensitivity to CM tuning. The CMOS VCO is implemented in 22nm FDSOI with a core area of 0.19 mm². The VCO dissipates < 0.45mW from 350mV supply while achieving a peak figure-of-merit (FOM) of 192–195.8 dBc/Hz across the 20% continuous tuning range of 4.06-to-4.96 GHz. To the authors knowledge, the 4-port resonator-based CMOS VCO has the highest reported FOM for oscillators with sub-0.5mW power consumption and the lowest supply voltage (350mV) for complementary designs.

RMo3C-2 13:50

X-Band NMOS and CMOS Cross-Coupled DCO's with a "Folded" Common-Mode Resonator Exhibiting 188.5dBc/Hz FoM with 29.5% Tuning Range in 16-nm CMOS FinFet

R. Levinger, D. Ben-Haim, I. Gertman, S. Bershansky, R. Levi, J. Kadry, G. Horovitz; Intel, Israel

Abstract: This paper presents two X-band state of the art digitally controlled oscillators (DCO's), one utilizes CMOS and the other NMOS as cross-coupled pairs. Both designs include a "folded" common-mode resonator in order to enhance performance while minimizing the required area. The implemented DCO's cover 9 to 12.1 GHz and 9.3 to 12.4 GHz for the NMOS and CMOS designs respectively, achieving a frequency tuning range (FTR) of 29.5%. Measured phase noise referred to 6.1 GHz and at 1 MHz offset is -118.5 and -114 dBc/Hz for NMOS and CMOS respectively. The NMOS design consumes 3.6 mW while the CMOS design consumes 1.1 mW both from a 0.8 V supply, obtained figure of merit (FoM) for both designs is higher than 188.5 dBc/Hz. Both designs are very compact with an area less than 0.054 mm².

RMo3C-3 14:10**A 18.2–29.3GHz Colpitts VCOs Bank with -119.5dBc/Hz Phase Noise at 1MHz Offset for 5G Communications**

F. Quadrelli¹, F. Panazzolo¹, M. Tiebout¹, F. Padovan¹, M. Bassi¹, A. Bevilacqua²; ¹Infineon Technologies, Austria, ²Università di Padova, Italy

Abstract: This paper describes a bank of four SiGe BiCMOS oscillators tailored to cover the 18.2–29.3 GHz frequency range, needed to tackle the needs of 5G communications. The Colpitts oscillator topology is leveraged to achieve a lower absolute phase noise compared to Class-C oscillators, at the expense of deteriorated figure of merit. Benefiting from the proper technology choice, a careful tank design was carried out to maximize Q, minimize K_{vco} and phase noise variations. The four oscillators feature state-of-the-art phase noise, ranging from -119.5 dBc/Hz to -116.5 dBc/Hz at 1MHz offset for 18.2 GHz and 29.3 GHz carrier frequency, respectively. For each oscillator the phase noise variation is only <2 dB over -20°C to 85°C temperature range and <6 dB over the whole 47% tuning range.

RMo3C-4 14:30**A 9.6mW Low-Noise Millimeter-Wave Sub-Sampling PLL with a Divider-Less Sub-Sampling Lock Detector in 65nm CMOS**

Hao Wang, Omeed Momeni; University of California, Davis, USA

Abstract: A 40.5 GHz sub-sampling phase-locked loop (SSPLL) with only 9.6 mW power consumption is presented. The proposed Sub-Sampling Lock Detector (SSLD) samples the output signal with on-chip generated 900 MHz reference, and can automatically detect and rectify the unlock or locked-to-wrong-harmonic states. This is done without using traditional power-consuming divider-based frequency-locked loop (FLL). The proposed SSPLL hence achieves low power, low in-band phase noise and robust operation simultaneously.

RMo3C-5 14:50**A -40-dBc Integrated-Phase-Noise 45-GHz Sub-Sampling PLL with 3.9-dBm Output and 2.1% DC-to-RF Efficiency**

Sangyeop Lee¹, Kyoya Takano¹, Shinsuke Hara², Ruibing Dong¹, Shuhei Amakawa¹, Takeshi Yoshida¹, Minoru Fujishima¹; ¹Hiroshima University, Japan, ²NICT, Japan

Abstract: This paper presents a millimeter-wave (mmW) sub-sampling PLL in 40nm CMOS. Sub-sampling PLL reduces the in-band phase noise due to the charge pump lower than the ordinary $N^2 \times$ when frequency is multiplied by N. Two sub-sampling phase detectors (SSPD) and charge pumps (SSCP) are employed to cancel mixing products due to sub-sampling around the VCO output tone and to enhance loop gain. The out-of-band phase noise, dictated by the VCO phase noise, is reduced by employing a VCO consisting of transmission-line resonators, large MOSFET switches, and inverse-class-F output matching. The proposed PLL, operating at 45 GHz, achieves -40-dBc integrated phase noise (0.1 kHz–40 MHz), 3.9-dBm output power, and 2.1% DC-to-RF efficiency.

Monday 3 June 2019

15:55–17:15

252AB

Session RMo4A: Millimeter-Wave PAs for 5G and Phased Arrays

Chair: Patrick Reynaert, Katholieke Universiteit Leuven

Co-Chair: Margaret Szymanowski, NXP Semiconductors

RMo4A-1 15:55

A High Efficiency 39GHz CMOS Cascode Power Amplifier for 5G Applications

Hyun-chul Park, Byungjoon Park, Yunsung Cho, Jaehong Park, Jihoon Kim, Jeong Ho Lee, Juho Son, Kyu Hwan An, Sung-Gi Yang; Samsung, Korea

Abstract: We present a 39GHz CMOS cascode power amplifier (PA) with a two-step (L-C and C-L) second harmonic termination. We analyze the distortion mechanism in a cross-coupled capacitor neutralization technique and suggest the termination scheme to enhance both linearity and efficiency of PAs. This scheme can suppress the second harmonic feedback components generated in the middle of the cascode cell and extend the range of linear output power (P_{out}). Our two-stage PA shows power gain of >24.5dB, saturation output power (P_{sat}) of >16.2dBm and power-added-efficiency (PAE) of >32% over the full 39GHz band from 37 to 40GHz. Under the 5G new radio modulation, the PA achieves linear P_{out} of 8.2dBm/10.3dBm and PAEs of 11.9%/16.5% at EVMs of -30.0dB/-25.3dB, respectively.

RMo4A-2 16:15

A Compact E-Band PA with 22.37% PAE 14.29dBm Output Power and 26dB Power Gain with Efficiency Enhancement at Power Back-Off

Liang Chen, Lei Zhang, Li Zhang, Yan Wang; Tsinghua University, China

Abstract: This paper presents a compact power amplifier (PA) with efficiency enhancement technique at power back-off region in 65-nm CMOS technology for E-band applications. Cross-coupled transistor pair, generating negative impedance is introduced to enhance power back-off efficiency and small signal power gain. Neutralization and transformer-based matching networks are employed to improve gain and stability. The measured P_{sat} , OP_{1dB} and peak PAE are 14.29 dBm, 12.03 dBm and 22.37%, respectively. A 26 dB power gain with 3 dB bandwidth of 5 GHz is achieved. The measured peak gain varies from 26 dB to 31 dB and the P_{1dB} power added efficiency increases from 6% to 13.3% by adjusting the control voltages of cross-coupled transistor pair. Compact layout of the PA yields a core area of 0.025 mm², and the total DC power consumption is 120 mW, enabling compact and efficient integration into phased array transceivers.

RMo4A-3 16:35

An E-Band Compact Power Amplifier for Future Array-Based Backhaul Networks in 22nm FD-SOI

Umut Çelik, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a compact high output power, linear power amplifier (PA) for array based small to medium range mm-Wave base stations. Transformer based matching and cascode architecture is used to achieve record level power density in 22nm FD-SOI. The PA achieves 17.8dB gain, 17.8dBm saturated output power (P_{sat}) with 17.3% power-added efficiency (PAE). Core area is as low as $0.052 \times 0.38\text{mm}^2$, making this PA an ideal candidate for large array systems. AMPM is less than 2.1 degrees at 1dB compression point (P1dB) at 76GHz and less than 3 degrees from 60GHz to 85GHz. To the authors' knowledge, this PA has the highest power density achieved in E-band CMOS PAs.

RMo4A-4 16:55

An E-Band Fully-Integrated True Power Detector in 28nm CMOS

Valdrin Qunaj, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents the design of a power amplifier with a low-power fully-integrated E-band true power detector in a 28nm CMOS technology. The power detector is able to measure the true output power with a dynamic range of 27.2dB at a frequency of 75GHz for a linearity error of $\pm 0.5\text{dB}$. The detector has a low power consumption of $66\mu\text{W}$ and occupies an active area of $54 \times 130\mu\text{m}^2$. Furthermore, the integrated detector is able to measure antenna load variations. The power amplifier design uses capacitive neutralization for gain and stability enhancement and achieves a peak gain of 23.1dB. The measured P_{sat} , OP1dB and peak PAE at 75GHz are 11.6dBm, 9.7 dBm and 22.8% respectively.

RMo4A-5 17:15

A Coupler-Based Differential Doherty Power Amplifier with Built-In Baluns for High mm-Wave Linear-Yet-Efficient Gbit/s Amplifications

Huy Thong Nguyen, Hua Wang; Georgia Tech, USA

Abstract: We propose a Doherty power amplifier architecture with impedance inverting balun and impedance scaling balun to support Doherty active load modulation and Power Back-Off (PBO) efficiency enhancement at high mm-Wave frequencies. Unlike transformer baluns often used at RF frequencies, mm-Wave coupler-based baluns are employed to provide well balanced differential-to-single-ended conversion and absorb device output parasitic capacitance. Moreover, this paper reports that coupler-based balun with 45° electrical length exhibits impedance inverting behavior, which is utilized to construct Doherty active load modulation network in the reported PA design. Adaptive biasing circuit further enhances the Main/Auxiliary PA cooperation. The measured Doherty PA exhibits 20.1dBm P_{sat} , 19.3dBm P_{1dB} , and 26% peak PAE. At 7dB PBO, the measured PAE is 16.6%, demonstrating 1.45 \times efficiency enhancement compared to an ideal class-B PA with the same peak PAE at P_{1dB} .

Monday 3 June 2019

15:55–17:15

254AB

Session RMo4B: Receiver Circuits in CMOS-SOI Technology

Chair: Kamran Entesari, Texas A&M University

Co-Chair: Danilo Manstretta, Università di Pavia

RMo4B-1 15:55

VSWR Robust Linearizer to Improve Switch IMD by >20dB

Thomas Meier, Atif Mehmood, Jonas Kaps; RF Innovation, Germany

Abstract: A novel circuit design approach is able to reduce intermodulation products of FET based RF switches by more than 20dB. Isolation remains unaffected, insertion loss adder is 0.1dB only and robust VSWR performance is shown. The necessary additional die area is very small keeping the cost adder at a minimum.

RMo4B-2 16:15

A Blocker-Tolerant Two-Stage Harmonic-Rejection RF Front-End

Faizan Ul Haq¹, Mikko Englund², Yury Antonov¹, Kari Stadius¹, Marko Kosunen¹, Kim B. Östman³, Kimmo Koli², Jussi Ryyänen¹; ¹Aalto University, Finland, ²Huawei Technologies, Finland, ³Nordic Semiconductor, Finland

Abstract: SAW-less wideband receivers need to operate linearly in the presence of strong out-of-band blockers. In this paper, we introduce a blocker tolerant harmonic rejection RF front-end which is able to suppress blockers present at the local oscillator harmonics. The suppression is achieved by applying harmonic rejection in two stages, such that the first harmonic rejection already occurs at the output of LNA. The proposed front-end achieves this harmonic rejection with simpler 6-phase LO clocking and reduced number of base-band signal paths compared to 8-phase HR architectures. Further, the proposed design does not require any precise gain coefficients and implementing the harmonic rejection in two stages makes it more mismatch tolerant. In addition, near-band blocker linearity is improved by implementing a third order base-band feedback response which acts in conjunction with N-path filtering. Implemented in a 28nm FDSOI process, the front-end demonstrate 18–37dB harmonic rejection from the first stage and around 46–53dB of harmonic rejection from the second stage with a state-of-the-art blocker compression point of 2.5dBm for a third harmonic blocker and a near-band blocker compression point of -6.5dBm.

RMo4B-3 16:35

A Low Noise Figure 28GHz LNA in 22nm FDSOI Technology

Chi Zhang¹, Frank Zhang¹, Shafiullah Syed¹, Michael Otto², Abdellatif Bellaouar¹;

¹GLOBALFOUNDRIES, USA, ²GLOBALFOUNDRIES, Germany

Abstract: This paper presents a 28GHz low noise amplifier (LNA) implemented in 22nm FDSOI technology. The LNA is based on inductively degenerated common source topology with cascode device. With several special layout techniques, the LNA achieved best in class noise figure (NF). At 28GHz, the LNA has a gain of 12dB, input referred third-order intercept point (IIP3) of 3.0dBm and input reference 1-dB compression point (IP1dB) of -7.6dBm. The 1-dB and 3-dB bandwidth of the LNA is 8.5GHz and 15.1GHz, respectively. The lowest achieved NF is 1.46dB at 24GHz with power dissipation (P_{DC}) of 9.8mW. Another LNA with larger device width was also implemented to achieve better NF. For this LNA, the lowest achieved NF is 1.35dB at 24GHz with P_{DC} of 13.0mW. It could also achieve 1.8dB NF at 28GHz at 5.0mW P_{DC} .

RMo4B-4 16:55

A 1.7-dB Minimum NF, 22–32GHz Low-Noise Feedback Amplifier with Multistage Noise Matching in 22-nm SOI-CMOS

Bolun Cui¹, John R. Long¹, David L. Harame²; ¹University of Waterloo, Canada,

²GLOBALFOUNDRIES, Germany

Abstract: A transformer-feedback low-noise amplifier (LNA) implemented in 22-nm SOI-CMOS with interstage noise matching is described. The LNA peak gain is 21.5dB at 22GHz, with a -3dB bandwidth (BW) of 19–36GHz. Minimum noise figure (NF) is 1.7dB centered at 28GHz, and remains below 2.2dB across 10GHz. Third-order input intercept (IIP_3) is -13.4dBm at peak gain when dissipating 17.3mW. Input and output return losses are >10dB across 22–32GHz (effective BW). Modulation of the FET backgate voltage increases NF by <0.5dB, while reducing power consumption to just 5.6mW.

Monday 3 June 2019

15:55–17:15

257AB

Session RMo4C:

Mixed Signal Circuits for High Speed RF and Optical Transceivers

Chair: Antoine Frappé, ISEN Lille

Co-Chair: Raja Pallela, MaxLinear

RMo4C-1 15:55

A 112-GS/s 1-to-4 ADC Front-End with More than 35-dBc SFDR and 28-dB SNDR up to 43-GHz in 130-nm SiGe BiCMOS

X.-Q. Du¹, M. Grözing¹, A. Uhl¹, S. Park¹, F. Buchali², K. Schuh², S.T. Le², M. Berroth¹; ¹Universität Stuttgart, Germany, ²Nokia Bell Labs, Germany

Abstract: A 112 GS/s 1-to-4 ADC front-end in IHP 130 nm SiGe BiCMOS based on charge sampling is presented. In experimental tests, the ADC front-end achieves more than 35 dBc SFDR and more than 28 dB SNDR up to 43 GHz. Furthermore, sampling of 100 Gbaud (=200 Gb/s) PAM-4 signals with an EVM of 11.3% for 400k received symbols is demonstrated.

RMo4C-2 16:15

A Dual-28Gb/s Digital-Assisted Distributed Driver with CDR for Optical-DAC PAM4 Modulation in 40nm CMOS

Qiwen Liao¹, Shang Hu², Jian He¹, Bozhi Yin², Patrick Yin Chiang², Jian Liu¹, Nan Qi¹, Nanjian Wu¹; ¹Chinese Academy of Sciences, China, ²Fudan University, China

Abstract: This paper presents a dual 28Gb/s modulator driver with on-chip PAM4 clock and data recovery (CDR) in 40nm CMOS. Used in the 400G Ethernet, 56Gb/s PAM4 signal is recovered by the CDR and demodulates into dual-28Gb/s NRZ data streams to drive the silicon photonic MZM DAC. Push-pull driver cells are employed to reuse the current for power saving with high-swing output. A digital-assisted distributed topology is proposed, extending the driver bandwidth and enabling low-power flexible pre-emphasis within each segment. Precise retiming is implemented by phase interpolation for the velocity match both in distributed driver segments and MZM DAC segments. Measurement results show the CDR+driver achieves 4Vpp differential voltage swing, 1.78ps RMS jitter and 1.34W power consumption (including PAM4 CDR and dual-channel driver) at 50Gb/s PAM4 input, while the standalone driver contributes to 1.5ps RMS jitter at 28Gb/s NRZ outputs.

RMo4C-3 16:35

A 77dB-SFDR Multi-Phase-Sampling 16-Element Digital Beamformer with 64 4GS/s 100MHz-BW Continuous-Time Band-Pass $\Delta\Sigma$ ADCs

Rundao Lu, Sunmin Jang, Yun Hao, Michael P. Flynn; University of Michigan, USA

Abstract: This paper tackles the fundamental limitation of distortion in large-scale digital beamforming. SNR improves by 3dB for every doubling of array size; however, distortion is correlated

and so is not improved by the array gain. This work introduces the concept of multiple ADCs per element, with each sampling at a different phase, to both reduce distortion of the ADCs and RF frontend. A further advantage is that multi-phase-sampling with continuous-time band-pass delta-sigma modulators (CTBPDSMs) reduces the ADC clock-jitter sensitivity. A prototype 16-element 1GHz-IF digital beamformer employs four multi-phase-sampling sub-ADCs per element. The prototype beamformer IC integrates 64 4GS/s sub-ADCs and digital processing to generate four simultaneous beams. Bit-stream digital beamform processing efficiently handles the aggregate 0.256TS/s from the entire ADC array. The measured beamformer SNDR and SFDR are 56dB and 77dB, respectively. Multiphase sampling improves measured HD3 by 9dB.

RMo4C-4 16:55

A Wideband Digitally Controllable RFIC with Gain and Wavelength Tunability and Built-In Self Test Functionalities for Optical Transceiver Modules in FTTx Applications

Sreekesh Lakshminarayanan¹, Harman Malhotra¹, David Navara², Norbert Reiss², Klaus Hofmann¹; ¹Technische Universität Darmstadt, Germany, ²DEV Systemtechnik, Germany

Abstract: This paper presents a wideband RF mixed-signal integrated circuit for optical transceiver modules in FTTx applications. The RF transceiver has an operating frequency range of 700 MHz to 2.5 GHz and a gain which is tunable to the range of 31.5 dB in 0.5 dB steps. Built-in self testing is incorporated with a 3-bit digital-controlled ring oscillator for testing the basic functionality of the circuit. Wavelength tunability for the optical transceiver module is realized by means of a digital-controlled current source which has a ± 60 mA output current range and a resolution of 1 mA. The RF and analog parts of the circuit operate on a 3.3 V supply, whereas the digital core has a 1.2 V supply voltage. The die occupies 5.07 mm² in area and the IC has a maximum power consumption of 674.74 mW.

RMo4C-5 17:15

A Compact Single-Ended Dual-Band Receiver with Crosstalk and ISI Reductions for High-Density I/O Interfaces

Jieqiong Du¹, Jia Zhou¹, X. Shawn Wang¹, Chien-Heng Wong¹, Huan-Neng Chen², Chewn-Pu Jou², Mau-Chung Frank Chang¹; ¹University of California, Los Angeles, USA, ²TSMC, Taiwan

Abstract: A compact single-ended dual-band receiver is presented, consisting of one baseband using PAM-2 signaling and a coherent RF band using PAM-2/PAM-4 signaling. Exploiting the orthogonality between different bands and between adjacent PCB channels, the receiver reduces crosstalk and relaxes equalization requirements, enabling low-BER data transmission at frequencies where channel loss and crosstalk are high. The receiver adopts a passive-mixer-first architecture to improve the linearity and a flipped source-follower-based low-pass filter to improve the energy efficiency. Occupying 0.004 μm^2 in TSMC 28nm technode, the proposed single-ended receiver achieves 0.45 pJ/bit at 9 Gb/s/pin for closely spaced 5-inch FR-4 channels and 0.6 pJ/bit at 6 Gb/s/pin for lossy and strongly coupled 22-inch FR-4 channels.

Tuesday 4 June 2019

08:00–09:40

252AB

Session RTu1E: Special Session: 5G Circuits and Systems

Chair: Tim LaRocca, Northrop Grumman

Co-Chair: Hongtao Xu, Fudan University

RTu1E-1 08:00

A 26dBm 39GHz Power Amplifier with 26.6% PAE for 5G Applications in 28nm Bulk CMOS

Kaushik Dasgupta, Saeid Daneshgar, Chintan Thakkar, James Jaussi, Bryan Casper, Intel, USA

Abstract: Continued demand for 5G cellular connectivity in mobile handheld devices, where antenna real-estate is at a premium, necessitates high output power from individual transmitter elements. While more expensive heterogeneous and SOI CMOS process based power amplifiers (PAs) provide high P_{out} at good efficiencies, deep sub- μ m bulk CMOS still remains the technology of choice for cost and integration benefits. This paper presents a 5G mm-Wave PA at 39GHz that generates a saturated P_{out} of 26dBm with a peak power-added efficiency (PAE) of 26.6% and a saturated power gain of 28.6 dB. The output stage utilizes compact layout & triple-well transistors to enable efficient yet reliable device stacking and a compact, 4-way, low-loss, series-parallel power combiner further enhances P_{out} . High average power measurements have been demonstrated during single-carrier as well as 5G NR OFDM modulations at competitive efficiencies. Long term reliability measurements using aging acceleration techniques demonstrate the robustness of the implemented PA. This PA achieves one of the highest ITRS figure-of-merit among reported 5G mm-Wave works in CMOS and also the highest output power among deep sub- μ m (<90nm) 5G bulk CMOS PAs.

RTu1E-2 08:20

A 24–43GHz LNA with 3.1–3.7dB Noise Figure and Embedded 3-Pole Elliptic High-Pass Response for 5G Applications in 22nm FDSOI

Li Gao, Gabriel M. Rebeiz, University of California, San Diego, USA

Abstract: This paper presents a 20–44 GHz low-noise amplifier in 22 nm FDSOI with low noise figure and low DC power consumption. The LNA is based on a 3-stage cascode amplifier which is co-designed with embedded high-pass filters so as to results in a very sharp rejection at < 16 GHz, exhibiting an elliptic filter response. This is ideal for wideband 5G amplifiers as it greatly reduces the 2nd the 3rd harmonic interference issues arising from X and Ku-band blockers (8–16 GHz). A wideband transformer-based input matching is used resulting in $S_{11} < -9$ dB at 20–40 GHz. The measured gain is > 17 dB at 20–43 GHz with a peak of 23 dB at 40 GHz. The LNA achieves a NF of 3.1–3.7 dB (3.4 ± 0.3 dB) at 24–43 GHz, an in-band IIP3 of -13.2 to -19 dBm at 20–40 GHz, all at a power consumption of 20.5 mW. Operation at 12 mW is also shown, with a maximum gain and minimum NF of 18.2 dB and 3.4 dB at 24–43 GHz. To our knowledge, the LNA represents the highest FoM achieved at this frequency range to-date and includes an embedded 3-pole filter response.

RTu1E-3 08:40**A 4-Element 28GHz Millimeter-Wave MIMO Array with Single-Wire Interface Using Code-Domain Multiplexing in 65nm CMOS**

Manoj Johnson¹, Armagan Dascuru², Kai Zhan¹, Arman Galioglu², Naresh Adepu², Sanket Jain¹, Harish Krishnaswamy², Arun Natarajan¹; ¹Oregon State University, USA, ²Columbia University, USA

Abstract: Millimeter-wave MIMO systems with digitization of every element enable spatial multiplexing, virtual arrays for radar, digital beamforming (DBF) for high mobility scenarios. However, per-element digitization results in a formidable I/O challenge in large-scale tiled MIMO mmWave arrays. This work demonstrates a 28GHz 4-element MIMO RX with a single-wire interface that multiplexes the baseband signals of all elements and the LO reference through code-domain multiplexing. System considerations are presented and the approach is validated through DBF after de-multiplexing of the baseband signals from the single wire. Each element in the array achieves 16 dB conversion gain while consuming 60mA from 1.2V. The IC occupies 5.75mm² in 65-nm CMOS.

RTu1E-4 09:00**A 16-Element Phased-Array CMOS Transmitter with Variable Gain Controlled Linear Power Amplifier for 5G New Radio**

Yunsung Cho, Woojae Lee, Hyun-chul Park, Byungjoon Park, Jeong Ho Lee, Jihoon Kim, Jooseok Lee, Seokhyeon Kim, Jaehong Park, Sangyong Park, Kyu Hwan An, Juho Son, Sung-Gi Yang; Samsung, Korea

Abstract: This paper presents a 28-GHz 16-element phased-array transmitter for the fifth-generation (5G) new radio (NR) applications, focusing on the power amplifier (PA). The IC was fabricated using a 28-nm bulk CMOS technology with a flip-chip package, and evaluated with 5G NR signal having an 800-MHz total bandwidth. Each channel of the 16 phased-array transmitter has a 16 dBm output at 1-dB compression point and a large gain range from 24 to 63 dB. The full 16-element array achieves an average output power of 18 dBm with a record-level system error vector magnitude (EVM) of less than -33.5 dB (<2.1%) at a total power consumption of 1.63 W (102 mW of per channel) including all biases, digital control, and power-management-unit (PMU) blocks, over the frequency band from 26.5 to 29.5 GHz.

A 37–40GHz Phased Array Front-End with Dual Polarization for 5G MIMO Beamforming Applications

Ankur Guha Roy¹, Ozgur Inac¹, Amitoj Singh¹, Tsvika Mukatel², Ohad Brandelstein², Thomas W. Brown¹, Salah Abughazaleh¹, Joseph S. Hayden III¹, Byungho Park¹, Greg Bachmanek¹, Te-Yu Jason Kao¹, Josef Hagn³, Sidharth Dalmia¹, Doron Shoham², Brandon Davis¹, Iris Fisher², Raanan Sover², Amit Freiman², Bin Xiao¹, Baljit Singh¹, Jonathan Jensen¹; ¹Intel, USA, ²Intel, Israel, ³Intel, Germany

Abstract: This paper presents a dual polarized 37–40 GHz transmitter-receiver (TRX) phased array front-end RFIC implemented in a 28nm bulk RF-CMOS process. The TRX front-end contains 8 channels, 4-vertical (V) and 4-horizontal (H). Each transmit (TX) or receive (RX) channel consists of PA or LNA, 5-bit passive phase shifter, coarse and fine gain control amplifiers. The TX channel shows an op1dB of 10.2 dBm at the antenna bump. The RX channel shows a noise figure (NF) of 6 dB. TX and RX channels show an EVM of -32.57 dB and -29.80 dB respectively. A 4×4 antenna array was implemented on PCB using 4 TRX front-end RFICs. Beam patterns with different 5G-modulated waveforms were characterized.

Tuesday 4 June 2019

08:00–09:40

254AB

Session RTu1F:

Energy-Efficient Wake-Up Receivers and IoT Transceivers

Chair: Renaldi Winoto, Mojo Vision

Co-Chair: Yuan-Hung Chung, MediaTek

RTu1F-1 08:00

An 802.11ba 495 μ W -92.6dBm-Sensitivity Blocker-Tolerant Wake-Up Radio Receiver Fully Integrated with Wi-Fi Transceiver

Renzhi Liu¹, Asma Beevi K.T.¹, Richard Dorrance¹, Deepak Dasalukunte¹, Mario A. Santana Lopez², Vinod Kristem¹, Shahrnaz Azizi¹, Minyoung Park¹, Brent R. Carlton¹; ¹Intel, USA, ²Intel, Mexico

Abstract: An 802.11ba-based wake-up radio (WUR) receiver is presented. The WUR receiver prototype is integrated within an 802.11a/b/g/n/ac Wi-Fi transceiver, occupying 0.05mm² for RF/analog frontend and 0.08mm² for digital baseband. The WUR receiver consumes 495 μ W standalone and consumes 667 μ W from Wi-Fi system supply. The receiver has a measured sensitivity of -92.6dBm and can tolerate -40.5dBm Wi-Fi adjacent channel blocker with 3dB receiver de-sensitization. The WUR receiver can operate when the Wi-Fi system is in sleep mode and can turn on Wi-Fi radio upon receiving 802.11ba-based wake-up packet over the air.

RTu1F-2 08:20

A -80.9dBm 450MHz Wake-Up Receiver with Code-Domain Matched Filtering Using a Continuous-Time Analog Correlator

Vivek Mangal, Peter R. Kinget; Columbia University, USA

Abstract: A continuous-time, clockless analog correlator uses pulse-position-encoded analog signal processing with VCOs as integrators and pulse-controlled relaxation delays; it operates as a matched filter to despread asynchronous wake-up codes. A correlator prototype has been designed in 65nm CMOS-LP technology, consumes 37nW from 0.54V, and performs code-domain filtering with an 11-bit Barker code for a wake-up receiver. The hardware of the proposed n-bit correlator architecture scales with O(n) compared to O(n²) for asynchronous switched-capacitor correlators. A -80.9dBm 40nW wake-up receiver with 9dB better sensitivity and 3dB improved selectivity to AM interference thanks to the correlator is demonstrated.

RTu1F-3 08:40

A 4 \times 4 \times 4-mm³ Fully Integrated Sensor-to-Sensor Radio Using Carrier Frequency Interlocking IF Receiver with -94dBm Sensitivity

Li-Xuan Chuo¹, Yejoong Kim¹, Nikolaos Chiotellis¹, Makoto Yasuda², Satoru Miyoshi³, Masaru Kawaminami², Anthony Grbic¹, David Wentzloff¹, Hun-Seok Kim¹, David Blaauw¹; ¹University of Michigan, USA, ²Mie Fujitsu Semiconductor, Japan, ³Fujitsu Electronics, USA

Abstract: Ultra-low power mm-scale IoT platforms enable newly emerging applications such as pervasive agricultural monitoring and bio-sensing. Although there is an increasing interest in sensor-to-sensor communication, as defined in Bluetooth v5.0, prior research in mm-scale wireless systems is mostly limited to asymmetric sensor-to-gateway communication. This paper introduces a $4 \times 4 \times 4$ mm³ fully integrated radio system that integrates a transceiver chip, antenna, power management unit and baseband processor for sensor-to-sensor mesh networks. The proposed system uses a low power 32 kHz reference frequency and a carrier frequency interlocking IF receiver. It achieves -94 dBm sensitivity with 97 μ W power consumption and -12.6 dBm EIRP for sensor-to-sensor mesh network communication.

RTu1F-4 09:00

A 55nm SAW-Less NB-IoT CMOS Transceiver in an RF-SoC with Phase Coherent RX and Polar Modulation TX

P.S. Tseng¹, W. Yang², M.J. Wu², L.M. Jin², D.P. Li², E.C. Low², C.H. Hsiao¹, H.T. Lin¹, K.H. Yang¹, S.C. Shen¹, C.M. Kuo¹, C.L. Heng², G.K. Dehng¹; ¹MediaTek, Taiwan, ²MediaTek, Singapore

Abstract: A SAW-Less NB-IoT transceiver for IoT devices with >10 years battery life and >164dB MCL is presented. Tunable RX Front-end supports 26 NB-IoT bands, achieves <-140dBm Narrowband Reference Signal Received Power (NRSRP) and tolerates up to -15dBm out-of-band blocking. RX phase continuity across sub-frames reduces RX power consumption by 30%. The Polar TX achieves >+4dBm output power, <5% EVM, and <-57dB 300kHz SEM. The 55nm transceiver consumes 11.8mW/25.8mW for receiving / transmitting, and occupies 2.23mm² die area in a 5.6×5.6mm² packaged chip.

RTu1F-5 09:20

A 1.04–4V, Digital-Intensive Dual-Mode BLE 5.0/IEEE 802.15.4 Transceiver SoC with Extended Range in 28nm CMOS

Nam-Seog Kim¹, Myoung-Gyun Kim¹, Ashutosh Verma², Gyungseon Seol¹, Shinwoong Kim¹, Seokwon Lee¹, Chilun Lo¹, Jaeyoul Han¹, Ikkyun Jo¹, Chulho Kim¹, Chih-Wei Yao², Jongwoo Lee¹; ¹Samsung, Korea, ²Samsung, USA

Abstract: The proposed fully-integrated digital-intensive TRX SoC allows dual-mode protocols of BLE 5.0 and IEEE 802.14.5 with extended-range wireless connectivity and simple ad-hoc mesh networks for the IoTs in smart homes. A 1.04–4V with dual-mode supply schemes enables the SoC to be applied for various IoT systems energy-effectively and extends battery lifetime cost-effectively. The TRX employs a low insertion loss CMOS transmit-receive switch, a class-D power amplifier with HD2 calibration, a low-IF RX architecture with $\Delta\Sigma$ ADC-based complex filter, and a low power ADPLL with LMS-based two-point direct frequency modulation. The TRX implemented in a 28nm CMOS process achieves the maximum output power of +10dBm while consuming 45mW at the TX, <-102dBm at IEEE802.15.4 mode while consuming 6mW at the RX.

Tuesday 4 June 2019

10:10–11:50

252AB

Session RTu2E:

Special Session: 5G Millimeter-Wave Beamforming Systems

Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

Co-Chair: Arun Natarajan, Oregon State University

RTu2E-1 10:10

A 24.5–43.5GHz Compact RX with Calibration-Free 32–56dB Full-Frequency Instantaneously Wideband Image Rejection Supporting Multi-Gb/s 64-QAM/256-QAM for Multi-Band 5G Massive MIMO

Min-Yu Huang¹, Taiyun Chi², Fei Wang¹, Sensen Li¹, Tzu-Yuan Huang¹, Hua Wang¹; ¹Georgia Tech, USA, ²Speedlink Technology, USA

Abstract: This paper presents a 24.5–43.5GHz compact RX frontend achieving 32–56dB full-frequency instantaneously wideband image rejection, which can cover major mm-Wave 5G bands at 24.5/28/37/39/43 GHz. It utilizes a transformer-based IQ network able to accommodate large load impedance transformation with robust I/Q generation, which provides impedance up-scaling and passive voltage amplification to boost the LO swing. It achieves a low-loss mm-Wave I/Q LO generation with a compact size (0.14mm²) and state-of-the-art instantaneously broad bandwidth 25–50GHz without calibration or switching/tunable elements. After image rejection, the wideband desired RX signal is successfully demodulated, showing state-of-the-art 12Gb/s 64-QAM with -27.6dB EVM and 8Gb/s 256-QAM with -33.47dB EVM under wideband modulated image signals with the same modulation scheme and data rate. To the best of authors' knowledge, this paper is the first demonstration receiver frontend to support broadband modulated multi-Gb/s 64-/256-QAM image rejection with no calibration, switching/tuning elements, or external controls, enabling wideband low-latency 5G MIMOs in complex EM environments.

RTu2E-2 10:30

A 39GHz 64-Element Phased-Array CMOS Transceiver with Built-In Calibration for Large-Array 5G NR

Yun Wang¹, Rui Wu¹, Jian Pang¹, Dongwon You¹, Ashbir Aviat Fadila¹, Rattanan Saengchan¹, Xi Fu¹, Daiki Matsumoto¹, Takeshi Nakamura¹, Ryo Kubozoe¹, Masaru Kawabuchi¹, Bangan Liu¹, Haosheng Zhang¹, Junjun Qiu¹, Hanli Liu¹, Wei Deng¹, Naoki Oshima², Keiichi Motoi², Shinichi Hori², Kazuaki Kunihiro², Tomoya Kaneko², Atsushi Shirane¹, Kenichi Okada¹; ¹Tokyo Institute of Technology, Japan, ²NEC, Japan

Abstract: This paper presents a 39GHz 64-element phased-array transceiver based on 4-element transceiver chipset with LO phase shifting architecture and built-in gain phase calibration. A phase-to-digital-converter (PDC) and a high-resolution phase detection mechanism are proposed. The built-in calibration has an measured accuracy of 0.08-degree RMS phase error and 0.01-dB RMS gain error. The LO phase shifting based transceiver has a 0.04-dB maximum gain variation over the 360° full tuning range. The proposed pseudo-single-balanced mixer realizes -70 dBm LO-feedthrough (LOFT) cancellation and maximum 0.5° LO-to-LO isolation. The 8TX-8RX phased-array transceiver module 1-m OTA measurement supports 5G new radio (NR) 400MHz 256QAM OFDMA modulation with -30.0dB EVM. The 64-element transceiver has a EIRP_{MAX} of 53dBm. The 4-element chip consumes a power of 1.5W in TX mode and 0.5W in RX mode.

RTu2E-3 10:50

A 24.2–30.5GHz Quad-Channel RFIC for 5G Communications Including Built-In Test Equipment

D. Dal Maistro¹, C. Rubino¹, M. Caruso¹, M. Tiebout¹, I. Maksymova¹, M. Ilıc¹, P. Thurner¹, M. Zaghi¹, K. Mertens¹, S. Vehovc², I. Tsvelikh², E. Schatzmayr¹, M. Druml¹, R. Druml¹, M. Mueller¹, M. Anderwald¹, J. Wuertele², U. Rueddenklau²; ¹Infineon Technologies, Austria, ²Infineon Technologies, Germany

Abstract: A wideband quad-channel beamforming RFIC for worldwide 5G infrastructure applications in 130nm SiGe BiCMOS features an Rx single channel gain and NF of 22 and 4dB respectively at a total power consumption of 1.6W. Tx performance includes a P1dB of 18dBm CW and 11.5dBm RMS output power at 3% EVM and 1.8W total power consumption. Beamforming is based on a temperature invariant lumped true time delay and a phase invariant programmable gain amplifier. Integrated built-in test equipment including LO-generation, signal injection and detection enables low-cost RF production testing and array calibration.

RTu2E-4 11:10

A Highly Linear 28GHz 16-Element Phased-Array Receiver with Wide Gain Control for 5G NR Application

Youngchang Yoon, Kyu Hwan An, Daehyun Kang, Kihyun Kim, Sangho Lee, Jae Sik Jang, Donggyu Minn, Bohee Suh, Jooseok Lee, Jihoon Kim, Meeran Kim, Jeong Ho Lee, Sung Tae Choi, Juho Son, Sung-Gi Yang; Samsung, Korea

Abstract: This paper presents a 28GHz 16-element phased-array receiver in a 28nm bulk RF CMOS process targeting 5G NR application. The receiver implements a high-gain low-NF LNA, a linearity enhanced RF amplifier with post-distortion, and RF/IF step attenuators for a wide gain range and fine gain step control. Thereby, the presented receiver demonstrated a system NF of 3.5dB, a gain control range of 50dB (1dB step), and an EVM of -37.7/-43.1dB with 5G NR 800/100MHz signals while consuming a low power of 0.54W (equivalent to 33.5mW per channel).

Tuesday 4 June 2019

10:10–11:50

254AB

Session RTu2F:

Broadband, Reconfigurable, and Multimode PAs and Transmitters

Chair: Oleh Krutko, Xilinx

Co-Chair: Jeffrey S. Walling, Tyndall National Institute

RTu2F-1 10:10

A Quadrature Class-G Complex-Domain Doherty Digital Power Amplifier

Shih-Chang Hung, Si-Wook Yoo, Sang-Min Yoo; Michigan State University, USA

Abstract: An efficient digital quadrature power amplifier is presented. It shows a good system efficiency (SE) at back-off, demonstrating four efficiency peaks with the combination of a dual-supply Class-G and complex-domain Doherty (CDD) in the IQ plane. The proposed digital quadrature transmitter in 65-nm CMOS demonstrates 27.8-dBm peak output power (P_{out}) with a peak SE of 32.1%. For an 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM signal with 13.1-dB (12.4-dB) peak-to-average power ratio (PAPR), it demonstrates an error vector magnitude (EVM) of -42.0 dB (-43.3 dB) at an average P_{out} of 14.7 dBm (15.4 dBm). The average SE measured with a 20-MHz single-carrier 1024-QAM signal with 6.8-dB PAPR at 21-dBm P_{out} is 18.4%.

RTu2F-2 10:30

A Frequency Tuneable Switched-Capacitor PA in 65nm CMOS

Zhidong Bai, Ali Azam, Jeffrey S. Walling; University of Utah, USA

Abstract: A frequency tuneable, switched capacitor power amplifier (SCPA) is introduced that allows it to operate in relatively narrow channel bandwidths (10's of MHz) while enabling operation across a much wider frequency band (>1GHz). An SCPA is connected in series with a fixed inductor and a digitally programmable capacitor (DPC) that allows frequency tuning of the SCPA resonance. A prototype is fabricated in a 65nm CMOS process and embedded with the DPC on a printed circuit board for validation. The measured prototype operates from supply voltages of 1.2 and 2.4 V and achieves linear operation over 58.8% fractional bandwidth (1.4–2.5 GHz) with less than 1.7 dB output power variation. Due to its linearity, no digital pre-distortion is required to achieve measured ACLR<-30 dBc and EVM<3.9%-rms over all operating frequencies when transmitting an LTE 64-QAM, 20 MHz OFDM symbol at >14.1 dBm.

RTu2F-3 10:50

A Broadband High-Efficiency SOI-CMOS PA Module for LTE/LTE-A Handset Applications

A. Serhan¹, D. Parat¹, P. Reynier¹, R. Berro¹, R. Mouro¹, C. De Ranter², P. Indirayanti², M. Borremans², E. Mercier¹, A. Giry¹; ¹CEA-Leti, France, ²Huawei Technologies, Belgium

Abstract: This paper presents a broadband high-efficiency linear Doherty power amplifier (DPA) for LTE/LTE-A handset applications. The proposed PA is implemented in a 130nm SOI technology and packaged using flip-chip on a laminate substrate. At 2.5GHz, the PA shows a PAE of 44%, a power gain of 27dB, and an E-UTRA ACLR of -35dBc at 28dBm output power using a 10MHz LTE uplink signal without DPD. Moreover, the PA reaches a maximum FOM ($PAE + |ACLR|$) of 80 and maintains a FOM greater than 70 over 31% of fractional bandwidth around 2.3GHz without using DPD. When using DPD, the ACLR is improved by 10dB leading to a maximum FOM of 90. To the best of our knowledge, these performances represent the best linearity-efficiency performances compared to recently published LTE PAs for handset applications.

RTu2F-4 11:10

A 27GHz Adaptive Bias Variable Gain Power Amplifier and T/R Switch in 22nm FD-SOI CMOS for 5G Antenna Arrays

Christian Elgaard, Stefan Andersson, Peter Caputa, Eric Westesson, Henrik Sjöland; Ericsson, Sweden

Abstract: A 27 GHz fully integrated, variable gain, two stage Power Amplifier (PA) and a Transmit/Receive (T/R) switch targeting 5G antenna array systems are presented. The PA uses adaptive bias, tracking the input signal amplitude, which improves saturated output power (P_{sat}) with 1.4 dB and 1 dB output compression (OP_{1dB}) by 3 dB. For a supply voltage of 1.2V, the PA reaches a P_{sat} of 17.4dBm and an OP_{1dB} of 16.5 dBm, with a power added efficiency of 19.5% and 17.3%, respectively. The power gain can be controlled with 5-bits from 5.2 to 34 dB. The T/R-switch has an insertion loss of 1.63/1.46 dB in TX/RX mode, and for reliability reasons all switch devices are on in TX-mode. The complete PA and T/R-switch only occupies 0.146mm² in a 22nm FD-SOI CMOS technology.

Tuesday 4 June 2019

13:30–15:10

253ABC

Session RTuIF: Interactive Forum

Chair: Fred Lee, Verily Life Sciences

Co-Chair: Antoine Frappé, ISEN Lille

RTuIF-1

A 9dB Noise Figure Fully Integrated 79GHz Automotive Radar Receiver in 40nm CMOS Technology

Tomotoshi Murakami, Nobumasa Hasegawa, Yoshiyuki Utagawa, Tomoyuki Arai, Shinji Yamaura; DENSO, Japan

Abstract: This paper presents a low noise and fully integrated automotive radar receiver in 40 nm CMOS technology. The receiver adopts the direct conversion architecture, and it consists of a low noise amplifier (LNA), mixer, and analog baseband blocks. The three-stage LNA and the low noise mixer improve the whole receiver noise figure (NF). Integrated low-dropped out regulators (LDOs) generate 1.1 V for the LNA and the mixer core from 1.8 V supply. The receiver chip also includes a frequency doubler, phase-locked loop (PLL), bandgap reference bias circuit, and a serial peripheral interface (SPI). The die is packaged using the wafer level chip size package (WLCSP). The receiver achieves 9.0 dB NF at 81 GHz local (LO) and 76.8 dB maximum gain. Moreover, the receiver front-end shows -22.3 dBm IP1dB, and consumes 143 mW power dissipation, and 0.8 mm² chip area.

RTuIF-2

A Compact 76–81GHz 3TX/4RX Transceiver for FMCW Radar Applications in 65-nm CMOS Technology

Liang Chen, Lei Zhang, Weiping Wu, Li Zhang, Yan Wang; Tsinghua University, China

Abstract: This paper presents a compact 76–81 GHz 3TX/4RX transceiver for FMCW radar applications in 65-nm CMOS technology. Three individual transmitters (TXs) and four receivers (RXs) are integrated for MIMO operation to achieve higher resolution and sensitivity. A wideband frequency sextupler cascaded with a Wilkinson power divider is employed as the local oscillation (LO) chain to lower down the frequency of FMCW signal generator and simplify the design of LO distribution network. Each transmitter channel achieves above 12.2 dBm output power from 76–81 GHz and a peak 14.2 dBm output power is obtained at 77 GHz. The receiver conversion gain from low noise amplifier input to baseband output is programmable from 46.3 dB to 102.45 dB for adapting to different detection distances. The measured noise figure of the receiver chain is 11 dB at 5 MHz intermediate frequency (IF). The transceiver including all dc bonding pads occupies a silicon area of 1.8 mm × 4 mm, and the power dissipation of the whole chip is 721.8 mW.

RTuIF-3

A Full-Band Multi-Standard Global Analog & Digital Car Radio SoC with a Single Fixed-Frequency PLL

Lucien J. Breems¹, Jan van Sinderen¹, Tom Fric², Hans Stoffels², Franco Fritschij², Hans Brekelmans¹, Hendrik van der Ploeg², Ulrich Moehlmann³, Robert Rutten¹, Muhammed Bolatkale¹, Shagun Bajoria¹, Jan Niehof¹, Bert Oude-Essink², Gerard Lassche²; ¹NXP Semiconductors, The Netherlands, ²Catena, The Netherlands, ³NXP Semiconductors, Germany

Abstract: This paper presents a wideband car radio SoC for global multi-standard and multi-channel analog and digital broadcast radio. One of the major challenges of a wideband receiver is that the RF circuits and A/D converters need to have very high in-band IIP3 while the receiver NF should be low. These IIP3 and NF requirements are difficult to meet simultaneously. Key techniques to achieve low noise and very high linearity are high gain-bandwidth multi-inverter-based amplifiers supplied by PVT-tracking low-ohmic low dropout regulators, very linear high-speed 1-bit $\Delta\Sigma$ ADCs and a mixer-less wideband AM front-end architecture. In FM mode the measured in-band IIP3 is 17.5dBm at a NF of 6dB. At maximum gain the NF is 4.1dB in DAB mode.

RTuIF-4

Laser Spectral Linewidth Reduction Using an Integrated Pound-Drever-Hall Stabilization System in 180nm CMOS SOI

Mohamad Hossein Idjadi, Firooz Aflatouni; University of Pennsylvania, USA

Abstract: An Integrated Pound-Drever-Hall laser stabilization system is demonstrated where the electronic and photonic components are monolithically integrated in the GF7RFSOI CMOS SOI process. An off-chip Fabry-Perot cavity with quality factor of 48000 is used as the frequency reference to reduce the linewidth of a commercially available distributed feedback laser from 246 kHz to 7 kHz. The electronic-photonic chip consumes 83 mW and occupies 1.6 mm² area.

RTuIF-5

22nm FD-SOI Technology with Back-Biasing Capability Offers Excellent Performance for Enabling Efficient, Ultra-Low Power Analog and RF/Millimeter-Wave Designs

S.N. Ong¹, L.H.K. Chan¹, K.W.J. Chew¹, C.K. Lim¹, W.L. Oo¹, Abdellatif Bellaouar², Chi Zhang², W.H. Chow¹, T. Chen², R. Rassel², J.S. Wong¹, C.W.F. Wan¹, J. Kim¹, W.H. Seet¹, David L. Harnane³; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, USA, ³Research Foundation CUNY, USA

Abstract: This paper addresses the impact of back-gate biasing to DC, RF/millimeter-Wave (mmWave) and high frequency (HF) noise in 22nm FD-SOI technology (GLOBALFOUNDRIES' 22FDX technology). The front-gate and the back-gate cut-off frequency f_T , together with the maximum oscillation frequency f_{MAX} , were extracted from the four-port S-parameters data. The

maximum achieved front-gate/back-gate f_T and f_{MAX} for the NFET is 350/85 GHz and 370/23 GHz respectively. In addition, 22FDX technology demonstrated a tuneable HF noise parameter by using the back-gate biasing to achieve best-in-class low noise level. Two front-end (FE) modules were presented, which exploit the unique feature of back-gate. This unique feature allows superior designs with excellent combination of performance, power consumption and development cost, for emerging applications such as IoT, Telecommunication UE, RF and mmWave circuits with high speed connectivity and networking.

RTuIF-6

A Low Power Fully-Integrated 76–81GHz ADPLL for Automotive Radar Applications with 150MHz/ μ s FMCW Chirp Rate and -95dBc/Hz Phase Noise at 1MHz Offset in FDSOI

Ahmed R. Fridi¹, Chi Zhang¹, Abdellatif Bellaouar¹, Man Tran²; ¹GLOBALFOUNDRIES, USA, ²Mantric Technology, Canada

Abstract: In this paper, a fully integrated 76–81 GHz All Digital PLL for FMCW automotive radar applications is presented. It features a 20 GHz digital PLL followed by a $4\times$ multiplier and buffer. The proposed ADPLL is implemented in a 22nm fully depleted SOI CMOS technology. It achieves up to 150 MHz/ μ s FMCW chirp rate over a 4 GHz bandwidth and dissipates 85mW only.

RTuIF-7

An 82.2-to-89.3GHz CMOS VCO with DC-to-RF Efficiency of 14.8%

A. Tarkeshdouz¹, M. Haghi Kashani¹, E. Hadizadeh Hafshejani¹, S. Mirabbasi¹, E. Afshari²;

¹University of British Columbia, Canada, ²University of Michigan, USA

Abstract: In this paper, we present a 90-GHz CMOS voltage-controlled oscillator (VCO) that operates from 82.2 to 89.3 GHz. The proposed VCO utilizes a device-centric method to achieve a high-efficiency oscillator with DC-to-RF efficiency closer to the efficiency limits of the employed transistors. Using the swing-independent bias condition for the CMOS transistors at the frequency of interest, we incorporate an active feedback network with minimal power overhead to provide the maximum achievable swing at the gate terminal of the core transistor, thereby increasing the power added efficiency. Utilizing this method, a high-efficiency VCO with center frequency of 85.75 GHz is designed and implemented in a 65-nm CMOS process. In this VCO, the trade-offs among efficiency and tuning range are also considered and the VCO achieves a peak DC-to-RF efficiency of 14.8% at 89.3 GHz and a wide tuning range of more than 8.3% while consuming only 8.5 mW of dc power from a 1.2-V supply. Compared to the prior art, the proposed VCO demonstrates a DC-to-RF efficiency of more than 14% at frequencies up to 100 GHz. The fabricated circuit occupies a silicon area of less than 0.25 mm² including the pads.

RTuIF-8

A 62GHz Tx/Rx 2×128-Element Dual-Polarized Dual-Beam Wafer-Scale Phased-Array Transceiver with Minimal Reticle-to-Reticle Stitching

Umut Kodak¹, Bhaskara Rupakula¹, Samet Zehir², Gabriel M. Rebeiz¹; ¹University of California, San Diego, USA, ²IDT, USA

Abstract: This paper presents a 62 GHz transmit/receive (TRX) dual-polarized/dual-beam wafer-scale phased-array with 2×128-elements spaced $\lambda/2$ apart in the x- and y-directions. Two reticles each containing 2×64-element arrays are stitched together in the IF/LO domain to form a super-reticle occupying an area of 21×42 mm². Each 64-element reticle-based phased-array includes RF-beam-forming TRX channels with 5-bit phase control, 9-bit gain control for each polarization, two 64:1 nested Wilkinson divider/combiners with bidirectional amplifiers, dual-transceivers with a common LO path for transmit and receive modes, and an active distribution network in the IF and LO domains to allow for tiling at the 64-element sub-array level. Also, high-efficiency quartz superstrate dipole antennas are used on the reticle to eliminate any RF transitions between the TRX channels and the antennas, resulting in a true wafer-scale array. The 2×128-element arrays scans to $\pm 50^\circ$ with side-lobe levels <-10 dB for both polarizations, achieving 43 dBm and 41 dBm saturated EIRP for V- and H-polarizations, respectively. To our knowledge, this paper presents the first dual-polarized dual-beam large-scale transmit/receive phased-array built using a reticle stitching technique.

RTuIF-9

A 1–4GHz 4×4 MIMO Receiver with 4 Reconfigurable Orthogonal Beams for Analog Interference Rejection

Sajad Golabighezelahmad, Eric Klumperink, Bram Nauta; University of Twente, The Netherlands

Abstract: A highly reconfigurable multi-beam MIMO receiver with 4 RF inputs and 4 outputs is proposed, allowing for digital MIMO but also analog interference rejection by spatial notch filtering through 4 reconfigurable orthogonal beams. A segmented constant-Gm vector modulator with improved interference tolerance and RF frequency range is proposed, allowing current-domain beamforming before I-V conversion by a transimpedance amplifier. A 1–4 GHz 22 nm FD-SOI prototype chip achieves >29 spatial notch suppression for in-band interference signals. In the notches, an IIP3 of +17 dBm and in-band B1dB of -12 dBm is achieved at 44.5 dB gain. Sub-3dB system noise figure is achievable in the corner points of vector modulator constellation. On the circle points, noise figure degrades about 2.5 dB. However, in-band, in-notch B1dB and IIP3 improve by 32dB and 43dB, respectively. The chip of 0.52 mm² active area consumes 75–115mW at an LO-frequency of 1–4 GHz from a 0.8V supply.

RFIC 2019 Lunchtime Panel Session

Monday, 3 June 2019

12:00–13:15

BCEC, Room 162AB

RFIC2019 Panel Sessions Chair: Donald Y.C. Lie, Texas Tech University, USA

The Internet of Things (IoT) – Back to the Future, or No Future?

Panel Organizers and Moderators:

Oren Eliezer, PHAZR, USA

Debopriyo Chowdhury, Broadcom, USA

Panelists: **Fari Assaderaghi**, Sr. VP & CTO, NXP Semiconductors, USA

Min Hao, Founder & Chairman, Shanghai Quanray Electronics

Professor, Fudan University, China

Alessandro Piovaccari, Sr. VP & CTO, Silicon Labs, USA

Alain Serge Porret, VP, CSEM, Switzerland

Chirag Bhavsar, Sr. Manager, Amazon, USA

Abstract: Well... It's been 4 years since our RFIC 2015 lunchtime panel "The Internet of Things (IoT) — What's All the Hype?", so has the market for IoT devices been exploding since then or did the hype burst? Four more years into the future — what will it look like? How will the accelerated introduction of 5G and the developments in 'big data' and artificial intelligence (AI) affect it? Can we be hopeful as RFIC designers that it will provide us with endless employment and research opportunities?

Come equipped with your own outlook and questions and join the debate with the panel of experts from the industry and academia. Hear what IoT RF industry leaders from Amazon, NXP and Silicon Labs say, as well as the experts' opinions from CSEM (Swiss Center for Electronics and Microtechnology) and Shanghai Quanray Electronics. There won't be a better place to have your lunch!

IMS/RFIC 2019 Lunchtime Joint Panel Session

Tuesday, 4 June 2019

12:00–13:15

BCEC, Room 162AB

IMS2019 Panel/Rump Sessions Chair: Matthew Morton, Raytheon, USA
RFIC2019 Panel Sessions Chair: Donald Y.C. Lie, Texas Tech University, USA

Will Artificial Intelligence (AI) and Machine Learning (ML) Take Away my Job as an RF/Analog Designer?

Panel Organizers and Moderators:

Osama Shana'a, *MediaTek, USA*

Francois Rivet, *University of Bordeaux, France*

Panelists: **Ron Rohrer**, *Professor, Southern Methodist University, USA*

Taylor Hogan, *Senior Architect, Cadence, USA*

Thomas Rondeau, *DARPA MTO Program Manager, USA*

Paul Franzon, *Professor, North Carolina State University, USA*

Modi Sankalp, *MathWorks, USA*

Abstract: Machine learning (ML) and artificial intelligence (AI) are no longer futuristic concepts. They are already making their marks not only in applications that are purely data-analytics related, but also in communications, transportation, navigation, autonomous driving, finance, e-commerce, gaming, and many more fields. For example, ML/AI have already replaced humans in driving cars/trucks and in store cash registers. With AI also entering our territory of RF system and IC development, should we expect that our jobs as ‘conventional’ designers will soon be taken away? What will future RF systems and ICs be like, with AI being incorporated in them, as well as in the tools used to design them?

Our distinguished panelists from academia, DARPA, CAD/EDA, and RF industries will debate what we may expect to see in the near and distant future, and how we should prepare ourselves for the inevitable realities. You don't want to miss this!

RFIC 2019 Technical Lecture

Sunday, 2 June 2019

11:45–13:15

BCEC, Room 160ABC

Chair: Danilo Manstretta, Università di Pavia, Italy

This year the RFIC Symposium Sunday Program offers a new educational experience for the attendees. The Technical Lecture is an interactive course delivered by a distinguished speaker during lunchtime. Participants will have the opportunity to take an on-line test and will receive a Certificate of Attendance from IEEE Educational Activities. Admission is included with all RFIC Sunday workshops at no added cost and requires only a nominal fee for others, however don't forget to register early since seats will be limited to the first 250 registrants!

Fundamentals of mm-Wave IC Design in CMOS

Speaker: **Ali Niknejad**, *Professor, University of California, Berkeley, USA*



Abstract: CMOS technology advances have enabled CMOS to operate in the mm-wave spectrum, opening the potential for low cost consumer applications of mm-wave technology including ultra-high-speed networking, gigabit mobile communication, for example 5G New Radio (NR), and automotive radar for enhanced safety and autonomous driving vehicles. Making CMOS operate in the mm-wave bands requires more than a transistor, as passive devices play an equally important role in making the performance of such devices realizable. This tutorial will review key performance metrics for key building blocks (gain, low noise, power) and how to realize such performance using a modern CMOS technology node. Electromagnetic co-design of active and passive circuits and utilization is emphasized in the tutorial.

WORKSHOPS AND SHORT COURSES

Workshops and Short Courses are offered on Sunday, Monday and Friday at the Boston Convention and Exhibition Center. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 2 JUNE 2019

WSA (Full-day): Sunday 08:00–17:15

Microwave Materials: Enabling the Future of Wireless Communication

Sponsor: **IMS**

WSB (Full-day): Sunday 08:00–17:15

RF Circuit Design: Device Technologies for Tomorrow

Sponsor: **RFIC**

Organizers: **F. Rivet**, *University of Bordeaux*
G. Hueber, *Silicon Austria Labs*
T. LaRocca, *Northrop Grumman*

Abstract: The 5G and IoT future, with enhanced Mobile Broadband (eMBB), ultra-reliable low-latency self-driving car communication and Massive Machine learning, are driving RFIC designers to discover and investigate new design techniques using state-of-the-art technology. This workshop will provide the community in-depth understanding of new and underlying FDSOI CMOS capability (extended back biasing, flip-well, etc.), FinFET and GaN technologies, followed by advanced RFIC examples such as high-speed direct RF sampling and 60GHz CMOS. An introduction to emerging 3D and heterogeneous technology combining high-speed InP with digital CMOS for RFIC will provide both the experienced designer and early researchers attendee with a broad and deep overview of technology for next-generation RFIC design.

Speakers:

1. “State-of-the-Art Analog, RF and mm-Wave Design Techniques Using 28nm FD-SOI CMOS, or How the Life of the Analog/RF Designer Became Brighter!”, **A. Cathelin**, *STMicroelectronics*
2. “Body Biasing in 28nm UTBB FD-SOI CMOS Technology — A Device Approach to the Circuit Design”, **M. Videnović-Mišić**, *Silicon Austria Labs*
3. “mm-Wave Radar Circuit Design Techniques in FDSOI CMOS Technology”, **A. Bellaouar**, *GLOBALFOUNDRIES*
4. “Opportunity of CMOS FD-SOI from IoT to 5G”, **B. Martineau**, *CEA-Leti*

5. “Solving the 5G Data Transport Layer Problem with mm-Wave CMOS Products”, **J. Laskar**, *MAJA Systems*
6. “Driving Silicon to Limit: mm-Wave Solution with FinFET Technology”, **H.J. Lee**, *Intel*
7. “Heterogeneous Integration Using the Dielet Approach for IoT and 5G”, **S.S. Iyer**, *University of California, Los Angeles*
8. “On-Chip Circulators from DC to RF with Direct Sampling GaN Switches”, **Y.E. Wang**, *University of California, Los Angeles*

WSC (Full-day): Sunday 08:00–17:15

Recent Advances in

Integrated Antenna-in-Package and Antenna-on-Chip Technologies and Techniques for 5G, Radar, and Emerging mm-Wave Applications

Sponsor: **RFIC**

Organizers: **A. Natarajan**, *Oregon State University*
E. Balboni, *Analog Devices*

Abstract: Interfacing mm-wave ICs with antennas remains a critical challenge for emerging mm-wave communication, sensor, and radar transceivers. This workshop will focus on the integration of antenna, antenna-arrays and antenna interfaces for microwave and mm-wave sensors and communications applications. The state-of-the-art in Antenna-in-Package (AiP) technology, targeting 5G arrays and 77GHz automotive radar, will be presented. In addition, the workshop will explore emerging Antenna-on-Chip (AoC) approaches focusing on techniques for improved efficiency, bandwidth and manufacturability. Such approaches include combining lenses and superstrates with on-chip antennas, multi-port antennas on high-resistivity substrates as well as micromachining techniques to minimize substrate losses and maximize antenna efficiency and bandwidth. Techniques to further extend system-level performance using antenna-IC co-integration and multi-port driven radiators will also be discussed. Workshop participants should get a very good overview of integrated antenna performance and limitations from this workshop.

Speakers:

1. “Antenna-IC Interfaces for Scalable mm-Wave Arrays for 5G and Beyond-5G Applications”, **A. Natarajan**, *Oregon State University*
2. “Embracing the ‘Half-Wavelength’ Challenge in Terahertz Regime: Radiator and Receiver 2D Arrays with Large Scale and High Density”, **R. Han**, *MIT*
3. “Multi-Port Integrated Antennas and Transceiver Architectures for Antenna-Level Signal Processing for Future mm-Wave Systems”, **K. Sengupta**, *Princeton University*
4. “Antenna-Electronics Co-Design — Multi-Feed Antennas Based mm-Wave Front-Ends for On-Antenna Power Combining, Active Load Modulation, and Polarization-Division-Duplex Communication”, **T. Chi**, *Rice University*

5. “W-Band Antenna-in-Package and Phased Array Module Integration for Portable Polarimetric Imaging”, **A. Valdes-Garcia**, *IBM T.J. Watson Research Center*
6. “Integration of On-Chip and On-Board Antennas and Arrays for 100–600GHz CMOS Transceivers”, **E. Socher**, *Tel Aviv University*
7. “mm-Wave Packaging and Antenna Integration for 5G Applications and Beyond”, **T. Kamgaing**, *Intel*
8. “The Limits of Antenna & Interconnect Integration for Large-Scale Phased Arrays”, **S. Shahramian**, *Nokia Bell Labs*

WSD (Half-day): Sunday 13:30–17:15
**State-of-the-Art RF Receivers: Leading Edge Industrial Architectures
 and New Systems on the Horizon**

Sponsor: **RFIC**

Organizers: **F. Lee**, *Verily Life Sciences*
R. Harjani, *University of Minnesota*

Abstract: Four engaging technical leaders from industry and academia will cover the latest in high-performance RF receiver architectures. To frame the workshop, Dr. Jon Strange will present the latest advancements in commercial receiver ICs and wireless systems. The following three speakers will cover receiver techniques on the horizon: Dr. Tong Zhang will share self-interference cancellation techniques in frequency-division-duplex and full-duplex receivers; Dr. Peter Kinget will motivate compressed sensing systems for interference detection; and Dr. Ramesh Harjani will discuss how N-path mixer-first receivers are used for spread-spectrum interference mitigation. Finally, to adjourn the workshop, a short but lively panel discussion will be moderated to discuss the likely future of RF receiver architectures.

Speakers:

1. “Architectures and Circuits for Cellular Receivers: An Industrial Perspective”, **J. Strange**, *MediaTek*
2. “Self-Interference Cancellation Techniques in Frequency-Division-Duplex (FDD) and Full-Duplex (FD) Receivers”, **T. Zhang**, *Verily Life Sciences*
3. “Compressed Sensing Based Radio Architectures for Rapidly Finding Interferers in the Spectral and Spatial Domains”, **P.R. Kinget**, *Columbia University*
4. “Spread-Spectrum In-Band Interference Mitigation Techniques Using N-Path Mixer-First Designs”, **R. Harjani**, *University of Minnesota*

WSE (Full-day): Sunday 08:00–17:15
Analog and RF Hardware Security:
Motivation, Challenges, and Solutions

Sponsor: **RFIC**

Organizers: **A. Fayed**, *The Ohio State University*
 B. Sadhu, *IBM T.J. Watson Research Center*
 J.J. McCue, *Air Force Research Laboratory*

Abstract: Powerful design, characterization, and implementation tools of electronic devices have become easier than ever to acquire by commercial and government entities alike. This, along with the know-how of electronic design becoming globally accessible, opens the door to various activities that pose serious security risks. Some of these activities are incentivized only by commercial interests and profit, such as counterfeiting and IP theft, and others are driven by more malicious motives such as spying on, disrupting of, or interfering with the operation of a system. Regardless of the motivation, the question of how to improve the immunity of electronic devices to nefarious activities is a pressing one. This workshop discusses the security challenges associated with the analog, RF, and power portions of electronic systems, their place in the grand scheme of hardware security, why they are particularly vulnerable, how they can be exploited, and potential ways to address their security vulnerabilities.

Speakers:

1. “The Landscape of Analog Hardware Security”, **B. Dupaix, J.J. McCue**, *Air Force Research Laboratory*
2. “Obfuscation of Analog IPs”, **S. Ghosh**, *Pennsylvania State University*
3. “Securing Analog Intellectual Property: Split Manufacturing, PUFs, and Beyond”, **I. Savidis**, *Drexel University*
4. “Using Analog Side-Channel Signals for Malware and Hardware Trojan Detection”, **A. Zajić**, *Georgia Tech*
5. “Exploiting On-Chip Power Management for Side-Channel Security”, **S. Mukhopadhyay**, *Georgia Tech*
6. “Analog Mixed Signal Approaches to IC Security”, **N. Maghari**, *University of Florida*
7. “Securing RF/Analog Circuits Through Lifetime via Multi-Variate Authentication and Identification”, **S. Ozev, J. Kitchen**, *Arizona State University*
8. “Statistical and Machine Learning-Based Solutions for Trusted and Secure Analog/RF ICs”, **Y. Makris**, *University of Texas at Dallas*

WSF (Full-day): Sunday 08:00–17:15

5G mm-Wave to Sub-THz Circuit and System Techniques

Sponsor: **RFIC**

Organizers: **M. Wiklund**, *Qualcomm*
 D. Belot, *STMicroelectronics and CEA-Leti*
 P. Busson, *STMicroelectronics*

Abstract: For more than a decade mm-wave has been a technology waiting to take off. We have 5G, radar, 802.11ay and many more product scenarios than when 802.15.3c (WPAN) was drafted. This workshop will present state-of-the-art circuits and techniques for 5G mm-wave to sub-THz that are driving product development now and in the near future. Where are we today in terms of circuit design? Which technology, which spectrum allowance, which standardization?

Speakers:

1. “5G and Beyond 5G Roadmap: What is Forecast in the Next Decade(s) for mm-Wave and THz Communications”, **E. Calvanese Strinati**, *CEA-Leti*
2. “Silicon Based Transceivers for High Data Rate mm-Wave Communications Targeting Beyond 5G Spectrum”, **K. Okada**, *Tokyo Institute of Technology*
3. “Silicon Based High Data Rate mm-Wave Links for Short and Medium Range Communications”, **A. Arbabian**, *Stanford University*
4. “CMOS THz Imager for Security and Health Applications”, **H. Sherry**, *TiHive*
5. “Silicon Based THz Source and Imager for Health Applications”, **A. Siligaris**, *CEA-Leti*
6. “III-V and SiGe Transceivers for High Data Rate mm-Wave Communications Targeting Beyond 5G Spectrum”, **H. Zirath**, *Chalmers University of Technology*
7. “mm-Wave Phased-Arrays for 5G Systems”, **G.M. Rebeiz**, *University of California, San Diego*
8. “mm-Wave to Sub-THz High Data Rate Links for 5G and Beyond”, **Y. Li**, *Ericsson*

WSG (Full-day): Sunday 08:00–17:15

Electronic-Photonic Integrated Systems for Lidar and Sensing

Sponsor: **RFIC**

Organizers: **H. Hashemi**, *University of Southern California*
 H. Krishnaswamy, *Columbia University*

Abstract: Complex electronic-photonic integrated systems for fiber optical communication applications are now produced commercially at high volume. In particular, the silicon photonic integrated system ecosystem, including foundry processes, design tools, and packaging, has greatly matured over the past few years. The silicon photonic market alone is estimated to be worth \$500M in 2018, \$1B in 2020, and over \$2B by 2024 [Source: Yole Développement]. A large number of

other applications can benefit from electronic-photonics integrated systems, in particular within the silicon photonic technology platform. Three-dimensional (3D) cameras, already used in iPhone X, can become mainstream in smartphones. Solid-state infrared lidars can enable low-cost sensors for self-driving cars and drones. Electronic-photonics integrated sensors may be used in biomedical applications. This workshop brings some of the prominent researchers from academic and industrial research labs to cover the latest advancements of electronic-photonics integrated systems with emphasis on sensors.

Speakers:

1. “Integrated Photonics for Lidar, RF Signal Processing, and Quantum Sensing”,
C. Sorace-Agaskar, *MIT Lincoln Laboratory*
2. “Optical Frequency Synthesis and Control: From Communication to Sensing”,
F. Aflatouni, *University of Pennsylvania*
3. “Integrated Electro-Optical PLL for Linear FMCW Modulation of a Tunable Laser”,
B. Behroozpour, *Robert Bosch*
4. “Integrated Opto-Electronic Phase Locked Loops for High Performance Lidar”,
H. Krishnaswamy, *Columbia University*
5. “Recent Progress Toward Automotive Lidar on a Chip”, **L. Maleki**, *Cruise Automation*
6. “Silicon Arrays and Sensors: Opportunity, Progress, and Challenge”, **A. Hajimiri**,
Caltech
7. “Lidar and Beam Steering Technologies Based on Silicon Photonics”, **M. Lipson**,
Columbia University
8. “Optical Phased Arrays”, **H. Hashemi**, *University of Southern California*

WSH (Full-day): Sunday 08:00–17:15

Power Amplifier and Transmitter Designs for Emerging Sub-6GHz 5G Communications

Sponsor: **RFIC**

Organizers: **D. Chowdhury**, *Broadcom*
 J.S. Walling, *Tyndall National Institute*

Abstract: It is suggested that 5G communications will be comprised of a combination of the existing cellular and ISM bands in the sub-6GHz spectrum, along with near mm-wave bands (e.g., K and Ka) and mm-wave bands (e.g., W and V). This workshop focuses on power amplifier and transmitter designs and architectures in the sub-6GHz spectrum that can include highly digital architectures (DPAs, charge-based TX), as well as architectural innovation (e.g., Cartesian combiners and magnetic free circulators). To explore the pathways that will enable 5G communications, the workshop will highlight recent trends in PAs and transmitters that can be used to enable digital beamforming, multi-beam TX, enhanced energy efficiency and linearity. Additionally, we will explore the emerging topics of coexistence and simultaneous transmit and receive (i.e. full-duplex operation).

Speakers:

1. “Duplexing and Co-Existence in Emerging RF Wireless Systems”, **H. Krishnaswamy**, *Columbia University*
2. “Analog and Digital Wideband Envelope Tracking for 5G”, **J. Yan¹, T. Nakatani¹, P. Theilmann¹, D. Kimball², I. Telliez¹**, ¹*MaXentric Technologies*, ²*University of California, San Diego*
3. “Modulating Transmitter Power Supplies for Improved Battery Life in Wideband Applications”, **D. Chowdhury**, *Broadcom*
4. “Bits-In RF-Out Transmitters”, **M.S. Alavi, L. de Vreede**, *Technische Universiteit Delft*
5. “Energy-Efficient and Area-Saving Techniques in Digital Power Amplifiers”, **H. Xu**, *Fudan University*
6. “A Digital Transmitter Based on Class-G Quadrature Switched-Capacitor Power Amplifier with Efficiency Enhancement and Linearization Techniques”, **S.M. Yoo**, *Michigan State University*
7. “Emergent Reconfigurable DPAs and Beamforming Transmitters for 5G”, **J.S. Walling, A. Azam, Z. Bai, W. Yuan**, *University of Utah*

WSI (Full-day): Sunday 08:00–17:15
Design Challenges in 5G IoT

Sponsor: **RFIC**

Organizers: **G. Hueber**, *Silicon Austria Labs*
 H.M. Lavasani, *Case Western Reserve University*
 Y.H. Liu, *Holst Centre*

Abstract: The 5G and IoT future with enhanced Mobile Broadband (eMBB), Ultra-Reliable and Low Latency Communications (URLLC) and massive Machine Type Communications (mMTC) is open for new applications in high volume deployment that will benefit from 5G’s ultra-fast networks and real-time responsiveness, such as mMTC for solar-powered nodes (street-light) or other innovations to help city-wide infrastructure, or device-to-device public safety communications without a need for cellular coverage. Novel applications and network techniques demand that RFIC designers discover and investigate new designs to allow the high volume of use-cases based on and beyond 5G. The motivation of this workshop is to capture what is the state at the edge of IoT technology, what is the demand of the industry in the context of innovation, and what are circuit and architectural concepts that are demanded or enforced by 5G IoT standardization. We focus especially on RFIC circuits design and technologies competing for today’s and tomorrow’s applications in 5G IoT.

Speakers:

1. “Evolving 5G NR to Connect the Internet of Things”, **J. Smee**, *Qualcomm*
2. “A cm-Scale Self-Powered Intelligent & Secure IoT Edge Mote Featuring an Ultra-Low-Power Wake-Up-Radio in 14nm Trigate CMOS”, **D. Kurian**, *Intel*
3. “What is Required of 5G to Make it Attractive for IOT?”, **Y.H. Liu**, *imec*

4. “ULP Radios and Their Application in 5G IoT”, **D. Wentzloff**, *University of Michigan*
5. “Ultrasound-Enabled Connectivity for Next-Generation IoT Systems”, **A. Rekhi**, *Stanford University*
6. “Benefits of 22FDX for NB-IOT RF Integration”, **T. McKay**, *GLOBALFOUNDRIES*
7. “How Silicon Technology can Address 5G IoT Challenges”, **F. Ganesello**, *STMicroelectronics*
8. “mm-Wave Wireless Powered IoT”, **H. Gao**, *Technische Universiteit Eindhoven*

WSJ (Full-day): Sunday 08:00–17:15
Quantum Computing for RFIC Engineers:
Concepts, Devices, Systems, and Opportunities

Sponsor: **RFIC**

Organizers: **J.C. Bardin**, *UMass Amherst*
M. Babaie, *Technische Universiteit Delft*

Abstract: As the field of quantum computing continues to grow, numerous opportunities will emerge for RFIC designers to contribute. For instance, quantum processors are typically interfaced to using microwave control and readout, and, for the field to continue to succeed, these interfaces must be simplified and integrated. The goal of this workshop is, first to provide enough background so that the need for RFIC designers is clear, and then to describe the current state-of-the-art in quantum computing hardware as well as where the field is heading. The workshop will begin with a tutorial designed to introduce RF circuit designers to the field of quantum computing. Following this, world experts will present research spanning a wide range of topics including CMOS-compatible qubit technology, quantum limited amplification, microwave qubit readout, CMOS RFICs for quantum computing, and system-level challenges related to building a practical quantum computer.

Speakers:

1. “An Introduction to Quantum Computing for RFIC Engineers”, **J.C. Bardin**¹, **D. Sank**²,
¹*UMass Amherst*, ²*Google*
2. “Si MOS-Based Spin Qubits for Quantum Computing”, **L. Hutin**, *CEA-Leti*
3. “An Introduction to Parametric Amplifiers for Superconducting Quantum Information”,
J. Aumentado, *NIST*
4. “Adapting Microwave Control to Evolving Quantum Computers”, **D. Ristè**, *Raytheon*
5. “Scaling Up of Quantum Computers: the Importance of Interconnects and Fast Electrical Characterization”, **J.S. Clarke**, *Intel*
6. “Cryogenic CMOS Interfaces for Quantum Computers”, **F. Sebastiano**, *Technische Universiteit Delft*
7. “System Design Considerations for Noisy Intermediate-Scale Quantum Machines”,
M. Reagor, *Rigetti Computing*

WSK (Full-day): Sunday 08:00–17:15
Efficient mm-Wave Power Amplifier Design for
5G and Wireless Broadband Transmitters

Sponsor: **RFIC**

Organizers: **J. Kitchen**, *Arizona State University*
 O. Eliezer, *PHAZR*
 D.Y.C. Lie, *Texas Tech University*

Abstract: There is a growing demand for high data rate, short-range communications to support near-future 5G networks and wireless broadband networks (WLAN), with speculation that 50 billion mm-wave wireless devices will be deployed worldwide by 2024. These transceivers will require mm-wave power amplifiers (PAs) that operate at frequencies well above 10GHz and support wide instantaneous bandwidths. This workshop brings together experts from academia and industry to highlight recent works and performance trends in mm-wave PAs; detail advanced architectures and design concepts using silicon CMOS, FINFETs, and GaN; discuss techniques to maintain high PA efficiency at mm-wave while meeting the stringent 5G linearity requirements; and introduce new PA architectures to achieve broadest reported bandwidths. Additionally, this workshop examines process technology and assembly limitations for delivering power at these high frequencies, with comparisons between silicon, GaN, and GaAs processes.

Speakers:

1. “mm-Wave Power Amplifiers in Silicon — State-of-the-Art and Several Recent Architecture/Circuit Examples”, **H. Wang**, *Georgia Tech*
2. “Broadband PA Design in CMOS and SOI for 5G Applications”, **P. Reynaert**, *Katholieke Universiteit Leuven*
3. “mm-Wave Power Amplifiers in FINFET Technology”, **C. Hull**, *Intel*
4. “High-Efficiency RF-PA Supply Modulation Techniques for mm-Wave Amplifiers”,
J.S. Paek, *Samsung Electronics*
5. “mm-Wave GaN PAs for 5G High-Performance Transmitters”, **E. Leclerc**, *United Monolithic Semiconductors*
6. “GaN and GaAs Process Technologies and PA Architectures to Support mm-Wave Frequencies”, **E. Reese**, *Qorvo*
7. “mm-Wave Power — What Can GaN Do?”, **M. Siddiqui**, *Northrup Grumman*
8. “Design Considerations for Sub-6GHz 5G Power Amplifiers”, **T. Faughn**, *Skyworks Solutions*
9. “Summary and Highlights of Our mm-Wave Broadband PA Design Workshop”,
D.Y.C. Lie¹, **O. Eliezer**², ¹*Texas Tech University*, ²*PHAZR*

WSL (Full-day): Sunday 08:00–17:15

Integrated Phased Array ICs for 5G and Beyond

Sponsor: **RFIC**

Organizers: **E. Afshari**, *University of Michigan*
H. Xu, *Fudan University*

Abstract: Future applications, such as 5G, SatCom, AR/VR and radar imaging, need a large-scale array system. Such a system requires highly integrated RFICs for the growing channel number, easy system integration and cost/area optimization. This workshop addresses key design challenges in components, integration and overall system in such systems. The focus would be on manufacturing friendly techniques for interfacing mm-wave arrays with antennas both for single-element and large-scale arrays, and will also help to understand evolution from Phased Arrays to MIMO Arrays.

Speakers:

1. “Silicon Phase Arrays: Past, Present, and Future”, **A. Hajimiri**, *Caltech*
2. “RF/mm-Wave FEM Applications with SOI/SiGe Processes”, **C. Li**, *GLOBALFOUNDRIES*
3. “Hybrid Beamforming-MIMO Architectures Leveraging Best of Both Worlds for 5G and Beyond”, **P. Heydari**, *University of California, Irvine*
4. “mm-Wave CMOS Phased-Array Transceiver for 5G New Radio”, **K. Okada**, *Tokyo Institute of Technology*
5. “Integrated RFICs in mm-Wave Array Systems for 5G and Beyond”, **S. Shahramian**, *Nokia Bell Labs*
6. “mm-Wave and Terahertz Signal Generation, Amplification, and Beam Steering in Silicon”, **O. Momeni**, *University of California, Davis*
7. “Fully-Integrated 94GHz Dual-Polarized TX and RX Phased Array ICs for 3D Real-Time Radar Imaging Applications”, **W. Lee**, *IBM T.J. Watson Research Center*

WSM (Full-day): Sunday 08:00–17:15

Sensors and Connectivity Enabling Autonomous Cars

Sponsor: **RFIC**

Organizers: **H. Hedayati**, *MACOM*
M. Ali, *Ubnder*
R. Han, *MIT*

Abstract: Autonomous driving has the potential to revolutionize not only transportation but also the entire society. Every year, more than a million lives are cut short due to traffic accidents.

Autonomous driving could significantly reduce these fatalities and improve the quality of life for millions of commuters. The intelligence behind such technology based on artificial intelligence and machine learning will rely on a number of advanced sensors and connectivity nodes generating and processing large amounts of data. This workshop will delve into the latest technologies that enable self-driving cars, focusing on sensing and connectivity and their impact on RFIC requirements and design.

Speakers:

1. “The Sensor Landscape for Automated Driving”, **B. McIntosh**, *Infineon Technologies*
2. “Digital Modulation: A Breakthrough in Radar Enabling High Performance at Lowest Cost”, **R. Reuter**, *Ubnder*
3. “Multi-Mode Image Radar System and its Challenges”, **D. Wang**, *Texas Instruments*
4. “In-Vehicle Networking for Future Cars”, **L. Van Dijk**, *NXP Semiconductors*
5. “mm-Wave Radar Sensors for Roadside Infrastructure Enabling Autonomous Driving”, **V. Issakov, W. Lehbrink**, *Infineon Technologies*
6. “Optimizing FMCW Radar Architecture for LO Chirp Detected Noise Reduction”, **D. Elad, J. Vovnoboy**, *ON Semiconductor*

SUNDAY SHORT COURSES – 2 JUNE 2019

SSA (Full-day): Sunday 08:00–17:15

The Dynamics, Bifurcation, and Practical Stability Analysis/Design of Nonlinear Microwave Circuits and Networks

Organizers: **A. Suarez**, *Universidad de Cantabria*
C. Silva, *Aerospace*

Abstract: This full-day course addresses the fundamental topic of stability in nonlinear microwave circuits and networks (MCNs), covering concepts, qualitative analysis, simulation, and engineering design. The many unique qualitative behaviors possible in common nonlinear MCNs will be illustrated, as well as the fundamental means by which these behaviors can abruptly arise with parameter changes (termed a bifurcation). Course attendees will learn about steady-state solutions, identify instability problems through small- and large-signal stability analysis, and understand dynamical mechanisms responsible for instabilities. The primary approaches for stability analysis (classical to advanced) will be presented and compared. Practical examples of instability, stability analysis, and stabilization design will be presented for MCNs such as power amplifiers, frequency multipliers/dividers, and voltage-controlled oscillators. Finally, the vast research area on harnessing nonlinear dynamics for engineering purposes will be surveyed, providing a glimpse into future nonlinear designs. The course will include video/hardware demonstrations and several live stability analysis sessions using ADS.

SSB (Full-day): Sunday 08:00–17:15
Build a 1GHz FMCW Radar in a Day

Organizers: D.S. Ricketts, North Carolina State University

Abstract: In this practical short course you will learn the system design of a frequency modulated continuous wave (FMCW) radar. After a short theory lecture, you will participate in teams to design and build a working radar at 1GHz. Each participant will design one component of the radar and then assemble the radar as a team for testing at the end of the day. The participants will build a power amplifier, low-noise amplifier, rat-race coupler and mixer. Baseband signal generation and components will be provided. No prior experience is needed, other than general microwave engineering knowledge.

MONDAY WORKSHOPS – 3 JUNE 2019

WMA (Full-day): Monday 08:00–17:15
Exploratory Semiconductor Devices for the
5G mm-Wave Era and Beyond

Sponsor: IMS

WMB (Full-day): Monday 08:00–17:15
Low Phase Noise Oscillator and Frequency Synthesizer Techniques

Sponsor: IMS

WMC (Full-day): Monday 08:00–17:15
5G: mm-Wave Power Amplifiers & Technology Benchmarking

Sponsors: IMS, RFIC

Organizers: D. Belot, STMicroelectronics and CEA-Leti
E. Kerhervé, IMS (UMR 5218)

Abstract: 5G spectrum is presently open world-wide to sub-6GHz and mm-wave bands at 26GHz, 28GHz, and other bands at 40GHz, 60GHz (V) and 71-86GHz (E) are under evaluation in most parts of the world. Different power amplifier architectures and process technology approaches are in competition to cover these 5G opened bands. This workshop will benchmark the state-of-the-art power amplifier techniques targeting mm-wave frequency for 5G applications, and will present the

status of different processes addressing the power amplifier applications such as silicon based, III-V, GaN and InP technologies. Finally we will discuss the match between these technologies' specificities and the different 5G application requests.

Speakers:

1. "Design Considerations for 5G mm-Wave Transmitters and Power Amplifiers", **S. Andersson, S. Mattisson, F. Tillman**, *Ericsson*
2. "mm-Wave InP Power Amplifier for High Speed Wireless Communications", **H. Hamada**, *NTT*
3. "mm-Wave GaN MMIC PA Design for High Efficiency and High Power", **Z. Popović**, *University of Colorado Boulder*
4. "PA Design in Silicon (SiGe & CMOS) and Other III-V Processes for Advanced Beamformed Applications", **E. Kerhervé¹, V. Knopik²**, ¹*IMS (UMR 5218)*, ²*STMicroelectronics*
5. "Wideband GaN-Based Supply-Modulated Power Amplifier Systems", **O. Bengtsson, S. Paul, S. Preis, N. Wolff**, *FBH*
6. "Transmitter Architectures for PA Efficiency", **E. McCune**, *EMC2*
7. "5G High Power RF Front-End Solution for Ka-Band", **M. Ayad**, *UMS*
8. "Process Technology Benchmarking for mm-Wave PA", **D. Belot**, *STMicroelectronics and CEA-Leti*

WMD (Full-day): Monday 08:00–17:15
Measurement and Design Techniques for
Next-Generation Communication Systems

Sponsors: **IMS, ARFTG**

WME (Full-day): Monday 08:00–17:15
mm-Wave Power Amplifier Design Innovations

Sponsors: **IMS, RFIC**

Organizers: **E. Niehenke**, *Niebenke Consulting*
J. Pierro, *Telephonics*
R. Quay, *Fraunhofer IAF*

Abstract: mm-Waves have found uses for radar, communications, and most recently in 5G applications and beyond. Power amplifiers are limiting components due to their energy consumption, bandwidth limitation, and gain limitation. This workshop will focus on recent innovations in power amplifier IC design techniques with specific emphasis on their realization at mm-wave frequencies. These include design and layout techniques for efficiency enhancement, linearity improvements,

thermal management, memory effects, and bandwidth and gain extension. Many of these state-of-the-art improvements can be linked to power amplifier device technology whose great variety will be covered including SOI, GaN, GaAs, SiGe, and CMOS as those differ drastically in their active and passive capabilities and available design features.

Speakers:

1. “GaN Technology is Revolutionizing mm-Wave Power”, **J. Schellenberg**, *QuinStar Technology*
2. “Wideband Design Techniques for mm-Wave Gallium Nitride MMICs”, **R. Quay, M. Ćwikliński, P. Brückner**, *Fraunhofer IAF*
3. “mm-Wave InP HEMT Power Amplification”, **W.R. Deal**, *Northrop Grumman*
4. “Methodology of High Efficiency mm-Wave GaN Power Amplifiers”, **H.P. Moyer**, *HRL Laboratories*
5. “RF to mm-Wave CMOS-SOI Power Amplifiers”, **S. Mohammadi**, *Purdue University*
6. “Power Amplifiers for 5G mm-Wave Applications”, **P. Asbeck**, *University of California, San Diego*
7. “HBT and CMOS Outphasing Power Amplifiers for mm-Wave Applications”, **J.F. Buckwalter**, *University of California, Santa Barbara*

WMF (Full-day): Monday 08:00–17:15
Measurement Challenges in Over-The-Air Testing

Sponsors: **IMS, ARFTG**

WMG (Half-day): Monday 08:00–11:50
Advanced Packaging Technologies for
High-Performance 5G Front-End Modules

Sponsor: **IMS**

WMH (Half-day): Monday 13:30–17:15
Recent Advancement and Trends in
3D Heterogeneous Integration for mm-Wave 5G and Terahertz

Sponsor: **IMS**

WMI (Full-day): Monday 08:00–17:15
Digital Signal Processing for Radio Frequency Identification

Sponsor: **IMS**

WMJ (Full-day): Monday 08:00–17:15
Advanced Nonreciprocal Technologies for High-Frequency Applications based on Novel Approaches and Nanoscale Concepts

Sponsor: **IMS**

WMK (Full-day): Monday 08:00–17:15
RF Integrated Magnetics – Devices, Integration and Applications

Sponsor: **IMS**

MONDAY SHORT COURSES – 3 JUNE 2019

SMA (Full-day): Monday 08:00–17:15
Demystifying Noise Parameter Measurements and Model Extraction

Organizers: **L. Dunleavy**, *Modelithics*
S. Dudkiewicz, *Maury Microwave*

Abstract: In modern communications systems, receivers are required to detect and receive very small signals, and at the same time not add a significant level of noise, otherwise the information contained within the signals may be overpowered and become unusable. In order to minimize the amount of added noise, low-noise circuit design becomes critical, and highly effective designs begin with accurate noise parameters or noise models. Noise parameters measurements and noise model extraction are extremely sensitive techniques, and the measurement/extraction system can itself become the dominant contributor of noise if the system is not calibrated accurately. Therefore understanding the sources of error, and using the best techniques and practices, is critical when attempting to accurately characterize noise parameters and extract a noise model. This short course aims to demystify noise parameter measurements and model extraction, and includes topics such as: an introduction to noise figure and noise parameter concepts; noise parameter calibration; measurement and extraction techniques and best practices; how to validate noise parameter data; an in-depth review of critical variables that affect the accuracy of noise parameter measurements; noise parameter de-embedding; and noise model theory and extraction.

FRIDAY WORKSHOPS – 7 JUNE 2019

WFA (Full-day): Friday 08:00–17:15

**Electroceuticals: Technologies and Modeling for
Electromagnetically-Mediated Medical Treatments**

Sponsor: **IMS**

WFB (Full-day): Friday 08:00–17:15

**The Analog vs. Digital Battle – A Fight of Paradigms to Optimize
Systems & PA Solutions for Wireless Infrastructure in 5G and Beyond**

Sponsor: **IMS**

WFC (Full-day): Friday 08:00–17:15

Towards a One-Chip Solution for GaN Front-Ends

Sponsor: **IMS**

WFD (Full-day): Friday 08:00–17:15

In-Band Full-Duplex Technologies and Applications

Sponsor: **IMS**

WFE (Full-day): Friday 08:00–17:15

**System Concepts and Digital Signal Processing for
Advanced Microwave Sensors and Imagers**

Sponsor: **IMS**

WFF (Full-day): Friday 08:00–17:15
Advanced Radar Systems for
Industrial, Medical and Consumer Applications

Sponsors: **IMS, RFIC**

Organizers: **J. Reinstädt**, *Infineon Technologies*
R. Weigel, *FAU Erlangen-Nürnberg*
V. Issakov, *Infineon Technologies*

Abstract: Radar sensors are used extensively almost everywhere to make daily life more comfortable and safe. Recent advances in silicon-based semiconductor technologies and packaging solutions enable the realization of cost-efficient low-power highly-integrated mm-wave radar sensor systems. In this full-day workshop we will discuss emerging (non-automotive) radar applications focusing on industrial, medical and consumer electronics, operating at mm-wave frequencies. Distinguished speakers from leading companies and academia will present a wide range of topics spanning from chip design of highly-integrated radar transceivers in silicon-based technologies, advanced system architectures (e.g. interferometry or MIMO radar), state-of-the-art and future trends on radar modulation techniques (e.g. FMCW using Micro-Doppler effect, PMCW, OFDM, Pulse-Doppler-Radar) up to the emerging applications (e.g. gesture recognition, object classification, glucose detection, vital sign monitoring). A brief concluding discussion will round-off the workshop to summarize the key learnings on the wide range of aspects presented during the day.

Speakers:

1. “Low-Power mm-Wave Sensors in CMOS and SiGe Technology”, **S.P. Voinigescu¹, J. Hasch²**, ¹*University of Toronto*, ²*Robert Bosch*
2. “UaV Detection Using Low-Cost 5G Phased-Arrays”, **A. Wang, T. Phelps, K. Kibaroglu, M. Sayginer, G.M. Rebeiz**, *University of California, San Diego*
3. “Highly-Integrated mm-Wave Radar Transceivers for Industrial and Consumer Applications”, **V. Issakov**, *Infineon Technologies*
4. “Zero-Effort Health Monitoring Using Radar Systems”, **G. Shaker**, *University of Waterloo*
5. “Radar-Based Vital Sign Monitoring”, **F. Michler, R. Weigel**, *FAU Erlangen-Nürnberg*
6. “Modulated Reflectors in Applications for Localization and as Low-Cost Radar Target Simulator”, **A. Stelzer¹, W. Scheiblhofer¹, A. Haderer²**, ¹*Johannes Kepler Universität Linz*, ²*Inras*
7. “Imaging MIMO Radar for Home Monitoring”, **V. Giannini**, *Ubnder*
8. “Multistatic MIMO OFDM Radar”, **B. Nuss, T. Zwick, M. Pauli**, *KIT*
9. “High Resolution 140GHz MIMO Radar for Contact-less Vital Sign Monitoring and Hand Gesture Recognition”, **A. Bourdoux**, *imec*
10. “Pulsed Radar for Various Applications”, **Y. Aoyagi**, *Furukawa Electric*
11. “Interferometric Industrial Distance Sensing by Six-Port Technology”, **A. Koelpin**, *Brandenburgische Technische Universität*
12. “Signal Processing Solutions for Object Detection, Tracking, and Classification using 60GHz FMCW Radar”, **M. Yan, M. Livshitz, A. Purkovic**, *Texas Instruments*

WFG (Half-day): Friday 13:30–17:15
Microwave Engineering Applications of
Machine Learning: Past, Present and Future

Sponsor: **IMS**

WFH (Half-day): Friday 08:00–11:50
Challenges for mm-Wave Remote Radio Units in 5G Infrastructure

Sponsor: **IMS**

SOCIAL EVENTS/GUEST PROGRAM

SUNDAY, 2 June 2019

RFIC Welcoming Reception: 19:00–21:00

RFIC2019 starts with a welcome event on Sunday for all attendees, which will be hosted at the Boston Convention and Exhibition Center immediately following the RFIC2019 Plenary Session.

MONDAY, 3 June 2019

IMS Welcome Event: 19:30–21:00

IMS2019 starts with a welcome event on Monday for all attendees, which will be hosted at the World Trade Center Headhouse immediately following the IMS2019 Plenary Session.

MONDAY, 3 June 2019 – THURSDAY, 6 June 2019

Guest Lounge: 07:00–13:00

Located at the Westin Boston Waterfront Hotel. Light refreshments will be provided for all registered guests. Registration is required.

TUESDAY, 4 June 2019

Young Professionals Panel Session: 17:30–19:00 and Networking Event: 19:30–21:30

The Young Professionals are planning a Lounge Area at the Boston Convention and Exhibition Center dedicated to Young Professionals where the panel session will be held followed by a short walk to Coppersmith for the networking event. Please refer to the conference website for detailed information on the panel session.

WEDNESDAY, 5 June 2019

Women in Microwaves Panel Session: 16:00–17:00 and Networking Event: 19:00–21:00

The Women in Microwaves Panel Session will be held at the Boston Convention and Exhibition Center room 162AB, followed by the Networking Event at the Envoy Hotel Rooftop Bar.

Industry-Hosted Cocktail Reception: 17:00–18:00

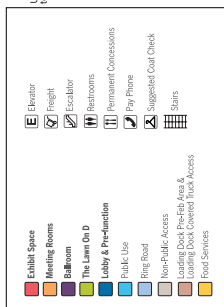
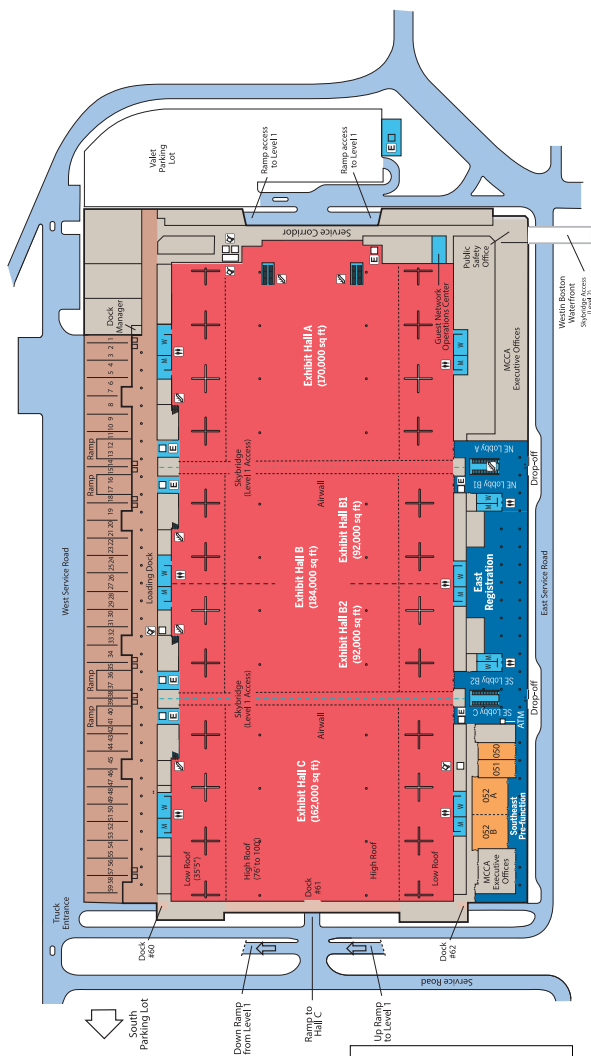
The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

Awards Banquet: 18:30–20:00

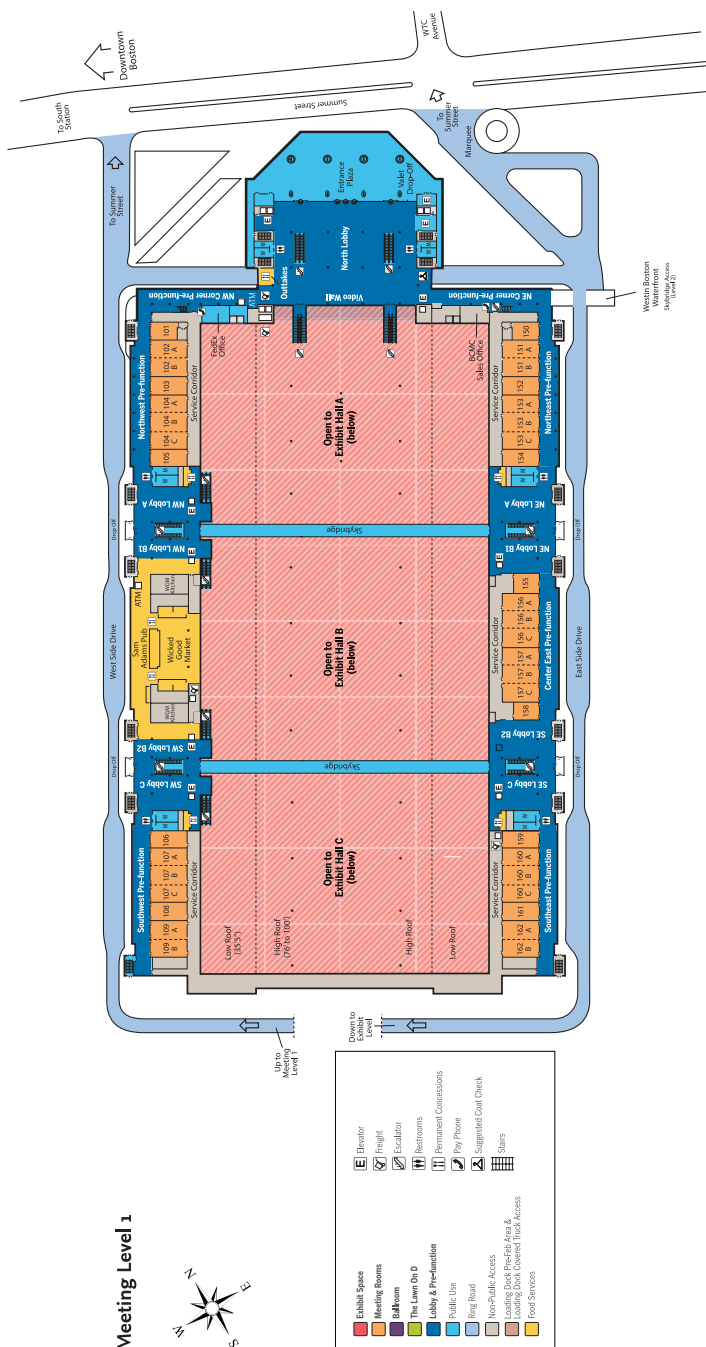
The MTT-S Awards Banquet will be hosted at the Westin Boston Waterfront Hotel Grand Ballroom and will feature exciting entertainment.

Boston Conference and Exhibition Center Maps

Exhibit Level



Boston Conference and Exhibition Center Maps (continued)



Boston Conference and Exhibition Center Maps (continued)

Meeting Level 2

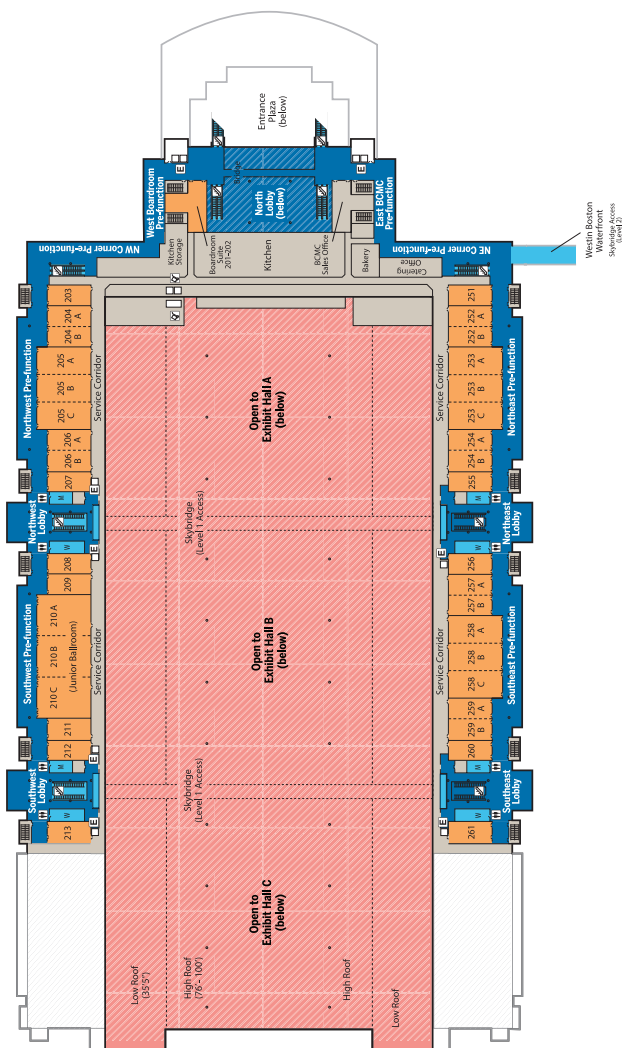
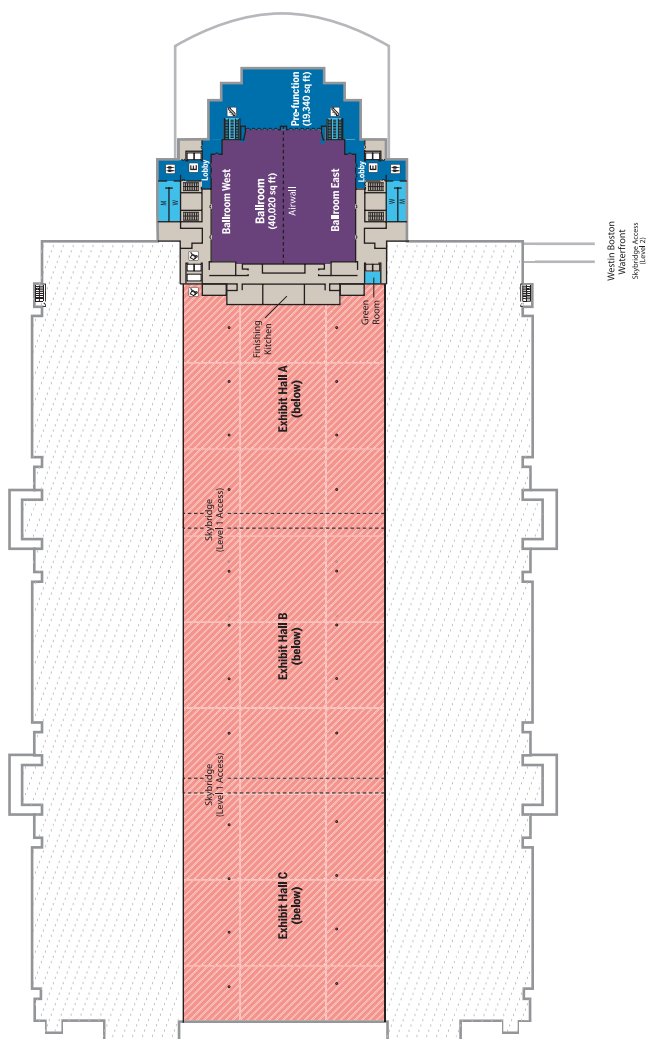


Exhibit Space	Elevator
Meeting Rooms	Escalator
Ballroom	Freight
The Lawn On D	Restrooms
Lobby & Pre-function	Permanent Concessions
Public Use	Pay Phone
Ring Road	Suggested Coat Check
New-Public Access	Stairs
Loading Dock Pre-Entry Area & Loading Dock General Truck Access	
Food Services	

Boston Conference and Exhibition Center Maps (continued)



Ballroom Level 3



	Exhibit Space		Elevator
	Meeting Rooms		Escalator
	Ballroom		Restrooms
	The Lawn On D		Permanent Concessions
	Lobby & Pre-Function		Pay Phone
	Public Use		Suggested Coat Check
	Ring Road		Stairs
	Non-Public Access		
	Loading Dock/Pre-Relief Area & Loading Dock, Covered Truck Access		
	Food Services		

NOTES

IEEE

445 Hoes Lane
Piscataway, NJ 08854, USA

2019 RFIC Symposium
Boston, Massachusetts, USA
2–4 June 2019



RFIC PROGRAM