



2018 IEEE Radio Frequency Integrated Circuits Symposium

Philadelphia, Pennsylvania, USA

10–12 June 2018



PROGRAM

Pennsylvania Convention Center
and
Loews Philadelphia Hotel

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society



RFIC Plenary, Reception, and Symposium Showcase

Sunday Evening, 10 June 2018

Pennsylvania Conference Center & Loews Philadelphia Hotel

After a busy day immersed in insightful workshops, enjoy a relaxing evening with your colleagues at these special Sunday night RFIC events, to be held in the Pennsylvania Conference Center and Loews Philadelphia Hotel.

17:30–19:00, Pennsylvania Conference Center, Ballroom — The Plenary Session kicks off the evening with the Student Paper Awards, RFIC Industry Best Paper Awards, and RFIC Tina Quach Service Award ceremony followed by two outstanding plenary speakers: Zachary J. Lemnios, the Honorable former US Assistant Secretary of Defense (Research and Engineering) and current Vice President of Physical Sciences & Government Programs at IBM Research, and Lars Reger, Senior Vice President and Chief Technology Officer of NXP's Automotive business unit.

19:00–21:00, Loews Philadelphia Hotel, Millennium Hall — RFIC Welcoming Reception Featuring Industry Showcase and Student Paper Award Finalists: Immediately following the Plenary Session is the RFIC Reception. Drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest developments in the wireless industry.

The RFIC Symposium Showcase Session, held concurrently with the RFIC Welcoming Reception, will highlight 10 selected papers submitted by authors from industry, and 11 selected papers by students from academia. From each of these groups of finalists, the top 3 will be selected and will be presented with plaques during the Plenary Session. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss microwave week's opening event. Please see <http://rfic-ieee.org/> for more details.

The RFIC Reception is sponsored by the RFIC Steering Committee and through the generous support of our corporate sponsors:

Diamond Sponsor



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RFIC Symposium Schedule (10–12 June 2018)

Event	Location	Sat 9 June	Sun 10 June	Mon 11 June	Tue 12 June
Registration	PCC, Level 2, Corridor	08:00–18:00	07:00–18:00	07:00–19:00	07:00–18:00
Workshop Speakers' Breakfast	PCC, Rooms 108AB		07:00–08:00		
Workshops & Short Courses	PCC, Rooms 102A–109A		08:00–17:30		
Workshop Lunch	PCC, Level 1, Foyer		11:30–13:30		
Plenary Session	PCC, Ballroom		17:30–19:00		
Reception & Symposium Showcase	LPH, Millennium Hall		19:00–21:00		
Interactive Forum	PCC, Exhibit Hall				13:30–15:10
Speakers' Breakfast	PCC, Rooms 108AB			07:00–08:00	
Technical Sessions	PCC, Rooms 201A, 201B, 204A			08:00–09:40 10:10–11:30 13:30–15:10 15:40–17:20	08:00–09:40 10:10–11:50
Panel Sessions	PCC, Room 201A			11:45–13:15	12:00–13:00

PCC: Pennsylvania Convention Center

LPH: Loews Philadelphia Hotel



Photo by Paul Loftland for PHICVB

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Welcome Message from Chairs

We invite you to participate in the 2018 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held in Philadelphia, Pennsylvania, on 10–12 June 2018. RFIC Symposium is the premier IC design conference focused exclusively on the latest advances in RF, Microwave and Millimeter-Wave integrated circuit (IC) technologies and designs, as well as innovations in high frequency analog/mixed-signal ICs. It is with great pleasure that we cordially invite you to participate in this global event!

The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), Automatic RF Techniques Group (ARFTG) and the Industry Exhibition to form “Microwave Week”, the largest worldwide RF/microwave technical meeting of the year. Microwave week will be held at the Pennsylvania Convention Center in the heart of downtown Philadelphia. This year, the Microwave Week will also host the International Microwave Biomedical Conference (IMBioC) that focuses on tying research in microwave and RF to applications in biological systems. Attendees will have the opportunity to interact with world experts, expand their network, and leave invigorated with new ideas and a drive to innovate.

RFIC 2018 will continue to offer a number of initiatives. The popular Industry Showcase Session, featuring poster presentations (and optional demos) of the most innovative and highly-rated industrial papers, will be the highlight during the RFIC Welcoming Reception in the evening of Sunday, 10 June 2018. The Student Paper Award Finalists will also be featured during the RFIC Welcoming Reception. The RFIC Interactive Forum will be held in the afternoon on Tuesday, 12 June 2018 along with the IMS Interactive Forum. In recognition of being selected, all of the RFIC student paper finalists will receive complimentary RFIC registration. Students may volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complimentary conference registration, meals, T-shirts, and other benefits. The joint RFIC/IMS PhD Student Sponsorship Initiative Program will continue to involve selected first and second-year PhD students in technical assignments during the conference in exchange for complimentary conference registrations, lodging and meals.

RFIC 2018 will open on Sunday, 10 June 2018, with 12 workshops (8 full-day and 4 half-day). These workshops cover a wide range of topics including: “RFIC Design in CMOS FinFET and FD-SOI”, “ICs for Quantum Computing and Quantum Technologies”, “5G mm-Wave Power Amplifiers, Transmitters, Beamforming Techniques and Massive MIMO”, “eXtreme-Bandwidth: Architectures for RF and mm-Wave Transceivers in Nanoscale CMOS”, “Integrated mm-Wave & THz Sensing Technology for Automotive, Industrial and Healthcare”, “Advanced Integrated RF Filtering Circuits and Techniques”, “Synthesizer Design and Frequency Generation-Synchronization Schemes for High-Performance Wireless Systems”, “High-performance WLAN Transceiver Design and Calibration Techniques”, “High Efficiency Power Amplification for Emerging Wireless Communications Solutions from Devices to Circuits and Systems”, “Millimeter-Wave Systems; Manufacturing, Packaging and Built-In Self-Test”, “Towards Direct Digital RF Transceivers”, and last but not least, “Ultra Low-Power Transceiver SoC Designs for IoT Applications”. These workshops cover some of the hottest topics in RFIC.

The RFIC Plenary Session will start at 17:30 and begin with the conference highlights, the presentation of the Student and Industry Paper Awards. The Plenary Session will conclude with focused talks on 5G and Automotive, beginning with the Honorable Zachary J. Lemnios, former US Assistant Secretary of Defense for Research and current Vice President of Physical Sciences & Government Programs at IBM T.J. Watson Research Center, who will enlighten us on “Compact Silicon Integrated mm-Wave Circuits: From Skepticism to 5G and Beyond”; the second talk will be given by Lars Reger, Senior Vice President and Chief Technology Officer of NXP’s Automotive business unit, who will share his vision on “The Road Ahead for Autonomous Cars — What’s in for RFIC”.

Immediately following the plenary session will be the RFIC ‘interactive’ Sunday reception that will highlight our Industry Showcase and Student Paper Award Finalists in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year, which will be held in the Millennium Hall at the Loews Philadelphia Hotel right after the Plenary Session!

On Monday and Tuesday, the RFIC will have multiple tracks of oral technical paper sessions, with two 5G-focused sessions on Monday morning, and other sessions focused on automotive radar, IoT, and THz imaging. Two entertaining panels will be featured during lunchtime on both days: the Monday panel session is titled “How Will the Future Self-Driving Cars See? LiDAR vs. Radar”, while the Tuesday panel session is titled “Can a Residential Wireless Gbps Internet Connection Compete with Wired Alternatives?”. The 5G summit occurring on Tuesday will provide high level 5G overview presentations that will complement the 5G-focused RFIC technical sessions. A separate registration will be required for the 5G summit.

On behalf of the RFIC steering and executive committees, we welcome you to join us at the 2018 RFIC Symposium in Philadelphia, Pennsylvania! Please visit the RFIC 2018 website (<http://rfic-ieee.org>) for more details and updates.



Walid Ali-Ahmad
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Haolu Xie, *Transa Semiconductor*
Hongtao Xu, *Fudan University*
Li-Wu Yang, *RF Integrated*
Yuxiang Zheng, *FutureWei Technologies*

RFIC 2018 Schedule

Saturday, 9 June 2018

08:00–18:00 Registration — Pennsylvania Convention Center (PCC), Level 2, Corridor

Sunday, 10 June 2018

07:00–18:00 Registration — PCC, Level 2, Corridor

07:00–08:00 Breakfast for Workshop and Short Course Speakers — PCC, Rooms 108AB

08:00–17:30 Workshops and Short Courses — PCC, Rooms 102A–109A

11:30–13:30 Lunch for Workshop and Short Course Attendees — PCC, Level 1, Foyer

17:30–19:00 RFIC Plenary — PCC, Ballroom

19:00–21:00 RFIC Welcoming Reception Featuring Industry Showcase and Student Paper Award Finalists — Loews Philadelphia Hotel (LPH), Millennium Hall

Monday, 11 June 2018

07:00–19:00 Registration — PCC, Level 2, Corridor

07:00–08:00 Breakfast for Workshop, Short Course, and Technical Session Speakers — PCC, Rooms 108AB

08:00–17:30 Workshops and Short Courses — PCC, Rooms 102A–109A

08:00–09:40 RMO1A — PCC, Room 201A: *Building Blocks for 5G Transceivers*

RMO1B — PCC, Room 201B: *Advances in Packaging, Modeling and Optical Phased Arrays*

RMO1C — PCC, Room 204A: *Techniques for High-Performance Frequency Synthesis*

09:40–10:00 Coffee Break — PCC, Grand Hall

10:10–11:30 RMO2A — PCC, Room 201A: *28GHz Phased Arrays, Beamformers and Sub-Components for 5G Applications*

RMO2B — PCC, Room 201B: *Technology Optimization for RF Applications*

RMO2C — PCC, Room 204A: *ADC-Based RF/Mixed-Signal Systems and Wireline Transceiver Techniques*

11:45–13:15 RFIC Panel Session — PCC, Room 201A: *How Will the Future Self-Driving Cars See? LiDAR vs. Radar*

12:00–13:00 Workshops Lunch — PCC, Grand Hall

13:30–15:10 RMO3A — PCC, Room 201A: *RF Front-Ends for Emerging Wireless Paradigms*

RMO3B — PCC, Room 201B: *Mixed Signal Transmitters and Power Amplifiers*

RMO3C — PCC, Room 204A: *cm/mm-Wave CMOS Integrated Phased-Array Building Blocks*

15:10–15:40 Coffee Break — PCC, Grand Hall

15:40–17:20 RMO4A — PCC, Room 201A: *Ultra-Low Power Radios for Security, Ranging and Connectivity*

RMO4B — PCC, Room 201B: *Silicon Integrated mm-Wave Transmitters*

RMO4C — PCC, Room 204A: *Highly Efficient mm-Wave Oscillators with Wide Tuning Range*

Tuesday, 12 June 2018

07:00–18:00 Registration — PCC, Level 2, Corridor

07:00–08:00 Breakfast for Technical Session Speakers — PCC, Rooms 108AB

08:00–09:40 RTU1A — PCC, Room 201A: *mm-Wave Power Amplifiers*

RTU1B — PCC, Room 201B: *Submillimeter Wave and Terahertz ICs*

RTU1C — PCC, Room 204A: *mm-Wave Radar and Beamforming Transceivers*

09:40–10:10 Coffee Break — PCC, Exhibit Hall

10:10–11:50 RTU2A — PCC, Room 201A: *mm-Wave LNAs and RF Receiver Front-Ends*

RTU2B — PCC, Room 201B: *Wireless Transceivers and Transmitters for Connectivity and Cellular*

12:00–13:00 RFIC Panel Session — PCC, Room 201A: *Can a Residential Wireless Gbps Internet Connection Compete with Wired Alternatives?*

13:30–15:10 Interactive Forum — PCC, Exhibit Hall

Schedule: Plenary, Reception, and Symposium Showcase

Sunday Evening, 10 June 2018

Pennsylvania Conference Center & Loews Philadelphia Hotel

17:30–19:00

RFIC Plenary

Pennsylvania Conference Center, Ballroom

Chair: Walid Ali-Ahmad, University of California, San Diego

Co-Chair: Stefano Pellerano, Intel

- 17:30 Welcome Message from General Chair and TPC Chairs,
Student Paper Awards, Industry Paper Awards, Tina Quach Service Award
- 18:00 *Compact Silicon Integrated mmWave Circuits: From Skepticism to 5G and Beyond*
Honorable Zachary J. Lemnios, IBM Research
- 18:30 *The Road Ahead for Autonomous Cars — What's in for RFIC*
Lars Reger, NXP Semiconductors

19:00–21:00

RFIC Welcoming Reception

Featuring Industry Showcase and Student Paper Awards Finalists

Loews Philadelphia Hotel, Millennium Hall

The RFIC “Interactive” Reception starts immediately after the Plenary Session and will highlight the Industry Showcase and Student Paper Awards Finalists in an engaging social and technical evening event with food and drinks. This event is supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year! Authors of these showcase and top student papers will present their innovative work, summarized in poster format, and some authors will also have hardware demonstrations..



Plenary Speaker 1

Honorable Zachary J. Lemnios
Vice President
Physical Sciences & Government Programs
IBM Research

Compact Silicon Integrated mmWave Circuits: From Skepticism to 5G and Beyond

Abstract: Silicon integration of millimeter wave (mmWave) circuits began with early investments from DARPA almost 20 years ago, with the DARPA TEAM (Technology for Efficient Agile Microelectronics) program. By convincing skeptics that mmWave circuits, traditionally implemented using discrete III-V blocks, could function reliably when fully integrated into silicon-based SiGe and CMOS processes, this technology has broadly evolved across today's highly integrated systems. The development of comprehensive CMOS and SiGe PDK (Process Development Kit) and the supporting modeling and design infrastructure provided a viable path for circuit designers to adopt this technology.

The tremendous volume reduction of ~1000X coupled with a ~1000X increase in integration complexity brought about by silicon-integration has already enabled the first generation of mmWave commercial automotive radar and data communication products, and placed mmWave as a key component of the next global mobile communications standard — 5G. This level of multi-antenna mmWave system sophistication was unimaginable a decade ago.

This talk will review the journey of mmWave technology over the last two decades, and outline the possibilities of a future where multi-functional mmWave circuits are a key differentiator in vertically integrated “Antennas to AI” cognitive systems.

About Zachary J. Lemnios

Mr. Lemnios leads Physical Sciences and Government Programs, globally across IBM Research, to extend fundamental scientific understanding and breakthroughs that enable the future of information technology. Strategic initiatives include quantum computing, neuromorphic devices and architectures, molecular imaging, silicon nanophotonics, and magnetic memory technology. This team has been responsible for leading technical breakthroughs across the industry and many of IBM's major awards, including: Nobel Prizes, Kavli Prizes, and the Millennium Technology Prize.

Mr. Lemnios previously served as VP Research Strategy and Worldwide Operations. In that role, he led the formation and execution of the IBM Research strategy and operations across IBM's twelve global laboratories and network of laboratories, led the IBM Global Technology Outlook and worked across IBM to set the strategic direction of IBM Research.

Prior to joining IBM, Mr. Lemnios served three terms in high level civilian leadership in the Department of Defense with detailed and extended interactions across the whole of US government and with leaders across US allied nations. Mr. Lemnios was confirmed as The Honorable Assistant Secretary of Defense (Research & Engineering) by the United States Senate. In this position, Mr. Lemnios was the Chief Technology Officer for Department of Defense and shaped the Department's technical strategy to support the President's national security objectives and the Secretary's priorities. He launched Department and international initiatives in large data analytics, decision support, engineering education, electronic warfare, cyber, autonomy, advanced propulsion, hypersonics, and rail gun concepts as future capabilities for the nation. Mr. Lemnios also served as the Chief Technology Officer of MIT Lincoln Laboratory and led the development of advanced technologies in support of national security.

Mr. Lemnios received his BSEE from the University of Michigan and his MSEE from Washington University in St. Louis and an honorary degree of Doctor of Humane Letters from Tiffin University. He has served on numerous national security, industry and academic committees. He has authored over 40 papers, holds 4 patents in advanced GaAs device and MMIC technology and is a Fellow of the IEEE. Mr. Lemnios received special recognition from the Australian Government Department of Defence and was awarded Office of Secretary of Defense Medal for Exceptional Public Service and the Office of Secretary of Defense Medal for Outstanding Public Service.

Sunday, 10 June 2018

18:00–18:30

PCC Ballroom



Plenary Speaker 2

Lars Reger
Automotive Chief Technology Officer
Business Unit Automotive
NXP Semiconductors

The Road Ahead for Autonomous Cars – What's in for RFIC

Abstract: Our cars are morphing into connected, self-driving “robots” that can sense the environment, think and act autonomously. Today’s cars are loaded with technologies that enable new in-vehicle experiences or safety and automation applications like advanced driver assistance systems (ADAS). Connectivity is ultimately redefining the way cars are conceptualized and built. In cars of the future, all of the interfaces — radio, cellular, WiFi, Bluetooth, GPS, vehicle-to-everything (V2X) communications, and more — can be integrated into a single, secure smart antenna that serves as both a transmitter and receiver of communications with a variety of channels, standards, and bandwidths. However, various wireless technologies can also introduce cyber security risks. As the car becomes a hub of connectivity, it opens potential attack opportunities for hackers. How secure can a fully connected car be? What should future car architectures look like to enhance security? How will RFIC technology and connectivity transform the driving experience of tomorrow and what are the next big innovations to expect?

About Lars Reger

Lars Reger is Senior Vice President and Chief Technology Officer of NXP’s Automotive business unit. NXP is the world’s largest supplier of automotive semiconductors and driving the market for securely connected, self-driving cars. Focus areas in its portfolio are secure and smart car access, car infotainment, advanced driver assistance systems, in-vehicle networks, body, and safety. As CTO, Lars is responsible for managing R&D and new business activities for NXP Automotive.

Prior to joining NXP in 2008, Lars gained deep insight into the microelectronics industry — with a strong focus on the automotive sector — in various functions with Siemens, Infineon, Siemens VDO and Continental. Before joining NXP, Lars was Director of Business Development and Product Management within the Connectivity business unit at Continental. His past roles at Infineon included Head of the Process and Product Engineering departments, Project Manager for Mobile System Chips, and Director of IP Management. He began his career with Siemens Semiconductors as Product Engineer in 1997. Lars holds a university degree in physics from Rheinische-Friedrich-Wilhelms University of Bonn and an executive MBA from London Business School.

The Industry Showcase

Chair: Oren Eliezer, PHAZR

The Industry Showcase Session, held concurrently with the plenary reception, will highlight 10 selected papers submitted by authors from industry and focused on state of the art RFIC technology. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The top-three industry papers will be announced during the RFIC Plenary Session. The list below specifies the authors of each of the 10 papers, as well as the session and time for its oral presentation.

A 22nm FDSOI Technology Optimized for RF/mmWave Applications

¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, Germany, ³GLOBALFOUNDRIES, USA, ⁴CEA-LETI, France, ⁵GLOBALFOUNDRIES, India

S.N. Ong¹, S. Lehmann², W.H. Chow¹, C. Zhang³, C. Schippel², L.H.K. Chan¹, Y. Andee², M. Hauschild³, K.K.S. Tan¹, J. Watts³, C.K. Lim¹, A. Divay⁴, Jen Shuang Wong¹, Z. Zhao⁵, Madabusi Govindarajan¹, C. Schwan², A. Huschka², A. Bellaouar³, W.L. Oo¹, J. Mazurier², C. Grass², R. Taylor³, Kok Wai Johnny Chew¹, S. Embabi³, G. Workman³, A. Pakfar², S. Morvan², K. Sundaram¹, M.T. Lau¹, B. Rice², D. Harame²

RM02B-1 10:10

A Robust Reconfigurable Front-End for Non-Contiguous Multi-Channel Carrier Aggregation Receivers

¹Toga Networks, Israel, ²Huawei Technologies, China

Dror Regev¹, Shimi Shilo¹, Doron Ezri¹, Junping Zhang²

RM01A-2 8:20

A Dual-Core 60GHz Push-Push VCO with Second Harmonic Extraction by Mode Separation

¹Infineon Technologies, Germany, ²Infineon Technologies, Austria

Vadim Issakov¹, Fabio Padovan²

RM04C-3 16:20

A 264- μ W 802.15.4a-Compliant IR-UWB Transmitter in 22nm FinFET for Wireless Sensor Network Application

¹Intel, USA, ²University of Texas at Dallas, USA

Renzhi Liu¹, Brent R. Carlton¹, Stefano Pellerano¹, Farhana Sheikh¹, Divya Shree Vemparala¹, Ahmed Ali², V. Srinivasa Somayazulu¹

RM04A-2 16:00

A Compact 75GHz LNA with 20dB Gain and 4dB Noise Figure in 22nm FinFET CMOS Technology

Intel, USA

Woorim Shin, Steven Callender, Stefano Pellerano, Christopher Hull

RTU2A-2 10:30

A Compact 75GHz PA with 26.3% PAE and 24GHz Bandwidth in 22nm FinFET CMOS

Intel, USA

Steven Callender, Stefano Pellerano, Christopher Hull

RTU1A-2 8:20

Q-Band CMOS Transmitter System-on-Chip for Protected Satellite Communication

Northrop Grumman, USA

T. LaRocca, K. Thai, R. Snyder, R. Jai, O. Fordham, N. Daftari, B. Wu, Y. Yang, M. Watanabe

RMO4B-1 15:40

A 28nm CMOS Wireless Connectivity Combo IC with a Reconfigurable 2x2 MIMO WiFi Supporting 80+80MHz 256-QAM, and BT 5.0

¹Samsung, Korea, ²Samsung Cambridge Solution Centre, UK

Chia-Hsin Wu¹, Chris Hunter², Jongdae Bae¹, Huijung Kim¹, Jisoo Chang¹, Jacob Sharpe², Inhyo Ryu¹, Seongwon Joo¹,

Byeongwan Ha¹, Won Ko¹, Joungyun Yim¹, Sangwook Han¹, Taewan Kim¹, Daeyoung Yoon¹, Inyoung Choi¹,

Sangyun Lee¹, Qing Liu¹, Myounggyun Kim¹, Jiyoung Lee¹, Shinwoong Kim¹, Alexander Thoukydides²,

Michael Cowell², Thomas Byunghak Cho¹

RTU2B-1 10:10

A 57–71GHz Beamforming SiGe Transceiver for 802.11ad-Based Fixed Wireless Access

Sivers IMA, Sweden

Erik Öjefors, Mikael Andreasson, Torgil Kjellberg, Håkan Berg, Lars Aspemyr, Richard Nilsson, Klas Brink,

Robin Dahlbäck, Dapeng Wu, Kristoffer Sjögren, Mats Carlsson

RTU1C-5 9:20

Monitoring Architecture for a 76–81GHz Radar Front End

¹Texas Instruments, India, ²Texas Instruments, USA

Karthik Subburaj¹, Brian Ginsburg², Pankaj Gupta¹, Krishnanshu Dandu², Sreekiran Samala², Dan Breen²,

Karthik Ramasubramanian¹, Tim Davis², Zahir Parkar¹, Dheeraj Shetty¹, Rohit Chatterjee¹, Zeshan Ahmad²,

Neeraj Nayak², Meysam Moallem², Eunyoung Seok², Karan Bhatia², Shankar Ram Narayanamoorthy¹,

Anjan Prasad Easwaran¹, Tom Altus², Sriram Murali¹, Vito Giannini², Indu Prathapan¹, Sachin Bharadwaj¹,

Sumeer Bhatara¹, Venkatesh Srinivasan², Sai Gunaranjan¹, Sundararajan Rangachari¹

RTU1C-2 8:20

The Student Paper Awards Finalists

Chair: Brian Floyd, North Carolina State University

One of the missions of RFIC Symposium is to promote academic research and education. As part of the Student Paper Awards program, several finalists are nominated every year by the RFIC Technical Program Committee to enter the final contest where the top-three papers are selected. All finalists benefit from a complimentary RFIC registration. Authors of these papers will be present at the RFIC plenary reception to discuss their innovative work, summarized in poster format. The top-three student papers will be announced during the RFIC Plenary Session. Each winner will receive an honorarium and a plaque. The list below specifies the authors of each of the 11 papers, as well as the session and time for its oral presentation.

A Secure TOF-Based Transceiver with Low Latency and Sub-cm Ranging for Mobile Authentication Applications

Haixin Song, Zhendong Ding, Woogeun Rhee, Zhihua Wang
Tsinghua University, China
RMO4A-1 15:40

A 29–37GHz BiCMOS Low-Noise Amplifier with 28.5dB Peak Gain and 3.1–4.1dB NF

Zhe Chen, Hao Gao, Domine Leenaerts, Dusan Milosevic, Peter G.M. Baltus
Technische Universiteit Eindhoven, The Netherlands
RTU2A-3 10:50

An 8.8-GS/s 8b Time-Interleaved SAR ADC with 50-dB SFDR Using Complementary Dual-Loop-Assisted Buffers in 28nm CMOS

X. Shawn Wang¹, Chi-Hang Chan², Jieqiong Du¹, Chien-Heng Wong¹, Yilei Li¹, Yuan Du¹, Yen-Cheng Kuan³, Boyu Hu¹, Mau-Chung Frank Chang¹
¹University of California, Los Angeles, USA, ²University of Macau, China, ³National Chiao Tung University, Taiwan
RMO2C-1 10:10

A 28GHz Packaged Chireix Transmitter with Direct On-Antenna Outphasing Load Modulation Achieving 56%/38% PA Efficiency at Peak/6dB Back-Off Output Power

Sensen Li, Taiyun Chi, Huy Thong Nguyen, Tzu-Yuan Huang, Hua Wang
Georgia Tech, USA
RMO2A-4 11:10

A -195dBc/Hz FoM_r 20.8-to-28-GHz LC VCO with Transformer-Enhanced 30% Tuning Range in 65-nm CMOS

S. Lightbody¹, A.H.M. Shirazi¹, H. Djahanshahi², R. Zavari², S. Mirabbasi¹, S. Shekhar¹
¹University of British Columbia, Canada, ²Microsemi, Canada
RMO4C-1 15:40

A 10GHz Digital Phase Noise Filter with 14dB Noise Suppression and -127dBc/Hz Noise Sensitivity at 1MHz Offset

Tongning Hu, Shilei Hao, Qun Jane Gu
University of California, Davis, USA
RMO1C-4 9:00

A Low Power PWM Optical Phased Array Transmitter with 16° Field-of-View and 0.8° Beamwidth

Reza Fatemi, Aroutin Khachaturian, Ali Hajimiri
Caltech, USA
RM01B-3 8:40

A 28GHz CMOS Phased-Array Transceiver Featuring Gain Invariance Based on LO Phase Shifting Architecture with 0.1-Degree Beam-Steering Resolution for 5G New Radio

Jian Pang¹, Rui Wu¹, Yun Wang¹, Masato Dome¹, Hisashi Kato¹, Hongye Huang¹, Aravind Tharayil Narayanan¹, Hanli Liu¹, Bangan Liu¹, Takeshi Nakamura¹, Takuya Fujimura¹, Masaru Kawabuchi¹, Ryo Kubozoe¹, Tsuyoshi Miura¹, Daiki Matsumoto¹, Naoki Oshima², Keiichi Motoi², Shinichi Hori², Kazuaki Kunihiro², Tomoya Kaneko², Kenichi Okada¹
¹Tokyo Institute of Technology, Japan, ²NEC, Japan
RM02A-1 10:10

A Flexible Low-Latency DC-to-4 Gbit/s Link Operating from -40 to +200°C in 28nm CMOS for Galvanically Isolated Applications

Simon Ooms, Patrick Reynaert
Katholieke Universiteit Leuven, Belgium
RM02C-4 11:10

An 8-Element, 1–3GHz Direct Space-to-Information Converter for Rapid, Compressive-Sampling Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna-Weight Modulation

Matthew Bajor, Tanbir Haque, Guoxiang Han, Ciyuan Zhang, John Wright, Peter R. Kinget
Columbia University, USA
RM03A-4 14:30

Fully-Integrated Non-Magnetic 180nm SOI Circulator with >1W P1dB, >+50dBm IIP3 and High Isolation Across 1.85 VSWR

Aravind Nagulu¹, Andrea Alì², Harish Krishnaswamy¹
¹Columbia University, USA, ²CUNY Advanced Science Research Center, USA
RM03A-1 13:30

Student Paper Contest Eligibility: The student must have been a full-time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must be the lead author of the paper and must present the paper at the Symposium. A memorandum is sent to the advisor to certify that the work was done by the student.

Judging Procedure: Student papers are reviewed and admitted to the conference in the same manner as all other conference papers. After the paper review process is completed, the technical program subcommittees recommend student paper finalists. The student paper contest committee consisting of one representative from each subcommittee is then formed to review all the finalists and select the top three papers. Papers accepted for the competition are judged on content.

Monday 11 June 2018

08:00–09:40

201A

Session RM01A: Building Blocks for 5G Transceivers

Chair: Steven Turner, BAE Systems

Co-Chair: Waleed Khalil, The Ohio State University

RM01A-1 8:00

A 25.1–27.6GHz Tunable-Narrowband Digitally-Calibrated Merged LNA-Vector Modulator for 5G Phased Arrays

Rahul Singh, Susnata Mondal, Jeyanandh Paramesh; Carnegie Mellon University, USA

Abstract: This paper presents a compact differential quadrature generation scheme using transformer coupled-resonators for use in scalable 5G phased-array architectures. In this work, quadrature generation is seamlessly integrated with the load of an LNA gain stage, thus obviating the need for an explicit quadrature hybrid in the vector modulator. A 25.1-to-27.6 GHz phased array channel employing the proposed scheme is implemented in 65 nm CMOS. The merged LNA-vector modulator is demonstrated to be digitally tunable across 2.5 GHz, and achieved greater than 430 MHz bandwidth (quadrature error $\leq \pm 6.4^\circ$), small RMS phase error ($\leq 2.6^\circ$), while occupying a composite area of only 0.123 mm². An on-chip calibration scheme to achieve quadrature locking at a desired frequency is also presented.

RM01A-2 8:20

A Robust Reconfigurable Front-End for Non-Contiguous Multi-Channel Carrier Aggregation Receivers

Dror Regev¹, Shimi Shilo¹, Doron Ezri¹, Junping Zhang²; ¹Toga Networks, Israel, ²Huawei Technologies, China

Abstract: A new architecture for multi-channel carrier aggregation receivers is proposed for eliminating risks of VCO injection pulling and mitigating performance degradation resulting from Multi-LO mutual coupling. A fully integrated receiver front-end is implemented, enabling the realization of a robust multi-LO triple-carrier-aggregation system operating in the 5.2–5.8GHz band. The RFIC demonstrates EVM better than 30dB for all three non-contiguous 80MHz channels. It is implemented in 65nm CMOS LP process and occupies a die area of 1mm².

RM01A-3 8:40

A True Time Delay 16-Element 4-Beam Digital Beamformer

Sunmin Jang¹, Rundao Lu¹, Jaehun Jeong², Michael P. Flynn¹; ¹University of Michigan, USA, ²Broadcom, USA

Abstract: Large phased arrays are limited by inaccurate beam steering (squinting) and by distortion in analog-to-digital conversion. This paper introduces the first integrated digital true time delay beamforming receiver. The true time delay eliminates squinting, making it ideal for large-array wide-bandwidth applications. The beamformer incorporates a new current-steering DAC architecture

providing a constant output impedance to improve ADC linearity. This significantly reduces distortion, leading to an SFDR improvement of 13.7 dB from the array. The prototype achieves an EVM better than -37 dB for 5 MBd 256-QAM and 512-QAM. The measured beam patterns are near-ideal for both conventional and adaptive beamforming. The prototype digital beamformer supports 16 antennas and 4 independent beams. It occupies only 0.29 mm² and consumes 453 mW.

RM01A-4 9:00

A 9.4–11.7GHz VCO in 0.12 μ m SiGe BiCMOS with -123dBc/Hz Phase Noise at 1MHz Offset for 5G Systems

Eric C. Wagner, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 9.4–11.7 GHz VCO designed in 0.12 μ m SiGe BiCMOS with a 4-bit transformer-coupled capacitor bank. The oscillator uses a cross-coupled design utilizing 0.12 μ m PMOS active devices and consumes 30 mA from a 2.5 V supply. A state-of-the-art phase noise of -123 dBc/Hz is measured at 1 MHz offset from the carrier resulting in a FoM and FoMT of -184 and -188, respectively. The application areas are in 5G 28 GHz and 39 GHz local oscillators with $\times 2$ and $\times 3$ frequency multipliers.

Monday 11 June 2018

08:00–09:40

201B

Session RM01B: Advances in Packaging, Modeling and Optical Phased Arrays

Chair: Richard Chan, Qorvo

Co-Chair: Tzung-Yin Lee, Skyworks Solutions

RM01B-1 8:00

Chip-Package-PCB Co-Design of Power Combiners in SESUB and WLCSP Technology with Re-Distribution Layers

Thanh Vinh Dinh¹, Sidina Wane², Dominique Lesénéchal¹, Philippe Descamps¹, Laurent Leyssenne³, Damienne Bajon⁴, ¹LaMIPS, France, ²Energy-Vision, France, ³Thales, France, ⁴ISAE, France

Abstract: We present SESUB (Semiconductor Embedded in Substrate) and WLCSP (Wafer-Level-Chip-Scale Packaging) integration of Power Combiners for WLAN and 5G applications. The proposed technology solutions offer optimized Electromagnetic-Thermal-Mechanical performances for Energy-Efficient Chip-Package-PCB distributed Co-Design. PDK-Library oriented RLC Lumped-model topologies are compared to broadband distributed Layout design. Prototype demonstrators are designed and experimentally verified for emerging 5G and IoT applications both for frequencies below 6GHz and in the mm-Wave domain (28GHz, 39GHz). Innovative broadband physics-based RLC equivalent circuit models valid from DC to mm-Wave frequencies is proposed and verified against measurement.

RM01B-2 8:20

An Efficient mm-Wave Integrated Circuit Synthesis Method with Accurate Scalable Passive Component Modeling

Zhijian Pan, Wei Zhu, Qiang Yao, Di Li, Zuochang Ye, Yan Wang; Tsinghua University, China

Abstract: With the operating frequency of radio-frequency (RF) integrated circuits (ICs) ascending gradually to millimeter-wave (mm-wave) regime, the RF IC design automation methods encounter great challenges due to the complicated distributed effects and parasitic effects. In this work, a new synthesis framework for mm-wave ICs is presented, which is featured by two progressive stages: offline preparation and online synthesis. In the former stage, to cope with the difficulty of mm-wave IC synthesis caused by passive components, a scalable modeling method is proposed, in which geometric parameters are incorporated into rational functions to accurately model the S-parameters up to 120GHz. Benefited from the dedicated offline preparation, during the online synthesis, the circuit performance evaluation and optimization are carried out without the time-consuming EM simulation. High-quality solutions can be obtained by using evolutionary algorithms with enough iterations. We applied the proposed approach to the design of a four-stage differential wideband low-noise amplifier (LNA) covering various mm-wave applications. The synthesized LNA is implemented in 65nm CMOS technology and the measured results show that it achieves the highest bandwidth (34GHz) with other comparable performances to the similar state-of-the-art CMOS broadband LNAs.

The synthesis only costs 26min, which is more than 50× time speed-up compared to the existing mm-wave synthesis methods.

RM01B-3 8:40

A Low Power PWM Optical Phased Array Transmitter with 16° Field-of-View and 0.8° Beamwidth

Reza Fatemi, Aroutin Khachaturian, Ali Hajimiri; Caltech, USA

Abstract: An optical phased array (OPA) transmitter system with a high-swing electrical PWM driver achieving the highest reported grating-lobe-free field-of-view to beamwidth ratio of 16°/0.8° for a two-dimensional aperture is presented. This ratio translates to 400 resolvable spots — which is 30× more numerous than the state-of-the-art. This scalable OPA, with a sparsely populated aperture, overcomes optical routing difficulties in planar photonic processes while maintaining the desired transmitter beam characteristics. To reduce the power consumption, a row-column electrical connection grid for the 144 optical phase shifters decreases the number of electrical drivers from 144 to 37. The PWM driver chip incorporates a breakdown-voltage multiplying architecture to increase the output voltage swing. The 65nm CMOS electronic driver chip and the photonic chip, fabricated through a standard silicon photonics process, occupy 1.7mm² and 2.08mm² of active area respectively.

RM01B-4 9:00

A CMOS-SOI Power Amplifier Technology Using EDNMOS for Sub 6GHz Wireless Applications

Rui Tze Toh¹, Shyam Parthasarathy², Shaoqiang Zhang¹, Madabusi Govindarajan², Jen Shuang Wong¹, Kok Wai Johnny Chew¹, Luis Andia¹, Diing Shenp Ang³; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, India, ³Nanyang Technological University, Singapore

Abstract: Technology benchmarking results specific to power amplifiers (PA) application designed using extended drain NMOS (EDNMOS) on SOI is presented. Improved kink free conductance characteristics of this device leads to superior performance when the optimized EDNMOS is used standalone as a PA output stage or in a cascode arrangement with other faster devices. The CMOS technology with this device is a viable alternative for designing watt level power amplifier on SOI.

Monday 11 June 2018

08:00–09:40

204A

**Session RM01C: Techniques for High-Performance Frequency
Synthesis**

Chair: Salvatore Levantino, Politecnico di Milano

Co-Chair: Joseph Cali, BAE Systems

RM01C-1 8:00

**A 15.6–18.2GHz Digital Bang-Bang PLL with -63dBc In-Band Fractional
Spur**

Dmytro Cherniak¹, Luigi Grimaldi¹, Fabio Padovan², Matteo Bassi², Roberto Nonis², Carlo Samori¹, Salvatore Levantino¹; ¹Politecnico di Milano, Italy, ²Infineon Technologies, Austria

Abstract: This paper describes a 15.6–18.2GHz fractional-N bang-bang digital PLL fabricated in 28nm CMOS. To compensate for the nonlinearity of the digital-to-time converter and reduce the level of fractional spurs, two alternative pre-distortion techniques are introduced. The adoption of those algorithms operating continuously in background is demonstrated to reduce the level of the in-band fractional spur at 300kHz from -20dBc to -57dBc and -63dBc, respectively. The fabricated PLL achieves FoM of -237.2dB.

RM01C-2 8:20

**A 14nm FinFET Sub-Picosecond Jitter Fractional-N Ring PLL for 5G Wireless
Communication**

Seungjin Kim, Byungki Han, Mingyu Cho, Seunghyun Oh, Jongwoo Lee, Thomas Byunghak Cho; Samsung, Korea

Abstract: This paper presents a ring-VCO based sub-picosecond RMS jitter fractional-N PLL by employing a $31\times$ reference multiplier to provide 60dB suppression on the $\Delta\Sigma$ quantization noise. By using 4-bit automatic bias calibration (ABC) and two-step digitally calibrated replica-biased regulator (DCRR), the effect of supply noise on MDLL and VCO is vastly alleviated to ensure robust jitter performance even in noisy SoC environment. Implemented in a 14nm FinFET process, the proposed PLL achieves $< 1\text{ps}_{\text{RMS}}$ jitter at 7GHz while consuming 36.3mW. This PLL guarantees that the ADC achieves an SNDR greater than 52dB at 400MHz bandwidth, thereby greatly relieving the data conversion requirements in 5G wireless communication.

RM01C-3 **8:40**

A 1.33mW, 1.6ps_{rms}-Integrated-Jitter, 1.8–2.7GHz Ring-Oscillator-Based Fractional-N Injection-Locked DPLL for Internet-of-Things Applications

Jiang Gong¹, Yuming He¹, Ao Ba¹, Yao-Hong Liu¹, Johan Dijkhuis¹, Stefano Traferro¹, Christian Bachmann¹, Kathleen Philips¹, Masoud Babaie²; ¹Holst Centre, The Netherlands, ²Technische Universiteit Delft, The Netherlands

Abstract: This paper presents a 1.8–2.7 GHz low-power ring-oscillator-based fractional-N injection-locked digital PLL (IL-DPLL) in 40-nm CMOS for Internet-of-Things clock generation. A two-path injection technique is proposed to improve the in-band phase noise and the integrated jitter of the implemented PLL by ~6 dB and ~1.8×, respectively. Furthermore, a digital foreground calibration is introduced to effectively reduce reference spurs in a short calibration time of 2 μs. In the worst-case channel, the proposed DPLL using a 64MHz reference input shows a 1.6 ps integrated jitter, -43.6 dBc reference spur, -45.8 dBc fractional spur and 1 kHz frequency resolution while consuming 1.33mW power.

RM01C-4 **9:00**

A 10GHz Digital Phase Noise Filter with 14dB Noise Suppression and -127dBc/Hz Noise Sensitivity at 1MHz Offset

Tongning Hu, Shilei Hao, Qun Jane Gu; University of California, Davis, USA

Abstract: In this paper, we present a digital phase noise filter with a time-amplifier based TDC (TA-TDC) enabled frequency discriminator. The TA-TDC boosts the system sensitivity and suppresses the limit cycle jitters that constrains quantized systems. At 1 MHz offset, it demonstrates 14 dB phase noise suppression with -127 dBc/Hz sensitivity for a 10 GHz clock. The integrated jitter over the bandwidth from 10 kHz to 100 MHz is 81 fs. Its phase noise suppression frequency offset range is from 40 kHz to 8 MHz. The digital phase noise filter (DPNF) is fabricated in a 65 nm CMOS process and dissipates 53 mW.

RM01C-5 **9:20**

A 5.5–7.3GHz Analog Fractional-N Sampling PLL in 28-nm CMOS with 75fs_{rms} Jitter and -249.7dB FoM

Wanghua Wu¹, Chih-Wei Yao¹, Kunal Godbole¹, Ronghua Ni¹, Pei-Yuan Chiang¹, Yongping Han¹, Yongrong Zuo¹, Ashutosh Verma¹, Ivan Siu-chuang Lu¹, Sang Won Son¹, Thomas Byunghak Cho²; ¹Samsung, USA, ²Samsung, Korea

Abstract: We present a low jitter, DTC-based analog fractional-N PLL with novel, background DTC gain calibration and reference clock duty cycle correction for high performance applications. The PLL achieves a 75-fs rms jitter, integrated from 10 kHz to 10 MHz and a -249.7 dB figure of merit at fractional mode. The measured fractional-N spurs are less than -64 dBc across the 5.5–7.3 GHz output frequency. Implemented in 28-nm CMOS, this PLL consumes 18.9 mW and occupies 0.5 mm².

Monday 11 June 2018

10:10–11:50

201A

Session RMO2A: 28 GHz Phased Arrays, Beamformers and Sub-Components for 5G Applications

Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

Co-Chair: Stefano Pellerano, Intel

RMO2A-1 10:10

A 28GHz CMOS Phased-Array Transceiver Featuring Gain Invariance Based on LO Phase Shifting Architecture with 0.1-Degree Beam-Steering Resolution for 5G New Radio

Jian Pang¹, Rui Wu¹, Yun Wang¹, Masato Dome¹, Hisashi Kato¹, Hongye Huang¹, Aravind Tharayil Narayanan¹, Hanli Liu¹, Bangan Liu¹, Takeshi Nakamura¹, Takuya Fujimura¹, Masaru Kawabuchi¹, Ryo Kubozoe¹, Tsuyoshi Miura¹, Daiki Matsumoto¹, Naoki Oshima², Keiichi Motoi², Shinichi Hori², Kazuaki Kunihiro², Tomoya Kaneko², Kenichi Okada¹; ¹Tokyo Institute of Technology, Japan, ²NEC, Japan

Abstract: This paper presents a CMOS implementation of 28-GHz 4-element phased-array transceiver for 5G new radio. The proposed LO phase shifting architecture realizes very fine 0.04° phase tuning step and gain-invariant feature. An 8-element transceiver demonstrates the measured 0.1-degree beam-steering resolution and less than 0.2dB gain variation over the whole phase tuning range. In a 5-meter distance, the transceiver achieves 6.4Gb/s in 256QAM for beam angle of $\pm 50^\circ$ together with a maximum data rate of 15Gb/s in 64QAM, and consumes 1.2W/chip in TX mode and 0.59W/chip in RX mode.

RMO2A-2 10:30

A Wideband High-Power Multi-Standard 23–31GHz 2×2 Quad Beamformer Chip in SiGe with >15dBm OP1dB Per Channel

Berktag Ustundag, Kerim Kibaroglu, Mustafa Sayginer, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 2×2 quad-core beamformer transmit/receive (TRX) chip with a peak OP1dB of 17 dBm and an OP1dB >15 dBm at 23–31.5 GHz, achieved using an asymmetrical switch design. The chip is built in SiGe BiCMOS and results in a PAE >10% at 23–31 GHz at P1dB. Each channel in the 2×2 chip contains 6-bit phase control, 20–26 dB gain control and with a measured IP1dB of -19 dBm and an NF <6.1 dB at 23–31 GHz. The beamformer chip is tested at 27 GHz and using a 16-QAM 7 Gbaud waveform (28 Gbps data rate) and results in <9.8% EVM. The chip is also tested at 22–30 GHz using a 64-QAM 1 Gbaud waveform (6 Gbps) and results in an EVM of 3–3.5% over the entire bandwidth. To our knowledge, this work achieves the widest bandwidth and the highest output power at record PAE levels in the Tx mode, and can support all worldwide 5G bands around 28 GHz.

RMO2A-3 10:50

A Dual-Polarized Dual-Beam 28GHz Beamformer Chip Demonstrating a 24Gbps 64-QAM 2×2 MIMO Link

Kerim Kibaroglu, Mustafa Sayginer, Ahmed Nafe, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 28 GHz 2×4 element transmit/receive (TRX) phased-array quad beamformer chip in SiGe BiCMOS and its use in a polarization based 2×2 MIMO link. The 2×4 TRX beamformer chip contains 8 channels, with each 4 channels combined on-chip using a Wilkinson network into two common ports for the vertical (V) and horizontal (H) polarizations. Each channel contains 6-bit phase control, 20–25 dB gain control and delivers 11–12 dBm power at the output 1 dB compression point (OP1dB) in the TX mode and has 4.8 dB noise figure (NF) in the RX mode. The beamformer chip is flipped on a printed circuit board (PCB) containing a 2×2 dual-polarized antenna array with low cross-polarization levels. A wireless link is demonstrated using two phased-array boards operating with two independent data streams simultaneously. A data rate of 12 Gbps per polarization (24 Gbps total data rate) is achieved using 16-/64-QAM waveforms. To our knowledge, this is the first demonstration of a single-aperture 2×2 MIMO link at millimeter-waves.

RMO2A-4 11:10

A 28GHz Packaged Chireix Transmitter with Direct On-Antenna Outphasing Load Modulation Achieving 56%/38% PA Efficiency at Peak/6dB Back-Off Output Power

Sensen Li, Taiyun Chi, Huy Thong Nguyen, Tzu-Yuan Huang, Hua Wang; Georgia Tech, USA

Abstract: This paper presents a packaged 28GHz Chireix outphasing transmitter (TX) for power amplifier (PA) efficiency enhancement at peak and back-off output power (PBO). It utilizes a high-efficiency dual-feed loop antenna (DLA)-based non-isolating power combiner to realize direct on-antenna power combining and more importantly, outphasing active load modulation. The proposed Chireix TX contains two phase-shifted sub-TXs simultaneously driving a DLA on package. The TX chips are implemented in a 45nm CMOS SOI process and integrated with the DLA by flip-chip packaging. The measurements demonstrate a 56% PA drain efficiency (η_p) at saturated power (P_{sat}), with 38% η_p at 6dB PBO, achieving 1.36× efficiency enhancement over ideal Class-B operation. The high efficiency of this Chireix TX enables up to 34%/10.5dBm PA average efficiency/output power (η_{ave}/P_{ave}) while amplifying 15Gb/s 64-QAM signal at 28GHz with EVM/ACLR better than -27.5dBc/-28dBc in a wireless radiation testing environment.

Monday 11 June 2018

10:10–11:50

201B

Session RMO2B: Technology Optimization for RF Applications

Chair: Edward Preisler, TowerJazz

Co-Chair: Alvin Joseph, GLOBALFOUNDRIES

RMO2B-1 10:10

A 22nm FDSOI Technology Optimized for RF/mmWave Applications

S.N. Ong¹, S. Lehmann², W.H. Chow¹, C. Zhang³, C. Schippel², L.H.K. Chan¹, Y. Andee², M. Hauschildt³, K.K.S. Tan¹, J. Watts³, C.K. Lim¹, A. Divay⁴, Jen Shuang Wong¹, Z. Zhao², Madabusi Govindarajan⁵, C. Schwan², A. Huschka², A. Bellaouar³, W.L. Oo¹, J. Mazurier², C. Grass², R. Taylor³, Kok Wai Johnny Chew¹, S. Embabi³, G. Workman³, A. Pakfar², S. Morvan², K. Sundaram¹, M.T. Lau¹, B. Rice², D. Haramé²; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, Germany, ³GLOBALFOUNDRIES, USA, ⁴CEA-LETI, France, ⁵GLOBALFOUNDRIES, India

Abstract: This paper describes a 22nm FDSOI technology optimized for RF/mmWave applications. The offering consists of high speed mmWave FET transistors, and a thick dual copper back-end. The offering is integrated with a low power digital technology (0.4V) and is extremely simple with less than 40 masks for an 8M process. The best performance for nFET/pFET f_T is 347/275 GHz and for f_{MAX} is 371/299 GHz. The RF cell layouts enable higher performance and improved wiring flexibility for the higher currents demanded in mmWave applications. The optimized pFET layout utilizes stress to increase performance while minimizing the parasitic capacitance. A strong pFET distinguishes this technology from many others enabling more efficient “complementary” RF/mmWave design. This combination of high performance mmWave FET transistors, low voltage logic, and low complexity mask build makes it ideal for a large suite of RF/mmWave application including IOT, 5G, and Radar.

RMO2B-2 10:30

f_T Enhancement of CMOS Transistor Using Isolated Polysilicon Gates

Xi Sung Loo¹, Moe Z. Win¹, Kiat Seng Yeo²; ¹MIT, USA, ²SUTD, Singapore

Abstract: This paper presents a layout method using isolated polysilicon gates to boost the current gain performance of CMOS transistor while preserving symmetrical contact geometry for mismatch consideration and enable flexibility in gate routing. It demonstrated less gate capacitances than conventional comb type layout due to reduction in polysilicon area. Consequently, 12GHz improvement in maximum transit frequency, f_T is recorded even for optimization at single gate level. Further, variants of isolated gate layouts are introduced to allow flexibility in optimizing the transistor gate parasitics. They are found to have negligible impact on gate resistance for the same double gate contact style. The advantages described are realized without compromising maximum power gain as demonstrated experimentally.

RM02B-3 10:50

A Small Signal AC Model Using Scalable Drain Current Equations of AlGaIn/GaN MIS Enhancement HEMT

H. Aoki¹, H. Sakairi², N. Kuroda², Y. Nakamura², K. Chikamatsu², K. Nakahara²; ¹Teikyo Heisei University, Japan, ²ROHM, Japan

Abstract: A small signal AC equivalent circuit with scalable drain current equations of AlN/GaN metal-insulator-semiconductor (MIS)-HEMTs has been developed for embedded source field-plate structures. The scalable source field-plate capacitance is included in addition to the dispersion, gate, and drain capacitances. The models are implemented in Verilog-A source codes. The model parameters are extracted from measured data of the G-S-G transistor test structures that we fabricated. The results show good agreements between device measurements and simulations.

RM02B-4 11:10

AlScN/Diamond Surface Acoustic Wave Resonators on Si Substrates with Frequency up to 33.7GHz

Lei Wang¹, Shuming Chen¹, Jinying Zhang², Jian Zhou¹, Jingting Luo³; ¹NUDT, China, ²UCAS, China, ³Shenzhen University, China

Abstract: The highest resonant frequency of surface acoustic wave (SAW) resonators up to 33.7 GHz are reported in this work, with an electromechanical coupling coefficient K^2 of 1.2%, insertion loss of 19.8 dB and Q factor of 2084. It is the first time that SAW devices work at Ka-band to our best knowledge. To achieve this, two new approaches are used. Firstly, a novel and efficient exposure process termed SELSP is proposed to fabricate high resolution interdigital transducers (IDTs). Secondly, a AlScN/diamond/Si layered structure is adopted to obtain high phase velocity and high K^2 . Comparing with the results of other recently reported state-of-the-art devices, the fabricated devices here show much higher frequency with comparable K^2 and lower insertion loss. This work opens the door for SAW devices to further applications in communication and detection fields with greater information throughputs and higher sensitivity.

Monday 11 June 2018

10:10–11:50

204A

Session RMO2C: ADC-Based RF/Mixed-Signal Systems and Wireline Transceiver Techniques

Chair: Yuxiang Zheng, FutureWei Technologies

Co-Chair: Fred Lee, Verily Life Sciences

RMO2C-1 10:10

An 8.8-GS/s 8b Time-Interleaved SAR ADC with 50-dB SFDR Using Complementary Dual-Loop-Assisted Buffers in 28nm CMOS

X. Shawn Wang¹, Chi-Hang Chan², Jieqiong Du¹, Chien-Heng Wong¹, Yilei Li¹, Yuan Du¹, Yen-Cheng Kuan³, Boyu Hu¹, Mau-Chung Frank Chang¹; ¹University of California, Los Angeles, USA, ²University of Macau, China, ³National Chiao Tung University, Taiwan

Abstract: This paper presents an 8.8 GS/s 16-way time-interleaved asynchronous SAR ADC fabricated in 28-nm CMOS technology. A two-level 2×8 master-slave hierarchical interleaved architecture is employed. A complementary dual-loop-assisted buffer is proposed to achieve both high linearity and bandwidth with low power. This time-interleaved ADC achieves 38.4-dB SNDR and 50-dB SFDR with a Nyquist input at 8.8 GS/s sampling rate and consumes 83.4 mW, resulting in a 140 fJ/conv.-step Walden FOM with buffers.

RMO2C-2 10:30

A Direct $\Delta\Sigma$ Receiver with Current-Mode Digitally-Synthesized Frequency-Translated RF Filtering

Sushil Subramanian, Hossein Hashemi; University of Southern California, USA

Abstract: A 0.5–2.75 GHz, 10 MHz bandwidth, direct $\Delta\Sigma$ receiver architecture that uses a mixed-signal technique to eliminate the baseband channel select filter and provides higher order filtering at RF front-end using a single feedforward op-amp is described. The RF-to-bits system uses feedback FIR-DACs and impedance upconversion to provide equivalent 2nd order analog filtering before the $\Delta\Sigma$ ADC. Measurements demonstrate up to 38 dB gain for the inband signal, with up to 9 dB improvement for the out-of-band IIP3 and a peak SNDR of 35 dB. The receiver is designed in a 65 nm CMOS technology, has an active area of 0.15 mm², and consumes 9.3–16.2 mW of power, with a total energy efficiency of 5.5–9.8 pJ/1vl across the centre frequency range.

RMO2C-3 10:50

A Methodology for Accurate DFE Characterization

Alireza Sharif-Bakhtiar, Anthony Chan Carusone; University of Toronto, Canada

Abstract: A simulation methodology to accurately characterize DFEs is introduced. The methodology relies upon a few short simulations with carefully contrived input waveforms to extract the DFE's effective response in situ capturing all non-linearities and speed limitations in the feedback circuits. The method is applied to a conventional 1-tap DFE and an infinite-impulse response (IIR) DFE. Measurement results from an IIR DFE in 65 nm CMOS technology verify the methodology.

RM02C-4 **11:10**

A Flexible Low-Latency DC-to-4 Gbit/s Link Operating from -40 to +200°C in 28nm CMOS for Galvanically Isolated Applications

Simon Ooms, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a communication link for galvanically isolated (GI) applications. The proposed link employs a 120 GHz OOK transmitter and receiver with a PTFE fiber as directive channel to reduce transmission losses. The receiver is implemented with a replica temperature compensation loop to provide operation from -40 to +200°C and thereby overcome the limitations of existing optical and magnetically coupled solutions. The presented work reports an isolated communication link with a data rate of 4 Gbit/s and reports the lowest latency of 1 ns with less than 4.5% variation over the entire measured temperature range. The power consumption of the entire link is only 52.4mW and achieves 13.1 pJ/bit efficiency.

Monday 11 June 2018

13:30–15:10

201A

Session RM03A: RF Front-Ends for Emerging Wireless Paradigms

Chair: Ramesh Harjani, University of Minnesota

Co-Chair: Leon van den Oever, Qualcomm

RM03A-1 13:30

**Fully-Integrated Non-Magnetic 180nm SOI Circulator with >1W P1dB,
>+50dBm IIP3 and High Isolation Across 1.85 VSWR**

Aravind Nagulu¹, Andrea Alù², Harish Krishnaswamy¹; ¹Columbia University, USA, ²CUNY Advanced Science Research Center, USA

Abstract: There has been recent progress on CMOS non-magnetic circulators based on switch-based spatio-temporal conductivity modulation, but these initial demonstrations remain limited in transmitter power handling, linearity, and ability to combat antenna variations. This paper describes a non-magnetic circulator in 180nm SOI CMOS that uses no external components, and employs various linearity enhancement techniques such as device stacking, optimal switch biasing, and localized ESD design to achieve >1W TX-ANT P1dB and >+50dBm TX-ANT IIP3 at 1GHz. A new loss-free and inductor-free antenna balancing approach enables high isolation for as high as 1.85 ANT VSWR and beyond. The circulator also exhibits low insertion losses of 2.1dB/2.9dB in the TX-ANT and ANT-RX paths, and ANT-RX NF of 3.1dB. These results represent a 10–100× enhancement in linearity/power handling over prior CMOS non-reciprocal circulators, and are shown to lower the power consumption of a communication link when compared with state-of-the-art electrical balance duplexers in scenarios where dynamic range is limited by P1dB, NF.

RM03A-2 13:50

**Full Duplex Circulator-Receiver Phased Array Employing Self-Interference
Cancellation via Beamforming**

Mahmood Baraani Dastjerdi, Negar Reiskarimian, Tingjun Chen, Gil Zussman, Harish Krishnaswamy; Columbia University, USA

Abstract: In this paper, we show how phased-array beamforming can be synergistically combined with full-duplex (FD) to achieve wideband RF self-interference (SI) suppression with minimal link budget (transmitter (TX) and receiver (RX) array gain) penalty and with no additional power consumption. An N-path-filter-based circulator-receiver FD front-end enables phased-array beamforming at baseband with minimal overhead by virtue of its multi-phase outputs. A 65nm CMOS scalable 4-element full-duplex circulator-receiver array is demonstrated that repurposes spatial beamforming degrees of freedom (DoFs) to achieve SI suppression, enabling (i) 50dB overall RF array self-interference cancellation (SIC) over 16.25MHz (WiFi-like) bandwidth (BW) with less than 3.5/3dB degradation in TX and RX array gains, respectively, across 8 elements, and (ii) 100dB overall array SIC suppression including digital SIC at +16.5dBm TX array power handling.

RM03A-3 14:10

Mixer-First MIMO Receiver with Multi-Port Impedance Tuning for Decoupling of Compact Antenna Systems

Charley Wilson III, Jacob Dean, Brian A. Floyd; North Carolina State University, USA

Abstract: This paper introduces mutual impedance tuning for N-path mixer-first MIMO receivers, useful for dynamic decoupling of coupled-antenna systems. A two-port mixer-first MIMO receiver is realized in 45-nm SOI CMOS and includes polyphase baseband resistive-coupling networks. This coupled response is upconverted to radio frequency to realize tunable mutual impedance. The two receivers consume 16 mW and operate over 0.1–3 GHz. Each receiver achieves 3–6 dB noise figure and 14–40 dB conversion gain. When connected to two antennas placed an eighth-wavelength apart, measurements show that N-path decoupling improves signal-to-noise ratio by 7 dB.

RM03A-4 14:30

An 8-Element, 1–3GHz Direct Space-to-Information Converter for Rapid, Compressive-Sampling Direction-of-Arrival Finding Utilizing Pseudo-Random Antenna-Weight Modulation

Matthew Bajor, Tanbir Haque, Guoxiang Han, Ciyuan Zhang, John Wright, Peter R. Kinget; Columbia University, USA

Abstract: The Direct Space-to-Information Converter (DSIC) unifies conventional delay-and-sum analog beamforming (CBF) with compressed-sampling (CS) rapid DoA finding into a single reconfigurable phased-array architecture. The DSIC chip includes 8 direct-conversion paths each delivering 32dB conversion gain, 3.3dBm in-band IIP3 and 6.4dB NF while consuming 19.8mW from 1.2V. The DSIC is able to switch between CBF-reception mode and CS-DoA mode in less than 1 μ s. In CS-DoA mode, the DSIC finds the DoA of a single emitter in 1 μ s consuming 158nJ which is 4 \times faster and 1.5 \times less energy than a comparable CBF scanner. For applications where many antennas are used, the DSIC uses an order of magnitude less energy than similar architectures.

RM03A-5 14:50

An FDD/FD Capable, Single Antenna RF Front End from 800MHz to 1.2GHz with Baseband Harmonic Predistortion

Hazal Yüksel, Thomas Tapen, Zachariah Boynton, Emory Enroth, Alyssa Apsel, Alyosha C. Molnar; Cornell University, USA

Abstract: A highly-integrated dual technology (28nm and 130nm SOI) widely tunable software-defined RF duplexing front-end for FDD, FD, and TDD applications is presented. Predistortion and harmonic upconversion are used to cancel second and third harmonics generated by PA nonlinearity by up to 30 dB. A novel form of non-reciprocal, distributed degeneration is used to suppress TX noise that desensitizes the RX for full duplex operation. The distributed degeneration network improves RX noise figure by 7dB over baseline TX operation for same channel TX-RX. The transceiver achieves a 23dBm output power while maintaining more than 30dB of TX-RX isolation over the 0.8–1.2GHz band.

Monday 11 June 2018

13:30–15:10

201B

Session RM03B: Mixed Signal Transmitters and Power Amplifiers

Chair: Jeffrey Walling, University of Utah

Co-Chair: Debo Chowdhury, Broadcom

RM03B-1 13:30

A 1W Quadrature Class-G Switched-Capacitor Power Amplifier with Merged Cell Switching and Linearization Techniques

Si-Wook Yoo, Shih-Chang Hung, Sang-Min Yoo; Michigan State University, USA

Abstract: A quadrature Class-G switched-capacitor power amplifier (SCPA) is implemented with a merged cell switching (MCS) and an inherent mismatch compensation for dual-supply voltage. The MCS technique improves power added efficiency (PAE) by adopting Class-G operation in quadrature IQ-Cell shared SCPA architecture in an efficient manner. The mismatch compensation technique can minimize nonlinearity from the mismatches in multiple supply voltages. The SCPA achieves peak output power and PAE of 30.1dBm and 37.0%, respectively. For 802.11g 64-QAM OFDM signal with 10.6dB PAPR (20MHz single-carrier 256-QAM signal with 7.6dB PAPR), it demonstrates an average output power of 19.5dBm (22.5dBm) and PAE of 14.7% (18.3%), while achieving EVM of -40.7dB (-40.3dB).

RM03B-2 13:50

A 0.19mm² 128mW 0.8–1.2GHz 2-Beam 8-Element Digital Direct to RF Beamforming Transmitter in 40nm CMOS

Boyi Zheng, John Bell, Yan He, Lu Jie, Michael P. Flynn; University of Michigan, USA

Abstract: An order of magnitude improvement in area and power consumption per element is achieved by digital phase shifting combined with bandpass $\Delta\Sigma$ modulation and N-path filtering. The 8-element beamforming transmitter allows accurate steering of multiple independent beams. Key to the efficiency are the pairing of area-efficient bandpass $\Delta\Sigma$ modulation with N-path filtering to suppress quantization noise and careful frequency management to allow efficient digital phase shifting and up-conversion. The 40nm CMOS prototype generates two independent 1.2GHz beams, it consumes 128mW and occupies an active area of only 0.19mm², consuming only 16mW and 0.02mm² per element.

RM03B-3 14:10

A Wide-Band Transmitter and Low-Noise PLL for a Highly Integrated 4T-4R-2F ZIF Transceiver in 28nm

P. Litmanen¹, S. Akhtar², S. Finocchiaro², F. Dantoni²; ¹Qorvo, USA, ²Texas Instruments, USA

Abstract: A low power base station analog TX chain and low noise PLL supporting all 3GPP R13/14 bands from 400MHz to 6GHz are implemented as part of a 4 transmit/receive and 2 feedback receive SOC in 28nm. With 600MHz of instantaneous bandwidth, the TX outputs -9dBm of LTE20 power with

an ACLR of -68.6dBc and -159dBm/Hz noise floor at 2.6GHz while providing 40dB of gain control in 1dB steps. -60dBc of narrowband raw image rejection is obtained through analog quadrature correction. The PLL double sided integrated phase noise is -44dBc at 2.7GHz.

RM03B-4 14:30

A 30-dBm Class-D Power Amplifier with On/Off Logic for an Integrated Tri-Phasing Transmitter in 28-nm CMOS

Mikko Martelius¹, Kari Stadius¹, Jerry Lemberg¹, Enrico Roverato¹, Tero Nieminen², Yury Antonov¹, Lauri Anttila³, Mikko Valkama³, Marko Kosunen¹, Jussi Ryyänen¹; ¹Aalto University, Finland, ²CoreHW, Finland, ³Tampere University of Technology, Finland

Abstract: This paper presents an eight-unit class-D power amplifier (PA), implemented in 28-nm CMOS. The PA is designed to utilize tri-phasing modulation, which combines coarse-amplitude polar modulation with fine-resolution outphasing components. This new technique enables achieving the back-off efficiency of multilevel outphasing without linearity-degrading discontinuities in the output waveform. Each PA unit contains a cascaded output stage with a 3.6-V supply voltage, and on/off logic enabling multilevel operation controlled by low-voltage signals. The PA achieves a peak output power of 29.7 dBm with a 34.7% efficiency, and is verified to operate with aggregated LTE signals at bandwidths up to 60 MHz at 1.7-GHz carrier frequency.

Monday 11 June 2018

13:30–15:10

204A

**Session RM03C: cm/mm-Wave CMOS Integrated Phased-Array
Building Blocks**

Chair: Domine Leenaerts, NXP Semiconductors

Co-Chair: Osama Shana'a, MediaTek

RM03C-1 13:30

**Ka-Band CMOS 360° Reflective-Type Phase Shifter with ± 0.2 dB Insertion
Loss Variation Using Triple-Resonating Load and Dual-Voltage Control
Techniques**

Peng Gu, Dixian Zhao; Southeast University, China

Abstract: This paper demonstrates the design of a Ka-band 360° reflective-type phase shifter (RTPS). Triple-resonating load technique is used to reach broadband full 360° phase-shift range and achieve low insertion loss variation. With dual-voltage control technique adopted, insertion loss variation is further reduced. Implemented in 65nm CMOS technology, the proposed RTPS achieves 379° phase-shift range at 29 GHz with only one control voltage. With dual-voltage control, a measured phase-shift range of 360° with 8.3 ± 0.2 dB insertion loss is achieved at 29 GHz. It also ensures 360° phase-shift range and 8–9 dB insertion loss (i.e., <1 dB variation) across 27.8–31.2 GHz. The corresponding return loss across frequencies are better than 20 dB.

RM03C-2 13:50

**A 60GHz 360° Phase Shifter with 2.7° Phase Resolution and 1.4° RMS
Phase Error in a 40-nm CMOS Technology**

Bindi Wang, Hao Gao, M.K. Matters-Kammerer, Peter G.M. Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents a vector modulator based active phase shifter for the 56–65 GHz frequency band in a 40-nm digital CMOS technology. The design comprises a magnetically-enhanced quadrature hybrid with better than 1-degree phase imbalance and 18 dB tuning range variable gain amplifiers with transformer broadband matching to generate 360° full-range phase tuning. It achieves 2.7° phase resolution for the first time. The rms phase error of the phase shifter is 1.4° and the rms gain error is 0.13 dB at 60 GHz. The insertion loss is 0.4 dB. The power consumption is 38 mW.

RM03C-3 14:10

Low-Loss and Small-Size 28GHz CMOS SPDT Switches Using Switched Inductor

Wonho Lee, Songcheol Hong; KAIST, Korea

Abstract: In this paper, low-loss and small-size single-pole double-throw (SPDT) switches using a switched inductor are presented. The switched inductor is composed of a single inductor and two inductor switches which reconfigure the inductor between two output ports. It is designed to be connected to a turned-off series FET switch to resonate out the off-capacitance. All ports are matched to 50 Ohm by using the single inductor, which allows it to have low insertion loss (IL) and small size. Two types of SPDT switches which have the switched inductor are implemented in 65 nm CMOS process, one is a series type switch and the other is series-shunt type one. The series type one shows 0.89 dB IL, 18.2 dB isolation and the input P1dB of 12.55 dBm at 28 GHz, whereas the series-shunt type one shows 1.06 dB IL, 39 dB isolation and the input P1dB of 7.25 dBm. Both SPDT switches are operated in 25–39.5 GHz maintaining return loss less than -20 dB. Size of series and series-shunt type of the SPDT switches are 0.009 mm² and 0.01 mm², respectively.

RM03C-4 14:30

A Ka-Band CMOS Digital-Controlled Phase-Invariant Variable Gain Amplifier with 4-Bit Tuning Range and 0.5-dB Resolution

Yongran Yi, Dixian Zhao, Xiaohu You; Southeast University, China

Abstract: This paper presents a broadband digital-controlled variable gain amplifier (VGA) in 65-nm CMOS. The phase-invariant technique is proposed to minimize the phase variation under different gain modes. The proposed differential VGA achieves a measured gain tuning range of 7.5 dB and gain resolution of 0.5 dB with < 2.5° phase variation at 34 GHz. The RMS gain error is less than 0.15 dB. The VGA has a -1-dB bandwidth of 8 GHz (i.e., 30 GHz – 38 GHz) and -3-dB bandwidth of 15 GHz (i.e., 27 GHz – 42GHz). The measured P_{1dB} , P_{3dB} and PAE_{MAX} are 2.5 dBm, 5.5 dBm and 18.3%, respectively.

RM03C-5 14:50

A 5-Bit, 0.25dB Step Variable Attenuator at E-Band

Tyler N. Ross, Kimia T. Ansari, Sam Tiller, Morris Repeta; Huawei Technologies, Canada

Abstract: A variable attenuator operating over 71 GHz to 76 GHz is presented. The circuit design, based on a differential Π attenuator, allows for precise control over the attenuation due to a feedback control circuit. When manufactured using the CMOS portion of a 55 nm BiCMOS technology, the attenuator demonstrated the ability to obtain approximately 0.25 dB attenuation steps with an RMS phase error of 0.9° using a 5-bit digital control signal. The total DC power consumption of the attenuator (including control circuitry) is 1 mW and the circuit occupies 410 $\mu\text{m} \times 130 \mu\text{m}$ of chip area (1080 $\mu\text{m} \times 600 \mu\text{m}$ including test baluns and pads).

Monday 11 June 2018

15:40–17:20

201A

Session RM04A: Ultra-Low Power Radios for Security, Ranging and Connectivity

Chair: Gernot Hueber, NXP Semiconductors

Co-Chair: David Wentzloff, University of Michigan

RM04A-1 15:40

A Secure TOF-Based Transceiver with Low Latency and Sub-cm Ranging for Mobile Authentication Applications

Haixin Song, Zhendong Ding, Woogeun Rhee, Zhihua Wang; Tsinghua University, China

Abstract: This paper describes a low-power localization-verified transceiver system for secure wireless remote control and authentication applications. A pulse-based time-of-flight (TOF) method is employed for low latency localization to overcome the relay attack problem, while PPM and BPSK being used for spectrum-compliant short-range communication. Noncoherent edge-detection demodulation along with the PPM enables a short processing time between data demodulation and retransmission, satisfying the requirement of a bit-exchange step for secure distance-bounding protocols against the relay attack. Digital-intensive TOF localization with fine ranging resolution is performed by a $\Delta\Sigma$ time-to-digital converter (TDC). A prototype 3-to-5GHz pulse-based transceiver for localization and communication is implemented in 65nm CMOS. With duty-cycled operation, the transceiver consumes 14.2mW from a 1V supply and achieves the RMS ranging accuracy of 4.7mm.

RM04A-2 16:00

A 264- μ W 802.15.4a-Compliant IR-UWB Transmitter in 22nm FinFET for Wireless Sensor Network Application

Renzhi Liu¹, Brent R. Carlton¹, Stefano Pellerano¹, Farhana Sheikh¹, Divya Shree Vemparala¹, Ahmed Ali², V. Srinivasa Somayazulu¹; ¹Intel, USA, ²University of Texas at Dallas, USA

Abstract: A fully-integrated 802.15.4a-compliant IR-UWB transmitter (TX) in Intel 22nm FinFET Low Power process is presented. The TX consumes 264 μ W while transmitting -16.2dBm at 110kbps data rate in 8GHz band with 9.1% TX efficiency. The TX supports both coherent and non-coherent 802.15.4a operation and only requires a 32.768kHz real-time clock for non-coherent operation.

RM04A-3 16:20

A 486 μ W All-Digital Bluetooth Low Energy Transmitter with Ring Oscillator Based ADPLL for IoT Applications

Xing Chen¹, Jacob Breiholz², Farah Yahya², Christopher Lukas², Hun-Seok Kim¹, Benton Calhoun², David D. Wentzloff¹; ¹University of Michigan, USA, ²University of Virginia, USA

Abstract: This paper presents an all-digital Ring Oscillator (RO) based Bluetooth Low-Energy (BLE) transmitter (TX) for ultra-low-power radios in short range IoT applications. It employs a wideband ADPLL featuring an $f_{\text{RO}}/4$ RO, with an embedded 5-bit TDC. A 4 \times frequency edge combiner

is used to generate the 2.4GHz signal. This helps reduce the power consumption and enhance its phase noise performance at the same time. A switch-capacitor PA is optimized for high efficiency in low power mode. The TX is designed at the phase noise limit for BLE and in low power mode it consumes 486 μW while configured as a non-connectable advertiser, which has been validated by wirelessly communicating beacon messages to a mobile phone.

RM04A-4 16:40

A 217 μW -82dBm IEEE 802.11 Wi-Fi LP-WUR Using a 3rd-Harmonic Passive Mixer

Jaeho Im, Hun-Seok Kim, David D. Wentzloff; University of Michigan, USA

Abstract: A 40nm CMOS IEEE 802.11 Wi-Fi LP-WUR receiver is presented. The receiver demodulates OOK messages generated by an 802.11 OFDM Wi-Fi transmitter operating at 5.8GHz. The receiver improves sensitivity by allocating the image-less single sideband signal above the flicker noise floor. The 3rd harmonic down-conversion receiver reduces active power consumption, while rejecting unwanted harmonic components. The receiver achieves a sensitivity of -82dBm while consuming 217 μW at a BER of 10^{-3} and data-rate of 62.5kb/s.

RM04A-5 17:00

Ultra-Fast Bit-Level Frequency-Hopping Transmitter for Securing Low-Power Wireless Devices

Rabia Tugce Yazicigil¹, Phillip Nadeau², Daniel Richman³, Chiraag Juvekar¹, Kapil Vaidya⁴, Anantha P. Chandrakasan¹; ¹MIT, USA, ²Analog Devices, USA, ³D. E. Shaw Research, USA, ⁴IIT Bombay, India

Abstract: Current BLE transmitters are susceptible to selective jamming due to long dwell times in a channel. To mitigate these attacks, we propose physical-layer security through an ultra-fast bit-level frequency-hopping (FH) scheme by exploiting the frequency agility of bulk acoustic wave resonators (BAW). Here we demonstrate the first integrated bit-level FH transmitter (TX) that hops at 1 μs period and uses data-driven random dynamic channel selection to enable secure wireless communications with additional data encryption. This system consists of a time-interleaved BAW-based TX implemented in 65nm CMOS technology with 80MHz coverage in the 2.4GHz ISM band and a measured power consumption of 10.9mW from 1.1V supply.

Monday 11 June 2018

15:40–17:20

201B

Session RMO4B: Silicon Integrated mm-Wave Transmitters

Chair: Q. Jane Gu, University of California, Davis

Co-Chair: Mona Hella, Rensselaer Polytechnic Institute

RM04B-1 15:40

Q-Band CMOS Transmitter System-on-Chip for Protected Satellite Communication

T. LaRocca, K. Thai, R. Snyder, R. Jai, O. Fordham, N. Daftari, B. Wu, Y. Yang, M. Watanabe; Northrop Grumman, USA

Abstract: This paper reports the first fully integrated millimeter-wave CMOS transmitter system-on-chip (SoC) for protected communication enabling next generation terminals. A 200MHz DDR digital baseband input drives a complex frequency translator with sub-Hz frequency hopping resolution via an on-chip numerically controlled oscillator (NCO). Two 12b RZ DACs and quadrature modulator form a single-side band (SSB) up-converter achieving >30 dB spur rejection. An RF up-converter with a $\times 2$ multiplier drives a 24dBm Q-band CMOS stacked power amplifier. The SoC was demonstrated in a current AEHF terminal and achieved $5\times$ lower power consumption and size.

RM04B-2 16:00

An E-Band QPSK Transmitter Element in 28-nm CMOS with Multistate Power Amplifier for Digitally-Modulated Phased Arrays

Nai-Chung Kuo, Ali M. Niknejad; University of California, Berkeley, USA

Abstract: This work presents a 2-Gb/s E-band transmitter (Tx) element with a QPSK modulator, injection-lock LO sextupler, all-digital input interface, and a wideband 8-state power amplifier (PA) in 28-nm bulk CMOS. The PA has a saturation power of 15.7 dBm at 78 GHz and power added efficiency (PAE) of 8.9%. The Tx outputs 13.1 dBm when the PA is driven by the modulator, with a system efficiency of 4.7%. The injection-lock LO generation, modulator I/Q correction, and the digitally-modulated PA output magnitude make the Tx element a suitable building block for digitally modulated phased array applications.

RM04B-3 16:20

A Low EVM SiGe BiCMOS 40–100GHz Direct Conversion IQ Modulator for Multi-Gbps Communications Systems

Qian Ma, Hyunchul Chung, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 40–100 GHz wideband direct conversion IQ modulator with IQ correction capability and flip-chip packaging in GF8HP 0.12 μ m SiGe BiCMOS technology. The modulator chip covers Q-, V-, E-, and W-bands and is flipped on a low-cost RF board for connectorized measurements. The measured IQ modulator conversion gain is 5–8 dB at 40–100 GHz with an OP1dB of -2 to -5 dBm. A single-sideband (SSB) rejection higher than 42 dBc and an LO leakage

rejection better than 35 dBc is measured. A 64-QAM modulated waveform with a data rate of 12 Gb/s (2Gbaud/s) and 2.4% error vector magnitude (EVM) is successfully demonstrated at 72 GHz. To our knowledge, this modulator achieves state-of-the-art performance in terms of bandwidth, wideband SSB rejection, and EVM at multi-Gbps data rate, and with applications in millimeter-wave high data-rate 5G systems.

RMO4B-4 16:40

A 120GHz I/Q Transmitter Front-End in a 40nm CMOS for Wireless Chip to Chip Communication

Chae Jun Lee, Seung Hun Kim, Hyuk Su Son, Dong Min Kang, Joon Hyung Kim, Chul Woo Byeon, Chul Soon Park; KAIST, Korea

Abstract: This paper presents a 120 GHz low-power wideband I/Q transmitter in a 40 nm CMOS technology for wireless chip to chip communication. The proposed transmitter consists of an up-conversion mixer, a Quadrature Injection-Locked Oscillator (QILO), gain amplifiers, and a power amplifier. The cross-coupled-capacitor topology was used to improve the conversion gain of the up-conversion mixer. By adopting a linearizer, the power amplifier achieved an output P1dB of 11 dBm. The transmitter exhibited a conversion gain of 13.5 dB, a 3 dB bandwidth of 14 GHz, and an output P1 dB of 4.5 dBm. The maximum gain mismatch between the I and Q channels in the signal bandwidth are within 2 dB. The transmitter consumed only 271 mW and its chip size is 1.51 mm².

RMO4B-5 17:00

A 0.3-V 2.5-mW 154-to-195GHz CMOS Injection-Locked LO Generation with -186.5dB FoM

Xiaolong Liu, Howard C. Luong; HKUST, China

Abstract: A harmonic extraction technique is proposed to enhance the third-harmonic output amplitude and phase noise of LC oscillators and injection-locked frequency multipliers (ILFMs). Utilizing this technique, a cascaded ILFM-based LO generation is demonstrated. Implemented in a 65-nm CMOS process and consuming only 2.5 mW, the prototype achieves a frequency tuning range of 23.7% from 153.9 to 195.3 GHz while measuring phase noise of -106.8 dBc/Hz at 10-MHz offset, corresponding to FoM of -186.5 dBc/Hz and FoM_r of -194.1 dBc/Hz and occupying a core area of 0.08 mm².

Monday 11 June 2018

15:40–17:20

204A

Session RMO4C: Highly Efficient mm-Wave Oscillators with Wide Tuning Range

Chair: Foster Dai, Auburn University

Co-Chair: Ruonan Han, MIT

RMO4C-1 15:40

A -195dBc/Hz FoM_T 20.8-to-28-GHz LC VCO with Transformer-Enhanced 30% Tuning Range in 65-nm CMOS

S. Lightbody¹, A.H.M. Shirazi¹, H. Djahanshahi², R. Zavari², S. Mirabbasi¹, S. Shekhar¹; ¹University of British Columbia, Canada, ²Microsemi, Canada

Abstract: Low quality factor (Q) of varactors and increased ratio of parasitic capacitance to total tank capacitance impede the design of high-frequency voltage-controlled oscillators (VCOs) that must attain wide frequency tuning range (FTR) and low phase noise (PN). We propose a VCO topology which instead of directly connecting a varactor to the oscillator core, leverages a transformer to magnetically couple the varactor to the core. This approach increases the tuning range of the varactor by doubling the bias range, further reduces the parasitic capacitance seen by the varactor, and boosts the resonator tank Q due to impedance transformation. Thus, both PN and FTR are improved simultaneously. Measurement results for the prototype VCO implemented in 65-nm CMOS show an FTR of 29.8% from 20.77 to 28.02 GHz while consuming 12.65 to 15.12 mW. A PN of -106.6 dBc/Hz at a 1 MHz offset and an FoM_T of -195 dBc/Hz are attained.

RMO4C-2 16:00

A 31.8–40.8GHz Continuously Wide-Tuning VCO Based on Class-B Oscillator Using Single Varactor and Inductor

Jayol Lee, Dong-Woo Kang, Youngseok Baek, Bontae Koo; ETRI, Korea

Abstract: A 31.8–40.8GHz continuously voltage-tuning LC-tank CMOS differential VCO is presented that has been designed by using only a pair of varactors and single symmetric inductor available from library, and adopting class-B oscillator. The push-pull complementary class-B oscillator is applied in the VCO to isolate LC-tank resonator from external and internal loads, and to produce more negative resistance, and thus resulting in wide frequency tuning range. The VCO shows 24.8% tuning range, -93.5dBc/Hz phase noise at 1MHz offset, and -14dBm output power with 50Ω load. The VCO is manufactured using 40nm CMOS process with consuming 20mW in oscillator circuit.

RMO4C-3 16:20

A Dual-Core 60GHz Push-Push VCO with Second Harmonic Extraction by Mode Separation

Vadim Issakov¹, Fabio Padovan²; ¹Infineon Technologies, Germany, ²Infineon Technologies, Austria

Abstract: In this work we present a 60 GHz dual-core push-push Colpitts VCO in 0.13 μm SiGe

BiCMOS technology. We propose a circuit technique to extend a Colpitts VCO to a dual-core operation. Additionally, we propose a novel circuit technique that enables extraction of the second-harmonic from a VCO core for push-push operation by means of mode-separation. The principle takes advantage of the fact that the second harmonic is present in a differential VCO in a common-mode. Hence, the fundamental signal can be coupled out from a VCO in differential mode, whereas the second harmonic signal can be coupled via the common-mode. This enables extraction of signals, without loading the VCO core directly by input capacitance of the following buffer stages, which might deteriorate the phase noise. The VCO achieves in measurement a low phase noise of -107 dBc/Hz at 1 MHz offset at 62 GHz and an output power of -1.9 dBm. The VCO including buffer, biasing and frequency divider dissipates in dual-core operation 112 mA, whilst a single VCO core consumes only 24 mA from a single 1.8 V supply. The chip consumes area of 0.95 mm² including pads, buffer and frequency divider chain.

RM04C-4 16:40

A 200-GHz Sub-Harmonic Injection-Locked Oscillator with 0-dBm Output Power and 3.5% DC-to-RF-Efficiency

Songhui Li, David Fritsche, Corrado Carta, Frank Ellinger, Technische Universität Dresden, Germany

Abstract: This paper presents a sub-harmonic injection-locked oscillator (SHILO) fabricated in a 130-nm SiGe-BiCMOS technology. It consists of a frequency tripler and an injection-locked oscillator. The SHILO can be locked from 177 GHz to 201 GHz with an injected signal from 59 GHz to 67 GHz. At 195 GHz, the maximum output power is 0 dBm from 28.8mW DC power consumption and less than -21 dBm injected power at 65 GHz. The circuit outperforms the more-common chains of amplifiers and frequency multipliers to generate the local oscillator (LO) signal at frequencies around 200 GHz. To the best knowledge of the authors, the DC-to-RF efficiency of 3.8% is the highest reported compared to amplifier-based frequency-multiplier chains in signal sources at these frequencies.

RM04C-5 17:00

A 20.7–31.8GHz Dual-Mode Voltage Waveform-Shaping Oscillator with 195.8dBc/Hz FoM_r in 28nm CMOS

Yiyang Shu, Huizhen Jenny Qian, Xun Luo; UESTC, China

Abstract: A 20.7–31.8GHz dual-mode voltage waveform-shaping oscillator is presented in this paper. Dual-mode voltage waveform shaping resonator is proposed to excite two pairs of resonances, representing fundamental and third-order harmonic in two modes, respectively. Mode-switch-circuits are implemented to allocate specific mode without degrading the Q-factor of the resonator. As a result, the square-like voltage waveform can be obtained in dual-mode to reduce the ISF rms value for lower phase noise and further extend the tuning range. The oscillator is fabricated using a conventional 28nm CMOS technology with the core size of $420\mu\text{m}$ by $160\mu\text{m}$, which exhibits a measured phase noise of -102.46 dBc/Hz at 1MHz offset with a carrier frequency of 25.56GHz. A state-of-the-art FoM_r of 195.8dBc/Hz is achieved with the wide tuning range of 42.3% and power consumption of 5.5mW.

Tuesday 12 June 2018

08:00–09:40

201A

Session RTU1A: mm-Wave Power Amplifiers

Chair: Margaret Szymanowski, NXP Semiconductors

Co-Chair: Gary Hau, Qualcomm

RTU1A-1 8:00

A Continuous-Mode 23.5–41GHz Hybrid Class-F/F-1 Power Amplifier with 46% Peak PAE for 5G Massive MIMO Applications

Tso-Wei Li, Hua Wang; Georgia Tech, USA

Abstract: This paper presents a continuous-mode hybrid Class-F and inverse Class-F (i.e., Class-F/F-1) power amplifier (PA) to achieve high efficiency and wide bandwidth covering the potential 5G bands of 28, 37, and 39GHz. The proposed continuous-mode harmonically tuned output network provides the proper harmonic impedance terminations for the continuous Class-F and Class-F-1 operation modes at lower and higher frequency bands, respectively. Moreover, both modes present high efficiency and deliver almost the same saturated power P_{sat} with a P_{sat} variation less-than 0.1dB. The proposed PA is implemented in a 45nm CMOS SOI process, achieving 46% peak PAE, 54.3% P_{sat} output power 1dB bandwidth (23.5GHz to 41GHz), and 51% small-signal 3dB bandwidth (25.9GHz to 43.7GHz). Also, it achieves 43.4% PAE and 18.6dBm P_{sat} at 27GHz, 40.2% PAE and 18.6dBm P_{sat} at 37GHz, and 41.2% PAE and 18.5dBm P_{sat} at 39GHz, respectively, outperforming reported mm-Wave silicon PAs at similar frequencies. This is the first demonstrated continuous-mode hybrid Class-F/F-1 PA in CMOS to cover the 28, 37, and 39GHz mm-Wave 5G bands.

RTU1A-2 8:20

A Compact 75GHz PA with 26.3% PAE and 24GHz Bandwidth in 22nm FinFET CMOS

Steven Callender, Stefano Pellerano, Christopher Hull; Intel, USA

Abstract: This paper presents the design of an E-band PA in a 22nm FinFET CMOS process. The design utilizes device neutralization and low-k transformers for gain and bandwidth enhancement. A holistic design methodology is employed to further optimize PA efficiency. The PA achieves a peak gain of 18.6dB with a 3dB bandwidth of 62–86GHz (24GHz). At 75GHz, the measured P_{sat} , $OP_{1\text{dB}}$, and peak PAE are +12.6dBm, +5.7dBm, and 26.3%, respectively. The PA can amplify a 6Gb/s 16-QAM signal at an average P_{out} of +5dBm with a PAE of 10% and -26dB EVM(rms). Compact layout of the PA yields a core area of 0.054mm², enabling compact integration into phased array transceivers.

RTU1A-3 8:40

A K-Band Power Amplifier with 26-dBm Output Power and 34% PAE with Novel Inductance-Based Neutralization in 90-nm CMOS

Wei-Cheng Huang, Jung-Lin Lin, Yu-Hsuan Lin, Huei Wang; National Taiwan University, Taiwan

Abstract: A fully-integrated K-band transformer combined power amplifier (PA) with novel neutralization technique is presented and implemented in 90-nm CMOS technology for 5G and 24-GHz ISM-band applications. Four single-stage cascode cells are combined with transformers as two differential amplifier cells. Current-combining topology is used to combine the two differential amplifier cells to increase output power. The asymmetrical transformers are designed to compensate phase imbalance. The novel inductance-based neutralization structure is utilized to cope with the overall stability issue. Thus, the optimal transistor sizes can be chosen to achieve high output power and power added efficiency (PAE). The measurement results demonstrate 16.3-dB small-signal gain, saturated power (P_{sat}) of 26.0 dBm, output 1-dB compression point ($OP_{1\text{dB}}$) of 23.2 dBm, and peak PAE of 34% at 28 GHz. The chip size with all pads is 0.401 mm². To the authors' knowledge, this circuit demonstrates a superior output power and PAE performance compared with the reported K-band CMOS PAs.

RTU1A-4 9:00

A 14.8dBm 20.3dB Power Amplifier for D-Band Applications in 40nm CMOS

Dragan Simic, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a high output power, high gain, class-AB power amplifier (PA) in 40nm CMOS technology for D-band applications. Two-way transformer-based power-combining is implemented in order to increase output power. The supply voltage of the designed PA is 1V. The PA achieves a P_{SAT} of 14.8 dBm, small-signal gain of 20.3 dB and maximum PAE of 8.9% at 140 GHz.

RTU1A-5 9:20

A 31GHz 2-Stage Reconfigurable Balanced Power Amplifier with 32.6dB Power Gain, 25.5% PAE_{max} and 17.9dBm P_{sat} in 28nm FD-SOI CMOS

Florent Torres¹, Magali De Matos², Andrea Cathelin¹, Eric Kerhervé²; ¹STMicroelectronics, France, ²IMS (UMR 5218), France

Abstract: In this paper, a 31GHz reconfigurable balanced 2-stage power amplifier (PA) integrated in 28nm FD-SOI CMOS technology is demonstrated aiming for SoC implementation. Fine grain wide range power gain control with more than 10dB tuning range is enabled by body biasing feature while the design improves VSWR robustness, stability and reverse isolation by using optimized 90° hybrid couplers and capacitive neutralization over both stages. Maximum power gain of 32.6dB, PAE_{max} of 25.5% and P_{sat} of 17.9dBm are measured, while robustness to industrial temperature range and process spread is demonstrated. This PA exhibits a maximum ITRS figure of merit of 26,925 which is the highest reported around 30GHz to authors' knowledge.

Tuesday 12 June 2018

08:00–09:40

201B

Session RTU1B: Submillimeter Wave and Terahertz ICs

Chair: Hossein Hashemi, University of Southern California

Co-Chair: Vipul Jain, Anokiwave

RTU1B-1 8:00

A 410GHz OOK Transmitter in 28nm CMOS for Short Distance Chip-to-Chip Communications

Alexander Standaert, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a 410GHz OOK transmitter in 28nm bulk CMOS. The transmitter is packaged together with a metal coated 3D printed horn antenna and has a measured EIRP of -3.99 dBm. Modulated measurements are demonstrated through a dielectric waveguide channel. 5 Gbps is demonstrated over a 13 cm channel and up to 1 Gbps over a 61 cm long channel. The transmitter provides a solution for high frequency short distance chip-to-chip or intra-board interconnects.

RTU1B-2 8:20

A 308–317GHz Source with 4.6mW Peak Radiated Power and On-Chip Frequency-Stabilization Feedback in 0.13 μ m BiCMOS

Chen Jiang¹, Mohammed Aseeri², Andreia Cathelin³, Ehsan Afshari¹; ¹University of Michigan, USA, ²KACST, Saudi Arabia, ³STMicroelectronics, France

Abstract: In this paper, a 308–317GHz radiating source is presented. The output frequency of the 6 \times 4 radiator array is stabilized with an entirely on-chip frequency detection and feedback mechanism realized mainly by passive EM structures. This feedback mechanism eliminates the need for both frequency dividers and the off-chip reference, achieving much lower system cost and power consumption. Fabricated using a 0.13 μ m BiCMOS process, the proposed source achieves a peak radiated power and EIRP of 4.6mW and 24.7dBm, respectively, with a total dc power consumption of 1.18W. The frequency tuning range is larger than 2.7%. The measured phase noise at 1MHz offset is -80.1dBc/Hz.

RTU1B-3 8:40

A 280GHz +9dBm TRP Dense 2D Multi Port Radiator in 65nm CMOS

Nadav Buadana, Samuel Jameson, Eran Socher; Tel Aviv University, Israel

Abstract: A fully integrated and digitally controlled Multi-port dense 2D radiator is presented in this paper. Compared to conventional approach, the silicon die is here treated as a Dielectric Resonant Antenna (DRA). Each source consists of W-band Voltage Controlled Oscillator (VCO) connected to an exciting loop element to inject its 3rd harmonic to the DRA. Occupying only 1.4 \times 1.4 mm², the array elements are injection locked in frequency due to the tight coupling of the adjacent elements without the need of any locking signal. High resolution DACs are used to accurately set the frequency and a 3 wire SPI control interface is implemented. Fabricated in standard 65nm CMOS process, the

array achieves an EIRP of 24 dBm, a record TRP of +9 dBm and power density of 4mW/mm² with 1.8% efficiency at 280 GHz.

RTU1B-4 9:00

Heterodyne Sensing CMOS Array with High Density and Large Scale: A 240-GHz, 32-Unit Receiver Using a De-Centralized Architecture

Zhi Hu, Cheng Wang, Ruonan Han; MIT, USA

Abstract: This paper reports the first large-scale, dense sub-THz heterodyne array featuring: (1) compactness of units: two interleaved 4×4 arrays with $\lambda/2$ unit pitch are integrated in a 1.2-mm² space; (2) multi-functionality of circuits: each array unit simultaneously achieves LO generation, inter-unit synchronization, incident wave coupling and down-conversion; (3) global phase locking: a strongly-coupled 2D LO network is phase locked to a 75-MHz reference, enabling phase-coherent pairing with off-chip transmitters; (4) scalability: array scale increase and lower LO phase noise are facilitated by eliminating the global routing and power sharing of sub-THz LO; (5) parallelism: beam forming from the two sub-arrays can be processed concurrently. A chip prototype using bulk 65-nm CMOS technology is implemented with 980-mW DC power. Array-wide 240-GHz LO locking is achieved with a measured phase noise of -84 dBc/Hz (1-MHz offset). The measured sensitivity (BW=1 kHz) of a single unit is 38.8-pW. This is >6× improvement over prior sub-THz arrays with similar scale and density but without phase-detection capability.

RTU1B-5 9:20

Proximal-Field Radiation Sensors for Millimeter-Wave Integrated Radiators

Amirreza Safaripour, Bahar Asghari, Ali Hajimiri; Caltech, USA

Abstract: Integration of Proximal-Field Radiation Sensors (PFRS) with mm-wave integrated radiators enables extraction of valuable information about their far-field radiation properties from the surface waves inside the substrate and the electromagnetic fields in close proximity of the radiating antennas. In this paper, we present a 72 GHz 2×1 integrated radiator array with four on-chip PFRS units to show proximal-field sensing capability in calculation of far-field radiation properties solely through on-chip measurement of proximal fields.

Tuesday 12 June 2018

08:00–09:40

204A

Session RTU1C: mm-Wave Radar and Beamforming Transceivers

Chair: Vito Giannini, Uhnder

Co-Chair: Pierre Busson, STMicroelectronics

RTU1C-1 8:00

**A 35GHz mm-Wave Pulse Radar with Pulse Width Modulated by SDM
Realizing Sub-mm Resolution for 3D Imaging System**

Shunli Ma, Jincheng Zhang, Tianxiang Wu, Junyan Ren; Fudan University, China

Abstract: This paper describes a novel fully integrated mm-wave pulse radar chip with pulse width modulated by sigma-delta modulation (SDM) realizing sub-millimeter resolution for 3D imaging system. The carrier frequency is 35 GHz. For pulse radar system, the distance resolution is highly related to the pulse width. In this paper, the pulse widths of transmitted signals are modulated by SDM. The proposed pulse radar is composed of 35 GHz transmitter and receiver. The pulse generator consists of a 35 GHz phase-locked loop (PLL), a delay-locked loop (DLL) and a SDM. The receiver consists of low noise amplifier (LNA), envelope detector and time to voltage converter with calibration. The transmitter circuit consumes 61 mW with 10 dBm output power and receiver circuits consume 21 mW with -91.5 dBm sensitivity. The chip is fabricated in 65 nm CMOS process, the measurement results show the proposed radar chip can realize 0.2 mm distance resolution.

RTU1C-2 8:20

Monitoring Architecture for a 76–81GHz Radar Front End

Karthik Subburaj¹, Brian Ginsburg², Pankaj Gupta¹, Krishnanshu Dandu², Sreekirana Samala², Dan Breen², Karthik Ramasubramanian¹, Tim Davis², Zahir Parkar¹, Dheeraj Shetty¹, Rohit Chatterjee¹, Zeshan Ahmad², Neeraj Nayak², Meysam Moallem², Eunyoung Seok², Karan Bhatia², Shankar Ram Narayanamoorthy¹, Anjan Prasad Easwaran¹, Tom Altus², Sriram Murali¹, Vito Giannini², Indu Prathapan¹, Sachin Bharadwaj¹, Sumeer Bhatara¹, Venkatesh Srinivasan², Sai Gunaranjan¹, Sundararajan Rangachari¹; ¹Texas Instruments, India, ²Texas Instruments, USA

Abstract: This paper proposes architectures to comprehensively monitor the functionality of a 76-to-81GHz Frequency Modulated Continuous Wave (FMCW) radar front end, for safety critical automotive applications. These on-chip monitors periodically measure critical performance parameters and internal voltages of the radar transmitters (TX), receivers (RX) and local oscillator (LO), to detect failures in the field. They are implemented as a combination of mm-wave, analog, digital and firmware components in a radar IC in 45nm CMOS technology.

RTU1C-3 8:40

A 151-to-173GHz FMCW Transmitter Achieving 14dBm P_{sat} with Synchronized Injection-Locked Power Amplifiers and Five In-Phase Power Combining Doublers in 65nm CMOS

Shunli Ma, Tianxiang Wu, Jincheng Zhang, Junyan Ren; Fudan University, China

Abstract: This paper presents a novel frequency-modulated-continuous wave (FMCW) transmitter with 22 GHz frequency sweeping bandwidth and 14 dBm P_{sat} for FMCW imaging radar. The proposed transmitter consists of a high linearity and ultra-wideband VCO which utilizes an inductor with two second coils coupled with varactor. With a novel zero-phase coupler (ZPC), four injection-locking power amplifiers (ILPA) are synchronized with in-phase outputs. The ILPAs can realize high power efficiency. Moreover, the five-channel doubler with in-phase power combining realize maximum power efficiency. The transmitter can realize multi-rate FMCW sweeping with period from 1 μ s to 20s and the phase noise is -90 dBc/Hz @1MHz. The total power consumption is around 141mW while operating at a 1.2 V single supply. The chip was fabricated in a 65 nm LP CMOS technology.

RTU1C-4 9:00

A True Time Delay-Based SiGe Bi-Directional T/R Chipset for Large-Scale Wideband Timed Array Antennas

Moon-Kyu Cho, Ickhyun Song, John D. Cressler; Georgia Tech, USA

Abstract: This paper presents a true time delay (TTD)-based transmit/receive (T/R) chipset with 508 ps time delay and 31.5 dB amplitude control for large-scale wideband timed array. The proposed T/R chipset consists of a true time delay circuit, a switched T-type attenuator, and digital control circuits. To compensate the frequency dependent insertion loss characteristics of single-pole double-throw switches, artificial transmission line (ATL), passive-based attenuator, and wideband bi-directional active double-pole double-throw (DPDT) switches are included in the design. In addition, low-pass filters (LPFs) with T-type attenuators are applied to the reference signal path to minimize amplitude variations during time delay control. The proposed T/R chipset demonstrates a record delay-range bandwidth product and a flat in-band characteristic of -3.6 dB with ± 3.6 dB variation in both operations (transmit and receive) over 2–20 GHz.

RTU1C-5 9:20

A 57–71GHz Beamforming SiGe Transceiver for 802.11ad-Based Fixed Wireless Access

Erik Öjefors, Mikael Andreasson, Torgil Kjellberg, Håkan Berg, Lars Aspemyr, Richard Nilsson, Klas Brink, Robin Dahlbäck, Dapeng Wu, Kristoffer Sjögren, Mats Carlsson; Sivers IMA, Sweden

Abstract: A beamforming transceiver for 802.11ad-based wireless access applications manufactured in a $f_r/f_{\text{max}} = 250/340$ -GHz SiGe BiCMOS technology is presented. The transceiver is equipped with 16+16 separate RX/TX paths and provides more than 20 dBm combined output power and 6 dB NF in the standard 802.11ad 57–66 GHz band, as well as the 66-to-71-GHz extended fixed-wireless access frequency range. A low phase noise of -101 dBc at 1 MHz offset enables the use of up to 10 Gbit/s 128 QAM full-channel and 256 QAM half-channel single-carrier modulation.

Tuesday 12 June 2018

10:10–11:50

201A

Session RTU2A: mm-Wave LNAs and RF Receiver Front-Ends

Chair: Kamran Entesari, Texas A&M University

Co-Chair: Danilo Manstretta, University of Pavia

RTU2A-1 10:10

A 4.7mW W-Band LNA with 4.2dB NF and 12dB Gain Using Drain to Gate Feedback in 45nm CMOS RFSOI Technology

Li Gao, Qian Ma, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a W-band low-noise amplifier using 45nm CMOS RFSOI. The amplifier topology consists of a two-stage common-source design followed by a one-stage cascode, with drain-to-gate feedback applied to the last stage to further increase the gain. The measured gain is > 10 dB at 80–95 GHz with a peak of 12 dB at 90 GHz. The measured noise figure (NF) is < 4.9 dB at 85–95 GHz with minimum of 4.2 dB at 90 GHz. This is achieved with a total power consumption of 4.7 mW. To our knowledge, this represents record-performance in term of gain, NF and power consumption at W-band for all silicon technologies.

RTU2A-2 10:30

A Compact 75GHz LNA with 20dB Gain and 4dB Noise Figure in 22nm FinFET CMOS Technology

Woorim Shin, Steven Callender, Stefano Pellerano, Christopher Hull; Intel, USA

Abstract: This paper presents E-band (71–76 GHz) LNA design in 22nm CMOS FinFET technology. Stacked topology with DC current re-use for 2-stage cascaded LNA results in power efficient design with high performance. Measurement shows peak gain of 20 dB and minimum noise figure of 4 dB with 10.8 mA current consumption from 1 V supply. Measured 3-dB bandwidth is 10.4 GHz and input P_{idB} is -22.8 dBm. The active layout area of the LNA is 0.155 mm². To the authors' knowledge, these are the state-of-art values in terms of noise figure and DC power consumption among E-band CMOS LNAs reported in the literature.

RTU2A-3 10:50

A 29–37GHz BiCMOS Low-Noise Amplifier with 28.5dB Peak Gain and 3.1–4.1dB NF

Zhe Chen, Hao Gao, Domine Leenaerts, Dusan Milosevic, Peter G.M. Baltus; Technische Universiteit Eindhoven, The Netherlands

Abstract: This paper presents a 28.5 dB high-gain Ka-band low-noise amplifier (LNA) in a 0.25 μm SiGe:C BiCMOS technology. To achieve wide band (fractional bandwidth > 25%) simultaneous noise and power matching with compact size, a 3-winding transformer based dual-tank matching technique is proposed and implemented for the input matching. The LNA provides 28.5 dB peak gain at 32 GHz with a 3-dB gain bandwidth from 29 to 37 GHz. Within this bandwidth, it also

achieves simultaneously low-noise (3.1–4.1 dB) and power matching ($S_{11} < -10$ dB). The measured input IP₃ and P_{1dB} at 32 GHz are -12.5 dBm and -22.0 dBm, respectively, and the total DC power consumption is 80 mW.

RTU2A-4 11:10

Circuit Techniques for Enhanced Channel Selectivity in Passive Mixer-First Receivers

Edward C. Szoka, Alyosha C. Molnar; Cornell University, USA

Abstract: Two techniques are proposed to enhance channel selectivity in passive-mixer first receivers. Positive capacitive feedback and/or a shunting notch provides steeper baseband, and thus RF, impedance roll-off and improved adjacent-channel linearity. The receiver operates at RF frequencies from 2–11GHz and achieves a blocker P1dB compression of +1.8dBm and IIP₃ of +20dBm for a blocker frequency-offset of 70MHz ($BB_{BW}=30$ MHz) at $f_{RF}=5$ GHz. The NF ranges from 9 ± 1 dB to 11 ± 1 dB over the frequency range of $f_{RF}=2-8$ GHz. The chip has been fabricated in a 130nm SiGe BiCMOS technology.

RTU2A-5 11:30

A 750 μ W -88dBm-Sensitivity CMOS Sub-Harmonic Phase-Tracking Receiver

Bingwei Jiang, Howard C. Luong; HKUST, China

Abstract: A low-power phase-tracking receiver (PTRX) is proposed featuring a sub-harmonic mixer with a local oscillator (LO) operating at half of the carrier frequency. A co-design methodology together with current reuse technique is adopted to further improve the power efficiency. Fabricated in a 65nm CMOS process, the PTRX prototype measures noise figure of 7.1dB and sensitivity of -88dBm with 1-Mb/s BLE Gaussian-Frequency-Shift-Keying (GFSK) data while consuming 750 μ W at 0.4/0.6V supply voltages.

Tuesday 12 June 2018

10:10–11:50

201B

**Session RTU2B: Wireless Transceivers and Transmitters for
Connectivity and Cellular**

Chair: Magnus Wiklund, Qualcomm

Co-Chair: Yuan-Hung Chung, MediaTek

RTU2B-1 10:10

**A 28nm CMOS Wireless Connectivity Combo IC with a Reconfigurable 2×2
MIMO WiFi Supporting 80+80MHz 256-QAM, and BT 5.0**

Chia-Hsin Wu¹, Chris Hunter², Jongdae Bae¹, Huijung Kim¹, Jisoo Chang¹, Jacob Sharpe², Inhyo Ryu¹, Seongwon Joo¹, Byeongwan Ha¹, Won Ko¹, Jounghyun Yim¹, Sangwook Han¹, Taewan Kim¹, Daeyoung Yoon¹, Inyoung Choi¹, Sangyun Lee¹, Qing Liu¹, Myounggyun Kim¹, Jiyoung Lee¹, Shinwoong Kim¹, Alexander Thoukydides², Michael Cowell², Thomas Byunghak Cho¹; ¹Samsung, Korea, ²Samsung Cambridge Solution Centre, UK

Abstract: This paper presents a 28nm CMOS wireless connectivity combo IC with a 2×2 reconfigurable WiFi transceiver, and a BT 5.0 slim SOC. The WiFi transceiver can deliver 2G/5G Psat of 26.5/25.5dBm and 2G/5G NF of 3.6/3.8dB respectively, supporting contiguous/non-contiguous 80+80MHz bandwidth with 256-QAM modulation. The integrated slim BT SOC features to support legacy BT spec but also enable BT 5.0 new features, such as 2Mbps low-energy (LE) packet and stable modulation scheme.

RTU2B-2 10:30

**An Asymmetrical Parallel-Combined Cascode CMOS WiFi 5GHz 802.11ac RF
Power Amplifier**

Sergey Anderson, Nadav Snir; DSP Group, Israel

Abstract: A novel Asymmetrical Parallel-Combining (APC) Cascode topology for a CMOS PA is demonstrated in a WiFi 802.11ac transmitter operating in the 5GHz band. It is shown to offer enhancements in both linearity, achieving an error vector magnitude (EVM) below -35dB, as well as in efficiency, achieving power-added efficiency (PAE) of 4.6% at an output power level of 17.6dBm and supply voltage of 5V. The proposed low-complexity design covers the entire 802.11ac band without tunable elements, multigate transistors (MGTR), digital pre-distortion (DPD), load modulation or negative feedback control, thereby providing a very robust and cost-effective solution. The proposed PA was implemented in a 55nm CMOS process on a 0.76 mm×1.26 mm die and assembled in a 16-lead QFN (3mm×3mm) package.

RTU2B-3 10:50**A 0.62nJ/b Multi-Standard WiFi/BLE Wideband Digital Polar TX with Dynamic FM Correction and AM Alias Suppression for IoT Applications**

Ao Ba, Johan van den Heuvel, Paul Mateman, Cui Zhou, Benjamin Busze, Minyoung Song, Yuming He, Ming Ding, Johan Dijkhuis, Evgenii Tiurin, Suryasarman Madampu, Pepijn Boer, Stefano Traferro, Yan Zhang, Yao-Hong Liu, Christian Bachmann, Kathleen Philips; Holst Centre, The Netherlands

Abstract: A WiFi (IEEE 802.11g) and BLE combo transmitter (TX) for IoT applications is presented. A wideband digital polar architecture consisting of an all-digital PLL-based frequency modulator and a switched-capacitor digitally-controlled PA achieves optimal energy efficiency for both WiFi and BLE. The dynamic FM correction and AM alias suppression techniques are applied to support 20MHz 802.11g. Implemented in 28nm CMOS technology with 0.9V supply, this highly reconfigurable TX achieves -22dB EVM for 802.11g up to MCS4 and 1.6% FSK error for BLE. The transmitter only occupies 0.65 mm² and consumes 27mW and 15mW with 0dBm output power for WiFi and BLE, respectively. It results in an excellent energy efficiency of 0.62nJ/b.

RTU2B-4 11:10**A Wideband Transmitter for LTE-A HPUE Using CIM3 Cancellation**

Yangjian Chen¹, Arnaud Werquin¹, Mohammed Hassan¹, Christophe Beghein¹, Bernard Tenbroek¹, Jon Strange¹, Chi-Tsan Chen², Tzung-Han Wu², Yen-Horng Chen², Chinq-Shiun Chiu²; ¹MediaTek, UK, ²MediaTek, Taiwan

Abstract: A wide-band direct conversion transmitter (DCT) based on a compact voltage-mode passive modulator architecture successfully fulfilling the stringent power and linearity requirements of the LTE-A Band 41 high-power user equipment (HPUE) standard is presented. The voltage-mode architecture is low noise and power efficient, but generates a harmonic-rich spectrum at the modulator output, which through inter-modulation in the PA driver, creates counter-inter-modulation (CIM) products at the transmitter output. It is demonstrated that partial cancellation of CIM3 can be achieved by careful analysis and optimization of the multiple CIM3 mechanisms. This transmitter achieves -54dBc CIM3 at 3.3dBm output power, while supporting 60MHz bandwidth LTE-A CCA and covering a wide frequency range of 2.3–3.6GHz. The die area of the HPUE transmitter is 0.33mm² in 40nm CMOS.

RTU2B-5 11:30**A 40nm 4-Downlink and 2-Uplink RF Transceiver Supporting LTE-Advanced Carrier Aggregation**

Tzung-Han Wu¹, Yuan-Yu Fu¹, Sheng-Che Tseng¹, Ying-Tsang Lu¹, Yangjian Chen², Chien-Shan Chiang¹, Zong-You Li¹, Bo-Yu Lin¹, Min-Hua Wu¹, Jui-Chih Kao¹, Tzu-Yu Yeh¹, Li-Shin Lai¹, Chao-Wei Wang¹, Chih-Hao Eric Sun¹, Yen-Horng Chen¹, Chinq-Shiun Chiu¹, Shih-Chieh Yen¹, Guang-Kaai Dehng¹, George Chien³, Bernard Tenbroek²; ¹MediaTek, Taiwan, ²MediaTek, UK, ³MediaTek, Singapore

Abstract: A multi-band multi-mode LTE-Advanced (LTE-A) transceiver is demonstrated in this paper. There are 4 receivers (RX) to support inter-band and intra-band downlink (DL) carrier

aggregation (CA) with 256QAM modulation. The RX noise figure (NF) is better than 2.5 dB for RF frequencies < 2.7 GHz and the NF is 3.5 dB in the 5 GHz band. In addition, there are two transmitters (TX) to support inter-band and intra-band uplink (UL) CA with 64QAM modulation. The TX EVM is 1.59% in the 3.5 GHz band. The system architecture and circuit techniques to overcome the 4RX/2TX CA spurs and interferences are described in this paper. It is shown that there is no unwanted CA spur in the signal bandwidth.

Tuesday 12 June 2018

13:30–15:10

PCC Exhibit Hall

Session RTUIF: Interactive Forum

Chair: Ranjit Gharpurey, University of Texas at Austin

Co-Chair: Mohyee Mikhemar, Broadcom

RTUIF-1

Power Amplifier with Temperature Adaptive Biasing for Improved DEVM

Hamza Najjari¹, Christophe Cordier², Stéphane David², Serge Bardy², Jean-Baptiste Begueret¹; ¹IMS (UMR 5218), France, ²NXP Semiconductors, France

Abstract: This paper describes DEVM challenges and long packet issues during a linear Power Amplifier (PA) design. Based on Hetero-junction Bipolar Transistor (HBT) electrothermal behavior, a programmable temperature compensating bias is designed to improve the PA linearity. This temperature compensation is applied to a fully integrated 5 GHz BiCMOS HBT PA to improve the DEVM over a junction temperature range from 25°C to 180°C. For a long packet data transmission (4 ms), the power gain variation is reduced to only 156 m dB for an 8μs preamble and 27 m dB for a 90μs preamble. With the proposed temperature adaptive bias, the PA can achieve DEVM lower than -47 dB up to 16.5 dBm output power.

RTUIF-2

A 150μW -57.5dBm-Sensitivity Bluetooth Low-Energy Back-Channel Receiver with LO Frequency Hopping

Abdullah Alghaihab, Hun-Seok Kim, David D. Wentzloff; University of Michigan, USA

Abstract: A low power backchannel BLE wake-up receiver is presented. The receiver monitors the BLE advertising channels for a pre-programmed pattern. As in the BLE standard, frequency shift modulation (FSK) is chosen to be the modulation scheme of the signal that will be received. This makes the wake-up algorithm compatible with the standard, and hence, it can be generated by a commercial off-the-shelf device. The proposed receiver uses a dual-mixer to down-convert the RF input to reduce the LO power consumption by operating it at half the RF frequency. The receiver has a -57.5 dBm sensitivity while consuming 150 μW.

RTUIF-3

A 12.46μW Baseband Timing Circuitry for Synchronization and Duty-Cycling of Scalable Wireless Mesh Networks in IoT

Enkhbayasgalan Gantsog¹, Ivan Bukreyev¹, Frank Lane², Alyssa Apse¹; ¹Cornell University, USA, ²MixComm, USA

Abstract: This work presents baseband timing circuitry that enables scalable synchronization and aggressive duty-cycling of peer-to-peer IoT nodes for low-power wireless communication. The circuitry is compatible with commercial RF front ends and is insensitive to the phase and frequency offsets of the received signal due to the differential detector. An analog correlator enables low-latency

detection of a synchronization packet, or syncword. The detected syncword is used to advance the phase of a nonlinear pulse-coupled oscillator, which drives the network to a synchronized state. The circuits consume $12.46 \mu\text{W}$ in 0.01% duty-cycled mode while detecting a 63-bit syncword at 1.25 Mbps with $\text{BER} = 10^{-3}$ at $\text{SNR} = 5 \text{ dB}$. Synchronization of three wireless nodes is demonstrated.

RTUIF-4

An Analog Wide-Bandwidth Baseband Chain for 12Gbps 256QAM Direct-Conversion Receiver

B. Jalali¹, M. Moretto², A. Singh³, S. Shahramian³, Y. Baeyens³; ¹Acacia Communications, USA, ²Nokia, Italy, ³Nokia Bell Labs, USA

Abstract: This paper presents a broadband low-power baseband designed for a zero-IF phased-array receiver. It can support up to 12 Gbps 256QAM and 17Gbps 32QAM signalling. Baseband circuit provides filtering for RF channel bandwidths between 1.4 GHz to 6 GHz in 16 different steps. It incorporates variable-gain-amplifiers with total tuning range of 40 dB. DC offset up to $\pm 2.3\text{mA}$ at mixer output is cancelled. Baseband consumes 100mW per I and Q channel using double supplies of 1.5 V and 2.5 V. Design is fabricated in 0.18 μm SiGe BiCMOS process with f_T/f_{MAX} of 240/270GHz.

RTUIF-5

A Blocker-Tolerant Double Noise-Cancelling Wideband Receiver Front-End Using Linearized Transconductor

Duksoo Kim, Sangwook Nam; Seoul National University, Korea

Abstract: In this paper, a wideband receiver front-end using a linearization technique of transconductor is presented. A low-noise transconductance amplifier is designed to perform both linearization and noise cancellation simultaneously, achieving high input-referred third-order intercept point (IIP3) values and low noise figure. In addition, a wideband input matching and a second noise cancellation technique using a feedback path and an auxiliary path are applied. The designed wideband receiver, fabricated in 65 nm technology, operates in the 0.06–3 GHz frequency band and has a gain of 52.7 dB, a minimum noise figure of 1.4 dB, and a maximum IIP3 of 5.15 dBm.

RTUIF-6

A 10.56-GHz Broadband Transceiver with Integrated T/R Switching via Matching Network Re-Use in 28-nm CMOS Technology

Wei Zhu, Lei Zhang, Yan Wang; Tsinghua University, China

Abstract: In this paper, in which an innovative architecture with ultra-compact transformer-based transmit/receive (T/R) switching via matching network re-use is introduced to certify the input noise matching of low-noise amplifier (LNA) and the output matching of power amplifier (PA) simultaneously. A three-coil transformer is introduced in the PA input-stage to change the optimum load impedance of PA output stage, thereby further increasing the output power of PA without affecting the noise match of LNA, due to the linearity enhancement technology the P_{out} and P_{sat} of PA increased about 3.4 and 3.3-dBm, respectively. The new architecture is implemented in a 28-nm CMOS technology. Test results prove that the insertion loss of the proposed T/R switch introduced at

the RX and TX end is only 1.5-dB, benefit from this, RX obtained 4.3-dB noise figure, TX obtained 9.9 and 14.1-dBm OP_{1dB} and P_{sat} . With the matching network re-using T/R switch the whole transceiver only occupies 2.4×2.4 mm² chip area.

RTUIF-7

A Gradient Descent Bias Optimizer for Oscillator Phase Noise Reduction Demonstrated in 45nm and 32nm SOI CMOS

Mark Ferriss, Bodhisatwa Sadhu, Daniel Friedman; IBM T.J. Watson Research Center, USA

Abstract: This paper presents a technique for minimizing the phase noise of a CMOS PLL's oscillator. An integrated state-machine implements a gradient descent optimization algorithm to find the VCO bias voltage with the minimum frequency sensitivity to the bias voltage. This suppresses noise up-conversion within the oscillator for a key class of noise sources. The scheme is demonstrated in two separate PLLs. In a 45nm SOI CMOS 13.5-to-16.5 GHz PLL the phase noise is reduced from -90 to -103 dBc/Hz at 1MHz offset measured from a 15.5GHz carrier. In a 32nm SOI CMOS 17.5GHz-to-21GHz, the phase noise is reduced from -78.8 to -84.2 at 100kHz offset from an 18.1GHz carrier.

RTUIF-8

Truly Balanced K-Band Push-Push Frequency Doubler

Soenke Vehring, Georg Boeck; Technische Universität Berlin, Germany

Abstract: This paper presents a truly balanced push-push frequency doubler. The novel concept is based on two lumped quadrature couplers that provide a truly balanced signaling for two doubler cells. As a consequence, the output signal is inherently balanced and a lossy output transformer can be avoided. Hence, higher output power and efficiency can be achieved. As a proof of concept, a K-band doubler is implemented in a 65nm CMOS technology. At 0dBm input power, the circuit delivers 5dBm output power with more than 6% PAE. The chip draws 26mA from a 1.2V supply and the total chip area is 0.85×0.55 mm². The fundamental suppression is around 44 dBc. To the best of the authors knowledge, this is the first fully balanced push-push doubler and the achieved results exceed state-of-the-art performance. The concept is applicable to other technologies and frequencies as well.

RTUIF-9

A Crosstalk-Immune Sub-THz All-Surface-Wave I/O Transceiver in 65-nm CMOS

Yuan Liang¹, Chirn Chye Boon¹, Hao Yu²; ¹Nanyang Technological University, Singapore, ²SUSTC, China

Abstract: A surface-wave I/O transceiver is proposed and validated at 140 GHz in 65 nm CMOS. By generating, modulating and propagating surface plasmonic signal, the all-surface-wave I/O is prototyped with crosstalk-immune owing to the sub-wavelength localization of electromagnetic wave at the metal/dielectric interface. A four-way surface-wave signal source is power-combined via coupled oscillator network. A surface-wave modulator is realized by stacking two split-ring-resonator (SRR) unit-cells with opposite placement. It is further integrated into the all-surface-wave I/O with a surface-wave transmission line and matching converter. Measured results show that the proposed

dual-channel I/O delivers a localized 140 GHz surface-wave signal, demonstrating crosstalk-immune on-chip transmission by supporting 13.5 Gb/s data-rate communication with 2.6 pJ/bit power efficiency and a bit-error rate less than 10^{-12} .

RTUIF-10

300GHz OOK Transmitter Integrated in Advanced Silicon Photonics Technology and Achieving 20Gb/s

E. Lacombe¹, C. Belem-Goncalves¹, C. Luxey², F. Giancesello¹, C. Durand¹, D. Gloria¹, G. Ducournau³; ¹STMicroelectronics, France, ²Polytech'Lab (EA 7498), France, ³IEMN (UMR 8520), France

Abstract: In this paper, a 300 GHz 20 Gb/s On-Off Keying (OOK) transmitter is demonstrated in advanced Silicon-Photonics process. An integrated Silicon-Germanium photodiode is optically excited by the beatnote of two tunable lasers in order to up-convert data signals from baseband to 300 GHz. Using a receiver based on direct detection in III-V Schottky diode, measured Bit Error Rates (BER) below the value of 1.10^{-9} were achieved at 20 Gb/s in real time, and a real-time BER below the Forward Error Correction (FEC) was successfully measured at 25 Gb/s.

RTUIF-11

A 2.56Gbps Asynchronous Serial Transceiver with Embedded 80Mbps Secondary Data Transmission Capability in 65nm CMOS

Xiaoran Wang, Tianwei Liu, Shita Guo, Mitchell A. Thornton, Ping Gui; Southern Methodist University, USA

Abstract: A new asynchronous serial transceiver is proposed that is capable of transmitting and receiving a secondary data stream along with the primary data stream on a single asynchronous serial link. The proposed transceiver embeds the secondary data stream by modulating the phase of the primary data in accordance with it. The receiver recovers both the primary and secondary data simultaneously. In a standard receiver, which is not equipped with the phase demodulation capability, the secondary data appears as jitter of the primary data. The jitter caused by the secondary data still falls within the jitter budget of the transceiver, and having this much jitter would not adversely affect the functionality of the primary data recovery. The proposed system can be widely used in many data communication applications such as for transmitting a hidden signature for data authentication, or as control and/or additional data in an existing serial link. A prototype transceiver, implemented in a 65 nm CMOS process, demonstrates the proposed concept with 2.56 Gbps primary data and 80 Mbps secondary data channels.

RFIC 2018 Lunchtime Panel Session

Monday, 11 June 2018

11:45–13:15

PCC, Room 201A

How Will the Future Self-Driving Cars See? LiDAR vs. Radar

Panel Organizers and Moderators:

Hossein Hashemi, *University of Southern California, USA*

Amin Arbabian, *Stanford University, USA*

Panelists: **Juergen Hasch**, *Senior Expert, Corporate Sector Research and Advance Engineering, Robert Bosch, Germany*

Manju Hegde, *CEO & Co-Founder, Ubndr, USA*

Ron Kapusta, *System Architect, Autonomous Transportation and Safety, Analog Devices, USA*

Lute Maleki, *Senior Distinguished Engineer, GM Cruise, USA*

Karam Noujeim, *Head of Radar and Sensor Fusion, Intelligent Driving Group, Baidu, USA*

Abstract: In 2004, the Defense Advanced Research Projects Agency (DARPA) held its first Grand Challenge with \$1 million for grabs for any self-driving car that could travel a 150-mile route from California to Nevada. No self-driving car managed to finish the course. Fortunately, several teams succeeded in the subsequent 2005 second Grand Challenge, and a 2007 Urban Challenge. Since that event, almost all the traditional car companies as well as several startups in the field (nuTonomy, UBER, Zoox, and Waymo) have been working on deploying self-driving cars, with different levels of autonomy, in the market. Recent analysis, estimates that the self-driving car market will be several trillion dollars by 2050, with the potential to revolutionize transportation.

A self-driving car needs advanced sensors (eyes) as well as a powerful computing unit (brain). Various sensor technologies have been suggested to provide “sight” for self-driving cars. The top candidates (in no particular order) are cameras, LiDAR, and radar, and their combinations. The performance, cost, and reliability of vision systems have improved considerably thanks to the ubiquitous usage of image sensors in consumer products, as well as the advanced vision algorithms being deployed. On the other hand, radar and LiDAR have not enjoyed as much reduction in cost, area, and power consumption due to their limited commercial usage. As such, the past few years has witnessed a plethora of startup companies, as well as some established companies, working on development of low-cost, high-performance, and reliable radars, LiDARs, and associated signal processing algorithms (brain) for the emerging self-driving car market.

This expert panel covers the state of the art in radar and LiDAR technologies, and attempts to draw contrasts between the two approaches in the context of self-driving cars. Among other things, the panelists will argue whether radar can deliver the necessary performance to eliminate the need for LiDAR, and whether LiDAR can become cheap and compact enough to remove the need for radar in self-driving cars. Radar and LiDAR enabling self-driving cars may very well be the next multi-billion dollar business opportunity for the RF and microwave communities.

IMS/RFIC 2018 Lunchtime Panel Session

Tuesday, 12 June 2018

12:00–13:00

PCC, Room 201A

Can a Residential Wireless Gbps Internet Connection Compete with Wired Alternatives?

Panel Organizers and Moderators:

Amin Arbabian, *Stanford University, USA*

Oren Eliezer, *PHAZR, USA*

Rod Waterhouse, *Pharad, USA*

Dalma Novak, *Pharad, USA*

Panelists: **John Cioffi**, *CEO, ASSIA, USA & Professor Emeritus, Stanford University, USA*

Oleh Krutko, *Director of Engineering, Head of Millimeter Wave, Broadband, and Power Product Development, Qorvo, USA*

Mike Geen, *Head of Engineering, Filtronic Broadband, UK*

Pat Iannone, *Member of Technical Staff, Nokia Bell Labs, USA*

Wilhelmus Theunissen, *Facebook Connectivity Labs, USA*

Abstract: The demand for Internet bandwidth continues to grow rapidly; Nielsen's Law of Internet Bandwidth states that a user's connection speed grows by 50% per year. While we all may want a faster Internet connection, most people are unwilling to pay more to get higher data rates. Gigabit-per-second (Gbps) residential internet connections have typically been supported by well-established high-speed wired networks. However, there are a number of emerging technologies that offer the potential to compete directly with these approaches. Our expert panelists will discuss some of the technology advancements that are enabling Gbps internet connections and will debate the merits of both the wired and wireless technology alternatives, including 5G and satellite-based solutions.

WORKSHOPS AND SHORT COURSES

All Workshops and Short Courses are located at the Pennsylvania Convention Center. Specific room assignments will be provided onsite.

SUNDAY WORKSHOPS – 10 JUNE 2018

WSA (Half Day): Sunday 08:00–11:50 RFIC Design in CMOS FinFET and FD-SOI

Sponsor: **RFIC**

Organizers: **Magnus Wiklund**, *Qualcomm*
Tzung-Yin Lee, *Skyworks Solutions*

Abstract: Both CMOS FinFET and FD-SOI are the enabling technologies to achieve nanoscale CMOS beyond 20nm. This technological revolution allows highest integration density for high volume products at low cost. Due to the fundamental changes in how a transistor is built, there are tremendous impacts on its characteristics (e.g., f_t , V_{th} , VDD). Considering this change, traditional and well-known circuits and architectures need to be refined or even be re-invented. This workshop gives an overview of novel architectures and designs in the context of RF and millimeter-wave that benefit from FinFET and FD-SOI technologies. In several presentations, trends, design challenges, and how to overcome these challenges are shown by application/circuit examples. Furthermore, commoditization of 4G and emerging 5G cellular systems have continued to push applications of advanced Si/SiGe and SOI technology for integration, performance, and cost. This workshop will discuss the challenges and trade-offs of various Si-based technologies for 5G cellular applications, their respective modeling, automated design and layout perspectives for successful productization.

Speakers:

1. “The Paradigm Shift of RF and Millimeter-Wave Circuit Design with FinFET Technology: How to Keep up with the Next Generation of CMOS Process Technology for Circuit Optimization and Planning”, **Hyung-Jin Lee**, *Intel*
2. “Integration of a Wideband Direct-RF Radio in 16nm FinFET”, **Brendan Farley**, *Xilinx*
3. “Compiling Analog-to-Digital Converters in FDSOI”, **Trond Ytterdal**, *Norwegian Institute of Technology*
4. “Millimeter-Wave Circuit Design and Techniques in FDSOI CMOS Technology”, **Abdellatif Bellaouar**, *GLOBALFOUNDRIES*

WSB (Half Day): Sunday 08:00–11:50

ICs for Quantum Computing and Quantum Technologies

Sponsors: **RFIC, IMS**

Organizers: **Edoardo Charbon**, *EPFL, Technische Universiteit Delft, and Intel*
Ranjit Gharpurey, *University of Texas at Austin*

Abstract: Quantum computers (QCs) hold the promise to change computing as we know it today. What is generally not discussed is the importance of classical electronics to support a QC's computational core: the qubit. In this workshop, we look at the requirements of electronic circuits and systems supporting qubits, with a special interest in scalability issues and silicon (CMOS, SiGe, ...) compatibility of quantum-classical computing systems. World experts in the field will present their work and their visions for a possibly integrated QC of the future, often reflecting on architectural and design issues, with a keen interest in the design of high-speed and RF circuits and systems sought by QC architects. Finally, we will look at other applications that could benefit from qubits and, in general, quantum technologies, from the perspective of classical readout and control CMOS circuits and systems operating at cryogenic temperatures (Cryo-CMOS). We will conclude with a general vision of the field and its trends as well as perspectives for the future.

Speakers:

1. “Should RFIC Designers Care About Quantum Computing?”, **Stefano Pellerano**, *Intel*
2. “Fabrication and Integration of Superconducting Qubits and Circuits”, **William D. Oliver**, *MIT Lincoln Laboratory, and MIT*
3. “Superconducting Classical Circuits for Quantum Computing Readout and Control”, **Oleg Mukhanov**, *HYPRES*
4. “Silicon Germanium Cryogenic Low Noise Amplifiers for Quantum Computing”, **Joseph C. Bardin**, *University of Massachusetts Amherst*
5. “Cryo-CMOS Circuits and Systems for Scalable Quantum Computing”, **Masoud Babaie**¹, **Fabio Sebastiano**¹, **Andrei Vladimirescu**^{1,2,3}, **Edoardo Charbon**^{4,1,5}, ¹*Technische Universiteit Delft*, ²*ISEP*, ³*University of California, Berkeley*, ⁴*EPFL*, ⁵*Intel*

WSC (Full Day): Sunday 08:00–17:15

5G mm-Wave Power Amplifiers, Transmitters, Beamforming Techniques and Massive MIMO

Sponsor: **RFIC**

Organizers: **Patrick Reynaert**, *Katholieke Universiteit Leuven*
Leon van den Oever, *Qualcomm*
Ping Gui, *Southern Methodist University*

Abstract: The fifth Generation (5G) communication systems are expected to represent a major revolution in mobile wireless technologies. The focus of this workshop is on 5G systems that will

operate at mm-wave frequencies (28–80GHz) and may employ massive MIMO, in order to achieve enhanced data rates, higher spectral efficiency, extended battery life, and low system latency. Aspects that will be addressed are: system architecture, power-amplifier (PA) design, circuit techniques, technology choices, front-end and antenna interfaces, and user equipment/basestation. Moreover, this workshop brings together the advocates and experts of both bulk CMOS, SOI CMOS and SiGe, as well as GaN and other technologies, to explain in which cases certain technology may be the right choice.

Speakers:

1. “Millimeter-Wave Beamforming: System Level Challenges and Implications for RF Design”, **Vasanthan Raghavan**, *Qualcomm*
2. “Design Considerations for 5G mm-Wave Transceivers”, **Stefan Andersson**, *Ericsson*
3. “Power Amplifier Requirements for mm-Wave 5G Systems”, **Bror Peterson**, *Qorvo*
4. “Broadband, Linear, and High-Efficiency mm-Wave Power Amplifiers and Co-Designs with Antennas”, **Hua Wang**, *Georgia Tech*
5. “Reconfigurable Wideband Architectures and Antenna Co-Design and Co-Integration for Future MIMO Arrays”, **Kaushik Sengupta**, *Princeton University*
6. “Hybrid Beamforming Receivers for Millimeter-Wave MIMO Communication”, **Jeyanandh Paramesh**, *Carnegie Mellon University*
7. “5G Infrastructure Radio Design, Measurement and Standards Aspects”, **Raja Mir**, *Nokia*
8. “Enabling Cost-Effective 5G Phased Array mm-Wave Products by Optimizing the Flow from Design-for-Test to Production”, **Mustapha Slamani**, *GLOBALFOUNDRIES*

WSD (Full Day): Sunday 08:00–17:15
eXtreme-Bandwidth:
Architectures for RF and mmW Transceivers in Nanoscale CMOS

Sponsor: **RFIC**

Organizers: **Francois Rivet**, *University of Bordeaux*
Gernot Hueber, *NXP Semiconductors*

Abstract: With the advent of nano-scale CMOS technology, exciting new developments have recently taken place in the field of RF and mm-wave transmitters, receivers and frequency synthesizers. The low-voltage, fast speed, fine feature-size and low cost of the new technology have forever changed the way we design circuits, architectures and systems. Not only have RF/mm-wave circuits taken different topologies from what has been taught in textbooks but also their integration with digital processors has enabled new possibilities for digital assistance. The motivation of this workshop is to capture what is the state at the edge of technology, what is the demand of the industry in the context of high volume products, and what are circuit and architectural concepts that are demanded or enforced by the technology. We focus especially on circuit enabling extreme bandwidth using various techniques including MIMO, analog/digital signal processing, novel high-rate ADCs, techniques for channel bonding, carrier aggregation to reach data rates far beyond what is achievable nowadays.

Speakers:

1. “Millimeter-Wave CMOS Transceiver Toward 1 Tbps Wireless Communication”, **Kenichi Okada**, *Tokyo Institute of Technology*
2. “Wideband Transceiver Design for 5G mm-Wave Phased-Arrays in FinFET Technology”, **Steven Callender**, *Intel*
3. “300-GHz CMOS Wireless Transceiver and its Future”, **Minoru Fujishima**, *Hiroshima University*
4. “Multi-GHz Frequency Synthesis for Radar Applications”, **Bodhisatwa Sadhu**, *IBM T.J. Watson Research Center*
5. “Linear mm-Wave Power Amplifiers and Transceivers for 5G NR mm-Wave”, **Jeremy Dunworth**, *Qualcomm*
6. “Hybrid Architectures Leveraging Best of Both Worlds for Extreme-Bandwidth Communications”, **Payam Heydari**, *University of California, Irvine*
7. “Wideband mm-Wave Communication Systems: A Systematic Design Approach”, **Hasan Al-Rubaye, Gabriel M. Rebeiz**, *University of California, San Diego*

WSE (Full Day): Sunday 08:00–17:15
Integrated mm-Wave & THz Sensing Technology for
Automotive, Industrial and Healthcare

Sponsors: **RFIC, IMS**

Organizers: **Hongtao Xu**, *Fudan University*
Vito Giannini, *Ubnder*

Abstract: Recent advances in millimeter-wave and THz silicon technology have drawn strong interest in the RF community. mm-Wave sensors and THz imagers are becoming essential building blocks in several application domains. For example, in the automotive industry, mm-wave radars are considered as a key component for safety critical applications and autonomous driving cars. In the industrial world, drones and robotics will rely on such sensors to avoid obstacles or complete complex tasks. In the medical and pharmaceutical industry, THz prototypes find application in home patient monitoring, high-resolution imaging and spectroscopy. This workshop aims at covering the state of the art and the future development trends including FMCW and MIMO radars, as well as THz imagers. This includes silicon and systems operating at carriers beyond 30 GHz. Distinguished speakers from industry and academia will highlight system requirements, technology advances, challenges and solutions for implementations on system and silicon level.

Speakers:

1. “Autonomous Vehicles Systems and the Future of Riding”, **Sergio Pacheco**, *NXP Semiconductors*
2. “MIMO Radars and Beamforming with Multichip Cascading”, **Sreekiran Samara**, *Texas Instruments*
3. “MIMO Radar System Integration”, **Chris Pan**, *Ubnder*

4. “New SiGe Technologies with Cut Off Frequencies Towards 600 GHz and Their Potential Impact on Future mm-Wave Sensing in Automotive and Industrial Applications”, **Wolfgang Liebl**, *Infineon Technologies*
5. “mm-Wave for cm Accurate Ranging: Signals, Building Blocks and a Little Bit of Algorithms”, **Wim Dehaene**, *Katholieke Universiteit Leuven*
6. “Millimeter-Waves for Cars, People, Cells, and Molecules”, **Ilja Ocket**, *imec, and Katholieke Universiteit Leuven*
7. “Hyperimager: A Compact Multi-Spectral Imaging Platform”, **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*
8. “Large-Scale THz Active Arrays in Silicon for Bio-Chemical Sensing”, **Ruonan Han**, *MIT*
9. “Silicon Based Multispectral Terahertz Imaging”, **Richard Al Hadi**, *University of California, Los Angeles*
10. “An Integrated-Circuit Approach to Terahertz Nearfield Imaging”, **Ullrich Pfeiffer**, *Universität Wuppertal*

WSF (Full Day): Sunday 08:00–17:15
Advanced Integrated RF Filtering Circuits and Techniques

Sponsor: **RFIC**

Organizers: **Harish Krishnaswamy**, *Columbia University*
Mohyee Mikhemar, *Broadcom*

Abstract: The complexity of the conventional RF front-end SAW/BAW filtering and switching is the biggest hurdle in the pursuit of a true wideband software-defined radio for high performance wireless applications. It is also a challenge for many IoT systems with application-specific size or cost restrictions. Therefore, there have been serious efforts from the RFIC community to come up with RF filtering techniques that are suitable for CMOS integration. After more than a decade of promising research results, some of these techniques are starting to be used in mass market products. In this workshop, experts from academic, industry, and federal research institutions will present the state-of-the-art in the area of CMOS-integrated RF filtering such as N-path filters, electrical balance duplexers, and various linear periodic time varying (LPTV) systems that have been used, for example, to implement a fully-integrated non-magnetic CMOS circulator. Moreover, the commercial state-of-the-art performance of SAW/BAW technology and tunable RF components will be presented as a point of reference. Finally, the workshop will conclude with an interactive panel discussion about the potential and limitations of CMOS integrated RF filtering.

Speakers:

1. “Workshop Introduction: Integrated Antenna-Interface Components: A Blessing in Disguise for Wireless Transceivers”, **Harish Krishnaswamy**, *Columbia University*
2. “Pushing the Interference Robustness of CMOS N-Path Filters”, **Eric Klumperink**, *University of Twente*

3. “Demystifying the Analysis of LPTV Circuits Using Adjoint Networks”, **Shanthi Pavan**, *Indian Institute of Technology Madras*
4. “Solutions for Reconfigurable Mobile Device RF Front-Ends”, **Arthur Morris**, *WisSpry*
5. “Electrical-Balance Techniques for Tunable, Fully Integrated RF Front-Ends”, **Barend van Liempd**, *imec*
6. “Integrated Self-Interference Cancellation for Next-Generation Wireless Communication Systems”, **Jin Zhou**, *University of Illinois at Urbana-Champaign*
7. “Rethinking the RF Front-End: Integrated Magnetic-Free Non-Reciprocity and its Application in Emerging Wireless Communication Paradigms”, **Negar Reiskarimian**, *Columbia University*
8. “Using Sampling Aliases for Sharp Programmable Filtering: Some Radio Applications”, **Sudhakar Pamarti**, *University of California, Los Angeles*

WSG (Full Day): Sunday 08:00–17:15
Synthesizer Design and Frequency Generation/Synchronization
Schemes for High-Performance Wireless Systems

Sponsors: **RFIC, IMS**

Organizers: **Jaber Khoja**, *Rockwell Collins*
Ed Balboni, *Analog Devices*

Abstract: This workshop will focus on wireless systems demanding high performance local oscillators and clock generators. This includes cellular infrastructure, wireless backhauling, mm-wave radar and imaging, and data converters for communication systems. In all these applications, it would be desirable to implement the whole system in the same silicon technology process, while achieving low integrated phase noise ($<1\text{deg}$) and noise floor at mm-wave, low reference and integer boundary spurs ($<90\text{dBc}$). State-of-the-art RF to THz synthesizer architectures and building block details will be covered, including phase-locked loops, frequency doubler/tripler, injection locked divider, clock distribution, etc. Advanced PLL architectures such as inductor-less PLLs, SSPLL, ILPLL will also be discussed. In addition, this workshop will discuss the fundamentals of digital PLLs as well as the latest advancements in the field. Digital PLLs have great scalability and easy portability to new CMOS process nodes, and have today a wide range of applications from wireless to wireline systems, not limited to the GHz frequency range but spanning up to the millimeter-wave range. The workshop will introduce the main concepts to analyze and design digital PLLs, taking into account system design constraints, quantization noise and design of the mixed-blocks such as the DCO and the TDC. State-of-the-art techniques will be discussed, such as new architectures, TDCs and DCOs with high figure-of-merit, and digital-to-time converters.

Speakers:

1. “Methods of Distributed Synchronization in Future Wireless Networks”, **Jaber Khoja, Roger Dana**, *Rockwell Collins*
2. “Survey of Recent Advances in Microwave Frequency Synthesizers for Next Generation Radar, Cellular and Satellite Systems”, **Ed Balboni**, *Analog Devices*

3. “Improved Frequency Stability in Low Power Consuming Oscillators and Clocks: CSAC, MEMS and Dual-Mode Crystal Oscillators”, **Vladimir Stofanik**, *Slovak University of Technology in Bratislava*
4. “Low Noise Sapphire Resonator and Oscillators”, **Michael Tobar**, *University of Western Australia*
5. “VIDA Products Developed Miniaturized YIG Oscillators Enabled by Differential YIG Resonators”, **Ronald Parrott¹**, **Allen Sweet¹**, **Charles Fields²**, ¹*VIDA Products*, ²*Consultant*
6. “Millimeter-Wave Injection-Locked CMOS Frequency Synthesizers”, **Howard Luong**, *Hong Kong University of Science and Technology*
7. “Prediction and Mitigation of Spurs and Phase Noise in Fractional Synthesizers”, **Gord Allan**, *Analog Devices*
8. “CMOS/SiGe Millimeter-Wave Frequency Generation”, **Mona Hella**, *Rensselaer Polytechnic Institute*
9. “Injection Locking Techniques for Low-power Millimeter-Wave Phased Array Circuitry”, **James Buckwalter**, *University of California, Santa Barbara*

WSH (Full Day): Sunday 08:00–17:15

High-Performance WLAN Transceiver Design and Calibration Techniques

Sponsor: **RFIC**

Organizers: **Jean-Baptiste Begueret**, *University of Bordeaux*
Yuan-Hung Chung, *MediaTek*

Abstract: Ubiquitous wireless connectivity keeps driving the development of high-performance/low-power wireless systems and building blocks for next generation transceivers. Today, the best and fastest performances are provided by the 802.11ac standard, delivering speeds up to several Gbps. To achieve these data rate levels, the 11ac works exclusively in the 5 GHz band in which wide bandwidths (80/160 MHz) are available. Nevertheless, to improve the speed, the next generation 802.11ax answers this issue precisely: this technology will allow to quadruple the average data rate per user in a dense environment. The 11ax standard uses both 2.4 and 5GHz bands, wide channels (40 MHz, 80 MHz and, 160 MHz) and high order modulations (1024 QAM). The key technologies will be presented on how to achieve wider bandwidth, higher linearity, lower power consumption, better EVM, and high integration, such as fulfilling the requirements of 802.11ax standard. Moreover, the workshop will present/discuss digital and mixed-signal techniques for correcting RF and analog imperfections of a WLAN transceiver circuits.

Speakers:

1. “Discrete-Time Approach to Push High-Performance in WLAN Receivers”, **R. Bogdan Staszewski**, **Iman Madadi**, **Massoud Tohidian**, *University College Dublin*

2. “A 2.4-GHz High-Efficiency Multilevel Outphasing WLAN Transmitter and an Integration RF Subsampling Receiver for Adaptive PA Linearization”, **SungWon Chung¹, Philip A. Godoy², Taylor W. Barton³, Joel L. Dawson⁴**, ¹*University of Southern California*, ²*Marvell Semiconductor*, ³*University of Colorado Boulder*, ⁴*Eta Devices*
3. “WLAN Digital Power Amplifiers, Circuit & Calibration Techniques”, **Renaldi Winoto**, *Tectus*
4. “Challenges in WLAN Front End Modules Designs Supporting the Proposed 802.11ax Standard”, **Darcy Poulink, Bill Vaillancourt**, *Skyworks Solutions*
5. “WiFi Access Point Front End Module Trends and Challenges”, **Brad Nelson, Bob Baeten**, *Qorvo*
6. “High-Performance CMOS Frequency Synthesizer for WLAN Applications”, **Kenichi Okada**, *Tokyo Institute of Technology*
7. “High Performance Frequency Synthesis with Digital Calibration Techniques”, **Fa Foster Dai**, *Auburn University*
8. “Analog-to-Digital Converter Architecture for Low-Power and High-Speed Operation in Emerging Wireless Systems”, **Mike Shuo-Wei Chen, Jae-Won Nam**, *University of Southern California*

WSI (FULL Day): Sunday 08:00–17:15
High Efficiency Power Amplification for Emerging Wireless Communications Solutions from Devices to Circuits and Systems

Sponsors: **RFIC, IMS**

Organizers: **Jeffrey Walling**, *University of Utah*
Ayman Fayed, *The Ohio State University*
Debopriyo Chowdhury, *Broadcom*

Abstract: The “wireless revolution” is forcing the wireless industry to bring down consumer cost for wireless devices, while simultaneously increasing speed and performance. Consequently, RF transceivers are being implemented in CMOS digital integrated circuit (IC) processes. But, this poses design challenges for achieving watt-level RF power transmission that meets the spectral purity requirements of future wideband wireless communications. This workshop discusses the state-of-the-art architectures and trends for achieving RF power across the fields of devices, circuits and systems. We will explore options for power amplifiers (PAs) from the device level with presentations on GaN devices, to the power amplifier level, with presentations on CMOS and GaN PAs for emerging wireless communications solutions frequencies, and to the system level, with presentations on employing envelope tracking and on approaches for system level linearization.

Speakers:

1. “An Introduction to High-Frequency GaN-Based High Electron Mobility Transistors”, **Siddharth Rajan**, *The Ohio State University*
2. “Efficiency-Enhancement of GaN PAs for 5G Transmitters”, **Zoya Popovic**, *University of Colorado Boulder*

3. “CMOS PA Design at mm-Wave Frequencies”, **Patrick Reynaert**, *Katholieke Universiteit Leuven*
4. “Envelope Tracking for 5G Transmitters”, **Donald Kimball**, *MaXentric Technologies*
5. “A Wideband Envelope Tracking Solution for WLAN Systems”, **Debopriyo Chowdhury**, *Broadcom*
6. “Linearity, Bandwidth, and Back-Off Efficiency Enhancement Design Techniques for GHz Digitally Intensive CMOS Power Amplifiers”, **Jongseok Park**, *Georgia Tech*

WSJ (Full Day): Sunday 08:00–17:15
Millimeter-Wave Systems;
Manufacturing, Packaging and Built-In Self Test

Sponsors: **RFIC, ARFTG**

Organizers: **Didier Belot**, *CEA-LETI*
Mona Hella, *Rensselaer Polytechnic Institute*
Pierre Busson, *STMicroelectronics*

Abstract: This workshop discusses advanced manufacturing, packaging, and testing techniques for mm-wave systems. Topics include plastic waveguides, on-chip antenna arrays, wafer scale integration, as well as calibration and testing issues. New approaches for in-situ measurement of individual element’s response in large phased array systems are also presented. The workshop aims at bringing together experts from academia, industry and research labs to discuss the implementation and testing challenges and solutions for next generation wireless applications.

Speakers:

1. “Packaging Approaches for mm-Wave Applications”, **Tanja Braun**, *Fraunhofer IZM*
2. “Antenna Arrays in the mm-Wave Band”, **Kubilay Sertel**, *The Ohio State University*
3. “Code-Modulated Embedded Test for mm-Wave Phased Array”, **Brian Floyd**, *North Carolina State University*
4. “Built-In-Self-Test Methods for Phased-Array Beamforming ICs”, **Gabriel M. Rebeiz**, *University of California, San Diego*
5. “Millimeter-Wave Testing: the Struggle Between Feasibility and Mass Production Support”, **Mustapha Slamani**, *GLOBALFOUNDRIES*
6. “Plastic is Fantastic: How a Cheap Material Could Become the Next High Data Rate Communication Channel”, **Baudouin Martineau**, *CEA-LETI*
7. “Packaging Solution for Low Cost Si Based 100 Gb/s Wireless Links”, **Frederic Giancesello**, *STMicroelectronics*
8. “Polymer Microwave Fibers: A High-Speed, Robust and Low-Cost Alternative to Copper and Optical Wireline Communication”, **Patrick Reynaert**, *Katholieke Universiteit Leuven*

WSK (Half Day): Sunday 13:30–17:15

Towards Direct Digital RF Transceivers

Sponsors: **RFIC, IMS**

Organizers: **Eric Klumperink**, *University of Twente*
Waleed Khalil, *The Ohio State University*

Abstract: With significant advances in digital CMOS devices and their ft values reaching 300GHz, the direct digital-to-RF interface as well as early digitization becomes an increasingly more viable solution. RF systems hence widely use data-converters closer to the RF-port, as Moore's law makes digital signal processing in CMOS ever more powerful and cost effective. Direct digitization/analogization is still feasible only for certain applications, as dynamic range and speed requirements of the ADC and DAC often lead to a feasibility or power bottleneck. This workshop will review the state-of-the-art and trends in highly digital RF systems, highlighting key design challenges in different application domains as well as architectural solutions to address them. Techniques like channelization and time/frequency interleaving that can relax ADC and DAC requirements will be discussed as well as application examples. Finally, the workshop will review photonics-based data converters as they offer a compelling solution to the performance bounds set by sampling clock jitter.

Speakers:

1. "Theoretical Comparison of Direct-Sampling vs. Heterodyne RF Receivers", **Ramon Gomez**, *University of California, Irvine*
2. "Architectures for Frequency-Domain Channelization of Broadband Signals", **Ranjit Gharpurey**, *University of Texas at Austin*
3. "RF-Sampling DACs and ADCs Integrated in 16nm FinFet SoCs", **Bruno Vaz, Christophe Erdmann**, *Xilinx*
4. "Photonic Analog to Digital Converters for Direct Digital Receivers", **Ronald Esman, Oliver King, Thomas Cullen, Daniel Esman, Altin Pelteku**, *Rockwell Collins*

WSL (Half Day): Sunday 13:30–17:15

Ultra Low-Power Transceiver SoC Designs for IoT Applications

Sponsors: **RFIC, IMS**

Organizers: **Yanjie Wang**, *Intel*
Yao-Hong Liu, *imec*

Abstract: Internet-of-Things (IoT) is regarded as one important part of the future 5G mobile communication, and draws much attention from both academia and industry in recent years. Due to the expansion of IoT and especially wearable sensors, remote personal monitoring based on the huge amount of real-time data streams has become a clear trend in the healthcare and wellbeing domains. IoT edge nodes continue to integrate increasingly complex sensing, compute, and connectivity capabilities into smaller form factors, while pursuing energy autonomy through multi-

modal energy harvesting. This workshop explores the IoT designers' perspective on RFIC front-end, system designs/innovations, antenna/antenna-array designs, integrated sensors, packaging designs, as well as leading edge solutions for their energy harvesting, power management, etc.

Speakers:

1. "Ultra Low Power Crystal Free Radios", **Ali Niknejad, Osama Khan**, *University of California, Berkeley*
 2. "Ultra-Narrow Band Communications", **David Lachartre**, *CEA-LETI*
 3. "An Ultra-Low Power Dual-Core ARM®-Based Wireless MCU in 40 nm RF-NV CMOS for Battery Supplied IoT Applications", **Jean-Robert Tournet**, *NXP Semiconductors*
 4. "A Bidirectional Terahertz Pico-Radio in CMOS for Wireless Sensor Networks and Internet-of-Things", **Taiyun Chi**, *Speed Links*
 5. "Energy-Efficient Proprietary Transceivers for IoT and Smartphone-Based WPAN", **Woogeun Rhee**, *Tsinghua University*
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MONDAY WORKSHOPS – 12 JUNE 2018

WMA (Full Day): Monday 08:00–17:15

Wireless Technologies for Implantable and Wearable Systems

Sponsor: **IMS**

WMB (Full Day): Monday 08:00–17:15

Microwave to THz Imaging Technologies for Biomedical Applications

Sponsor: **IMS**

WMC (Full Day): Monday 08:00–17:15

3D-/4D-/Inkjet-Printed RF Components and Modules for IoT, 5G and Smart Skin Applications

Sponsor: **IMS**

WMD (Full Day): Monday 08:00–17:15

Power Amplifier Technologies for 5G Communications Systems

Sponsor: **IMS**

WME (Full Day): Monday 08:00–17:15

Digital Pre-Distortion and Post-Correction from DC to mm-Wave for Wireline and Optical Communications

Sponsor: **IMS, RFIC**

Organizers: **Hermann Boss**, *Robde & Schwarz*
Noriaki Kaneda, *Nokia Bell Labs*
SungWon Chung, *University of Southern California*

Abstract: This workshop overviews the recent advancements in digital pre-distortion (DPD) and digital post-correction (DPC) techniques over a broad range of spectrum from DC to mm-wave. Beyond the classical DPD applications on wireless and satellite power amplifier linearization, this workshop will culminate the applications of the DPD and DPC techniques for wireline and optical communications. For wireline communication, to advance the data rate limit, designers are leveraging a high-order modulation, which requires a digital-to-analog converter (DAC) based transmitter along with an analog-to-digital converter (ADC) based receiver. Since the poor linearity of high-speed data converters often becomes a performance bottleneck for such high performance wireline transceivers and also for wireline MIMO transceivers, DPC and DPD techniques become essential not only to the equalization of nonideal lossy channels but also to the linearization of nonlinearities in high-speed circuit elements. As the recent trend of using a high-order wideband modulation continues with Tb/s coherent optical communication, fiber nonlinearity has become a critical design challenge. A robust and low-power implementation of DPC and DPD, which includes the realization of nonlinearity tolerant modulation and coding schemes as well as adaptive pre-emphasis and equalization, is becoming increasingly important. This workshop for the first time brings together researchers from industry and academia working on diverse DPD and DPC techniques in wireless, wireline, and optical communications in one place, revisiting the fundamental principles in common as well as providing a unique opportunity to learn from cross-platform implementations.

Speakers:

1. “Linearization of Power Amplifiers Used in Radio Frequency Transmitters”, **Neil Braithwaite**, *Consultant*
2. “Model Order Reduction Techniques for Digital Predistortion in Highly Efficient Power Amplification Architectures”, **Pere Gilabert**, **Gabriel Montoro Lopez**, **Thi Pham**, *Universitat Politècnica de Catalunya*
3. “A Digital PLL Architecture with Digital-Signal-Processing Techniques for Spur Mitigation”, **Cheng-Ru Ho**, **Mike Chen**, *University of Southern California*
4. “ADC-Based Receiver Calibration and Equalization Techniques”, **Samuel Palermo**, *Texas A&M University*
5. “ADC Nonlinearity in Wireline Receivers”, **Anthony Carusone**, *University of Toronto*
6. “Digital Post-Correction of Nonlinearity with Memory Effects in GaN HEMT Track-and-Hold Circuits for High Performance ADCs”, **SungWon Chung**¹, **Puneet Srivastava**², **Xi Yang**³, **Tomás Palacios**³, **Hae-Seung Lee**³, ¹*University of Southern California*, ²*Analog Devices*, ³*MIT*

7. “A Feed Forward Equalization Transmitter Architecture Which is Robust to Coefficient Errors for High-Speed Wireline Communication”, **Byungsub Kim, Seungho Han, Sooeun Lee, Minsoo Choi, Jae-Yoon Sim, Hong-June Park**, *POSTECH*
8. “Digital Predistortion and Post Equalization Techniques in Optical Communications”, **Noriaki Kaneda**, *Nokia Bell Labs*
9. “Digital-Preprocessed Analog-Multiplexed DAC for Ultra-High-Speed Optical Transmission”, **Hirosh Yamazaki, Munehiko Nagatani, Fukutaro Hamaoka, Masanori Nakamura, Hideyuki Nosaka, Toshikazu Hashimoto, Yutaka Miyamoto, Shigeru Kanazawa**, *NTT*
10. “Digital Equalization in Ultra-High Capacity Coherent Optical Transmission”, **David Millar**, *MERL*

WMF (Full Day): Monday 08:00–17:15

Microwave Cells:

From Biological Effects to Innovative Techniques for Cell Analysis

Sponsor: **IMS**

WMG (Full Day): Monday 08:00–17:15

**Recent Advances in Efficiency and Linearity Enhancement Techniques
for RF Power Amplification**

Sponsor: **IMS**

WMH (Half Day): Monday 08:00–11:50

**Microwave and Millimeter-Wave Radiometers: Component
Technologies, System Architectures, and Emerging Applications**

Sponsors: **IMS, RFIC**

Organizers: **Hasan Sharifi, HRL Labs**
 Robert Schmid, Johns Hopkins University

Abstract: Radiometers precisely measure the electromagnetic radiation that is passively emitted by physical media. At microwave and millimeter-wave frequencies, radiometers can provide useful remote sensing observations under adverse conditions (rain, fog, etc.) and without external illumination where infrared and optical sensors fail. Over the past decade, both the underlying semiconductor technologies and the application spaces of radiometers have evolved significantly.

The continued performance increases of advanced node CMOS and scaled SiGe HBTs have enabled the development of radiometers for applications requiring low cost, high volume, and miniaturization. In addition, the recent development of terahertz InP/InGaAs HEMTs have enabled high-resolution radiometry at previously inaccessible frequencies. These advances necessitate a re-evaluation of architecture and technology tradeoffs to fully leverage the unique capabilities enabled by these technologies. Furthermore, while radiometers have traditionally been limited to use in niche scientific and military applications, the application spaces of these systems have grown substantially. Passive imaging systems are now widely implemented for public security, and noninvasive subcutaneous sensing radiometers are increasingly utilized for medical applications. In addition, the proliferation of CubeSats has created a demand for highly integrated radiometers which can enable continuous observations of the Earth's atmosphere and yield improved weather forecasting and climate modeling. This workshop will discuss radiometer theory and system architectures, and will highlight current state-of-the-art microwave and millimeter-wave radiometers in security imaging and scientific applications. A comparison of these systems will show how varying application spaces impose requirements which flow down through the system architecture and component designs to the semiconductor technologies. Calibration procedures and techniques for validating, operating, and ensuring accurate data retrieval from these systems will also be discussed.

Speakers:

1. "CMOS Systems-on-Chip for NASA Radiometry and Spectroscopy from Microwave to THz", **Adrian Tang**, *Jet Propulsion Lab*
2. "Millimeter-Wave Radiometers at 94 GHz and 140 GHz Using Advanced SiGe", **Gabriel M. Rebeiz**, *University of California, San Diego*
3. "Low Noise Radiometers for Passive Millimeter-Wave Imaging", **Harris Moyer**, *HRL Labs*
4. "An Overview of Millimeter-Wave Radiometry: Imaging Phenomenology and Applications", **David Wikner**, *US Army Research Laboratory*
5. "Microwave Radiometers for Earth Observation from Space", **Jeff Piepmeier**, *NASA's Goddard Space Flight Center*

WMI (Half Day): Monday 13:30–17:15
Automotive Radar and Vehicular Network Security

Sponsor: **IMS**

WMJ (Full Day): Monday 08:00–17:15
**Advanced Applications of Nonlinear Vector Network Measurements
for broadband RF Power Amplifiers Design and Linearization**

Sponsors: **IMS, ARFTG**

WMK (Full Day): Monday 08:00–17:15
Affordable Phased-Arrays for
SATCOM and Point-to-Point Systems Using Silicon Technologies

Sponsor: **IMS**

MONDAY SHORT COURSES – 12 JUNE 2018

SMA (Half Day): Monday 8:00–11:50
Practical Computer Modeling for
Electromagnetic Medical Device Designs

Sponsor: **IMS**

SMB (Half Day): Monday 13:30–17:15
Fundamentals of Magnetic-Resonance Imaging

Sponsor: **IMS**

FRIDAY WORKSHOPS – 15 JUNE 2018

WFA (Full Day): Friday 08:00–17:15
Ultra-Low-Power Nanowatt to Microwatt Receivers for the
Internet of Things

Sponsors: **IMS, RFIC**

Organizers: **N. Scott Barker**, *University of Virginia*
Songbin Gong, *University of Illinois at Urbana-Champaign*
Steven Bowers, *University of Virginia*

Abstract: Continued expansion of the internet of things (IoT) into more and ever smaller devices requires development of low power and ultra low power communications radios. The receivers for these devices can be particularly challenging as they seek to increase sensitivity in a noisy and interference filled environment while maintaining low dc power levels needed to maximize time between battery charges or to enable the complete elimination of the battery all together in favor of energy harvesting. Many of these devices are parts of sensor nodes, which spend the majority of their time in an asleep-yet-alert state where a wakeup receiver is the only powered on block. In such scenarios, the power consumption of the receiver can become the dominant power consumer of the

entire node. While much of the work up to this point has been in CMOS integrated circuits, new research in other technologies such as MEMS based receivers also show promise for the future. This workshop will address the design challenges associated with developing low power receivers for IoT applications including tradeoffs between RF frequency, data rate, sensitivity, power, and technology. Prominent researchers from both academia and industry will give insight into their individual design philosophy and vision for where the field is headed, followed by a moderated panel discussion to try to reconcile differences in their visions and take additional questions from attendee.

Speakers:

1. “Recent Trends in Ultra-Low Power Radios”, **David Wentzloff**, *University of Michigan*
2. “Nanowatt Wake-Up Receivers: Exploring Power and Sensitivity Trade-Offs”, **Patrick Mercier**, *University of California, San Diego*
3. “Radio Frequency Micro-Systems for IoT Inspired Front-End Signal Processing”, **Songbin Gong**, *University of Illinois at Urbana-Champaign*
4. “Resonant Micromechanical Receivers”, **Gianluca Piazza**, *Carnegie Mellon University*
5. “Design Considerations of Ultra Low Power Radios for the IoT”, **Nathan Roberts**, *PsiKick*
6. “Wirelessly-Powered Centimeter-Scale Nanowatt Radios in CMOS”, **Arun Natarajan**, *Oregon State University*
7. “Ultra-Low Power Receivers in Highly Scaled CMOS”, **Brent Carlton**, *Intel*
8. “Muting the Chatter: Maintaining Sensitivity of Nanowatt Receivers in High Interference Environments”, **Steven Bowers**, *University of Virginia*

WFB (Full Day): Friday 08:00–17:15

RF Front-Ends for Enhanced Mobile Communications Towards 5G

Sponsors: **IMS, RFIC**

Organizers: **Amelie Hagelauer**, *FAU Erlangen-Nürnberg*
Uwe Rueddenklau, *Infineon Technologies*
Vadim Issakov, *Infineon Technologies*

Abstract: The 5th generation (5G) wireless systems are the proposed telecommunication standards, which offer the next major disruptive technological step in mobile communications. The future 5G systems aim at much higher data rates, higher density of mobile users, lower network latency, spectral efficiency and enhanced signaling compared to the existing 4G systems. To achieve these goals, the operation will be extended to new frequency bands at mm-wave frequencies. Additionally, massive MIMO systems and novel system architectures like digital, hybrid or analog beamforming are expected to be extensively employed. Therefore, major research efforts towards 5G are focusing nowadays on RF front-ends beamforming transceivers and antenna arrays at mm-wave frequencies. Numerous new technological challenges need to be resolved not only on the level of portable user equipment (UE), but also on the level of wireless radio access networks (RAN) and backhaul, including macro-, micro and pico-cells. Particularly, the RAN infrastructure needs to support much higher data rates and enormous amount of data for 5G, as required by enhanced Mobile Broadband

(eMBB) applications. The goal of this full-day workshop is to address the transition from the current state-of-the-art 4G systems towards 5G with a particular focus on challenges related to hardware implementation of RF Front-End Modules (FEMs), beamforming transceivers and antenna arrays. Speakers from leading companies and academia will present several aspects related to semiconductor technology choice, circuit design techniques, novel system architectures, packaging, antenna arrays and network considerations. The talks will distinguish between challenges related to mobile radio user-equipment on the one hand, but also on the base-stations and backhaul networks on the other hand. A brief concluding discussion will round-off the workshop to summarize the key learnings on the wide range of aspects presented during the day.

Speakers:

1. “Millimeter-Wave RF Front-Ends for Enhanced Mobile Communications Towards 5G: An Industry View”, **Renato Lombardi**, *Huawei Technologies*
2. “mm-Wave Front-End Challenges for 5G Base Stations”, **Kristoffer Andersson**, *Ericsson*
3. “Power Amplifier Implementation Challenges in Front-Ends for 5G Mobile Broadband”, **Sergio Pires**, *Ampleon*
4. “Modular Phased-Array Solution with Beam-Steering Antennas for 5G Millimeter-Wave RAN”, **Nebojsa Maletic¹**, **Andrea Malignaggi¹**, **Dietmar Kissinger^{1,2}**, ¹*IHP*, ²*Technische Universität Berlin*
5. “Front-End Module Architecture & Silicon Technology Solutions for 5G Radio Interface”, **Anirban Bandyopadhyay**, *GLOBALFOUNDRIES*
6. “Antenna in Package Integration for 5G and Beyond”, **Mario Pauli**, **Thomas Zwick**, *Karlsruhe Institute of Technology*
7. “System Considerations for 5G mm-Wave Transceiver RAN vs. UE”, **Ludger Verweyen**, *Infineon Technologies*
8. “Challenges and Opportunities of mm-Wave for 5G Mobile Radio”, **Jonathan Jensen**, *Intel*
9. “28GHz CMOS Phased-Array Transceiver for 5G New Radio”, **Kenichi Okada**, *Tokyo Institute of Technology*
10. “mm-Wave RF Front-Ends for 5G”, **Barend van Liempd**, **Mark Ingels**, *imec*

WFD (Half Day): Friday 08:00–11:50

Advanced Synthesis Techniques for Reduced Size Filtering Networks

Sponsor: **IMS**

WFE (Half Day): Friday 13:00–17:15
Recent Advances in
Non-Linear and Non-Reciprocal RF Microwave Devices

Sponsors: **IMS, RFIC**

Organizers: **Dimitra Psychogiou**, *University of Colorado Boulder*
Michael Geiler, *Metamagnetics*

Abstract: Wireless communication, radar and electronic warfare systems are entering a new era in which the need for advanced functionality, low SWaP and low cost set contradicting requirements for their RF front-ends. In particular, the RF front-ends' SWaP is limited by their non-reciprocal counter parts (e.g., RF circulators, isolators) which either need large volume and external biasing in ferrite-based schemes or exhibit poor noise figure, power handling and dynamic range in active-based non-magnetic architectures. In order to overcome the aforementioned limitations, innovations are required in the areas of materials, process integration and modeling. Among them, the realization of devices that do not require magnetic biasing and are suitable for monolithic integration are of critical importance. It is the aim of this workshop to present recent progress in these areas by both academic and industry experts. In addition, recent developments in non-linear RF devices that exploit the presence of spin-waves in magnetic materials (i.e, frequency selective limiters and signal-to-noise enhancers) will also be presented. The first part of this workshop will focus on architectures and concepts that facilitate non-reciprocity by means of novel RF-design techniques using spatiotemporal modulation. New classes of non-reciprocal and non-linear RF devices including circulators, isolators, gyrators and antennas will be presented. The second part will focus on the design and monolithic integration of magnetic devices using self-biased materials as well as spin-wave-based RF components. Lastly, recent progress on magnetic miniaturized and monolithically integrated components (M3IC), a research effort that has been initiated and supported by DARPA will also be presented.

Speakers:

1. "Magnet-Free Non-Reciprocity Using Spatio-Temporal Modulation", **Andrea Alu**, *CUNY Advanced Science Research Center*
2. "Integrated Non-Reciprocal RF/mm-Wave Components and Beyond Through Temporal Modulation", **Harish Krishnaswamy**, *Columbia University*
3. "Time-Varying Electromagnetic Devices: Breaking the Fundamental Limits of Passives", **Yuanxun Ethan Wang**, *University of California, Los Angeles*
4. "Non-Linear Ferrite Signal Processing Devices", **John Adam**, *Northrop Grumman (retired)*
5. "Advances in Non-Reciprocal Devices and Materials", **Vincent Harris¹**, **Michael Geiler²**, ¹*Northwestern University*, ²*Metamagnetics*
6. "Magnetic Miniaturized and Monolithically Integrated Components", **Young-Kai Chen**, *DARPA*

WFF (Full Day): Friday 08:00–17:15
Techniques Passive Devices for Multi-Band Systems

Sponsor: **IMS**

WFG (Full Day): Friday 08:00–17:15
Advances in Linearization Techniques for 5G and Beyond

Sponsor: **IMS**

WFH (Full Day): Friday 08:00–17:15
**Module Integration and Packaging/IC Co-Integration for
Millimeter-Wave Communications and 5G**

Sponsors: **IMS, RFIC**

Organizers: **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center*
Kamal Samanta, *Sony*
Telesphor Kamgaing, *Intel*

Abstract: Rapidly growing demand for broadband cellular data traffic is driving fifth generation (5G) standardization towards deployment by 2020. One anticipated key to enabling gigabit-per-second 5G speeds is millimeter-wave (mm-wave) operation. mm-Wave bands offer 50 times the bandwidth available in existing RF bands but pose numerous technical challenges to the low-cost deployment of radio solutions. U.S. regulators recently issued a notice of inquiry for provision of mobile services in several frequency bands above 24 GHz. Additionally, reliable coverage over the typical 200 meter cell radius in non-line-of-sight dense urban conditions, and practical antenna array solutions for base station and user equipment (UE) have been demonstrated at 28 GHz and other mm-wave frequencies. High-volume implementation of the UE radio is also envisioned as multiple-element phased-array transceiver in silicon and/or III-V technologies. However, packaging constitutes a great technical challenge as co-design and co-integration of the transceiver and package will be critical in meeting both electrical and thermo-mechanical requirements in various applications ranging from handsets and backhaul radios to base stations. This workshop will focus on gathering a combination of academic and industry experts in mm-wave system integration and packaging to discuss novel integrated circuits, modules, and antenna solutions for potential mm-wave 5G radios. The speakers will present state-of-the-art research results in this area and ultimately help participants identify the enabling radio and packaging technologies for 5G cellular communications. Emphasis will be put on novel 3D integration approaches and advanced mm-wave system-on-package architectures based on IC/Package/antenna co-optimization. Novel materials and thermo-mechanical challenges associated with compact and large phased array systems in silicon and III-V technologies will also be discussed for 5G radios in different mm-wave frequency bands including 28 GHz, 39 GHz, 69 GHz, 67 GHz, 73 GHz and forward-looking frequencies above 90 GHz.

Speakers:

1. “Integration and Packaging of 5G and Millimeter-Wave Compact Radio Modules”, **Tauno Vähä-Heikkilä**, *VTT Technical Research Centre of Finland*
2. “PCB Interconnection Concepts for Highly Integrated Ka-Band Antenna for 5G and SATCOM Front-Ends”, **Marta Martinez, Jens Leiß, Rens Baggen, Constantine Kakoyiannis**, *IMST*
3. “5G Millimeter-Wave Front-End Module Implementation and Integration Aspects”, **Kamal Samanta, Chris Clifton**, *Sony*
4. “Advances in Polyjet- and Aerosoljet-Printed Millimeter-Wave Packages”, **Premjeet Chahal, John Papapolymerou**, *Michigan State University*
5. “mm-Wave Packaging and Integration for 5G Base Station and Portable Devices”, **Xiaoxiong Gu**, *IBM T.J. Watson Research Center*
6. “Silicon Based System on Package Phased Array Design for 5G”, **Danny Elad, Ofer Markish, Oded Katz, Benny Sheinman**, *ON Semiconductor*
7. “Wafer-Scale Compatible mm-Wave Dual-Polarization Antenna Co-Integration in Silicon”, **Arun Natarajan**, *Oregon State University*
8. “Millimeter-Wave Integrated Antenna Solutions”, **Loïc Marnat**, *CEA-LETI*
9. “Millimeter-Wave Phased Array Antenna and Front End Co-Design for Smartphones and Small Cells”, **Yu-Chin Ou**, *Qualcomm*

WFI (Full Day): Friday 08:00–17:15
Innovative Technologies for
RF and Millimeter-Wave Tuning and Switching

Sponsor: **IMS**

WFJ (Full Day): Friday 08:00–17:15
Design of Matching Networks for
Optimal Performance of Power Amplifiers and Transmitters

Sponsor: **IMS**

WFK (Full Day): Friday 08:00–17:15
The New GaN: Advancements in
Novel-Materials Based GaN Microwave and mm-Wave Technologies

Sponsor: **IMS**

FRIDAY SHORT COURSES – 15 JUNE 2018

**SFA (Half Day): Friday 08:00–11:50
Multi-Beam Antennas and Beam-Forming Networks**

Sponsor: IMS

**SFB (Half Day): Friday 13:30–17:15
Using Active Fiber Optic for Distributed Antenna System (DAS) System
in 5G MIMO System and Automobile Radar System**

Sponsor: IMS

REGISTRATION

For attendee registration: <https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=247>

For booth staff registration: <https://reg.mpassociates.com/reglive/signin.aspx?confid=254>

For questions regarding registration please contact Nannette Jordan, Registration Manager at nannette@mpassociates.com.

There are three registration periods, each with different rates. We appreciate your understanding that this multi-tiered registration structure allows the Steering Committee to work out the logistics more efficiently, while also serving the needs of our membership.

Early Bird Registration: 1 February – 14 May 2018

Advance Registration: 15 May – 8 June 2018

On-Site Registration: 9 June – 15 June 2018

The Early Bird Registration period provides discounted rates for those who want to plan ahead. Immediately following is Advance Registration, which ends just prior to the start of Microwave Week; the rates are higher than Early Bird, but lower than On-Site Registration.

Please note: Registration is required for all attendees including SESSION CHAIRS and PRESENTERS. Only paid attendees will be admitted to the workshops, technical sessions, and exhibition hall.

The following steps will guide you through the registration process:

Membership

From the dropdown menu, select the primary organization (IEEE, ARFTG, EuMA) to which you belong as well as your membership status. Next, type in your membership number. If you are a university student but not a member in any of these organizations, type in your university student identification number. To receive IEEE member rates, you must present your IEEE membership card when picking up your badge at the conference. Registrants who do not present a current IEEE membership card will be charged non-member rates. If you are not an IEEE member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit <http://www.ieee.org/services/join> or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Registration Categories

Conference Packages

Microwave Week includes the IMS technical program and exhibition (<http://ims2018.org/>), the RFIC Symposium (<http://rfic-ieee.org/>), the ARFTG Conference (<http://www.arftg.org/>) and the IMBioC Conference (<http://imbio-ieee.org/>).

- **SUPERPASS** registration includes: all IMS, RFIC, ARFTG, IMBioC technical sessions and electronic proceedings; one full-day workshop (or two half-day workshops); electronic proceedings for all three workshop days; 5G Summit and Panel, Physicians Panel, exhibition Tuesday through Thursday; RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening; IMS Plenary Session and Welcome Reception on Monday; and one ticket to the MTT-S Awards Banquet on Wednesday.

REGISTRATION (continued)

- **RFIC SYMPOSIUM** registration includes: RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening; RFIC technical sessions on Monday and Tuesday; IMS Plenary Session and Welcome Reception on Monday; exhibition Tuesday through Thursday; and RFIC electronic proceedings.
- **IMS** registration includes: IMS Plenary Session and Welcome Reception on Monday; IMS technical sessions on Tuesday through Thursday; exhibition Tuesday through Thursday; and IMS electronic proceedings.
- **ARFTG CONFERENCE** registration includes: ARFTG technical sessions, exhibition, and lunch on Friday; IMS Plenary Session and Welcome Reception on Monday; exhibition Tuesday through Thursday; and ARFTG electronic proceedings. ARFTG Conference member rates are available to both ARFTG and IEEE members.
- **IMBioC CONFERENCE** registration includes: IMBioC technical sessions, exhibition, and lunch on Friday, 15 June; IMS Plenary Session and Welcome Reception on Monday; exhibition Tuesday through Thursday; and IMBioC electronic proceedings. The International Microwave Biomedical Conference (IMBioC) is an international forum for the exchange of ideas and information on state-of-the-art research in microwave and RF theory and techniques that bridge the science and engineering gap as applied to biological systems. This conference is an ideal forum for sharing new ideas on emerging techniques and applications.
- **EXHIBITION** registration for the exhibit hall Tuesday through Thursday. Wednesday exhibition-only registration is free!

Individual Events to add to your Conference Package

- **5G SUMMIT:** IEEE MTT-S and IEEE ComSoc are offering a special joint 5G Summit — a special collaboration that compliments MTT-S’s “hardware and systems” focus with ComSoc’s “networking and services” focus. To fully integrate this special 5G Summit into Microwave Week, the summit will be held on Tuesday, 12 June from 08:00–17:00. The fee includes a morning refreshment break, boxed lunch, and an afternoon refreshment break.
- **TWO FULL-DAY WORKSHOPS:** Purchase two full-day workshops by selecting the option labeled “Two Full-Day Workshop Registration” and receive access to the electronic proceedings for all three workshop days (Sunday, Monday, and Friday). **IMPORTANT:** Must select the Two Full-Day workshop option to receive this. Workshop electronic proceedings are NOT available for individual sale.
- **FULL-DAY AND HALF-DAY WORKSHOPS:** The workshop fee includes access to the electronic proceedings for all workshops being presented on that particular day. Full-day workshops include a morning refreshment break, boxed lunch, and an afternoon refreshment break. Morning workshops include a morning refreshment break and a boxed lunch. Afternoon workshops include a boxed lunch and an afternoon refreshment break. **IMPORTANT:** Printed Workshop Notes will be available to those registered for a workshop by 14 May. Advance and onsite registrations for workshops are NOT guaranteed to include printed workshop notes; limited copies will be provided on a first-come first served basis. All workshop materials will be provided electronically (via the “cloud”) so that all workshop registrants may have the option of downloading and printing the notes on their own before traveling.

REGISTRATION (continued)

- **HALF-DAY SHORT COURSES:** The short course fee includes access to the selected short course and any materials that the short course organizers may provide. Morning short courses include a morning refreshment break and a boxed lunch. Afternoon short courses include a boxed lunch and an afternoon refreshment break. **IMPORTANT:** Printed Short Course Notes will be available to those registered for short courses by 14 May. Advance and onsite registrations for short courses are **NOT** guaranteed to include printed short course notes; limited copies will be provided on a first-come first-served basis. All short course materials will be provided electronically (via the “cloud”) so that all registrants have the option of downloading and printing the notes on their own before traveling.
- **RF BOOTCAMP:** This full-day course on Monday, 11 June will cover real-world, practical, modern design and engineering fundamentals needed by technicians, new engineers, engineers wanting a refresh, college students, as well marketing and sales professionals. Experts within industry and academia will share their knowledge of RF/Microwave systems basics, simulation and network design, network and spectrum analysis, and microwave antenna and radar basics. Attendees completing the course will earn two IEEE CEUs. The fee includes a morning refreshment break, boxed lunch, and an afternoon refreshment break.
- **INDUSTRY WORKSHOPS:** Industry Workshops are two-hour exhibitor-led presentations on in-depth technical topics in a workshop format off the exhibit floor. Industry Workshops offer practical training in areas that allow attendees to make immediate use of the materials presented. This year, IMS is offering 16 Industry Workshops covering a wide range of relevant topics. The IMS2018 Exhibitor Committee expects this platform to provide lively interaction and in-depth discussions between the exhibitors and attendees.

Extras

- **MTT-S AWARDS BANQUET:** The MTT-S Awards Banquet will be held on Wednesday, 13 June at the Loews Philadelphia Hotel in the Regency Ballroom from 18:30–21:00. The evening will include fine dining, an awards presentation, and excellent entertainment.
- **BOXED LUNCHES:** Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending panel sessions or the exhibition hall during lunchtime. Registrants are encouraged to purchase boxed lunches prior to Microwave Week, as onsite orders will not be accepted. Refunds for lunches are not available as these are ordered in advance. Note that boxed lunches are already included in the registration fee for workshops, short courses, 5G Summit, Physicians Panel and RF Boot Camp. Please note that specialized Kosher and allergy restricted box lunches are not available.
- **GUEST REGISTRATION:** Attendees registered for the technical portion of the conference (SUPERPASS, IMS, RFIC, ARFTG) may add a guest to their registration package at no additional charge. Guest registration includes: IMS Plenary Session and Welcome Reception on Monday; and exhibition and 5G demos on Tuesday through Thursday. Guest registration does not allow access to technical sessions, workshops, and short courses. This option does **NOT** include access to the Guest Lounge.
- **GUEST LOUNGE:** For a fee you may register your guest to have access to the Guest Lounge located at the the Courtyard Marriott. Guest Lounge will be open Monday through Thursday from 07:00–13:00. Coffee and tea service will be provided during these hours. Guest Lounge registration includes: IMS Plenary Session and Welcome Reception on Monday; and exhibition and 5G demos on Tuesday through Thursday and the Guest Lounge.

Guest registration does not allow access to technical sessions, workshops, and short courses. IMPORTANT: Guest Badge is limited to one person per technical registration (technical registration includes IMS, RFIC, ARFTG, Superpass) and children under the age of 14 are NOT permitted on the Exhibition Floor.

Payment

Individual payment must be paid at the time of registration and is payable in US dollars only, using a personal check drawn on a US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order, and purchase orders are NOT ACCEPTED and will be returned. Please make checks payable to "2018 IEEE MTT-S". Written requests for refunds will be honored if received by 14 May 2018. Refer to the Refund Policy for complete details.

Refund Policy

Written requests received by 14 May 2018 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email when requesting a refund. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027, USA
nannette@mpassociates.com

ON-SITE REGISTRATION

On-site registration for all Microwave Week events will be available on the Second Level in the Corridor of the Pennsylvania Convention Center:

Date	Time
Saturday, 9 June	08:00–18:00
Sunday, 10 June	07:00–18:00
Monday, 11 June	07:00–19:00
Tuesday, 12 June	07:00–18:00
Wednesday, 13 June	07:00–18:00
Thursday, 14 June	07:00–16:00
Friday, 15 June	07:00–12:00

Exhibit-Only Registration

Exhibit-only registration is available.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to the Exhibition, IMS Plenary and technical sessions, IMS Welcome Reception, RFIC Plenary and technical sessions, RFIC Industry Showcase, RFIC Reception and Exhibition, 5G Summit, and Three Minute Thesis (3MT®) Competition. The Press Lounge will be available from Monday through Thursday of Microwave Week.

ARFTG and IMBioC Registration

Late on-site registration will be available on the Second Level in the Corridor of the Pennsylvania Convention Center on Friday from 07:00–12:00. If at all possible, please pre-register earlier in the week.

REGISTRATION RATES

	Early Bird (1 Feb–14 May)		Advance (15 May–8 June)		On-Site (9–15 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Registration Rates in USD						
Superpass	\$1120	\$1690	\$1305	\$1950	\$1515	\$2250
IEEE Life Member (Retiree)	\$675	NA	\$785	NA	\$955	NA
Student	\$675	\$695	\$785	\$805	\$955	\$970
RFIC Sessions	\$260	\$365	\$295	\$430	\$315	\$465
IEEE Life Member (Retiree)	\$185	NA	\$205	NA	\$225	NA
Student	\$185	\$205	\$205	\$225	\$225	\$245
IMS Sessions	\$485	\$715	\$555	\$830	\$645	\$955
IEEE Life Member (Retiree)	\$85	NA	\$95	NA	\$115	NA
Student	\$85	\$150	\$95	\$165	\$115	\$190
Single Day Registration	\$245	\$355	\$285	\$415	\$325	\$495
ARFTG Sessions	\$270	\$400	\$315	\$460	\$350	\$520
IEEE or ARFTG Life Member (Retiree)	\$190	NA	\$220	NA	\$250	NA
Student	\$190	\$215	\$220	\$250	\$250	\$280
IMBioC Sessions	\$225	\$345	\$265	\$405	\$300	\$465
IEEE Life Member (Retiree)	\$150	NA	\$175	NA	\$195	NA
Student	\$150	\$190	\$175	\$225	\$195	\$245
Exhibit Only Pass	\$25	\$25	\$25	\$25	\$30	\$30
Wednesday Exhibition Only Pass	free	free	free	free	free	free

REGISTRATION RATES (continued)

Registration Rates in USD	Early Bird (1 Feb–14 May)		Advance (15 May–8 June)		On-Site (9–15 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
2 Full Day Workshops (includes electronic proceedings for all three workshop days)						
IEEE Life Member (Retiree)	\$485	\$705	\$225	\$775	\$660	\$975
Student	\$355	NA	\$395	NA	\$445	NA
	\$355	\$385	\$395	\$415	\$445	\$470
Full Day Workshop						
IEEE Life Member (Retiree)	\$190	\$275	\$205	\$300	\$250	\$375
Student	\$145	NA	\$155	NA	\$180	NA
	\$145	\$165	\$155	\$175	\$180	\$195
Half Day Workshop						
IEEE Life Member (Retiree)	\$95	\$145	\$110	\$165	\$135	\$195
Student	\$75	NA	\$80	NA	\$90	NA
	\$75	\$90	\$80	\$95	\$90	\$110
Half Day Short Course						
IEEE Life Member (Retiree)	\$225	\$335	\$260	\$400	\$300	\$455
Student	\$165	NA	\$190	NA	\$215	NA
	\$165	\$180	\$190	\$205	\$215	\$230
5G Summit						
IEEE Life Member (Retiree)	\$190	\$275	\$205	\$300	\$250	\$375
Student	\$145	NA	\$155	NA	\$180	NA
	\$145	\$165	\$155	\$175	\$180	\$195
RF Boot Camp						
	\$135	\$135	\$160	\$160	\$160	\$160
Industry Workshops (each of the three workshop days)						
	\$25	\$25	\$25	\$25	\$25	\$25
Focus Group Sessions						
Young Professionals Panel Session	NA	NA	NA	NA	NA	NA
Women in Microwaves Panel Session	NA	NA	NA	NA	NA	NA

REGISTRATION RATES (continued)

Registration Rates in USD		Early Bird (1 Feb–14 May)		Advance (15 May–8 June)		On-Site (9–15 June)	
		Member	Non-Member	Member	Non-Member	Member	Non-Member
Events							
RFIC Sunday Evening Only (includes: RFIC Plenary Session, Industry Showcase and Reception)		\$50	\$75	\$60	\$90	\$70	\$105
MITT-S Award Banquet (Wednesday Evening)		\$75	\$75	\$75	\$75	\$75	\$75
Focus Group Events							
Young Professionals Panel and Networking Reception (Tuesday)		NA	NA	NA	NA	NA	NA
Women in Microwaves Panel and Networking Reception (Thursday)		NA	NA	NA	NA	NA	NA
Special Events							
HAM Lecture and Networking Reception (Tuesday)		NA	NA	NA	NA	NA	NA
Physicians Lunch Panel (Thursday)		NA	NA	NA	NA	NA	NA
Guest Registration							
Guest Badge (access to exhibition only)		NA	NA	NA	NA	NA	NA
Guest Lounge (access to guest lounge and exhibition)		\$75	\$75	\$75	\$75	\$75	\$75
Lunch (Kosher & allergy restricted box lunches not available)							
Monday Boxed Lunch		\$35	\$35	\$35	\$35		
Tuesday Boxed Lunch		\$35	\$35	\$35	\$35	\$35	\$35
Wednesday Boxed Lunch		\$35	\$35	\$35	\$35	\$35	\$35
Thursday Boxed Lunch		\$35	\$35	\$35	\$35	\$35	\$35
Electronic Proceedings Download							
RFIC		\$50	\$75	\$60	\$90	\$70	\$105
IMS		\$50	\$75	\$60	\$90	\$70	\$105
ARFTG		\$50	\$75	\$60	\$90	\$70	\$105
IMBioC		\$50	\$75	\$60	\$90	\$70	\$105

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning — if required — and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 38 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Currently, 38 countries participate in the Visa Waiver Program: Andorra, Australia, Austria, Belgium, Brunei, Chile, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Japan, Latvia, Liechtenstein, Lithuania, Luxembourg, Malta, Monaco, The Netherlands, New Zealand, Norway, Portugal, San Marino, Singapore, Slovakia, Slovenia, South Korea, Spain, Sweden, Switzerland, Taiwan, United Kingdom.

For more information, see <https://travel.state.gov/content/visas/en/visit.html>.

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, <https://www.cbp.gov/>, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. To allow sufficient time for processing, please submit your requests for letters of support well in advance of your interview dates, to IMS2018Visa@gmail.com. All requests should include complete name (as in your passport) and current mailing address as this information is to be included in the letter for submission to the US Consulate. Also please contact IMS2018Visa@gmail.com for additional visa assistance queries.

Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (currently posted on the IMS2018 website).

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative source of information is the U.S. Government website at <https://travel.state.gov/content/visas/en/visit.html>.

SOCIAL EVENTS/GUEST PROGRAM

SUNDAY, 10 June 2018

RFIC Welcoming Reception: 19:00–21:00

RFIC2018 starts with a welcome event for all attendees, which will be hosted at the Loews Philadelphia Hotel immediately following the RFIC2018 Plenary Session.

MONDAY, 11 June 2018

IMS Welcome Event: 19:00–20:30

IMS2018 starts with a welcome event for all attendees, which will be hosted at the Reading Terminal Market immediately following the IMS2018 Plenary Session.

MONDAY, 11 June 2018 – THURSDAY, 14 June 2018

Guest Lounge: 07:00–13:00

Located at the Courtyard Marriott Philadelphia Downtown. Light refreshments will be provided for all registered guests.

TUESDAY, 12 June 2018

Young Professionals Panel Session and Networking Event

The Young Professionals are planning a panel session and networking event at the Pennsylvania Convention Center. Please refer to the conference website for detailed information on the panel session.

WEDNESDAY, 13 June 2018

Industry-Hosted Cocktail Reception: 17:00–18:00

The Industry-Hosted Reception is scheduled on the exhibition floor right before the MTT-S Awards Banquet.

Awards Banquet: 18:30–20:00

The MTT-S Awards Banquet will be hosted at the Loews Philadelphia Hotel and will feature exciting entertainment performed by the Motor City Revue Band featuring the Philly sound.

THURSDAY, 14 June 2018

Women in Microwaves Panel Session and Networking Event





















The Women in Microwaves Panel Session and Networking Event will be held at the Philadelphia Academy of Fine Arts.

PENNSYLVANIA CONVENTION CENTER MAPS

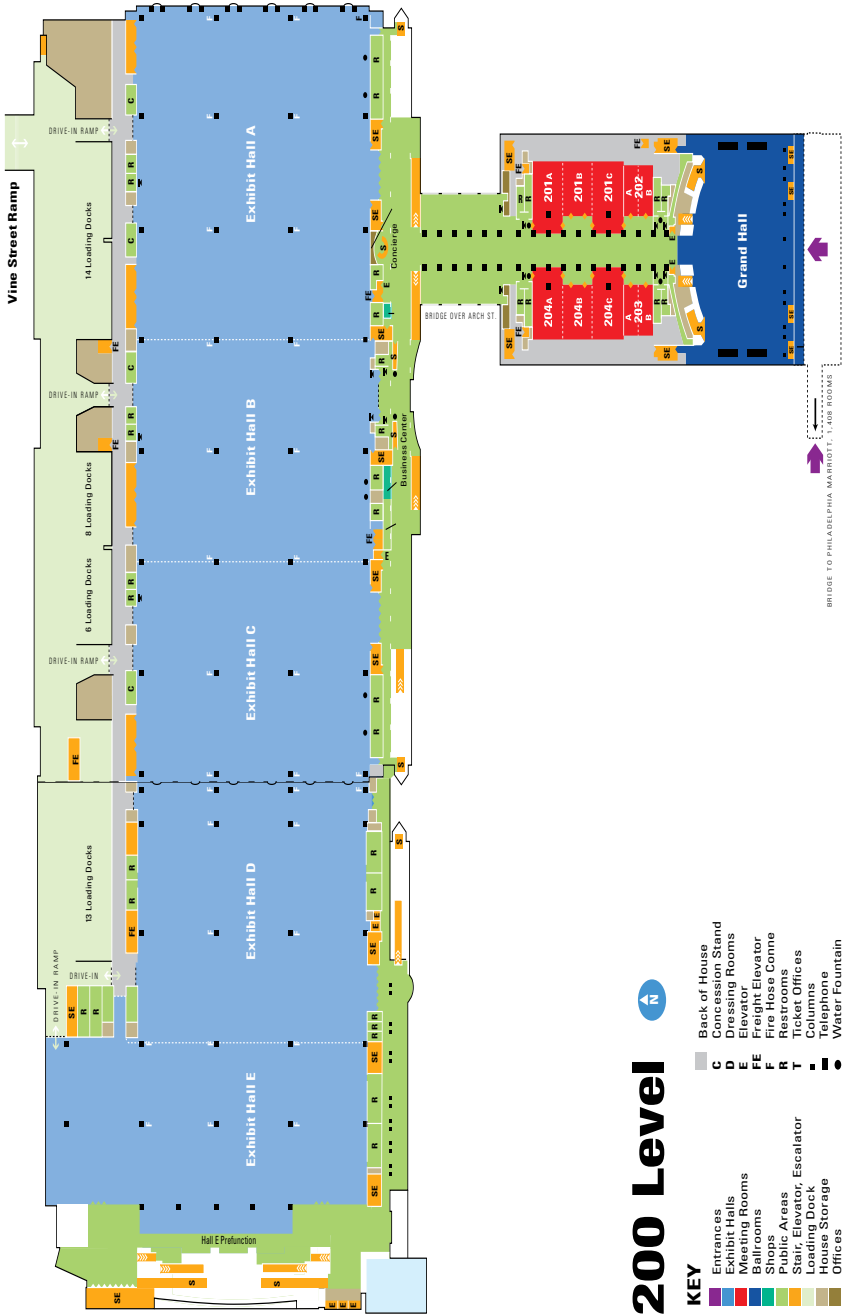


100 Level

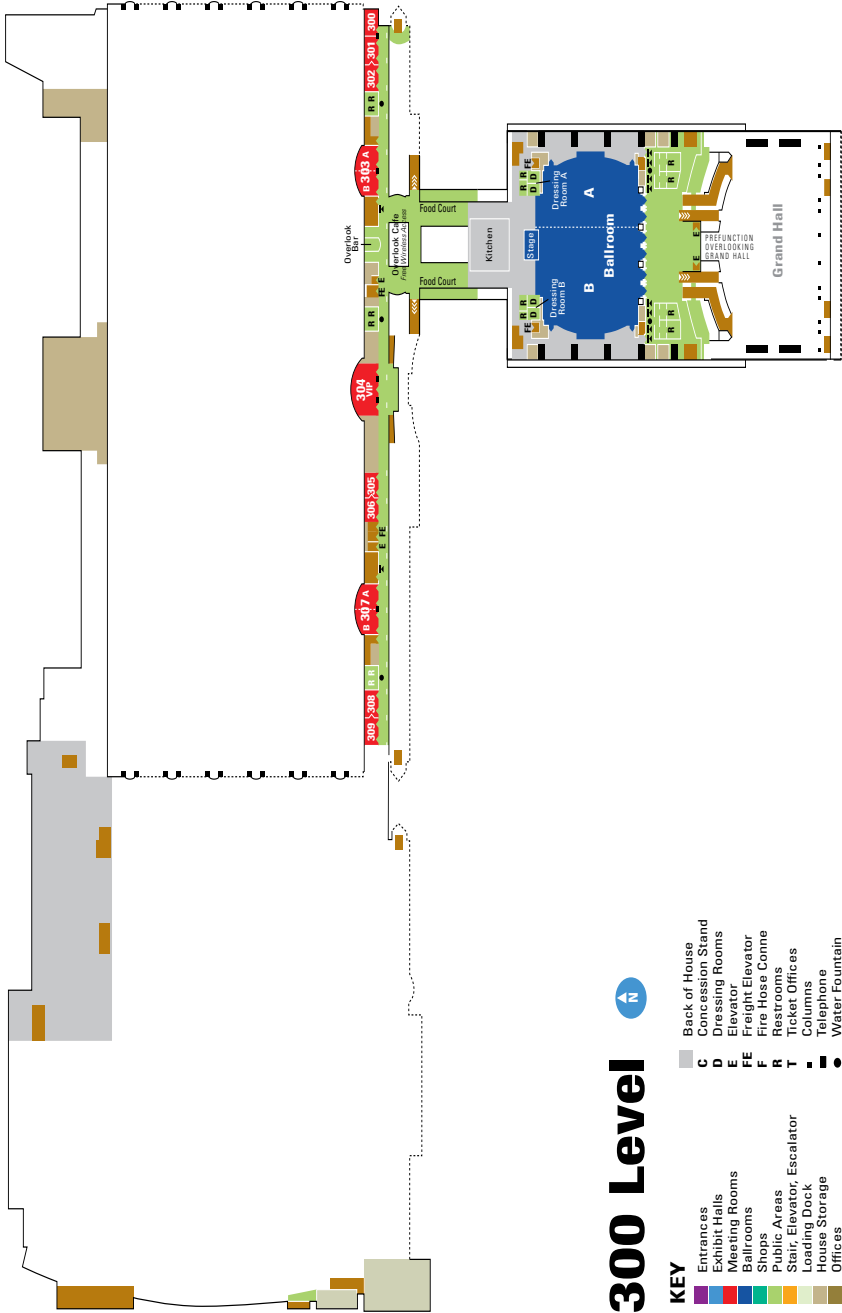
KEY

-  Entrances
-  Restrooms
-  Meeting Rooms
-  Ballrooms
-  Shops
-  Areas
-  Stair/Elevator, Escalator
-  Loading Dock
-  House Storage
-  Offices
-  Back of House
-  Concession Stand
-  Rooms
-  Elevator
-  Freight Elevator
-  Fire Hose Connection
-  Ticket Office
-  Columns
-  Telephone
-  Water Fountain

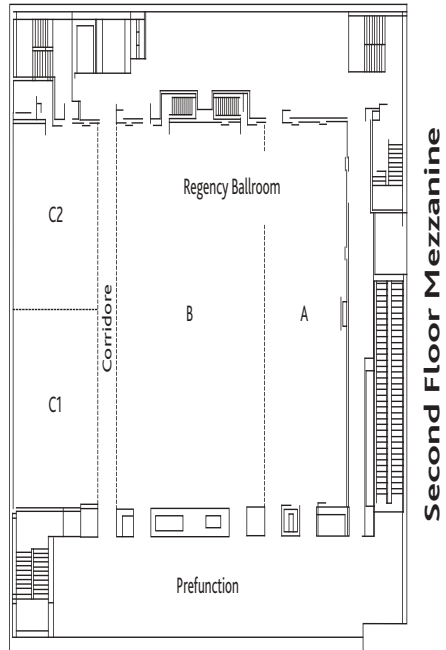
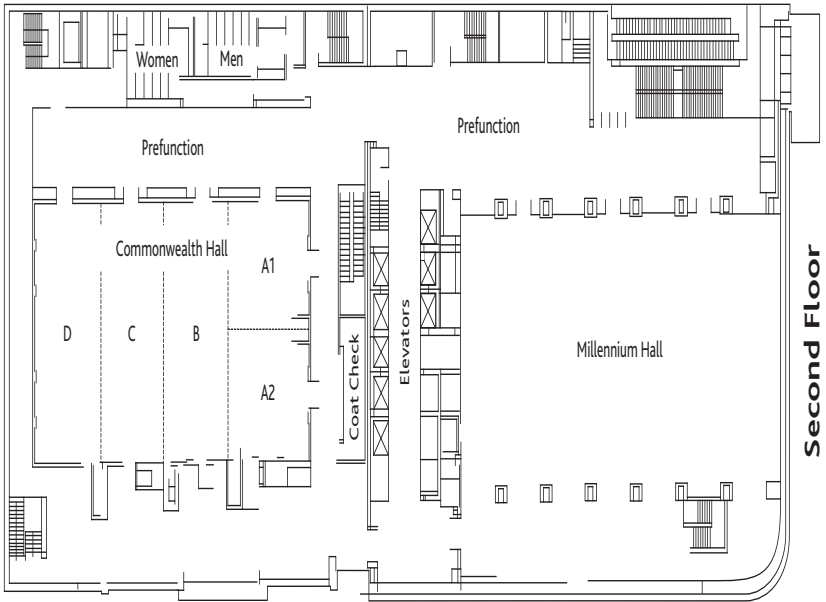
PENNSYLVANIA CONVENTION CENTER MAPS (continued)



PENNSYLVANIA CONVENTION CENTER MAPS (continued)



Loews Philadelphia Hotel MAP



NOTES

IEEE

445 Hoes Lane
Piscataway, NJ 08854, USA

2018 RFIC Symposium

Philadelphia, Pennsylvania, USA
10–12 June 2018



RFIC PROGRAM