2017 IEEE Radio Frequency Integrated Circuits Symposium

Honolulu, Hawaii, USA
4–6 June 2017

IEEE

PROGRAM

Hawaii Convention Center
and
Hilton Hawaiian Village Waikiki Beach Resort

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
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RFIC Plenary, Reception, Joint Industry Showcase & Interactive Forum

Sunday Evening, 4 June 2017
Hilton Hawaiian Village Waikiki Beach Resort
Mid-Pacific Conference Center

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in the Hilton Hawaiian Village Waikiki Beach Resort, Mid-Pacific Conference Center.

18:00–19:30, Hilton, Mid-Pacific Conference Center, Coral Ballroom — The Plenary Session kicks off the evening with the Student Paper Awards, RFIC Industry Best Paper Award, and RFIC Tina Quach Service Award ceremony followed by two outstanding 5th generation wireless plenary speakers, Dr. Seizo Onoe, CTO and EVP of NTT DOCOMO, INC., and Prof. Gabriel M. Rebeiz, Distinguished Professor at the University of California, San Diego.

19:30–21:30, Hilton, Mid-Pacific Conference Center, Coral Lounge — RFIC Welcoming Reception Featuring Joint Industry Showcase & Interactive Forum: Immediately following the Plenary Session is the RFIC Reception. Drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest developments in the wireless industry.

The Industry Showcase Session, held concurrently with the plenary reception, will highlight 10 selected papers submitted by authors from the industry. Jointly with the Industry Showcase, the Interactive Forum Session will present 15 papers in poster format. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also give a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and the Super-pass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but don't want to miss microwave week's opening event. Please see http://rfic-ieee.org/ for more details.

The RFIC Reception is sponsored by the RFIC Steering Committee and through the generous support of our corporate sponsors:

Diamond Sponsor

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RFIC Symposium Schedule (4–6 June 2017)

Event	Location	Sat 3 June	Sun 4 June	Mon 4 June	Tue 6 June
Registration	HCC, Level 1, Main Lobby	08:00–19:00	07:00–19:00		07:00–18:00
Workshop Speakers' Breakfast	HCC, Level 3, Rooms 323 A–C		07:00–08:00		
Workshops & Short Courses	HCC, Level 3, Rooms 312–325		08:00–17:00		
Workshop Lunch	HCC, Level 3, Ala Halawai Center Concourse		12:00–13:00		
Plenary Session	Hilton, Mid-Pacific Conference Center, Coral Ballroom		18:00–19:30		
Reception, Joint Industry Showcase & Interactive Forum	Hilton, Mid-Pacific Conference Center, Coral Lounge		19:30–21:30		
Speakers' Breakfast	HCC, Level 3, Rooms 323 A–C			07:00–08:00	
Technical Sessions	HCC, Level 3, Rooms 312–313B			08:00–09:40 10:00–11:40 13:30–15:10 15:30–17:10	08:00–09:40 10:00–11:40
Panel Sessions	HCC, Level 3, Rooms 316C			11:45–12:45	

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The RFIC Symposium is the premier IC conference focused exclusively on the latest developments in RF, Microwave, and Millimeter-Wave Integrated Circuit technology and innovation from both industry and academia.

Welcome Message from Chairs

We invite you to participate in the 2017 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held in Honolulu, Hawaii, on 4–6 June 2017. RFIC Symposium is the premier IC design conference focused exclusively on the latest advances in RF, Microwave and Millimeter-Wave integrated circuit (IC) technologies and designs, as well as innovations in high frequency analog/mixed-signal ICs. We cordially invite you to participate in this global event!

The RFIC Symposium is an annual IEEE conference that is combined with the International Microwave Symposium (IMS), ARFTG and the Industry Exhibition to form "Microwave Week", the largest worldwide RF/microwave technical meeting of the year. Microwave week will be held at the Hawaiian Convention Center in Honolulu Hawaii which is in close proximity to nearby Waikiki. Attendees will have the opportunity to interact with world experts, expand their network, and leave invigorated with new ideas and a drive to innovate.

RFIC 2017 will continue to offer a number of initiatives: the 2-page industry brief format, allowing the latest state-of-the-art RF IC design results to be presented without requiring die photos and detailed schematics, will continue in 2017. The popular Industry Showcase Session, featuring poster presentations (and optional demos) of the most innovative and highly-rated industrial papers (both two and four page formats), will be the highlight during the RFIC Reception in the evening of Sunday, 4 June 2017. Again this year, the Industry Showcase will be held jointly with the Interactive Forum (IF) Session during the RFIC Reception, which will offer the attendees an enhanced interactive experience in a relaxed environment. To improve academic submissions, all of the RFIC student paper finalists will receive complimentary RFIC registration. Students may volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complimentary conference registration, meals, T-shirts, and other benefits. The joint RFIC/IMS PhD Student Sponsorship Initiative Program will continue to involve selected first and second-year PhD students to complete technical assignments during the conference in exchange for complimentary conference registrations, lodging and meals.

RFIC 2017 will open on Sunday, 4 June 2017, with 16 workshops (10 full-day and 6 half-day). These workshops cover a wide range of topics including: "5G mm-Wave IC Front-End Co-Design with Antenna, Packaging, and Testing for Future SOC Solutions", "Advanced Concepts and Architectures for Future RF and mm-Wave Transceivers in Nanoscale CMOS", "CMOSpace: Challenges and Accomplishments of Designing Advanced CMOS SoC for Space Communication and Instrumentation", "Efficiency Enhancement Techniques for Linear and High Bandwidth Power Amplifiers", "Energy-Efficient RF Transceiver IC and System Design for Healthcare Applications", "Frequency Synthesis and Clock Distribution for Massive MIMO and Phased-Arrays in 5G Communication Systems and Beyond", "High Performance Power Efficient Clock Generation for Internet of Things Applications", "Highly Digital CMOS Transmitters with Embedded Power Amplifiers", "Microwave through Sub-THz Imaging and Sensor Array Technology for Security, Industrial, Commercial and Medical Applications", "Millimeter Wave for 5G: Which Systems with Which Frequency Band — 5G RF Transceiver Design and System Aspects", "Polar, ET, Out-Phasing, Doherty, Pre-Distortion: Which One Survives at mm-Wave Frequencies?", "RFIC Design Challenges for the IoT at Scale", "RFIC Design for Automotive Radar", "RFIC Design in CMOS FinFET and FD-SOI", "RF-Inspired Silicon Photonic", "The Many Flavors of CMOS/Bipolar RF Harmonic Oscillators". These workshops cover some of the hottest topics in RFIC design.

The RFIC Plenary Session will be held in the evening beginning with the conference highlights, the presentation of the Student Paper Awards and the Industry Best Paper Award. The plenary session will conclude with focused talks on "5G" beginning with Dr. Seizo Onoe, CTO and EVP of NTT Docomo who will enlighten us on the "Deployment Realities of 5G". The second talk will be given by the Wireless Communications Industry Chair Professor at UCSD and National Academy of Engineering member, Prof. Gabriel Rebeiz, who will share his vision on "RFIC/Silicon-Based Phased Arrays and Transceivers for 5G".

Immediately following the plenary session will be the RFIC 'interactive' Sunday reception that will highlight our industry show-case and interactive forum papers in an engaging social and technical evening event supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year!

On Monday and Tuesday, the RFIC will have multiple tracks of oral technical paper sessions. Two entertaining panels will be featured during lunchtime on both days. The Monday panel session is titled "5th Generation Wireless — Where is That Going and What's in It for Me?" while the Tuesday panel session will be a gameshow-quiz titled "Who Wants to be a Millimeterwavionaire?". Make sure to bring your opinions and questions and come prepared to answer technical trivia at the Tuesday panel to win prizes. The afternoon 5G summit technical talks will provide high level 5G technology overview that will complement the 5G-focused RFIC morning technical sessions. A separate registration will be required for the 5G summit.

On behalf of the RFIC steering and executive committees, we welcome you to join us at the 2017 RFIC Symposium in Honolulu Hawaii! Please visit the RFIC 2017 website (http://rfic-ieee.org) for more details and updates.

Kevin W. Kobayashi
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Qorvo

Walid Ali-Ahmad
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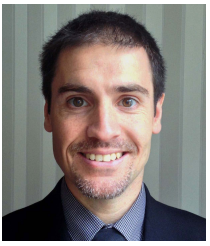

Stefano Pellerano
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Yuxiang Zheng, *Huawei Technologies*

RFIC 2017 Schedule

Saturday, 3 June 2017

08:00–19:00 Registration — Hawaii Convention Center (HCC), Level 1, Main Lobby

Sunday, 4 June 2017

07:00–19:00 Registration — HCC, Level 1, Main Lobby
07:00–08:00 Workshop Speakers' Breakfast — HCC, Level 3, Rooms 323 A–C
08:00–17:00 Workshops and Short Courses, HCC, Level 3, Rooms 312–325
12:00–13:00 Workshops Lunch — HCC, Level 3, Ala Halawai Center Concourse
18:00–19:30 RFIC Plenary — Hilton Hawaiian Village Waikiki Beach Resort (Hilton), Mid-Pacific Conference Center, Coral Ballroom
19:30–21:30 RFIC Welcoming Reception Featuring Joint Industry Showcase & Interactive Forum — Hilton, Mid-Pacific Conference Center, Coral Lounge

Monday, 5 June 2017

07:00–19:00 Registration — HCC, Level 1, Main Lobby
07:00–08:00 Speakers' Breakfast — HCC, Level 3, Rooms 323 A–C
07:00–08:00 Workshop Speakers' Breakfast — HCC, Level 3, Rooms 323 A–C
08:00–17:00 Workshops and Short Courses, HCC, Level 3, Rooms 312–325
08:00–09:40 RMO1A — HCC, Room 312: *28GHz Phased-Array Transceivers for 5G systems*
RMO1B — HCC, Room 313A: *Advanced Technologies for Optical, Millimeter-Wave and Radio Frequency Applications*
RMO1D — HCC, Room 313B: *High-Performance Frequency Synthesizers*
09:40–10:00 Break — HCC, Level 3, Ala Halawai Center Concourse
10:00–11:20 RMO2A — HCC, Room 312: *Radio Building Blocks for 5G Systems*
10:00–11:40 RMO2B — HCC, Room 313A: *Modeling and Characterization for Emerging High Frequency and RF Front-End Applications*
RMO2D — HCC, Room 313B: *Millimeter-Wave and THz Sources*
11:45–12:45 RFIC Panel Session — HCC, Room 313C
12:00–13:00 Workshops Lunch — HCC, Level 3, Ala Halawai Center Concourse
13:30–15:10 RMO3A — HCC, Room 312: *Ultra-Low Power Wake-Up Receivers*
RMO3B — HCC, Room 313A: *Next Generation Transmitters and Receivers for Cellular and Wireless Connectivity*
RMO3D — HCC, Room 313B: *X Band PAs and Beyond*
15:10–15:30 Break — HCC, Level 3, Ala Halawai Center Concourse
15:30–17:05 RMO4A — HCC, Room 312: *Low-Power Transceivers*
RMO4B — HCC, Room 313A: *RF Circuits for Emerging Applications and Gigabit Optical Links*
RMO4D — HCC, Room 313B: *Reconfigurable Receiver Front-Ends*

Tuesday, 6 June 2017

07:00–18:00 Registration — HCC, Level 1, Main Lobby
07:00–08:00 Speakers' Breakfast — HCC, Level 3, Rooms 323 A–C
08:00–09:40 RTU1A — HCC, Room 312: *RF Front-End Building Blocks*
RTU1B — HCC, Room 313A: *Advanced Millimeter-Wave Circuit Techniques*
RTU1D — HCC, Room 313B: *Reconfigurable Multi-Mode PAs*
09:40–10:00 Break — HCC, Level 1, Exhibit Hall II
10:00–11:40 RTU2A — HCC, Room 312: *Full-Duplex, Interference-Resilient and Harmonic-Rejection Receivers*
RTU2B — HCC, Room 313A: *System-on-Chip for Millimeter-Wave and Above*
RTU2D — HCC, Room 313B: *Power Amplifiers in Advanced Technologies*
11:45–12:45 RFIC Panel Session — HCC, Level 3, Room 316C

Schedule: Plenary, Reception, Joint Industry Showcase & Interactive Forum

Sunday Evening, 4 June 2017
Hilton Hawaiian Village Waikiki Beach Resort

18:00–19:30
RFIC Plenary
Mid-Pacific Conference Center, Coral Ballroom

Chair: Kevin W. Kobayashi, Qorvo

Co-Chair: Walid Ali-Ahmad, Qualcomm

Co-Chair: Stefano Pellerano, Intel

18:00 Welcome Message from General Chair and TPC Chairs,
Student Paper Awards, Industry Best Paper Award, Tina Quach Service Award

18:30 *Deployment Realities of 5G*
Seizo Onoe, NTT DOCOMO

19:00 *RFIC/Silicon-based Phased Arrays and Transceivers for 5G*
Gabriel M. Rebeiz, University of California, San Diego

19:30–21:30
RFIC Welcoming Reception
Featuring Joint Industry Showcase & Interactive Forum
Mid-Pacific Conference Center, Coral Lounge

The RFIC "Interactive" Reception starts immediately after the Plenary Session and will highlight 10 industry show-case and 15 interactive forum papers in an engaging social and technical evening event with food and drinks. This event is supported by the RFIC Symposium corporate sponsors. You will not want to miss the RFIC Reception this year! Authors of these showcase and interactive forum papers will present their innovative work, summarized in poster format. Some industry showcase papers will also have demonstrations. The press will cover this event giving the attendees an excellent opportunity to hear the latest RFIC developments and breakthroughs in person. After the reception, you will be able to enjoy the numerous shops in the Hawaiian Village and an evening stroll along Waikiki beach.

Best Student Paper Award Finalists

One of the missions of RFIC Symposium is to promote academic research and education. As part of the Best Student Paper Award program, several finalists are nominated every year by RFIC Technical Program Committee to enter the final contest where the top-three best papers are selected. All finalists benefit from a complimentary RFIC registration. The top-three Best Student Papers will be announced during the RFIC Plenary Session on 4 June 2017 in Honolulu. Each winner will receive an honorarium and a plaque. This year's Best Student Paper Award finalists are:

Validation of a Functional Principle for a Broadband Millimeter-Wave Power Detection Structure in a Recent BiCMOS Technology
F. Trenz[1], R. Weigel[1], Dietmar Kissinger[2]
[1]FAU Erlangen-Nürnberg, Germany, [2]IHP, Germany
RMO1B-4 09:00

A Low-Noise Inductor-Less Fractional-N Sub-Sampling PLL with Multi-Ring Oscillator
Dongyi Liao, Ruixin Wang, Fa Foster Dai
Auburn University, USA
RMO1D-5 09:20

A 29-to-57GHz AM-PM Compensated Class-AB Power Amplifier for 5G Phased Arrays in 0.9V 28nm Bulk CMOS
Marco Vigilante, Patrick Reynaert
Katholieke Universiteit Leuven, Belgium
RMO2A-2 10:20

Accurate Modelling and Optimization of Inhomogeneous Substrate Related Losses in SPDT Switch IC Design for WLAN Applications
Fadoua Gacim, Philippe Descamps
CRISMAT, France
RMO2B-1 10:00

An Ultra-Wideband Harmonic Radiator with a Tuning Range of 62GHz (28.3%) at 220GHz
Ali Mostajeran, Ehsan Afshari
Cornell University, USA
RMO2D-5 11:20

A 335μW -72dBm Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets
Jaeho Im, Hun-Seok Kim, David D. Wentzloff
University of Michigan, USA
RMO3A-3 14:10

A Wideband Linear Direct Digital RF Modulator Using Harmonic Rejection and I/Q-Interleaving RF DACs
M. Mehrpoo, Mohsen Hashemi, Yiyu Shen, Rene van Leuken, Morteza S. Alavi, Leo C.N. de Vreede
Technische Universiteit Delft, The Netherlands
RMO3B-1 13:30

Sunday, 4 June 2017 **18:00–18:30** **Hilton Coral Ballroom**

SiGe BiCMOS Linear Modulator Drivers with 4.8-V_{pp} Differential Output Swing for 120-GBaud Applications
Robert J.A. Baker[1], James Hoffman[1], Peter Schvan[2], Sorin P. Voinigescu[1]
[1]University of Toronto, Canada, [2]Ciena, Canada
RMO4B-4 16:30

85–110GHz CMOS Tunable Nonreciprocal Transmission Line with 45dB Isolation for Wideband Transceivers
Chang Yang, Ping Gui
Southern Methodist University, USA
RMO4D-5 16:50

A Wideband Receiver Employing PWM-Based Harmonic Rejection Downconversion
Heechai Kang, Wei-Gi Ho, Vineet Singh, Ranjit Gharpurey
University of Texas at Austin, USA
RTU2A-5 11:20

Fully-Scalable 2D THz Radiating Array: A 42-Element Source in 130-nm SiGe with 80-μW Total Radiated Power at 1.01THz
Zhi Hu, Ruonan Han
MIT, USA
RTU2B-2 10:20

Student Paper Contest Eligibility: The student must have been a full time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must be the lead author of the paper and must present the paper at the Symposium. A memorandum will be automatically sent to the advisor to certify that the work was done by the student.

Judging Procedure: Student papers are reviewed and admitted to the conference in the same manner as all other conference papers. After the paper review process is completed, each technical program subcommittee recommends a maximum of two student papers as finalists. A student paper contest committee consisting of one representative from each subcommittee is then formed to review all the finalists and select the top three papers. Papers accepted for the competition are judged on content.

Li Lin
Student Programs Chair
Consultant

Plenary Speaker 1

Seizo Onoe
Chief Technology Officer and Executive Vice President, NTT DOCOMO

Deployment Realities of 5G

Abstract: 5G is stimulating our imagination and expectations for a new world that it may bring about by the year 2020. 5G is aimed at meeting a wide range of requirements such as further enhanced mobile broadband, massive connections and extremely long battery life for IoT, and reliable critical communications with low latency. Furthermore, it is highly expected to invent new business models and ecosystems across the industries. 5G discussion is gathering momentum and so heated that it is becoming a sort of boom, which is sometimes generating unintended misconceptions and myths. Today we as the whole industry are making various strong efforts for 5G, including accelerated standardization activities toward its early realization, forming of alliances, and experimental trials. In the talk, 5G technologies, schedule, lessons learnt from the past generations, and experimental trials and their results are discussed. The observed 5G myths are also described.

About Seizo Onoe

Seizo Onoe was named Chief Technology Officer and Executive Vice President and a Member of the Board of Directors in June 2012. Mr. Onoe became a Senior Vice President and General Manager of the R&D Strategy Department in June 2008. He was a Vice President and took positions as General Manager of the Radio Access Network related development departments from July 2002 to June 2008. He has been responsible for leading initiatives in the research and development of the analog cellular system, the digital cellular system, W-CDMA/ HSPA, LTE, LTE-Advanced and 5G. He is working on the research and development of radio access networks, core networks, consumer devices and cloud services. He has worked for NTT and NTT DOCOMO since 1982, acquiring more than 30 years of experience. Mr. Onoe has a master's degree in electronics from the Kyoto University Graduate School of Engineering.

Sunday, 4 June 2017 **18:30–19:00** **Hilton Coral Ballroom**

Plenary Speaker 2

Gabriel M. Rebeiz
Distinguished Professor, University of California, San Diego

RFIC/Silicon-Based Phased Arrays and Transceivers for 5G

Abstract: The 5G standard promises a revolution in wireless data transfer with Gbps links over kilometers at millimeter-wave frequencies. This is possible using high-gain antenna arrays resulting in "directive communications" between the base-station and the user, either in a phased-array or in a MIMO configuration. A key challenge is the construction of low-cost phased-arrays and wideband transceivers at 20–60 GHz. Prof. Rebeiz will present the progression of phased-array systems from defense-oriented applications to becoming the cornerstone of commercial 5G systems, and the role of silicon RFICs and advanced packaging to making this happen.

About Gabriel M. Rebeiz

Gabriel M. Rebeiz is one of the fathers of silicon RFIC phased-arrays. Starting in 2001 with his work at Boeing and MACOM, Prof. Rebeiz has taken this technology from its infancy to fully-deployed SATCOM phased-arrays, 60 GHz base-station phased-arrays, automotive radar phased-arrays, and now, 28 GHz 5G systems operating. He holds a Ph.D. in electrical engineering from the California Institute of Technology (Caltech), and is currently the Wireless Communications Industry Endowed Chair Professor at UCSD. He has graduated 85 Ph.D. students and post-docs, has more than 650 IEEE publications, and has received the Microwave Prize twice, both on phased-array topics. In 2016, Prof. Rebeiz was elected to the National Academy of Engineering for his contribution to low-cost phased arrays.

Sunday, 4 June 2017 **19:00–19:30** **Hilton Coral Ballroom**

Industry Showcase

Chair: Brian Floyd, North Carolina State University

The Industry Showcase Session, held concurrently with the plenary reception and the Interactive Forum, will highlight 10 selected papers submitted by authors from industry. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. The Best Industry Paper Award will be awarded to the author of one selected paper among these. This year's Industry Showcase papers are listed below.

A 28GHz CMOS Direct Conversion Transceiver with Packaged Antenna Arrays for 5G Cellular System
LG Electronics, Korea
Hong-Teuk Kim, Byoung-Sun Park, Seung-Min Oh, Seong-Sik Song, Jong-Moon Kim, So-Hyeong Kim, Tak-Su Moon, Seung-Yeon Kim, Ji-Young Chang, Sung-Woong Kim, Woo-Seong Kang, Seung-Yoon Jung, Geum-Young Tak, Jin-Kyoung Du, Yu-Suhk Suh, Yo-Chuol Ho
RMO1A-3 08:40

A 73GHz PA for 5G Phased Arrays in 14nm FinFET CMOS
Intel, USA
Steven Callender, Stefano Pellerano, Christopher Hull
RTU2D-5 11:20

A Fully Integrated 75–83GHz FMCW Synthesizer for Automotive Radar Applications with -97dBc/Hz Phase Noise at 1MHz Offset and 100GHz/mSec Maximal Chirp Rate
ON Semiconductor, Israel
Jakob Vovnoboy, Run Levinger, Nadav Mazor, Danny Elad
RMO1D-2 08:20

A 200μm × 200μm × 100μm, 63nW, 2.4GHz Injectable Fully-Monolithic Wireless Bio-Sensing System
[1]Verily, USA, [2]Google, USA, [3]Cobalt Robotics, USA
S. O'Driscoll[1], S. Korhummel[1], P. Cong[1], Y. Zou[1], K. Sankaragomathi[1], J. Zhu[2], T. Deyle[3], A. Dastgheib[1], B. Lu[1], M. Tierney[1], J. Shao[1], C. Gutierrez[1], S. Jones[1], H. Yao[1]
RMO4B-3 16:10

95μW 802.11g/n Compliant Fully-Integrated Wake-Up Receiver with -72dBm Sensitivity in 14nm FinFET CMOS
[1]Intel, USA, [2]Carnegie Mellon University, USA
Erkan Alpman[1], Ahmad Khairi[2], Minyoung Park[1], V. Srinivasa Somayazulu[1], Jeffrey R. Foerster[1], Ashoke Ravi[1], Stefano Pellerano[1]
RMO3A-2 13:50

A 4mW-RX 7mW-TX IEEE 802.11ah Fully-Integrated RF Transceiver
Holst Centre, The Netherlands
Ao Ba, Kia Salimi, Paul Mateman, Pepijn Boer, Johan van den Heuvel, Jordy Gloudemans, Johan Dijkhuis, Ming Ding, Yao-Hong Liu, Christian Bachmann, Guido Dolmans, Kathleen Philips
RMO4A-2 15:50

Sunday, 4 June 2017 **19:30–21:30** **Hilton Coral Lounge**

A Wideband SiGe BiCMOS Transceiver Chip-Set for High-Performance Microwave Links in the 5.6–43.5GHz Range

[1]Nokia Bell Labs, USA, [2]Nokia, France

Y. Baeyens[1], S. Shahramian[1], B. Jalali[1], P. Roux[1], J. Weiner[1], A. Singh[1], M. Moretto[2], P. Boutet[2], P. Lopez[2]

RTU2B-3 10:40

A 12-b, 1-GS/s 6.1mW Current-Steering DAC in 14nm FinFET with 80dB SFDR for 2G/3G/4G Cellular Application

Samsung, Korea

Jaekwon Kim, Woojin Jang, Yanghun Lee, Seunghyun Oh, Jongwoo Lee, Thomas Byunghak Cho

RMO4B-1 15:30

RF-pFET in Fully Depleted SOI Demonstrates 420GHz F_T

[1]GLOBALFOUNDRIES, USA, [2]GLOBALFOUNDRIES, Singapore, [3]GLOBALFOUNDRIES, Germany, [4]CEA-LETI, France

Josef Watts[1], Kumaran Sundaram[2], Kok Wai Johnny Chew[2], Steffen Lehmann[3], Shih Ni Ong[2], Wai Heng Chow[2], Lye Hock Chan[2], Jerome Mazurier[4], Christoph Schwan[3], Yogadissen Andee[4], Thomas Feudel[3], Luca Pirro[4], Elke Erben[3], Edward Nowak[1], Elliot Smith[3], El Mehdi Bazizi[3], Thorsten Kammler[3], Richard Taylor III[1], Bryan Rice[3], David Harame[3]

RMO1B-3 08:40

A Precision 140MHz Relaxation Oscillator in 40nm CMOS with 28ppm/°C Frequency Stability for Automotive SoC Applications

Infineon Technologies, Austria

Dmytro Cherniak, Roberto Nonis, Fabio Padovan

RSUIF-15 19:30

Sunday 4th June 2017
19:30–21:30
Hilton Coral Lounge
Session RSUIF: Interactive Forum
Chair: Waleed Khalil, Ohio State University
Co-Chair: Jennifer Kitchen, Arizona State University

RSUIF-1 19:30
An FTNC Receiver with +32.5dBm Effective OB-IIP3 Using Baseband IM3 Cancellation

Yudong Zhang, Jianxun Zhu, Peter R. Kinget; Columbia University, USA

Abstract: An IM3 cancellation technique is proposed and implemented in a 65nm CMOS 0.5–2.5GHz FTNC (frequency translational noise-cancelling) receiver with a wideband auxiliary path which also offers wideband interferer awareness. It achieves 8.8MHz BB BW, 40dB conversion gain, 3.3dB NF, +5dBm OB-IIP3, and -6.5dBm OB-B1dB without IM3 cancellation while consuming 36mW at 1.2V. Using IM3 cancellation, the equivalent OB-IIP3 for two-tone interferers is up to +32.5dBm with an extra 34mW of power consumption. For two -15dBm modulated interferers 18.8dB cancellation is demonstrated over 10MHz.

RSUIF-2 19:30
Envelope Time-Domain Characterizations to Assess In-Band Linearity Performances of Pre-Matched MASMOS Power Amplifier

F. Simbélie[1], V. Gillet[1], S. Laurent[1], P. Médrel[1], Y. Creveuil[2], M. Régis[2], M. Prigent[1], R. Quéré[1]; [1]XLIM, France, [2]ACCO Semiconductor, France

Abstract: This paper reports on an innovative in-band linearity performances characterization dedicated to nonlinear RF power amplifiers, here, pre-matched MASMOS power amplifier. It consists of a generic multi-tones test signal that emulates the statistical properties of the applicative signal and allows signal and intermodulation output component separation for in-band C/I (signal to intermodulation power ratio) calculation. Two types of tests are successively discussed. The first one are standards VSA-based measurement performed with a 16-QAM and 256-QAM modulated signal. Secondly, a specific multi-tones signal is presented and compared with the reference VSA measurement. It is shown that the proposed generic stimulus can be used to evaluate, in specific conditions, the in-band interferences that degrade the Error Vector Magnitude (EVM) in the case of a nonlinear link.

RSUIF-3 19:30

Improving the Linearity of Wideband Receiver Systems by Component IM3 Phasor Manipulation

Gabor Varga, Fabian Speicher, Arun Ashok, Iyappan Subbiah, Moritz Schrey, Ralf Wunderlich, Stefan Heinen; RWTH Aachen University, Germany

Abstract: A linearity improvement technique for receiver systems is presented and verified on a 130nm CMOS high-IF upconverter with 470–790MHz input and 2.4–2.6 GHz output frequency range, enabling WLAN and LTE transceivers to be used as TV White Space Devices. The upconverter reaches a stable IIP_3 of 15 dBm, NF of 8 dB and Gain of 7 dB. A linearized LNA and mixer are used as a composite architecture to combine low NF with, even though, high IIP_3. Instead of further maximizing the linearity of the components, the overall performance is optimized on the system level by manipulation and complementary exploitation of the remaining third order intermodulation products of the components.

RSUIF-4 19:30

A Fully-Integrated SOI CMOS Complex-Impedance Detector for Matching Network Tuning in LTE Power Amplifier

D. Nicolas[1], A. Serhan[1], A. Giry[1], T. Parra[2], E. Mercier[1]; [1]CEA-LETI, France, [2]LAAS, France

Abstract: This paper describes a wide dynamic-range and accurate complex-impedance detector for adaptive power amplifier load tuning systems. The detector IC, fabricated in a 130 nm SOI technology, consumes 7 mA under 2.5 V supply voltage. It can handle LTE signals with an input power from 0 dBm up to 40 dBm thanks to its variable attenuator system. System level measurements show that the detector has a very good accuracy in sensing the mismatched load impedance value in the VSWR region from 2:1 to 6:1.

RSUIF-5 19:30

V-Band Flip-Chip pHEMT Balanced Power Amplifier with CPWG-MS-CPWG Topology and CPWG Lange Couplers

Wei-Ling Chang[1], Jen-Yi Su[1], Chinchun Meng[1], Chia-Hung Chang[1], Guo-Wei Huang[2]; [1]National Chiao Tung University, Taiwan, [2]National Nano Device Laboratories, Taiwan

Abstract: A V-band balanced two-stage power amplifier MMICs with Lange couplers is demonstrated using 0.15 μm GaAs pHEMT technology in this paper. A CPWG-MS-CPWG topology with via holes at the transistors as the transition between coplanar waveguide with backside ground (CPWG) and microstrip (MS) is employed for the two-stage amplifier. CPWG is applied to realize the flip-chip transition interface for both input and output ports of the amplifier and interstage MS matching has the advantage of small size. The structure parameters of the CPWG Lange coupler and matching network are designed and optimized for power combining. Finally, a 60-GHz balanced two-stage power amplifier using a CPWG-MS-CPWG structure delivers the small signal gain of 18 dB, OP_{1dB} of 12 dBm and P_{sat} of 15 dBm.

RSUIF-6 19:30

Multi-Standard 5Gbps to 28.2Gbps Adaptive, Single Voltage SerDes Transceiver with Analog FIR and 2-Tap Unrolled DFE in 28nm CMOS

Mohammad Mahani[1], Rod Zavari[1], Su-Tarn Lim[1], David Hong[1], Karl Scheffer[1], Peter Graumann[1], Hans Ransijn[2], Tomas Dusatko[3], Stanley Ho[3], Philip Snyder[2], Jomy Joy[4], Suresh Nalluri[4], Tony Zortea[2]; [1]Microsemi, Canada, [2]Multiphy, USA, [3]Inphi, Canada, [4]Texas Instruments, India

Abstract: A low-power multi-standard transceiver in CMOS 28 nm is presented. The transceiver can be configured to cover the range from 5 Gbps to 28.2 Gbps. Both transmitter and receiver use a supply of 0.92 V. Transmitter uses a 3-tap Finite Impulse Response (FIR) filter and receiver uses a 3-tap analog FIR and 2-tap unrolled Decision Feedback Equalizer (DFE). The entire transceiver uses single level 0.92 V power supply with an analog power consumption of 242.3 mW at 28.2 Gbps. Total area of the transceiver including the Clock Synthesis Unit (CSU) is 0.88 mm^2.

RSUIF-7 19:30

A Harmonic-Selective Wireless Full-Band-Capture Receiver with Digital Harmonic Rejection Calibration

Hao Wu, David Murphy, Hooman Darabi; Broadcom, USA

Abstract: A 30mW Full-Band-Capture receiver based on harmonic selection is presented. The prototype receiver employs a 32-phase non-overlapping LO, and is capable of simultaneously receiving multiple wireless signals arbitrarily located between 600MHz and 3GHz. The receiver achieves 2.4 to 5dB NF and tolerates more than -10dBm out-of-band blockers. A digital harmonic rejection calibration is also proposed to overcome phase and amplitude mismatches in the 32-phase LO and down-conversion paths.

RSUIF-8 19:30

A 40GHz PLL with -92.5dBc/Hz In-Band Phase Noise and 104fs-RMS-Jitter

Ying Chen[1], Louis Praamsma[1], Nikola Ivanisevic[2], Domine M.W. Leenaerts[1]; [1]NXP Semiconductors, The Netherlands, [2]KTH, Sweden

Abstract: This paper demonstrates a fully integrated low phase noise PLL at 40GHz, implemented in a 0.25-μm SiGe:C BiCMOS technology. An in-band phase noise improvement of 1.4dB to 3.2dB is measured across the locking range using the proposed double-gain PFD. The PLL achieves an in-band phase noise <-92.5dBc/Hz and an integrated RMS jitter of 104fs, a 25% improvement over conventional PFD. The reference spurs are <-73dBc across the whole locking range.

RSUIF-9 19:30

A High-Efficiency Linear Power Amplifier for 28GHz Mobile Communications in 40nm CMOS

Yang Zhang, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a high-efficiency, linear power amplifier (PA) for 28GHz mobile communications in 40nm CMOS technology. The design and layout are optimized for high linearity while maintaining high gain and output power. A capacitance neutralized differential pair with source degeneration inductor for linearity enhancement is discussed. The inductive degeneration technique greatly increases the optimal load impedance, which enables a low loss parallel power combining. The complete PA achieves a measured saturated output power of 18.1dBm with 41.5% power-added efficiency (PAE). With 6 Gb/s QAM-64 signals, the proposed PA achieves an average output power of 8.4dBm and 8.8% PAE, with -25 dBc EVM. All measurements are performed with a fixed bias condition.

RSUIF-10 19:30

An Analysis of Phase Noise Requirements for Ultra-Low-Power FSK Radios

Xing Chen, Hun-Seok Kim, David D. Wentzloff; University of Michigan, USA

Abstract: This paper presents an analysis of the influence of phase noise (PN) on FSK radios and derives the total PN requirement for a low power FSK link based on Bit Error Rate (BER) performance. A simple noise model is built, including phase noise and white noise from the AWGN channel, to analyze its influence on the BER of an ULP FSK RX. It shows that to achieve a 10^{-4} BER, the minimum PN requirement can be more relaxed than current synthesizer designs. The trade-off between PN, data rate, and frequency deviation of FSK modulation is also studied, showing how bandwidth can be traded for relaxed PN while maintaining the same spectral efficiency (bits/Hz). This result implies we could migrate from LC-VCOs to ring oscillators with a simple PLL for wireless communication using FSK and significantly reduce the power of radios. A chip was fabricated to test the accuracy of the model at different PN levels, showing agreement among theoretical analysis, simulations, and measurements.

RSUIF-11 19:30

A Ka-Band 4-Ch Bi-Directional CMOS T/R Chipset for 5G Beamforming System

JangHoon Han, JinHyun Kim, Jeongsoo Park, JeongGeun Kim; Kwangwoon University, Korea

Abstract: This paper presents a Ka-band 4-channel bi-directional T/R chipset in 65 nm CMOS technology for 5G beamforming system. The proposed T/R chipset can provide bi-directional operation with moderate gain and dual polarization. Each channel consists of bi-directional gain blocks, a 5-bit step attenuator and a 5-bit phase shifter including tuning bits. The phase and attenuation coverage are 348° with the LSB of 11.25° and 31 dB with the LSB of 1 dB, respectively. The gain of 13 dB (Tx mode) and 6 dB (Rx mode) are achieved at 28 GHz including the 4-way power divider/combiner.

RSUIF-12 19:30

A 32GHz 20dBm-P_{SAT} Transformer-Based Doherty Power Amplifier for Multi-Gb/s 5G Applications in 28nm Bulk CMOS

Paramartha Indirayanti, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a 32 GHz transformer-based Doherty power amplifier (PA) in a 28 nm bulk CMOS process. There are two techniques proposed: linearization by means of AM-PM and AM-AM compensation of the class AB and the class C amplifiers; and parallel-series-parallel power power combiner, wherein a current-mode parallel combiner complements the Doherty's voltage-mode series combiner to boost the output power. A saturated output power (P_{SAT}) of 19.8 dBm and an OP1dB of 16 dBm are accomplished from 1V supply while supporting 15 Gb/s 64-QAM amplification at 11.7 dBm average output power. The chip achieves 21% PAE at P_{SAT} and occupies 0.59 mm^2 active area.

RSUIF-13 19:30

A 10–40GHz Frequency Quadrupler Source with Switchable Bandpass Filters and >30dBc Harmonic Rejection

Hyunchul Chung, Qian Ma, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 10–40 GHz wideband frequency quadrupler in GF8HP 0.13 μm SiGe BiCMOS process. Three bands (low-, mid-, and high-band) are implemented on-chip for wideband operation. An on-chip 4-pole switchable elliptic bandpass filter is also used to result in greatly improved harmonic rejection ratio (HRR). The measured worstcase HRR is 32–48 dBc at 11–40 GHz with an output power of +1 to -8 dBm for P_{in} = 1 dBm (25–32 dB at 10–11 GHz). The output power and HRR remain nearly constant with P_{in} of 0–7 dBm. The chip is 3.96 mm^2 and consumes 60 mW in low- and mid-band modes, and 84 mW for the high-band mode. To our knowledge, this wideband frequency quadrupler represents state-of-the-art performance in terms of bandwidth, HRR and P_{out}. Application areas are wideband low-harmonic content sources for wideband measurement systems, high-resolution imaging systems and digital beamforming phased-arrays.

RSUIF-14 19:30

Joint TX and Feedback RX IQ Mismatch Compensation for Integrated Direct Conversion Transmitters

Hunsoo Choo, Charles Sestok, Xiaoxi Zhang, Nikolaus Klemmer; Texas Instruments, USA

Abstract: The direct conversion (DC) architecture has been adopted for wireless base-station transceivers due to its cost and area efficiency. The shortcomings of DC transceivers need to be overcome to meet their high performance requirements. In-phase (I) and quadrature phase (Q) mismatch is one of most significant impairments. This paper presents an integrated, on-line mismatch compensation system which calibrates frequency-dependent transmitter (TX) and feedback receiver (FBRX) IQ mismatches using the digital TX signal as a reference. The proposed method was fabricated in 45nm CMOS technology. Measurements show 60 dBc TX ACPR for 20MHz LTE low-IF signals. TX EVM of 0.8% is achieved with 20MHz zero-IF LTE signals.

RSUIF-15 19:30

A Precision 140MHz Relaxation Oscillator in 40nm CMOS with 28ppm/°C Frequency Stability for Automotive SoC Applications

Dmytro Cherniak, Roberto Nonis, Fabio Padovan; Infineon Technologies, Austria

Abstract: The need for high-frequency, low-power, wide temperature range, precision on-chip reference clock generation makes relaxation oscillator topology an attractive solution for various automotive applications. This paper presents for the first time a 140MHz relaxation oscillator with robust-against-process-variation temperature compensation scheme. The high-frequency relaxation oscillator achieves 28 ppm/°C frequency stability over the automotive temperature range from -40 to 175°C. The circuit is fabricated in 40nm CMOS technology, occupies 0.009mm^2 and consumes 294µW from 1.2V supply.

Monday 5th June 2017
08:00–09:20
HCC Room 312
Session RMO1A: 28GHz Phased-Array Transceivers for 5G Systems
Chair: Stefano Pellerano, Intel Corporation
Co-Chair: Hossein Hashemi, University of Southern California

RMO1A-1 08:00
Bi-Directional Flip-Chip 28GHz Phased-Array Core-Chip in 45nm CMOS SOI for High-Efficiency High-Linearity 5G Systems
Umut Kodak, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 0 mW two-channel 28 GHz bi-directional phased-array chip packaged using flip-chip interconnects in 45nm CMOS SOI. The design alternates switched-LC phase shifters with switched attenuators to result in 5-bit phase control with an rms gain and phase error <0.8 dB and 5°, respectively at 25–33 GHz. In the RX mode, the measured gain is -10 dB and the NF is 10 dB with an input P_{1dB} of 5 dBm. In the TX mode, the measured output P_{1dB} is -2 dBm. This work presents an efficient solution for the construction of high-linearity and high-power phased-array base-stations by combining GaAs front-ends with a passive silicon core chip.

RMO1A-2 08:20
A 28-GHz Phased-Array Transceiver with Series-Fed Dual-Vector Distributed Beamforming
Yi-Shin Yeh[1], Ed Balboni[2], Brian Floyd[1]; [1]North Carolina State University, USA, [2]Analog Devices, USA

Abstract: This paper presents a 28-GHz four-element phased-array transceiver in 130-nm SiGe BiCMOS technology for 5G cellular application. The array employs scalar-only weighting functions within each front-end and a global quadrature function, enabling small footprint for each element. A dual-vector series feed network also reduces size of the array. Measurements show that each receive front-end achieves 8.7 to 11.5 dB gain, 4.5 to 6.9 dB noise figure, -25.4 to -18.4 dBm input 1-dB compression point, and < 0.5dB/2.1° RMS gain/phase error at 24 to 28 GHz. Each transmit front-end achieves 9.4 to 14.3 dB gain, 5.5 to 10.6 dBm output 1-dB compression point, and < 0.4dB/4.2° RMS gain/phase error at 24 to 28 GHz. The four-element transceiver array occupies 2.9 mm^2 area and consumes 1.08 W in transmit mode and 0.68 W in receive mode.

RMO1A-3 08:40

A 28GHz CMOS Direct Conversion Transceiver with Packaged Antenna Arrays for 5G Cellular System

Hong-Teuk Kim, Byoung-Sun Park, Seung-Min Oh, Seong-Sik Song, Jong-Moon Kim, So-Hyeong Kim, Tak-Su Moon, Seung-Yeon Kim, Ji-Young Chang, Sung-Woong Kim, Woo-Seong Kang, Seung-Yoon Jung, Geum-Young Tak, Jin-Kyoung Du, Yu-Suhk Suh, Yo-Chuol Ho; LG Electronics, Korea

Abstract: This paper describes a 28GHz CMOS direct conversion transceiver with packaged 2×4 patch antenna arrays for 5G communication. Test results show good RF performances of Rx NF 6.7dB, Maximum Tx EIRP 31.5dBm (1PA P_{out_sat} =10.5dBm), LO integrated phase noise -37.8dBc (0.67°), Rx/Tx EVM around 2.2% (-33.1dB) at mid RF power, and well-fitted beam control capability.

RMO1A-4 09:00

An Ultra Low-Cost 32-Element 28GHz Phased-Array Transceiver with 41dBm EIRP and 1.0–1.6Gbps 16-QAM Link at 300 Meters

Kerim Kibaroglu, Mustafa Sayginer, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a 32-element phased-array architecture suitable for fifth-generation (5G) communication links. A 28–32 GHz silicon core chip is designed with 4 transmit/receive elements each with 14 dB gain control, 6-bit phase control, 4.6 dB measured noise figure (NF) in the RX mode and 10 dBm output 1 dB compression point (OP1dB) in the TX mode. Eight of these chips are flipped on a low-cost printed circuit board (PCB) with integrated antennas and Wilkinson combiners. The 32-element array has a measured EIRP of 41 dBm at P1dB, can scan to ±20° and ±50° in E- and H-planes, and consumes 4.2 W and 6.4 W in RX and TX modes, respectively. The array is used in a 300 meter wireless link and achieves a data rate of 1.0–1.6 Gbps at 16-QAM for all scan angles with <12% EVM. To our knowledge, this represents state-of-the art in 28 GHz phased-arrays in terms of chip performance and integration level.

Monday 5th June 2017
08:00–09:20
HCC Room 313A
Session RMO1B: Advanced Technologies for Optical, Millimeter-Wave and Radio Frequency Applications

Chair: Freek van Straten, Ampleon
Co-Chair: Richard Chan, QORVO

RMO1B-1 08:00

Sub-THz Source Integrated in Low-Cost Silicon Photonic Technology Targeting 40Gb/s Wireless Links

Elsa Lacombe[1], Frederic Gianesello[1], Cedric Durand[1], Guillaume Ducournau[2], Cyril Luxey[3], Daniel Gloria[1]; [1]STMicroelectronics, France, [2]IEMN, France, [3]EpOC-UNS, France

Abstract: Following the race for transmitting/receiving at higher data rate, we can observe intensive development of millimeter-wave wireless systems in low-cost CMOS technology. Data rates above 10 Gb/s are now targeted in order to address the data traffic bottleneck of backhaul links for the 5G wireless network. To do so, antenna-systems operating at sub-THz frequencies show great potential, leveraging high-performance photonic technology. This paper presents a sub-THz source based on a SiGe PIN photodiode integrated in low-cost Silicon Photonic technology. Using a laser beat-note, the photodiode delivers an output power ranging from -20 dBm to -29 dBm between 125 and 325 GHz. Leveraging this wide operating band, data rate exceeding 40 Gb/s can be targeted.

RMO1B-2 08:20

RF NMOS Switch with Dedicated Sinks for Reduced Leakage Current

M.S.M. Al-Sa'di, J.J.T.M. Donkers, P.H.C. Magnée, I. Brunets, J.W. Slotboom; NXP Semiconductors, The Netherlands

Abstract: In this paper we introduce a method to significantly reduce the substrate leakage current in an RF NMOS switch device without degrading the device figure-of-merit ($R_{on} \times C_{off}$), and with no increase in device complexity. This is based on modifying the structure layout, and introducing dedicated sinks. These sinks prevent the substrate's minority carriers from reaching the source/drain regions, thereby removing it from the signal path. In addition, this approach allows independent tuning of two parameters, leakage and $R_{on} \times C_{off}$ figure-of-merit.

RMO1B-3 08:40

RF-pFET in Fully Depleted SOI Demonstrates 420GHz F_T

Josef Watts[1], Kumaran Sundaram[2], Kok Wai Johnny Chew[2], Steffen Lehmann[3], Shih Ni Ong[2], Wai Heng Chow[2], Lye Hock Chan[2], Jerome Mazurier[4], Christoph Schwan[3], Yogadissen Andee[4], Thomas Feudel[3], Luca Pirro[4], Elke Erben[3], Edward Nowak[1], Elliot Smith[3], El Mehdi Bazizi[3], Thorsten Kammler[3], Richard Taylor III[1], Bryan Rice[3], David Harame[3]; [1]GLOBALFOUNDRIES, USA, [2]GLOBALFOUNDRIES, Singapore, [3]GLOBALFOUNDRIES, Germany, [4]CEA-LETI, France

Abstract: We report an experimental pFET with 420GHz f_T, which to the best of our knowledge is the highest value reported for a silicon pFET. The transconductance is 1800μS/μm. The technology is fully depleted silicon on insulator (FDSOI) with the pFET channel formed by SiGe condensation. This outstanding performance is achieved by a combination of layout and process optimization which minimizes capacitance and maximizes compressive strain on the channel. The technology features a high-k metal gate and short gate length (20nm drawn) in addition to the SiGe channel for high mobility.

RMO1B-4 09:00

Validation of a Functional Principle for a Broadband Millimeter-Wave Power Detection Structure in a Recent BiCMOS Technology

F. Trenz[1], R. Weigel[1], Dietmar Kissinger[2]; [1]FAU Erlangen-Nürnberg, Germany, [2]IHP, Germany

Abstract: In this paper, a functional principle for a broadband thermal detector suited for a monolithical integration is shown. Two tantalum load resistors are heated by an input signal, while the temperature at a fixed distance is recorded on chip with a differential temperature sensing bridge. An integrated differential to single-ended stage amplifies the bridges differential voltage and provides an output voltage proportional to the input power of the detector. The thermal resistance and capacitance between the load resistor and the sensing cell act as a low pass filter in the electrical regime. Based on this concept, a detector chip has been designed, which has been analyzed in thermal simulations. The realized detector has been characterized on-chip and bonded to a microwave substrate for a system performance estimation. Its input impedance is tuned to 50 Ohms and measured matching is better than -15 dB from 150MHz to 110GHz. With a low supply voltage of 1.5V and its active area of around 80×36μm², the detector is suitable for an integrated power measurement solution.

Monday 5th June 2017
08:00–09:40
HCC Room 313B
Session RMO1D: High-Performance Frequency Synthesizers
Chair: Jeyanandh Paramesh, Carnegie Mellon University
Co-Chair: Jaber Khoja, Rockwell Collins

RMO1D-1 08:00
A 59-to-276GHz CMOS Signal Generation for Rotational Spectroscopy
Xiaolong Liu[1], Yue Chao[2], Howard C. Luong[1]; [1]HKUST, China, [2]Qualcomm, USA

Abstract: An ultra-wideband sub-THz signal generation system is proposed for rotational spectroscopy employing a magnetic-tuning varactor-less quad-band voltage-controlled oscillator (QB-VCO), a locking-range-enhanced dual-mode injection-locked frequency divider (DM-ILFD), a power-efficient injection-locked oscillator (ILO) as a driver, and sub-THz mixers with frequency multipliers for frequency extension. Implemented in a 65-nm CMOS process and consuming 54 mW, the prototype measures an ultra-wide frequency tuning range from 58.8 to 275.6 GHz with 10-MHz offset phase noise from -115.8 dBc/Hz to -89.2 dBc/Hz while occupying a core area of 0.9 mm × 0.72 mm.

RMO1D-2 08:20
A Fully Integrated 75–83GHz FMCW Synthesizer for Automotive Radar Applications with -97dBc/Hz Phase Noise at 1MHz Offset and 100GHz/mSec Maximal Chirp Rate
Jakob Vovnoboy, Run Levinger, Nadav Mazor, Danny Elad; ON Semiconductor, Israel

Abstract: We present a SiGe BiCMOS fully integrated 75–83 GHz FMCW synthesizer for automotive radar applications. Performance enhancements were achieved by utilizing the bulk-drain parasitic variable capacitance of P-channel transistors, embedded in a gm-boosted Colpitts VCO, for frequency control. This mechanism was incorporated in a dual path PLL, providing low loop bandwidth variation over the whole output frequency range, -97 dBc/Hz phase noise at 1 MHz offset and maximum chirp rate of 100 GHz/mSec.

RMO1D-3 08:40
A Subharmonically Injection-Locked PLL with 130fs RMS Jitter at 24GHz Using Synchronous Reference Pulse Injection from Nonlinear VCO Envelope Feedback
Dongseok Shin, Shinwoong Park, Sanjay Raman, Kwang-Jin Koh; Virginia Tech, USA

Abstract: This paper presents an 8 GHz subharmonically injection-locked PLL (SILPLL), which is cascaded with a 24 GHz quadrature injection-locked oscillator in 130 nm CMOS. The proposed SILPLL adopts an envelope-detection based injection-timing calibration for synchronous reference

pulse injection to a VCO. With one of the largest frequency division ratios (N=80) reported so far, the SILPLL exhibits 124 fs and 130 fs RMS jitter at 8 GHz and 24 GHz, respectively, with <-49 dBc reference spur. The measured phase noise at 1 MHz offset is -114 dBc/Hz at 8 GHz and -104 dBc/Hz at 24 GHz.

RMO1D-4 09:00

A Highly Reconfigurable RF-DPLL Phase Modulator for Polar Transmitters in Multi-Band/Multi-Standard Cellular RFICs

T. Buckel[1], T. Mayer[2], T. Bauernfeind[2], S. Tertinek[2], C. Wicpalek[2], A. Springer[1], R. Weigel[3], T. Ussmueller[4]; [1]Johannes Kepler Universität Linz, Austria, [2]DMCE, Austria, [3]FAU Erlangen-Nürnberg, Germany, [4]Universität Innsbruck, Austria

Abstract: A multirate, fractional-N RF digital phase-locked loop (DPLL) phase modulator implementation for polar transmitter supporting cellular communication standards up to 4G LTE-A is demonstrated for the first time. The RF-DPLL integrates LC-tank-based digital-controlled oscillator (DCO) cores with ΣΔ-noise shaping and fractional sample rate conversion to account for a broad range of frequency bands and spectral emission requirements. A two-point modulation with different sampling rates and signal scaling is applied to optimize the system for operation in narrow-band and wide-band phase modulation. DCO predistortion and DCO gain estimation is implemented to achieve sufficiently low in-band distortion. Measurement results of the RF-DPLL system as part of a polar transmitter implemented in 28-nm CMOS are shown, fulfilling 3GPP specifications for LTE-A uplink.

RMO1D-5 09:20

A Low-Noise Inductor-Less Fractional-N Sub-Sampling PLL with Multi-Ring Oscillator

Dongyi Liao, Ruixin Wang, Fa Foster Dai; Auburn University, USA

Abstract: In this paper, a compact inductor-less PLL using multiple coupled rings oscillator is presented. Sub-sampling technique with soft loop gain switching is applied to reduce the in-band phase noise. As a result, the loop bandwidth can be widened, which suppresses the phase noise from ring oscillator as well. Fractional-N mode is implemented by utilizing the multiple phase outputs inherently generated by the ring VCO. Using multiple rings instead of one allows generating more phases for finer frequency resolution without decreasing oscillation frequency. The coupled multi-ring oscillator with proper phase shift also achieves reduced phase noise comparing to their single-ring counterpart. The PLL was implemented in a 0.13μm CMOS technology, consuming 19 mW from a 1.3 V power supply. The measured largest in-band fractional spur at 2.08 MHz is -42 dBc. The measured integrated jitters were 571 fs and 690 fs around 1.2GHz output in integer mode and fractional mode respectively, achieving a FoM of -230 dB.

Monday 5th June 2017
10:00–11:20
HCC Room 312
Session RMO2A: Radio Building Blocks for 5G Systems
Chair: Walid Ali-Ahmad, Qualcomm
Co-Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

RMO2A-1 10:00
A 25–30GHz 8-Antenna 2-Stream Hybrid Beamforming Receiver for MIMO Communication

Susnata Mondal, Rahul Singh, Ahmed I. Hussein, Jeyanandh Paramesh; Carnegie Mellon University, USA

Abstract: This paper presents a 65 nm CMOS 25–30 GHz hybrid beamforming receiver with eight antenna inputs and two baseband output streams. The receiver uses the Cartesian-Combining architecture, which is introduced for two baseband streams. Each antenna signal is complex-weighted independently and combined with weighted signals from other antennas prior to downconversion. Each RF-domain complex weight is realized using a pair of 5-bit digitally controlled VGA's. The receiver achieves 34 dB conversion gain, 7.3 dB minimum noise figure, and 5 GHz of RF bandwidth while consuming only 27.5 mW power per antenna element (340 mW for the entire receiver). Two-element Cartesian-combining achieves a peak-to-null ratio of 20 dB. Use of mostly active phase shifting and combining approach made the design ultra-compact with 3.86 mm^2 core area for entire 8-element 2-stream receiver.

RMO2A-2 10:20
A 29-to-57GHz AM-PM Compensated Class-AB Power Amplifier for 5G Phased Arrays in 0.9V 28nm Bulk CMOS

Marco Vigilante, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a 29-to-57GHz (65% BW) AM-PM compensated class-AB power amplifier tailored for 5G phased arrays. Designed in 0.9V 28nm CMOS without RF thick top metal, the PA achieves a P_{sat}=15.1dBm±1.6dB and |AM-PM|<1° from 29-to-57GHz, with a peak PAE of 24.2%. Techniques are studied to realize the required load impedance and distortion cancellation over the wide band of operation, while allowing 2-way power combining to further increase the delivered POUT. The very low AM-PM distortion of the realized PA enables up to 10.1, 8.9, 5.9dBm average P_{OUT} while amplifying a 1.5, 3, 6Gb/s 64-QAM respectively at 34GHz with EVM/ACPR better than -25dBc/-30dBc, without any digital pre-distortion.

RMO2A-3 10:40

A Quad Channel 11-bit 1GS/s 40mW Collaborative ADC Based Enabling Digital Beamforming for 5G Wireless

Aurangozeb[1], Farshid Aryanfar[2], Masum Hossain[1]; [1]University of Alberta, Canada, [2]Straight Path Communications, USA

Abstract: A 4×11-bit 1 GS/s 40 mW Collaborative ADC in 65nm CMOS is presented for a 4-Ch MIMO receiver. It utilizes the correlation information between channels to perform energy efficient digitization of received signals. By utilizing 8 SAR units each with 6-bit level of resolution, four level of ADC resolutions (11, 9, 6, and 6-bit), is achieved dynamically for optimal performance. This collaborative ADC in compare to all-11 and all-9 bit has an area and power reduction of 50% and 41% respectively with only 10% degradation in overall SNDR.

RMO2A-4 11:00

A 16-Element 4-Beam 1GHz-IF 100MHz-Bandwidth Interleaved Bit-Stream Digital Beamformer in 40nm CMOS

Sunmin Jang[1], Jaehun Jeong[2], Rundao Lu[1], Michael P. Flynn[1]; [1]University of Michigan, USA, [2]Broadcom, USA

Abstract: This paper introduces a 16 element, 1GHz IF input, digital beamformer (DBF) that generates 4 independent simultaneous beams, with 100MHz bandwidth. Although DBF has several advantages over analog beamforming, including higher accuracy and multiple beam generation, application of on-chip DBF has been limited due to high power consumption and large die area. The proposed architecture addresses these issues by combining efficient Continuous-Time Band-Pass Delta Sigma Modulators (CTBPDSMs) with Interleaved Bit-Stream Processing (IL-BSP). IL-BSP saves 80% power and 80% area compared to a conventional DSP approach. The overall 16 element array has a measured 58.5dB SNDR and a 59.6dB SNR over a 100MHz bandwidth (11.2dB array gain). Thanks to the IL-BSP approach, the measured beam patterns are near ideal.

Monday 5th June 2017
10:00–11:40
HCC Room 313A
Session RMO2B: Modeling and Characterization for Emerging High Frequency and RF Front-End Applications

Chair: Tzung-Yin Lee, Skyworks Solutions
Co-Chair: Edward Preisler, TowerJazz

RMO2B-1 10:00

Accurate Modelling and Optimization of Inhomogeneous Substrate Related Losses in SPDT Switch IC Design for WLAN Applications

Fadoua Gacim, Philippe Descamps; CRISMAT, France

Abstract: This paper teaches the way to achieve an optimum substrate isolation in RF switch design thanks to Deep Trenches Isolation (DTI). The role of Deep Trench Isolation in substrate coupling around active blocks is analysed in link to its ability to break the conductive buried layers in the substrate. Then, an accurate modelling approach based on quasi-static approach developed for inhomogeneous substrate is investigated. The efficiency of this methodology is first demonstrated thanks to a comparison with a standard numerical method based on FEM (Finite Element Method). Then, experiments data are provided to support this theoretical analysis. The methodology is fully integrated in a commercial design flow and offers a perfect trade-off between accuracy and run time simulation. From available test data on single device and a full SP3T, a correlation better than 0.1dB is obtained between simulation and measurement up to 8 GHz.

RMO2B-2 10:20

A Simplified CMOS FET Model Using Surface Potential Equations for Inter-Modulation Simulations of Passive-Mixer-Like Circuits

Mahmood Baraani Dastjerdi, Harish Krishnaswamy; Columbia University, USA

Abstract: In many CMOS analog/RF circuits, such as passive mixers or N-path filters, the transistor operates as a switch. Switching circuits often experience source-drain reversal, and most transistor models exhibit discontinuities in second and higher-order derivatives of the drain current around zero drain-source bias. This introduces fundamental challenges in performing third-order inter-modulation distortion simulations. In this work, a method is presented to replace the factory models with equivalent surface potential models for static current in conjunction with a simple circuit to take into account second-order parasitics, namely, gate current and terminal capacitors. The modeling approach may be utilized even if device measurements are not available, is shown to be simultaneously more computationally efficient and accurate than prior approaches, and is validated through measurements from a 0.15–2.5GHz mixer-first receiver in 65nm CMOS that exhibits +34.8dBm out-of-band IIP3.

RMO2B-3 10:40

Broadband Effect of Linear Tapered Transitions Between Probe Pads and GCPW Signal Lines On-Chip

Tinus Stander; University of Pretoria, South Africa

Abstract: To effect a low-reflection interconnect between GSG probe pads and on-chip GCPW, a linear taper between the signal pad and the GCPW signal line is often included. This work evaluates, both in parametric simulation and experimentation, the effect of this taper shape to the input reflection in the band 1–110 GHz. It is found that, although longer tapers offer some advantage below 30 GHz, the taper ultimately impedes the input reflection of the interconnect.

RMO2B-4 11:00

Accurate EM Simulation of SMT Components in RF Designs

Weimin Sun; Skyworks Solutions, USA

Abstract: SMD is designed into many MCM/SiP products, but accurate EM simulation of SMD in a design has been a challenge. In fact, circuit simulation with an EM MCM model connected with vendor-provided SMT models often leads to a shift of harmonic trap notch. Such shift may be attributed to the intrinsic inductance of an EM port. In this paper, we focus on EM models of HFSS, present discovery of intrinsic port inductance in an HFSS model and discuss issues and techniques on how to handle lumped SMT ports in an HFSS EM model for more accurate SMD circuit simulation.

RMO2B-5 11:20

Variation of Intrinsic Components from Small-Signal Model of AlGaN/GaN HEMTs in Linear and Saturation Regions After Off-State Bias

Yue-ming Hsin, Yi-Nan Zhong, Zhen-Wei Liu; National Central University, Taiwan

Abstract: Current dispersion is an issue in AlGaN/GaN HEMTs. Different methods have been reported to investigate this phenomenon. This study reports an investigation of intrinsic components from small-signal model of AlGaN/GaN HEMTs right after off-state bias in linear and saturation regions in addition to drain-lag measurement. Different variations on the intrinsic components after off-state bias in linear and saturation regions were observed after switching from off-state bias. A significant current dispersion from drain-lag measurement is related to the increase in R_{ds} and decrease in C_{ds} extracted from small-signal model. However, less changes in C_{gs} and C_{gd} were observed.

Monday 5th June 2017
10:00–11:40
HCC Room 313B
Session RMO2D: Millimeter-Wave and THz Sources
Chair: Mohyee Mikhemar, Broadcom
Co-Chair: Ehsan Afshari, University of Michigan

RMO2D-1 10:00
An 8-Element Common-Mode-Coupled 106GHz Fundamental Oscillator with -111 dBc/Hz Phase Noise at 1MHz Offset

Alireza Imani, Hossein Hashemi; University of Southern California, USA

Abstract: Phase noise reduces in a coupled array of oscillators at an ideal rate of 3N dB for 2^N oscillators. Concept of "common-mode coupling" is introduced as a robust technique in reducing phase noise in mm-wave frequencies. A 106 GHz 8-element common-mode coupled Colpitts oscillator is implemented in a 130 nm SiGe HBT BiCMOS technology with a measured phase noise of -111 dBc/Hz at 1 MHz offset while consuming 90 mW. The core differential Colpitts oscillator uses a resonant biasing scheme to reduce phase noise. The improvement of phase noise compared to the stand-alone oscillator is 9 dB showing the effectiveness of the proposed coupling scheme.

RMO2D-2 10:20
A 195GHz Single-Transistor Fundamental VCO with 15.3% DC-to-RF Efficiency, 4.5mW Output Power, Phase Noise FoM of -197dBc/Hz and 1.1% Tuning Range in a 55nm SiGe Process

Hamid Khatibi[1], Somayeh Khiyabani[1], Andreia Cathelin[2], Ehsan Afshari[3]; [1]Cornell University, USA, [2]STMicroelectronics, France, [3]University of Michigan, USA

Abstract: A novel approach to design efficient high-output-power fundamental oscillators close to the f_{max} of the employed process is presented. The idea is based on shaping and optimizing the maximally efficient power gain (G_{ME}) of the circuit using a pair of internal/external feedback mechanisms. Solving a constrained optimization problem, an optimum pair of passive feedback network is designed to achieve the highest maximally efficient power gain in order to increase the output power and thence the DC-to-RF efficiency. A 195 GHz fundamental oscillator is designed in a 55 nm SiGe process ($f_{max} \simeq 340$GHz), which achieves a significantly higher DC-to-RF efficiency (15.3%) among all reported oscillators working above $f_{max}/3$ of their active devices. The oscillator generates a peak power of 4.5 mW (6.5 dBm) with the best phase noise of -82.3 dBc/Hz and the best FoM of -197 dBc/Hz measured at 100 KHz offset frequency, which is the best phase noise and FoM among all CMOS/SiGe mm-Wave oscillators. The proposed optimization-based method takes into account PVT variations as well as modeling errors of all components in the design process to guarantee the functionality of the fabricated circuit.

RMO2D-3 10:40

Energy Efficient Distributed-Oscillators at 134 and 202GHz with Phase-Noise Optimization through Body-Bias Control in 28nm CMOS FDSOI Technology

Raphaël Guillaume[1], François Rivet[2], Andreia Cathelin[1], Yann Deval[2]; [1]STMicroelectronics, France, [2]IMS (UMR 5218), France

Abstract: Two compact frequency generation topologies based on distributed oscillator architecture have been for the very first time integrated at 134GHz and 202GHz in a 10ML 28nm FDSOI CMOS technology. The efficient fundamental frequency generation enables output powers of 0.4dBm and 0.3dBm and 5.5% and 5.4% DC-to-RF efficiency respectively. The body tie of the 28nm FDSOI technology allows phase noise fine tuning through body-bias control. The measured optimum phase noises are -99.6dBc/Hz and -100.4dBc/Hz at 1MHz offset, for the two different oscillators. Robust design has been as well demonstrated, opening the way to mmW and sub-mmW SoC integration in deep submicron FDSOI CMOS.

RMO2D-4 11:00

A Lens-Integrated 430GHz SiGe HBT Source with up to -6.3dBm Radiated Power

Philipp Hillger[1], Janusz Grzyb[1], Stefan Malz[1], Bernd Heinemann[2], Ullrich Pfeiffer[1]; [1]Bergische Universität Wuppertal, Germany, [2]IHP, Germany

Abstract: This paper presents a 430 GHz source implemented in a 0.13-µm SiGe BiCMOS technology with f_T/f_{max} of 300 GHz/450 GHz. The source comprises a fundamental differential Colpitts cascode oscillator at 215 GHz driving a balanced common-collector doubler that utilizes inductive 2nd-harmonic feedback at the emitter output in order to boost the generated 2nd-harmonic current. The doubler is co-designed with a lens-coupled on-chip circular slot antenna providing the appropriate input impedance to the doubler output. In combination with a 3-mm diameter silicon-lens, the total peak radiated power is -6.3 dBm at a power dissipation of 165 mW. To the authors knowledge, the presented source shows the highest reported power for any silicon-based single-element radiator beyond 350 GHz.

RMO2D-5 11:20

An Ultra-Wideband Harmonic Radiator with a Tuning Range of 62GHz (28.3%) at 220GHz

Ali Mostajeran, Ehsan Afshari; Cornell University, USA

Abstract: An ultra-wideband mm-wave voltage controlled oscillator (VCO) is presented. By utilizing an optimum design of the passives embedding around the core transistor in a Colpitts structure, the VCO tuning range is enhanced. The impact of DC bias on the tuning bandwidth is discussed. The generated second harmonic is efficiently extracted and radiated using a wideband slot antenna. The chip is fabricated in a 55nm BiCMOS process. A state-of-the-art tuning bandwidth of 62.1GHz (28.3%) at a center frequency of 219.6GHz is achieved. With a measured peak radiated power of -3.7dBm, a DC to radiated power efficiency of 0.52% is obtained. To the best of our knowledge, this is the largest VCO bandwidth at mm-wave frequencies compared to the state of the art.

Monday 5th June 2017
13:30–15:10
HCC Room 312
Session RMO3A: Ultra-Low Power Wake-Up Receivers
Chair: David Wentzloff, University of Michigan
Co-Chair: Arun Natarajan, Oregon State University

RMO3A-1 13:30
A 2.4GHz BLE-Compliant Fully-Integrated Wakeup Receiver for Latency-Critical IoT Applications Using a 2-Dimensional Wakeup Pattern in 90nm CMOS

Ming Ding, Peng Zhang, Chuang Lu, Yan Zhang, Stefano Traferro, Gert-Jan van Schaik, Yao-Hong Liu, Jarkko Huijts, Christian Bachmann, Guido Dolmans, Kathleen Philips; Holst Centre, The Netherlands

Abstract: This paper presents a wakeup receiver for latency-critical IoT applications in 90nm CMOS, which is fully compliant to many popular IoT wireless standards with constant envelope modulations, such as Bluetooth Low Energy and IEEE802.15.4. Paired with a standard-compliant transmitter, the proposed wakeup receiver method minimizes the overhead in system power, area and complexity. The proposed 2-dimensional wakeup pattern reduces the latency of a wakeup event to below 100μs. Supplied at a battery voltage of 2V, the chip fully integrates a power management unit, a wakeup receiver with offset and noise suppression, a low power digital baseband with automatic gain control and RSSI estimation, and a crystal oscillator. With a BLE compliant signal, the chip achieves -58dBm sensitivity , and a >600s mean time without false alarm, consuming 195μA.

RMO3A-2 13:50
95μW 802.11g/n Compliant Fully-Integrated Wake-Up Receiver with -72dBm Sensitivity in 14nm FinFET CMOS

Erkan Alpman[1], Ahmad Khairi[2], Minyoung Park[1], V. Srinivasa Somayazulu[1], Jeffrey R. Foerster[1], Ashoke Ravi[1], Stefano Pellerano[1]; [1]Intel, USA, [2]Carnegie Mellon University, USA

Abstract: A 2.4GHz fully-integrated Wi-Fi compliant wake-up receiver in 14nm FinFET technology is presented. The receiver achieves -72dBm sensitivity and +20dBr adjacent channel interference rejection for 62.5kbps at 10^{-3} BER while consuming 95μW. The OOK-modulated wake-up packet can be transmitted using any legacy OFDM Wi-Fi transmitter.

RMO3A-3 14:10

A 335μW -72dBm Receiver for FSK Back-Channel Embedded in 5.8GHz Wi-Fi OFDM Packets

Jaeho Im, Hun-Seok Kim, David D. Wentzloff; University of Michigan, USA

Abstract: An ULP back-channel receiver is presented that demodulates binary a FSK back-channel signal embedded in 5.8GHz IEEE 802.11a Wi-Fi OFDM packets. The architecture of the back-channel receiver employs a two-step down-conversion where the first mixing stage downconverts using the 3rd harmonic of the LO for power efficiency. The LP-65nm CMOS receiver consumes 335μW with a sensitivity of -72dBm at a BER of 10^{-3} and data-rate of 31.25kb/s. The radio uses a balun and a 250kHz reference crystal as external components. The receiver uses a 1V supply voltage for analog blocks, and 0.85V for digital blocks including the LO and FLL.

RMO3A-4 14:30

A 365nW -61.5dBm Sensitivity, 1.875cm² 2.4GHz Wake-Up Receiver with Rectifier-Antenna Co-Design for Passive Gain

Kamala Raghavan Sadagopan[1], Jian Kang[1], Sanket Jain[1], Yogesh Ramadass[2], Arun Natarajan[1]; [1]Oregon State University, USA, [2]Texas Instruments, USA

Abstract: A 2.4 GHz 365nW wake-up receiver (WuRX) with RF envelope detection using rectifier-antenna co-design for passive voltage gain and RF filtering is presented. The RF frequency-tunable WuRX uses a programmable 32-bit OOK wake-up signature, achieving sensitivity of -61.5dBm for 2.5 kb/s without any off-chip matching components between IC and antenna. RF filtering in the high-Q rectifier-antenna interface results in 10^{-3} BER even with interferer-to-carrier ratio of 19.1 dB for CW blocker at 3MHz offset. The 65-nm CMOS WuRX IC occupies 1.1mm², while the WuRX (including antenna) occupies 1.875cm².

RMO3A-5 14:50

A 64μW, 23dB Gain, 8dB NF, 2.4GHz RF Front-End for Ultra-Low Power Internet-of-Things Transceivers

Anjana Dissanayake, Hyun-Gi Seok, Oh-Yong Jung, Sok-Kyun Han, Sang-Gug Lee; KAIST, Korea

Abstract: An ultra-low power (ULP) 2.4 GHz RF front-end which consists of a low noise amplifier (LNA) and a passive mixer in a standard 65nm CMOS is presented. LNA adopts a complementary input stage and a current reused 2nd gain stage to achieve a high gain under a low power dissipation with an added linearization method. RF Down-conversion is implemented with a highly linearized complementary passive mixer, which adopts transmission gate type switches.

With fully on-chip components, the front-end achieves 23 dB conversion gain, 8 dB NF, -36 dBm P1dB and -21 dBm IIP3 while dissipating a 64 μW power from a 0.6 V supply voltage. LNA achieves a high voltage gain of 26.3 dB and minimum NF of 5.5 dB with a P1dB of -27 dBm and IIP3 of -13 dBm.

Monday 5th June 2017
13:30–15:10
HCC Room 313A
Session RMO3B: Next Generation Transmitters and Receivers for Cellular and Wireless Connectivity

Chair: Julian Tham, Cypress Semiconductor

Co-Chair: Yuan-Hung Chung, MediaTek

RMO3B-1 13:30

A Wideband Linear Direct Digital RF Modulator Using Harmonic Rejection and I/Q-Interleaving RF DACs

M. Mehrpoo, Mohsen Hashemi, Yiyu Shen, Rene van Leuken, Morteza S. Alavi, Leo C.N. de Vreede; Technische Universiteit Delft, The Netherlands

Abstract: This paper presents a wideband linear direct digital RF modulator (DDRM) in 40nm CMOS technology. It features an advanced 2nd-order-hold interpolation filter and I/Q-interleaving harmonic rejection RF DACs. The 2×9-bit DDRM core occupies 0.21mm^2 and consumes only 110mW at 1 GHz. Within the 0.9–3.1GHz frequency range, the peak output power reaches +9.2dBm and the 3rd/5th harmonic rejection, C-IMD3, and OIP3 are respectively better than 30 dB, -44 dBc, and +25 dBm. The EVM and ACPR at 3 GHz for a 57-MHz 64-QAM signal are better than -30 dB and -45 dB, respectively, and ACPR remains as low as -44 dBc up to a wide bandwidth of 110 MHz.

RMO3B-2 13:50

A Dual Core Power Combining Digital Power Amplifier for 802.11b/g/n with +26.8dBm Linear Output Power in 28nm CMOS

Alden Wong, Philip Godoy, Ovidiu Carnu, Hao Li, Xingliang Zhao, Ashkan Olyaei, Amir Ghaffari, Sai-Wang Tam, Renaldi Winoto, Randy Tsang; Marvell Semiconductor, USA

Abstract: This paper presents a digital power amplifier with two cores that are power combined for a Psat of +32.5dBm. Assisted by an on-chip digital pre-distortion, a transmitted output power of +26.8dBm for 802.11g 54 Mbps 64-QAM is achieved. This is the highest reported linear output power for a digital power amplifier designed for 802.11b/g/n applications in bulk 28nm CMOS. A total area of 0.36mm^2 is used for the power amplifier cores and combiner. Drawing off of a 3.3V supply, this power amplifier has a drain efficiency of 21.2% at the maximum linear output power.

RMO3B-3 14:10

A Fully-Integrated Digital-Intensive Polar Doherty Transmitter

Yiyu Shen[1], M. Mehrpoo[1], Mohsen Hashemi[1], Michael Polushkin[1], Lei Zhou[1], Mustafa Acar[2], Rene van Leuken[1], Morteza S. Alavi[1], Leo C.N. de Vreede[1]; [1]Technische Universiteit Delft, The Netherlands, [2]Ampleon, The Netherlands

Abstract: This paper presents an advanced 2.3–2.8 GHz fully-integrated digital-intensive polar Doherty transmitter realized in 40nm standard CMOS. The proposed architecture comprises CORDIC, digital delay aligners, interpolators, digital pre-distortion (DPD) circuitry in combination with frequency-agile wideband phase modulators followed by the digital main and peak power amplifier (PA) operating in quasi-load insensitive class-E using an on-chip power combiner. At 2.5 GHz, its maximum output power is +21.4 dBm. Drain efficiency is 49.4% at peak power, and 33.7% at 6-dB power back-off. Applying DPD for a 20-MHz 64-QAM signal, the measured EVM is better than -30 dB while the average drain efficiency is 24%.

RMO3B-4 14:30

A 2×2 802.11ac WiFi Transceiver Supporting Per Channel 160MHz Operation in 28nm CMOS

Wen-Kai Li, Wei-Chia Chan, Tzung-Chuen Tsai, Hui-Hsien Liu, Wen-Ming Chang, Chang-Ming Lai, Tao Chiang, Chen-Lun Lin, Pi-An Wu, Hao-Wei Huang, Yen-Liang Yeh, Pang-Ning Chen, Jui-Lin Hsu, Sheng-Hao Chen, Chi-Yun Wang, Yu-Hsien Chang, Tsung-Hsun Yang, Ruey-Bo Sun, Wei-Hsiu Hsu, Jing-Hong Conan Zhan; MediaTek, Taiwan

Abstract: This paper presents a dual-band 2×2 WiFi transceiver in 28nm bulk CMOS. Achieved receiver and transmitter EVM floor at 5GHz for 160MHz per channel are -35dB and -33dB, respectively. The 2.4GHz integrated PA provides 26.5dBm saturated output power while its 5GHz counterpart delivers 26dBm. The 2.4GHz receiver features mixer first architecture while the transmitter includes a 2nd harmonic notch for emission control.

RMO3B-5 14:50

A Current-Efficient Wideband Cellular RF Receiver for Multi-Band Inter- and Intra-Band Carrier Aggregation Using 14nm FinFET CMOS

Youngmin Kim, Pilsung Jang, Taehwan Jin, Jaeseung Lee, Heeseon Shin, Suseob Ahn, Jungyeol Bae, Junghwan Han, Seungchan Heo, Thomas Byunghak Cho; Samsung, Korea

Abstract: A wideband cellular RF receiver for multi-band carrier aggregation employing a current-efficient wideband low noise amplifier and a frequency-band switchable transformer is demonstrated in a 14nm FinFET CMOS technology. The proposed wideband low-noise amplifier can support multiple-channel RF signals for intra-band carrier aggregation with high performance and low DC current consumption. Moreover, the frequency-band switchable transformer is used to support a size-efficient receiver up to 5 carrier components carrier aggregation. The receiver operates at frequencies between 0.6 to 2.7 GHz. The receiver has conversion gain more than 62 dB and noise figure less than 5 dB at all carrier aggregation combinations.

Monday 5th June 2017
13:30–15:10
HCC Room 313B
Session RMO3D: X Band PAs and Beyond
Chair: Jeffrey Walling, University of Utah
Co-Chair: Ranjit Gharpurey, University of Texas at Austin

RMO3D-1 13:30
Fully Integrated CMOS X-Band Power Amplifier Quad with Current Reuse and Dynamic Digital Feedback (DDF) Capabilities

Florian Bohn, Behrooz Abiri, Ali Hajimiri; Caltech, USA

Abstract: A 10GHz fully-integrated stacked PA quad with dynamic digital feedback and control loops provides total output power of 200mW at 37% PAE. It utilizes data provided by multiple on-chip sensors to maintain safe operating conditions and regulate the individual power PA power supply voltages and independent power control for each PA. This digitally controlled stacked PA quad with on-chip matching allows higher operation voltages while maintaining current consumption constant, leading to higher overall system efficiency, as ohmic drop losses under large supply-to-breakdown voltage ratios are reduced.

RMO3D-2 13:50
A 42–46.4% PAE Continuous Class-F Power Amplifier with C_{gd} Neutralization at 26–34GHz in 65nm CMOS for 5G Applications

Sheikh Nijam Ali[1], Pawan Agarwal[1], Shahriar Mirabbasi[2], Deukhyoun Heo[1]; [1]Washington State University, USA, [2]University of British Columbia, Canada

Abstract: This paper presents a wideband high efficiency continuous class-F (CCF) power amplifier (PA) at mm-Wave frequencies for the first time. A tuned load with a high-order harmonic resonance network is used to shape the current and voltage waveforms for the proposed CCF CMOS PA. Further, a transformer with a tunable coupling-coefficient (k_{tune}) is incorporated in the tuned load network to address the detrimental feedback effect caused by the increased transistor gate-drain capacitance (C_{gd}) in deep submicron CMOS technology. This technique allows precise neutralization of C_{gd}, reducing undesirable influence on the tuned load, and maximizing power-efficiency and stability. The CCF PA prototype, implemented in 65 nm CMOS exhibits more than 42% power added efficiency (PAE) over 8 GHz bandwidth (26–34 GHz), while delivering saturated output power (P_{sat}) of 14.75 dBm at 30 GHz. This design presents one of the highest reported PAEs among mm-Wave CMOS PAs, achieving 46.4% peak PAE at 29 GHz.

RMO3D-3 14:10

Waveform Engineering in a mm-Wave Stacked-HBT Switching Power Amplifier

Kunal Datta, Hossein Hashemi; University of Southern California, USA

Abstract: A new family of hybrid stacked power amplifiers (named as 'Class-K') are presented where each of the series stacked transistors can operate independently as different class of switching amplifiers. The voltage and current waveforms of the stacked transistors are shaped by independent harmonic load networks connected to the collector nodes of each of the stacked HBTs. A properly-designed Class-K amplifier can simultaneously achieve the high efficiency of Class-E/F amplifiers, high output power of Class-EF amplifiers, and high power gain of Class-E amplifiers. A proof-of-concept two-stage two-stacked balanced Class-K amplifier implemented in a 0.18 μm SiGe HBT BiCMOS process demonstrates 25.5 dBm output power and 26% peak PAE at 34 GHz.

RMO3D-4 14:30

Linear CMOS Power Amplifier at Ka-Band with Ultra-Wide Video Bandwidth

Daechul Jeong[1], Kyunghoon Moon[1], Seokwon Lee[1], Byungjoon Park[2], Jihoon Kim[2], Juho Son[2], Bumman Kim[1]; [1]POSTECH, Korea, [2]Samsung, Korea

Abstract: A highly linear power amplifier (PA) with ultra-wide video bandwidth is designed at a Ka-band for 5G application. To get a high linearity with high efficiency, a deep class-AB topology with 2nd harmonic control circuits is employed, reducing the 3rd order nonlinearity. Further, an efficient low-drop out (LDO) regulator is proposed to suppress the memory effect generated by the envelope and fundamental nonlinear mixing. The PA, composed of 3 cascaded common-source (CS) stages, achieves peak PAE of 21.8% at output power of 14 dBm with 22 dB gain. The 3rd order inter-modulation distortion (IMD3) at an output power of 5 dBm is under -30 dBc for a video bandwidth of 1 GHz. The PA and LDO are fabricated in a 65 nm CMOS process and occupy 0.53 mm^2.

RMO3D-5 14:50

Adaptive Gain and Phase Adjustment for Local Linearization of Power Amplifiers of Micro/mm-Wave Phase Arrays

Farid Shirinfar[1], Reza Rofougaran[2], Sudhakar Pamarti[1]; [1]University of California, Los Angeles, USA, [2]Movandi, USA

Abstract: A wideband, local Power Amplifier (PA) linearization technique is presented. The proposed Adaptive Gain and Phase Adjustment (AGPA) local linearization technique compensates for both AM-AM and AM-PM distortion of PA for large channel bandwidths of hundreds of megahertz. A 60GHz PA designed in a 28nm CMOS process is designed and measured. AGPA improves the OP1dB of the stacked PA by 2.8dB from 9.5dBm to 12.3dBm and reduces the IM3 products by 3dB with a tone spacing of 200MHz at 8dBm output power.

Monday 5th June 2017
15:30–17:10
HCC Room 312
Session RMO4A: Low-Power Transceivers
Chair: Gernot Hueber, NXP Semiconductors
Co-Chair: Yao-Hong Liu, imec

RMO4A-1 15:30
Crystal-Free Narrow-Band Radios for Low-Cost IoT

Brad Wheeler, Filip Maksimovic, Nima Baniasadi, Sahar Mesri, Osama Khan, David Burnett, Ali Niknejad, Kris Pister; University of California, Berkeley, USA

Abstract: A transceiver was designed and fabricated in 65 nm CMOS to verify the feasibility of using a free running, on-chip LC tank as the local oscillator in an IEEE 802.15.4 transceiver. The elimination of the off-chip frequency reference is possible while still using a standards based narrow-band architecture. A free running LC tank is shown to have frequency stability better than ± 40 ppm in the absence of temperature changes. Demodulator-based feedback is implemented to allow a receiver to track transmitter drift due to varying environmental factors and phase noise. The modulation accuracy of a free-running open loop Minimum Shift Key (MSK) transmitter is shown to be within the limits set by IEEE 802.15.4.

RMO4A-2 15:50
A 4mW-RX 7mW-TX IEEE 802.11ah Fully-Integrated RF Transceiver

Ao Ba, Kia Salimi, Paul Mateman, Pepijn Boer, Johan van den Heuvel, Jordy Gloudemans, Johan Dijkhuis, Ming Ding, Yao-Hong Liu, Christian Bachmann, Guido Dolmans, Kathleen Philips; Holst Centre, The Netherlands

Abstract: An IEEE 802.11ah-compliant RF transceiver with a direct-conversion receiver and a fully-digital polar transmitter is presented. For the receiver, a current-mode RF front-end covers the mandatory modes worldwide from 755MHz to 928MHz. The digitally-assisted analog baseband achieves variable gains and bandwidths with an automatic gain/DC-offset calibration. Implemented in 40nm CMOS with 1V supply, this receiver achieves -104dBm sensitivity in the 1MHz MCS0 mode (i.e., 300kbp/s). It fulfils the adjacent channel rejection requirements with at least 17dB margin. The digital polar transmitter achieves -31dB EVM and 10dB spectral mask margin.

RMO4A-3 16:10
A Sub-1V, 2.8dB NF, 475μW Coupled LNA for Internet of Things Employing Dual-Path Noise and Nonlinearity Cancellation

Mustafijur Rahman, Ramesh Harjani; University of Minnesota, USA

Abstract: A 0.7V low power LNA combines a 1:3 frontend balun with dual-path noise and non-linearity cancellation for improved noise performance at low power. In traditional techniques only the noise of the main path is cancelled while the noise of the auxiliary path is minimized by using

high power. In the proposed design, the noise and non-linearity of both the main and the auxiliary paths are mutually cancelled allowing for low power operation. The 2.8dB NF, -10.7dBm IIP3 LNA in TSMC's 65nm GP process consumes 475μW of power resulting in an FOM of 28.8dB which is 8.2dB better than the state of the art.

RMO4A-4 16:30

A Fully Integrated Reconfigurable Low-Power Sub-GHz Transceiver for 802.11ah in 65nm CMOS

Meng Wei, Zheng Song, Peiyi Li, Jianfu Lin, Junfeng Zhang, Jiachen Hao, Baoyong Chi; Tsinghua University, China

Abstract: A fully integrated reconfigurable low-power Sub-GHz transceiver for 802.11ah is presented. The receiver uses the low-IF/zero-IF reconfigurable architecture to support 1, 2 and 8MHz signal bandwidth, and the needed number of the Op-Amps in the analog baseband is reduced to 3 while providing 4^{th}-order channel filtering and programmable gain amplification. The transmitter uses the digital polar architecture, with the open-loop phase modulator to support wide signal bandwidth and the inverse Class-D digital power amplifier to enhance the power efficiency. A Class-C VCO with dynamic gate bias technique for robust start-up and AFC-assisted oscillation amplitude control technique is used in the fractional-N PLL frequency synthesizer. The transceiver has been implemented in 65nm CMOS. The measured results show that the receiver achieves <3.89dB NF and 47dB image rejection, and the frequency synthesizer achieves -127.8dBc/Hz phase noise at 1MHz offset and -94.6dBc/Hz in-band phase noise from a 1.536GHz carrier. The transmitter demonstrates 6.98% EVM for 900MHz pi/4-DQPSK signals at 6.3 dBm output power without pre-distortion. The receiver and the frequency synthesizer consume 6.4mA and 5.5mA current from a 1.2V power supply, respectively, and the DPA in the transmitter achieves 51.7% drain efficiency at 17.1dBm peak output power.

RMO4A-5 16:50

A 3.4Mbps NFC Card Emulator Supporting 40mm² Loop Antenna

Tieng Ying Choke[1], Ying Chow Tan[1], Chin Heng Leow[1], Junmin Cao[1], Liming Jin[1], Huajiang Zhang[1], Hon Cheong Hor[1], Eng Chuan Low[1], Weimin Shu[1], Osama Shana'a[2]; [1]MediaTek, Singapore, [2]MediaTek, USA

Abstract: For compact integration of 13.56MHz NFC functionality in mobile devices, a small planar loop antenna is a necessity. Active load modulation (ALM) is a commonly adopted technique to boost load modulation amplitude to overcome weak inductive coupling in small antennas. However, due to the challenges of phase synchronization, ALM is mainly limited to low data rate NFC applications. This paper describes the challenges of supporting NFC Very High Bit Rate (VHBR) Card Emulation Mode (PICC) in small antennas. An ultra-fast retimed phase synchronization PLL technique is proposed to overcome the technical challenges of ALM for high data rate uplink transmission. A sub-sampling ADC topology is implemented as VHBR ASK envelope demodulator. A clock extractor-based PLL provides precise synchronized continuous clock to the high speed sub-sampling ADC for accurate demodulation of all ASK envelopes with modulation index (MI) ranging from 8% to 100%.

Monday 5th June 2017
15:30–17:10
HCC Room 313A
Session RMO4B: RF Circuits for Emerging Applications and Gigabit Optical Links

Chair: Fred Lee, Google

Co-Chair: Ayman Fayed, Ohio State University

RMO4B-1 15:30

A 12-b, 1-GS/s 6.1mW Current-Steering DAC in 14nm FinFET with 80dB SFDR for 2G/3G/4G Cellular Application

Jaekwon Kim, Woojin Jang, Yanghun Lee, Seunghyun Oh, Jongwoo Lee, Thomas Byunghak Cho; Samsung, Korea

Abstract: A 14nm FinFET CMOS 12-b current-steering digital-to-analog (DAC) for 2G/3G/4G cellular applications is presented. A bit segmentation of 6-bit thermometer and 6-bit binary is adopted, and it utilizes the dynamic element matching (DEM) technique to suppress the spurious tones caused by the current source mismatches in 3-D FinFETs. In addition, to keep the voltage drop across each transistor within long-term reliability limit, output switches are designed with shielding transistors while achieving make-before-break operation with the proposed low crossing point level shifter. The active area of a single DAC is 0.036 mm^2, and its power consumption is 6.1 mW with SFDR of 80 dBc.

RMO4B-2 15:50

CMOS Integrated Galvanically Isolated RF Chip-to-Chip Communication Utilizing Lateral Resonant Coupling

Mahdi Javid[1], Richard Burton[2], Karel Ptacek[3], Jennifer Kitchen[1]; [1]Arizona State University, USA, [2]Atomera, USA, [3]ON Semiconductor, Czech Republic

Abstract: In this work, a high voltage (HV) galvanically isolated chip-to-chip communication circuit utilizing laterally coupled resonators is reported. The adjacently placed resonators provide high voltage galvanic isolation (GI) using horizontal space between resonators filled with oxide, which minimizes the need for thick inter-metal dielectrics. A previously unexplored application for lateral coupling is introduced as a passive communication channel for GIs. Magnetic coupling between resonators is used to transfer an upconverted digitally-modulated OOK control signal at 2.8 GHz through the galvanic isolator. This proposed method can be integrated using CMOS processes, without altering the native process or adding extra fabrication steps. The system is realized in a 0.25 μm BCD (Bipolar-CMOS-DMOS) process with only four metal layers for proof of concept. The design does not require exotic packaging and provides 3.3kV RMS isolation, small physical area of 0.95mm^2, and sub-20ns propagation delay. The implemented resonators inherently act as bandpass filters, thus enhancing circuit noise immunity to common mode transients.

RMO4B-3 16:10

A 200μm × 200μm × 100μm, 63nW, 2.4GHz Injectable Fully-Monolithic Wireless Bio-Sensing System

S. O'Driscoll[1], S. Korhummel[1], P. Cong[1], Y. Zou[1], K. Sankaragomathi[1], J. Zhu[2], T. Deyle[3], A. Dastgheib[1], B. Lu[1], M. Tierney[1], J. Shao[1], C. Gutierrez[1], S. Jones[1], H. Yao[1]; [1]Verily, USA, [2]Google, USA, [3]Cobalt Robotics, USA

Abstract: A wireless system-on-chip with integrated antenna, power harvesting and biosensors is presented that is small enough, 200μm × 200μm × 100μm, to allow painless injection. Small device size is enabled by: a 13μm × 20μm 1nA current reference; optical clock recovery; low voltage inverting dc-dc to enable use of higher quantum efficiency diodes; on-chip resonant 2.4GHz antenna; and array scanning reader. In-vivo power and data transfer is demonstrated and linear glucose concentration recordings reported.

RMO4B-4 16:30

SiGe BiCMOS Linear Modulator Drivers with 4.8-V_{pp} Differential Output Swing for 120-GBaud Applications

Robert J.A. Baker[1], James Hoffman[1], Peter Schvan[2], Sorin P. Voinigescu[1]; [1]University of Toronto, Canada, [2]Ciena, Canada

Abstract: Two linear, large-swing distributed amplifiers (DAs) are reported for future 120-GBaud fiber-optic systems. The measured differential gain and bandwidth are over 20 dB and 70 GHz, respectively, and the P_{1dB} is -2.5 dBm. Eye diagram measurements with at least 4.8-V_{pp} differential swing were performed for NRZ signals up to a record 120 Gb/s, and with 4-PAM and 8-PAM signals up to 64 GBaud, with the symbol rate limited by the speed and ENOB of the arbitrary waveform generator. As well, a bit error rate better than 10^{-12} is demonstrated at 64 Gb/s.

RMO4B-5 16:50

A 32Gb/s-NRZ, 15GBaud/s-PAM4 DFB Laser Driver with Active Back-Termination in 65nm CMOS

Bozhi Yin[1], Nan Qi[1], Jingbo Shi[1], Xi Xiao[2], Daigao Chen[2], Miaofeng Li[2], Zhiyong Li[3], Jiangbing Du[4], Zuyuan He[4], Rui Bai[5], Yi Wang[6], Jun Zheng[6], Fred Chang[6], Huanlin Zhang[6], Patrick Yin Chiang[1]; [1]Fudan University, China, [2]Wuhan Research Institute of Post & Telecommunication, China, [3]Chinese Academy of Sciences, China, [4]Shanghai Jiao Tong University, China, [5]PhotonIC Technology, China, [6]Applied Optoelectronics, USA

Abstract: A 32Gb/s-NRZ, 15GBaud/s-PAM4 configurable DFB Laser Diode Driver (LDD) is presented in standard 65nm CMOS. The driver employs a balanced-input, single-ended-output topology to deliver large current output, and integrates a tunable pre-emphasis to extend the bandwidth. An on-chip active back-termination (ABT) is proposed which absorbs loading reflections without sacrificing the effective modulation current. Directly wire-bonded to a DFB laser chip, the measurement results show 25.78Gb/s NRZ optical eye-diagram with 4dB Extinction Ratio (ER) and a 19.3% eye-mask margin referred to the 100G specification. The LDD delivers 60mA bias and 60mApp modulation current, consuming only 550mW power consumption.

Monday 5th June 2017
15:30–17:10
HCC Room 313B
Session RMO4D: Reconfigurable Receiver Front-Ends
Chair: Eric Klumperink, University of Twente
Co-Chair: Ramesh Harjani, University of Minnesota

RMO4D-1 15:30
A Direct RF-to-Information Converter for Reception and Wideband Interferer Detection Employing Pseudo-Random LO Modulation

Tanbir Haque, Mathew Bajor, Yudong Zhang, Jianxun Zhu, Zarion Jacobs, Robert Kettlewell, John Wright, Peter R. Kinget; Columbia University, USA

Abstract: The Direct RF-to-Information Converter (DRF2IC) unifies high sensitivity signal reception, narrowband spectrum sensing and energy-efficient wideband interferer detection into a fast-reconfigurable and easily scalable architecture. In reception mode, the DRF2IC RF front-end (RFFE) consumes 46.5mW and delivers 40MHz RF bandwidth, 41.5dB conversion gain, 3.6dB NF and -2dBm B1dB. 72dB out-of-channel blocker rejection is achieved in narrowband sensing mode. In compressed sensing wideband interferer detection mode, 66dB operational dynamic range, 40dB instantaneous dynamic range, 1.43GHz instantaneous bandwidth (IBW) is demonstrated and 6 interferers scattered over 1.26GHz are detected in 1.2uS consuming 58.5mW.

RMO4D-2 15:50
A 0.3GHz to 1.4GHz N-Path Mixer-Based Code-Domain RX with TX Self-Interference Rejection

Abhishek Agrawal, Arun Natarajan; Oregon State University, USA

Abstract: A code-domain N-path RX is proposed based on PN-code modulated LO pulses for concurrent reception of two code-modulated signals. Additionally, a combination of Walsh-Function and PN sequence is proposed to translate in-band TX self-interference (SI) to out-of-band at N-path RX output enabling frequency filtering for high SI rejection. A 0.3GHz–1.4GHz 65-nm CMOS implementation has 35 dB gain for desired signals and concurrently receives two RX signals while rejecting mismatched spreading codes at RF input. Proposed TX SI mitigation approach results in 38.5 dB rejection for -11.8dBm 1.46 Mb/s QPSK modulated SI at RX input. The RX achieves 23.7dBm OP1dB for in-band SI, while consuming ~35mW and occupies 0.31mm^2.

RMO4D-3 16:10

A 0.7 to 1GHz Switched-LC N-Path LNA Resilient to FDD-LTE Self-Interference at ≥40MHz Offset

Gengzhen Qi[1], Barend van Liempd[2], Pui-In Mak[1], Rui P. Martins[1], Jan Craninckx[2]; [1]University of Macau, China, [2]imec, Belgium

Abstract: This paper proposes a self-interference-resilient LNA for the FDD-LTE covering 0.7 to 1GHz. It incorporates a switched-LC N-path network with gain-boosting and optimum-biasing techniques to enhance the out-of-band (OOB) linearity at ≥40MHz offset. Implemented in 0.18μm SOI CMOS, the LNA achieves >31.2dB output rejection, +26.2dBm (+8dBm) OOB-IIP_3 (iB_{1dB}) at ≥40MHz offset and 6.8dB blocker NF at +4dBm blocker power for the default mode, while consuming a reasonable power of 48.4 to 62.5mW. When reconfigured to high-rejection mode, the LNA offers a tunable cancellation notch improving the output rejection to >50dBc.

RMO4D-4 16:30

A Mixer-First Receiver with Enhanced Selectivity by Capacitive Positive Feedback Achieving +39dBm IIP3 and <3dB Noise Figure for SAW-Less LTE Radio

Yuanching Lien[1], Eric Klumperink[1], Bernard Tenbroek[2], Jon Strange[2], Bram Nauta[1]; [1]University of Twente, The Netherlands, [2]MediaTek, UK

Abstract: A mixer-first receiver enhanced with capacitive positive feedback is proposed to obtain a steeper filter roll-off and enhanced linearity, while keeping low noise figure. It covers all sub-6GHz cellular bands and achieves a high IIP3 of +39dBm and blocker 1dB gain compression point of +12dBm for a blocker frequency-offset of 80MHz at f_{LO}=2GHz. The NF ranges from 2.4dB at f_{LO}=1GHz to 5.4dB at f_{LO}=6GHz. The chip has been fabricated in Globalfoundries 45nm SOI technology on a high resistivity substrate.

RMO4D-5 16:50

85–110GHz CMOS Tunable Nonreciprocal Transmission Line with 45dB Isolation for Wideband Transceivers

Chang Yang, Ping Gui; Southern Methodist University, USA

Abstract: The first CMOS nonreciprocal transmission line (TL) for wideband tunable full-duplex transceiver front ends, having over 45 dB isolation in a bandwidth of 1.5 GHz and tuning range of 85–110 GHz, is demonstrated. Offering tunable nonreciprocal propagation, this structure is based on a parametric time-varying TL modulated by a 10 GHz signal through distributed capacitive mixing. Two capacitive mixers together with a biasing network form a resonant type of wideband matching. Implemented in a chip area of 0.245 mm^2 in 65 nm CMOS, this nonreciprocal TL achieves over 45 dB isolation throughout its entire bandwidth, a maximum 6.5 dB insertion loss (IL) and over 10 dB return loss.

Tuesday 6th June 2017
08:00–09:40
HCC Room 312
Session RTU1A: RF Front-End Building Blocks
Chair: Gary Zhang, Guangdong University of Technology
Co-Chair: Bodhisatwa Sadhu, IBM T.J. Watson Research Center

RTU1A-1 08:00
A Bi-Directional, X-Band 6-Bit Phase Shifter for Phased Array Antennas Using an Active DPDT Switch

Yunyi Gong, Moon-Kyu Cho, John D. Cressler; Georgia Institute of Technology, USA

Abstract: This paper presents an X-band 6-bit phase shifter using active bi-directional double-pole, double-throw (DPDT) switches. The phase shifter is implemented in a 130-nm SiGe BiCMOS technology. Three additional tuning bits are included in the design to achieve accurate phase shifting performance. The phase shifter demonstrates a $>$ 11.5-dB gain in both directions of operation over the 8–12 GHz frequency range, with an RMS amplitude error $<$ 0.9 dB, an RMS phase error $<$ 2.2°, a return loss $>$ 10 dB and an input-referred 1 dB compression point of -15 dBm. The circuit has dimensions of 2.6 × 1.5 mm^2, including pads.

RTU1A-2 08:20
Low Power Highly Linear Band-Pass/Band-Stop Filter for 2–4GHz with Less than 1% of Fractional Bandwidth in 0.13μm CMOS Technology

Laya Mohammadi, Kwang-Jin Koh; Virginia Tech, USA

Abstract: A low power highly linear active filter supporting both band-pass and band-stop modes is implemented in 0.13μm CMOS. The frequency tunable (2–4GHz) active filter utilizes a linearized Q-boosting network and a linear varactor control scheme to mitigate linearity degradation when increasing filter Q. The BPF tolerates blockers to +16dBm 1 dB desensitization. In BPF mode, typical Q-tuning ranges 5–250, NF and IP_{-1dB} are 4~5.2dB and -6~+3dBm, respectively, resulting in a peak DR of 170 dB•Hz. In BSF mode, NF ranges 4~4.8dB and IP_{-1dB} is -1.8~0dBm at 2.5–4GHz. Typical current consumption is 14–19 mA from 2 V supply. Chip size is 0.35 mm^2.

RTU1A-3 08:40
A Feedforward Linearization Technique Implemented in IF Band for Active Down-Conversion Mixers

Hao Li[1], Xiao Yang[2], Carlos E. Saavedra[1]; [1]Queen's University, Canada, [2]Huaqiao University, China

Abstract: A feedforward linearization technique to cancel the third-order intermodulation (IM_3) of the down-conversion mixers is proposed, in which a low-frequency second-order intermodulation tone (IM_2) is created and multiplied by the mixer's output to generate the IM_3 tones for the cancellation. The proposed linearization technique is applied to an active mixer operating at 2 GHz.

Fabricated in a 0.13-μm CMOS process and operated at 1.2 V supply, the mixer with a unit-gain IF amplifier in series delivers 8.5 dB gain and 2.5 dBm IIP_3 without linearization. The linearization technique achieves 12-dB IIP_3 improvement with negligible gain reduction, less than 0.2 dB of noise penalty and an extra current of 4.2 mA.

RTU1A-4 09:00

A 1–30GHz 3-Bit Vector Modulator Based on Ultra-Wideband IQ-Generation for MIMO-Radar-Systems in SiGe BiCMOS

Benedikt Welp[1], Askold Meusling[2], Klaus Aufinger[3], Nils Pohl[4]; [1]Fraunhofer FHR, Germany, [2]Airbus Defence & Space, Germany, [3]Infineon Technologies, Germany, [4]Ruhr-Universität Bochum, Germany

Abstract: MIMO phased array radar systems benefit from beamforming in order to increase system dynamic and detection range. Therefore, an ultra-wideband IQ signal generation concept for driving a vector adder, which produces the desired phase shift in each channel of a MIMO phased array radar system, has been developed. The classic concept to generate wideband quadrature signals that uses a frequency doubler and a static frequency divider brings a 0°/180° phase uncertainty at the dividers outputs which makes this concept useless when using multiple TX-channels at once like in beamforming MIMO phased array radars. Therefore, the classical concept has been enhanced with two possible solutions which are presented in this work. The novel concepts are able to operate from 1–30 GHz.

RTU1A-5 09:20

A 0.05–6GHz Voltage-Mode Harmonic Rejection Mixer with up to 30dBm In-Band IIP3 and 35dBc HRR in 32nm SOI CMOS

Kerim Kibaroglu, Gabriel M. Rebeiz; University of California, San Diego, USA

Abstract: This paper presents a new harmonic rejection mixer (HRM) circuit that uses resistive scaling to achieve very high linearity and a harmonic rejection ratio (HRR) greater than 35 dBc. The mixer employs 4 double-balanced mixers driven by 8 LO phases with 12.5% duty cycle to isolate different paths. The mixer switches have been implemented with thin- and thick- oxide transistors to improve linearity further at the cost of reduced tuning range. The measured conversion loss at an IF of 100 MHz is 6.6–10.8 dB and 6.4–9.2 dB for an RF of 0.05–6 GHz and 0.05–4 GHz, and the measured in-band IIP3 is 23–19 dBm and 31–21 dBm. The power consumption is 29–126 and 98–298 mW for the thin-oxide and thick-oxide designs, respectively. To our knowledge, this is the highest linearity and widest tuning range reported to-date for a harmonic rejection mixer. Application areas are in high-linearity wideband receivers, and in base-station and instrumentation receivers with reduced front-end filtering requirements.

Tuesday 6th June 2017
08:00–09:40
HCC Room 313A
Session RTU1B: Advanced Millimeter-Wave Circuit Techniques
Chair: Hua Wang, Georgia Institute of Technology
Co-Chair: Pierre Busson, STMicroelectronics

RTU1B-1 08:00
An 80–106GHz CMOS Amplifier with 0.5V Supply Voltage
K. Katayama[1], S. Amakawa[1], K. Takano[1], T. Yoshida[1], M. Fujishima[1], K. Hisamitsu[2], H. Takatsuka[2]; [1]Hiroshima University, Japan, [2]Mie Fujitsu Semiconductor, Japan

Abstract: A low-power CMOS W-band amplifier that feeds on a 0.5-V supply is presented. It achieves a peak gain of 24.1 dB and consumes 12mW. This was made possible by (a) the use of Mie Fujitsu Semiconductor 55-nm CMOS technology with deeply depleted channel (DDC) MOSFETs, which are meant specifically for ultralow-power designs with sub-1V supply voltage, (b) high-f_{max} transistor layout, which gives about 1 dB higher gain in the W-band than the ordinary layout, and (c) single-ended negative-capacitance feedback technique, which gives wideband gain boosting comparable to its differential counterpart (with cross-coupled feedback capacitors) with half the power consumption of the latter.

RTU1B-2 08:20
A 77-GHz Active Millimeter-Wave Reflector for FMCW Radar
M. Sadegh Dadash[1], Juergen Hasch[2], Sorin P. Voinigescu[1]; [1]University of Toronto, Canada, [2]Robert Bosch, Germany

Abstract: An 18-mW active millimeter-wave reflector fabricated in 45-nm SOI CMOS technology exhibits a peak gain of 20 dB at 77 GHz, a 3-dB bandwidth of 5 GHz from 75.5 to 80.5 GHz, and a 50-Ω noise figure of 7.5–8.5 dB over the same frequency band. It consists of an LNA, a BPSK modulator and two variable gain output stages each driving a separate transmit antenna. The chip occupies 570μm×880μm and is flip-chip mounted on a 7mm×7mm flexible interposer with two transmit and one receive antenna.

RTU1B-3 08:40
A High-Performance Slow-Wave CPW with ESD Protection for Ultraflat Band Millimeter-Wave Applications
Wei Gao[1], Handoko Linewih[1], Suh-Fei Lim[1], Jian-Hsing Lee[2], Sern-Ee Leang[1]; [1]GLOBALFOUNDRIES, Singapore, [2]GLOBALFOUNDRIES, USA

Abstract: A high performance Slow-Wave Coplanar Waveguide (CPW) with distributed small pieces of ESD diodes in advanced CMOS process is presented to match 50Ω characteristic impedance. Optimized design of each segmented diode pairs and its Lateral Pickups experimentally achieves a very low RF loss of -1.55dB at 60GHz while passing at least 2.6kV HBM level. Its ultraflat frequency response up to 90GHz makes it also favourable for ultrafast digital I/Os with bit rate as high as 64Gb/s.

RTU1B-4 09:00

Circuit Building Blocks for Efficient In-Antenna Power Combining at 240GHz with non-50 Ohm Amplifier Matching Impedance

Christian v. Vangerow[1], Benjamin Goettel[1], Herman Jalli Ng[2], Dietmar Kissinger[2], Thomas Zwick[1]; [1]KIT, Germany, [2]IHP, Germany

Abstract: In this work active and passive circuit components suitable for efficient in-antenna power combining are investigated with focus on the matching impedance between the individual components. In the proposed concept, the input power is split by 1:4 couplers with 12.5Ω output impedance, which enables a very broadband input matching of the following single-ended amplifiers. To combine the output power of the parallelized amplifiers, an eight-feed integrated lens antenna (ILA) with 70Ω input impedance is used, which allows for compact matching to the optimum load impedance of the amplifiers. The individual circuit components are realized in IHP's SG13G2 technology and show excellent agreement with the simulation results. The four times parallelized amplifier shows a gain of roughly 5.5 dB at 240GHz excluding coupler losses.

RTU1B-5 09:20

A 27.9–53.5-GHz Transformer-Based Injection-Locked Frequency Divider with 62.9% Locking Range

Jingzhi Zhang, Huihua Liu, Yunqiu Wu, Chenxi Zhao, Kai Kang; UESTC, China

Abstract: An ultra-wide locking range transformer-based injection-locked frequency divider (ILFD) is presented. By making use of a 4th-order transformer-based resonator and an inductive gain peaking technique, the proposed ILFD can achieve high performance in terms of wide locking range and low power consumption. Fabricated in a standard 65nm CMOS process with a core area of 0.18mm^2, the ILFD measures a locking range of 62.9% from 27.9 to 53.5 GHz while consuming 5.8mW from a 1V power supply. Moreover, when operating at 0.8V power supply, the proposed ILFD consumes only 3.2mW with 48.9% locking range.

Tuesday 6th June 2017
08:00–09:40
HCC Room 313B
Session RTU1D: Reconfigurable Multi-Mode PAs
Chair: Patrick Reynaert, Katholieke Universiteit Leuven
Co-Chair: Gary Hau, Qualcomm

RTU1D-1 08:00
A Digital mm-Wave PA Architecture with Simultaneous Frequency and Back-Off Reconfigurability

Chandrakanth R. Chappidi, Xue Wu, Kaushik Sengupta; Princeton University, USA

Abstract: Spectrally-efficient operation with high power and high efficiency at deep back-off will be critical for the next-generation mm-Wave transmitters for 5G and beyond. In addition, as larger non-contiguous chunks of the mm-Wave spectrum open up, dynamic frequency reconfiguration while ensuring high spectral and energy efficiency can become key towards optimal utilization of spectral resources. In this paper, we present a generalized asymmetrical multi-port combiner based network synthesis approach that enables both frequency and back-off reconfigurability in a mm-Wave power amplifier (PA) architecture to maintain high-efficiency operation with spectrally efficient codes across a wide frequency range. As a proof of concept, a silicon-based PA is presented which operates between 30–55 GHz with peak P_{sat} of 23.7 dBm at 40 GHz and output collector efficiency (η_{out}) of 34.5% and 22% at the 0 and -6 dB back-off respectively. The PA maintains $\eta_{out} > 16\%$ at -6 dB back-off across the range. Non-constant modulation is demonstrated with pulse shaping and with data rates upto 4 Gbps across the frequencies from 30–50 GHz.

RTU1D-2 08:20
A Digitally-Tuned Triple-Band Transformer Power Combiner for CMOS Power Amplifiers

Rahul Singh, Jeyanandh Paramesh; Carnegie Mellon University, USA

Abstract: This paper presents the design and implementation of a CMOS transformer combiner that can be reconfigured to have similar efficiencies at widely separated frequency bands. Conventional transformer combiners employ a fixed tuning capacitance in the secondary network to optimize the efficiency for single frequency standard. In this work, we present a modified transformer combiner where digitally-switchable capacitors introduced at low-swing nodes within the combiner network enable frequency reconfiguration using CMOS switches. A 65 nm CMOS triple-band (2.5/3/3.5 GHz) power amplifier (PA) chip employing the reconfigurable combiner is also presented.

RTU1D-3 08:40

A Split-Array, C-2C Switched-Capacitor Power Amplifier in 65nm CMOS

Zhidong Bai, Wen Yuan, Ali Azam, Jeffrey S. Walling; University of Utah, USA

Abstract: A multiphase RF, C-2C split-array switched-capacitor power amplifier (SCPA) is introduced that allows the resolution and quality factor of the SCPA to be independently controlled. This allows the SCPA to be designed up to the resolution limit of the process, as determined by capacitor matching and jitter in the clock. In prior SCPAs, the resolution was limited by the choice of the output matching network quality factor and the minimum sized capacitor available in the process. A split-array, C-2C SCPA is implemented in 65nm CMOS and occupies $0.85\times2mm^2$. It delivers a peak output power of 24.05 dBm with a peak system efficiency (SE) of 40.6%. When transmitting a 1.4 MHz, 64 QAM LTE signal it outputs 18.8 dBm at 21.6% SE, with a measured EVM of 2.65%-rms at 1.8 GHz.

RTU1D-4 09:00

A 20dBm Outphasing Class E PA with High Efficiency at Power Back-Off in 65nm CMOS Technology

Ali Ghahremani, Anne-Johan Annema, Bram Nauta; University of Twente, The Netherlands

Abstract: This paper presents an outphasing class E PA (OEPA) in a 65nm CMOS technology, using a pcb transmission-line based power combiner. The OEPA can provide +20dBm output power from V_{DD}=1.25V at 1.4GHz with 61% drain efficiency (DE) and 58% power added efficiency (PAE). We introduced a technique to rotate and shift power and efficiency contours of the two branch PAs that enables more than 44dB output power dynamic range, reduces switch voltage stresses compared to conventional OEPAs and enables 41% DE and 24% PAE at 12.5dB back-off.

RTU1D-5 09:20

An S/X-Band CMOS Power Amplifier Using a Transformer-Based Reconfigurable Output Matching Network

Jaeyong Ko[1], Sungho Lee[2], Sangwook Nam[1]; [1]Seoul National University, Korea, [2]KETI, Korea

Abstract: A dual-band power amplifier (PA) with an integrated reconfigurable transformer is presented. The PA operating in the S/X-band is fully integrated using a 0.18-μm RF CMOS process. The switchable transformer is designed by tuning its primary winding and a shunt capacitor at 50Ω load with passive efficiency more than 62%/67% for S/X-band. The measurement results show saturated output power (P_{SAT}) of 24.3/21.2 dBm with peak drain efficiency (DE) of 34.8%/12.2% at 3.1/8.0 GHz, respectively. The 1-dB bandwidth is 0.7/1.25 GHz (2.8–3.5/7.5–8.75 GHz) for the S/X-band. This amplifier with the proposed transformer is suitable for use in an integrated dual-band high-resolution radar transceiver.

Tuesday 6th June 2017
10:00–11:40
HCC Room 312
Session RTU2A: Full-Duplex, Interference-Resilient and Harmonic-Rejection Receivers

Chair: Renaldi Winoto, Marvell Semiconductor

Co-Chair: Raja Pullela, MaxLinear

RTU2A-1 10:00

Low Power Wideband Receiver with RF Self-Interference Cancellation for Full-Duplex and FDD Wireless Diversity

E. Kargaran, S. Tijani, G. Pini, D. Manstretta, R. Castello; Università di Pavia, Italy

Abstract: Saw-Less Frequency Division Duplexing and Full-Duplex transceivers require very high receiver linearity. Self-Interference Cancellation can relax the specification but results in very high power. We propose a low-power direct-conversion single-ended receiver with passive SIC. A 28 nm CMOS prototype achieves an effective IIP3 > 25 dBm for both IB and OOB SI with only 20 dB cancellation and 25 dB isolation. Power consumption is 25mW, active area is 0.5 mm^2.

RTU2A-2 10:20

An FD/FDD Transceiver with RX Band Thermal, Quantization, and Phase Noise Rejection and >64dB TX Signal Cancellation

Sameet Ramakrishnan, Lucas Calderin, Ali Niknejad, Borivoje Nikolić; University of California, Berkeley, USA

Abstract: A transceiver system with active cancellation of the TX signal for full duplex (FD) or frequency division duplex systems (FDD) is presented. A replica cancellation digital-to-analog converter and highly linear receiver with +25dBm OOB IIP3 enable FDD operation without a duplexer at TX power up to +17dBm, FD operation without a circulator up to +5dBm, and FD operation with a circulator up to +13dBm. In addition to providing over 64dB of RF cancellation for a 20MHz modulated TX signal, the front-end demonstrates techniques to cancel noise sources in the RX band, including 3dB reduction of the thermal noise from the self-interference cancellation circuits, >25dB cancellation of quantization noise from the digital TX, and >20dB cancellation of TX LO phase noise in the RX band.

RTU2A-3 10:40

A CMOS UWB Receiver with Reconfigurable Notch Filters for Narrow-Band Interferers

Paria Sepidband, Kamran Entesari; Texas A&M University, USA

Abstract: In this paper, an interferer-tolerant receiver for the first group of ultra-wideband systems (3.1–4.8 GHz) is presented. The entire system operates in two modes; detecting and receiving. In the detecting mode, the locations of up to three blockers in 2.35–2.75 GHz and 5.1–5.9 GHz bands are reported to three notch filters used in the receiving path for rejection. In the receiving mode, the receiver operates normally with the activated notch filters. The entire system is integrated in a standard TSMC CMOS 65-nm technology and consumes up to 23.8 mW and 9.6 mW, in the receiving and detecting modes, respectively, with a 1 V voltage supply. The receiver can achieve an out-of-band IIP3 of as high as 18.9 dBm.

RTU2A-4 11:00

A Full-Duplex Receiver with 80MHz Bandwidth Self-Interference Cancellation Circuit Using Baseband Hilbert Transform Equalization

A. El Sayed[1], A. Ahmed[1], A.K. Mishra[1], A.H.M. Shirazi[1], S.-P. Woo[1], Y.-S. Choi[2], Shahriar Mirabbasi[1], S. Shekhar[1]; [1]University of British Columbia, Canada, [2]Intel, USA

Abstract: To enable simultaneous full-duplex radios, self-interference (SI) cancellation (SIC) circuits that attain large cancellation bandwidths (BWs) are needed to support modern standards such as Long-Term Evolution (LTE). For mobile applications, SIC should be linear, tunable, fully monolithic (compact form factor) and must be implemented at the radio-frequency (RF) front-end. Emulating the group delay (GD) and complex impedance of the SI channel, an SIC circuit is proposed that achieves an 80 MHz of SIC BW using just a single tap delay. GD is estimated using frequency translations and baseband (BB) low pass filtering, and complex impedance is emulated using a vector modulator (VM). We prove that the combination of GD and VM results in a time-domain Hilbert transform equalization (HTE), enabling broadband cancellation and reducing the number of GD taps needed, thereby saving area. Implementing HTE at BB using passive circuits further reduces area, power consumption and maintains linearity. A prototype in 0.13-μm CMOS process occupies 0.4 mm^2 and attains 23 dB of SIC measured over an 80-MHz signal BW, while consuming 13 mW. Total power and area including the receiver is 64.4 mW and 0.72mm^2, respectively.

RTU2A-5 11:20

A Wideband Receiver Employing PWM-Based Harmonic Rejection Downconversion

Heechai Kang, Wei-Gi Ho, Vineet Singh, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A wideband receiver employing single-stage harmonic-rejection mixers (HRM) is demonstrated. The HRM employs a 3-level PWM representation of a sinusoidal LO in combination with gain-ratios. The PWM LO signal is also used to perform gain control. The receiver gain with harmonic rejection is 26.4–30.1 dB using multi-phase PWM LO and 28–31.8 dB with single-phase PWM LO, for a gain range of 3.7 dB. The DSBNF at highest gain is 5.8 dB. The design demonstrates worst-case HR3/HR5 ratios of 47 and 49 dB without calibration for f_{LO}=100 MHz with a total power dissipation of 41.1 mW.

Tuesday 6th June 2017
10:00–11:40
HCC Room 313A
Session RTU2B: System-on-Chip for Millimeter-Wave and Above
Chair: Vito Giannini, UHNDER
Co-Chair: Tim LaRocca, Northrop Grumman Aerospace Systems

RTU2B-1 10:00
Highly-Miniaturized 2-Channel mm-Wave Radar Sensor with On-Chip Folded Dipole Antennas

Herman Jalli Ng[1], Wael Ahmad[1], Maciej Kucharski[1], Jeng-Hau Lu[2], Dietmar Kissinger[1]; [1]IHP, Germany, [2]National Chiao Tung University, Taiwan

Abstract: This paper describes a miniaturized 2-channel system-on-chip radar sensor in a SiGe BiCMOS technology. It includes on-chip folded dipole antennas that utilize a localized backside etching technique with a novel selective etching approach that is able to improve the radiation efficiency and the mechanical stability of the chip. The transceiver is equipped with a 30-GHz VCO that is complemented with a frequency quadrupler to generate a 120-GHz carrier signal. The 2 transmit channels can be combined to increase the effective isotropic radiated power by 6 dB and to implement a SIMO radar. The transceiver also includes BPSK modulators as well as I/Q receivers and can be utilized to build a flexible MIMO radar using frequency-modulated continuous-wave with time and delta-sigma modulator-based frequency division multiplexing as well as pseudo-random noise radar techniques. Radar measurement using digital-beamforming method with 10-GHz modulation bandwidth was performed to show the applicability of the proposed system.

RTU2B-2 10:20
Fully-Scalable 2D THz Radiating Array: A 42-Element Source in 130-nm SiGe with 80-μW Total Radiated Power at 1.01THz

Zhi Hu, Ruonan Han; MIT, USA

Abstract: This paper presents a 1-THz radiating array using IHP 130-nm SiGe process. It is based on a highly-scalable 2D structure that uses a square grid of slots to simultaneously (1) maximize and synchronize the fundamental oscillation (f_0=250 GHz) and 4th-harmonic generation ($4f_0$=1 THz) of a large array of transistors, (2) synthesize standing-wave patterns with near-field cancellation at f_0, $2f_0$ and $3f_0$ and efficient radiation at $4f_0$. The compact design enables implementation of 42 coherent radiators on a 1-mm^2 area. The chip consumes 1.1-W DC power and generates 80-μW total radiated power with 13-dBm EIRP.

RTU2B-3 10:40

A Wideband SiGe BiCMOS Transceiver Chip-Set for High-Performance Microwave Links in the 5.6–43.5GHz Range

Y. Baeyens[1], S. Shahramian[1], B. Jalali[1], P. Roux[1], J. Weiner[1], A. Singh[1], M. Moretto[2], P. Boutet[2], P. Lopez[2]; [1]Nokia Bell Labs, USA, [2]Nokia, France

Abstract: In this paper we present a chip-set of 4 wideband SiGe BiCMOS transceivers optimized for the stringent specifications of various microwave links in the 5–44 GHz range. Each receiver and transmitter covers full frequency bands of 5.6–8.5 GHz, 10–15.5 GHz, 17.5–26.5 GHz and 27–43.5 GHz and demonstrates high dynamic range and excellent noise figure and linearity. Radio links demonstrate error-free operation for channel bandwidths from 7 up to 112 MHz and modulations up to 4096 QAM.

RTU2B-4 11:00

A Fully-Integrated 94-GHz 32-Element Phased-Array Receiver in SiGe BiCMOS

Jean-Olivier Plouchart[1], Wooram Lee[1], Caglar Ozdag[2], Yigit Aydogan[3], Mark Yeck[1], Alper Cabuk[2], Asim Kepkep[2], Emre Apaydin[2], Alberto Valdes-Garcia[1]; [1]IBM T.J. Watson Research Center, USA, [2]MKR-IC, Turkey, [3]ASELSAN, Turkey

Abstract: A 94GHz phased array receiver IC in 130nm BiCMOS technology is reported. The design integrates 32 front ends with gain and phase control configurable using look-up table memory, two separate 16:1 power combiner trees, two 94GHz to ~10GHz (IF) down conversion mixers, an IF to baseband (BB) quadrature down conversion mixer, and a 42GHz PLL followed by a frequency doubler implementing the LO source. The IC occupies an area of 6.7mm×5.6mm and can either support a 32-element phased array or a 16-element polarimetric phased array if connected to 16 dual-polarized antennas. In on-wafer measurements at 94GHz and 25C, the design achieves maximum RF to IF array conversion gain of 39dB, maximum RF to BB array conversion gain of 69dB, 20dB of RF front-end gain programmability, NF of 6 dB, and RMS phase error <1.5° for a 5° phase step. Total power consumption varies from 3W to 4.6W from minimum to maximum RF front-end gain settings.

RTU2B-5 11:20

A 71–86GHz Bidirectional Image Selection Transceiver Architecture

Najme Ebrahimi, James F. Buckwalter; University of California, San Diego, USA

Abstract: A bidirectional image selection transceiver is presented that operates over 71–76 GHz and 81–86 GHz with only 3 GHz of LO tuning range. A sliding-IF architecture with bidirectional VGAs allows operation in transmit and receive modes. The sliding IF and narrow LO tuning range allow wideband image rejection using a single stage polyphase filter. The circuit is implemented in a 90-nm SiGe BiCMOS process. Measurements indicate conversion gain of -2.5 dB to 3 dB with less than ±0.75 dB variation over 10 GHz in TX mode and -4dB to 0 dB with less than ±1 dB variation over 10 GHz bandwidth in RX mode. With 16- and 64-QAM, the EVM is below 5% and 4% at data rates of 6 Gb/s and 9 Gb/s. The RF and LO circuitry consumes at most 150 mW and 250 mW.

Tuesday 6th June 2017
10:00–11:40
HCC Room 313B
Session RTU2D: Power Amplifiers in Advanced Technologies
Chair: Margaret Szymanowski, NXP Semiconductors
Co-Chair: Nick Cheng, Skyworks Solutions

RTU2D-1 10:00
Peaking PA Bias Circuit for an APT CMOS Doherty PA

Joonhoi Hur, Paul Draxler, Jeong-won Park, Anthony Segoria, Vladimir Aparin; Qualcomm, USA

Abstract: This paper presents a peaking PA bias circuit for an Average Power Tracking (APT) CMOS Doherty PA, where the common supply voltage changes as the target average power changes. In order to have Doherty efficiency characteristics with APT, the peaking PA must have an adaptive bias circuit that shifts the bias as the supply voltage changes, activating the peaking PA at the correct backoff (6dB) from the Posat for that supply voltage. This bias circuit is demonstrated on a CMOS Doherty PA using standard 0.18μm SOI. With the proposed bias circuit, the Doherty PA has specification compliant WCDMA performance (with DPD) up to 29dBm Pout, with 40–50% PAE (from 25–29dBm Pout) as the supply voltages ranges from 1.5V to 4V.

RTU2D-2 10:20
An X-Band Inverse Class-F SiGe HBT Cascode Power Amplifier with Harmonic-Tuned Output Transformer

Inchan Ju, John D. Cressler; Georgia Institute of Technology, USA

Abstract: This paper presents a highly efficient X-band inverse class-F SiGe HBT cascode power amplifier (PA) to overcome performance limitations imposed by device breakdown. Simultaneous fundamental and $2^{nd}/3^{rd}$ harmonic matching is achieved using an output transformer with an embedded capacitor at its center-tap, which enables inverse class-F operation. Use of a cascode topology with a low base impedance termination and minimum voltage-current waveform overlap extends the V_{CE} swing on the upper SiGe HBT in the cascode to beyond BV_{CBO}, boosting output power and power added efficiency (PAE). As proof of concept, the inverse class-F PA was implemented in 0.13-μm SiGe BiCMOS technology. Measured results show an output power of 25.8 dBm and 51.1% peak PAE at 10 GHz, when operated on a 3.0 V supply. To the authors' best knowledge, our work has the highest efficiency among all Si-based X-band PAs with comparable output power.

RTU2D-3 10:40

A 6–18GHz GaN Distributed Power Amplifier Using Reactive Matching Technique and Simplified Bias Network

Hongjong Park[1], Sangho Lee[1], Kwangseok Choi[1], Jihoon Kim[1], Hyosung Nam[2], Jaeduk Kim[3], Wangyong Lee[3], Changhoon Lee[4], Junghyun Kim[2], Youngwoo Kwon[1]; [1]Seoul National University, Korea, [2]Hanyang University, Korea, [3]LIG Nex1, Korea, [4]ADD, Korea

Abstract: Two-stage reactively matched gain cells are applied to design a high-gain multi-octave distributed power amplifier (DPA) in this paper. The proposed reactively matched distributed amplifier (RMDA) structure shows a high gain and high output power performance within a small die size. The DC bias network of each section is simplified to implement the proposed structure in an MMIC and the design guide for the bias network is provided. A 6–18 GHz GaN DPA fabricated with the commercial 0.25-μm GaN HEMT process shows output power reaching 40.3–43.9 dBm with 16–27% PAE. To the best of our knowledge, this is the first demonstration of a GaN DPA using reactively matched gain cells, and it exhibits excellent small-signal gain and RF power performance capabilities among other reported GaN PAs with a multi-octave bandwidth up to the Ku-band.

RTU2D-4 11:00

A Ka-Band Asymmetrical Stacked-FET MMIC Doherty Power Amplifier

Duy P. Nguyen, Thanh Pham, Anh-Vu Pham; University of California, Davis, USA

Abstract: We present a stacked-FET monolithic millimeter-wave (mmW) integrated circuit Doherty power amplifier (DPA). The DPA employs a novel asymmetrical stack gate bias to achieve high power and high efficiency at 6-dB power back-off (PBO). The circuit is fabricated in a 0.15-μm enhancement mode (E-mode) Gallium Arsenide (GaAs) process. Experimental results demonstrate output power at 1-dB gain compression (P_{1dB}) of 28.2 dBm, peak power added efficiency (PAE) of 37% and PAE at 6-dB PBO of 27% at 28 GHz. Measured small signal gain is 15 dB while the 3-dB bandwidth covers from 25.5 to 29.5 GHz. Using digital predistortion (DPD) with a 20 MHz 64 QAM modulated signal, an adjacent channel power ratio (ACPR) of -46 dBc has been observed.

RTU2D-5 11:20

A 73GHz PA for 5G Phased Arrays in 14nm FinFET CMOS

Steven Callender, Stefano Pellerano, Christopher Hull; Intel, USA

Abstract: This paper presents the design of an E-band PA in Intel 14nm FinFET/trigate CMOS process. Device layout optimizations are used to maximize device performance at mm-wave frequencies and overcome the impact of scaling on RF performance. Neutralization and low-k transformer-based matching networks are employed to improve gain and bandwidth. The PA achieves a peak gain of 11.9dB/16.7 dB at 71GHz with a bandwidth of 8.5GHz/7.4 GHz in low-gain/high-gain mode. At 71GHz, the measured Psat, OP_{1dB} and peak PAE are 7.3dBm, 1.6dBm, and 8.3%, respectively.

RFIC 2017 Lunchtime Panel Session

Monday, 5 June 2017
11:45–12:45
HCC, Room 313C

5th Generation Wireless — Where is That Going and What's in It for Me?

Panel Organizers and Moderators:
Oren Eliezer, *PHAZR, USA*
Brian Floyd, *North Carolina State University, USA*
Bodhisatwa Sadhu, *IBM T.J. Watson Research Center, USA*

Panelists: **Amitava Ghosh**, *Nokia Fellow and Head of Small Cell Research, Nokia Bell Labs, USA*
Gregory Chance, *Principal Engineer and 5G RF Architect, Intel, USA*
Nitin Jain, *Founder, Chairman and CTO, Anokiwave, USA*
Joy Laskar, *Co-Founder, CTO and Senior VP, Maja Systems, USA*
Gabriel M. Rebeiz, *Distinguished Professor, University of California, San Diego, USA*

Abstract: A panel of 5 experts from the industry and academia will debate different challenges associated with the development and deployment of 5th generation wireless systems; when and how the advancements in technologies such as massive MIMO, beamforming, phased arrays, and millimeter wave ICs will allow such systems to reach their performance and cost targets; and, of course, how will all that impact us, the community of RF engineers and end users.

IMS/RFIC 2017 Lunchtime Panel (Game Show)

Tuesday, 6 June 2017
11:45–12:45
HCC, Room 316C

Who Wants to be a Millimeterwavionaire?

Organizers and Moderators:
Earl McCune, *Eridan Communications, USA*
Sherry Hess, *National Instruments, USA*
Bodhisatwa Sadhu, *IBM T.J. Watson Research Center, USA*
Oren Eliezer, *PHAZR, USA*

Contestants: **You'll find out when you get there! Maybe you will be one of them?**

Abstract: Two teams of contestants, including preselected and randomly selected contestants from the audience, will compete in answering questions on RF and microwave theory and history, including IMS/RFIC conference trivia. Prizes will be awarded to the contestants, as well as to others in the audience who may be called upon for answers. Bring your lunch and be prepared for a great deal of entertainment and a little bit of learning too!

WORKSHOPS AND SHORT COURSES

Workshops and Short Courses are offered on Sunday, Monday and Friday at the Hawaii Convention Center. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 4 JUNE 2017

WSA (Full Day): Sunday 08:00–17:00
100–1000GHz: Crossroads for New Design Paradigms Connecting Devices, Circuits, Systems and Applications

Sponsors: **RFIC, IMS**

Organizers: **Kaushik Sengupta**, *Princeton University, USA*
Goutam Chattopadhyay, *Jet Propulsion Laboratory, USA*

Abstract: The decade of frequency spectrum spanning 100 GHz to 1000 GHz has promised a plethora of novel applications ranging from communication to sensing, spectroscopy and high-resolution imaging. The spectrum has been successful in attracting rapt attention (and controversies in perhaps equal measure) from scientists and engineers who have been dedicated to finding the killer application with the right technology for many years. However, it is only in the last decade, that we have seen unprecedented improvement in the technology space that has allowed early demonstrations of fully integrated complex systems at these frequencies including chip-scale and wafer-scale phased arrays, multi-GB/s communication systems, imaging and spectroscopy, to name a few. Not surprisingly, at the intersection between microwave and infra-red frequencies, the underlying technology space also spans from solid-state devices (III-V, silicon, hybrid etc) to photonics-based approaches. Now that we are closer than ever before to a potentially diverse set of technology that can successfully address the spectrum, it is time to look into the future to gauge the prospects that lie ahead and ask fundamental questions: What are the unique opportunities in this frequency range and what is the right technology? Is this evolving spectral space comparable to what mm-Wave (below 100 GHz) was a decade ago? Are there unique design methodologies and paradigms cutting across the various layers of abstraction that can break the classical trade-offs in efficiency and scalability. In this workshop, we bring experts working across the technology space to understand the challenges and discuss these fundamental opportunities that can open up the spectrum for transformative technology in the coming decade.

Speakers:

1. "Advanced InP HEMT Technology for Terahertz Amplifier Circuits", **Richard Lai**, *Northrop Grumman, USA*
2. "Characterization and Scaling of Silicon Devices and Benchmark Circuits for mm-Wave and THz Applications", **Sorin P. Voinigescu**, *University of Toronto, Canada*
3. "Wafer-Scale CMOS for THz Sources and Phased-Array Transmitters", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*

4. "Circuit-Electromagnetics-Systems Co-Design for High-Performance Terahertz Chip-Scale Systems", **Kaushik Sengupta**, *Princeton University, USA*
5. "Interconnecting Technologies for Terahertz Components and Instruments", **Goutam Chattopadhyay**, *Jet Propulsion Laboratory, USA*
6. "Photonics-Enabled Terahertz Technologies and Their Applications", **Tadao Nagatsuma**, *Osaka University, Japan*
7. "Polymer Waveguides as an Alternative to Optical and Copper High-Speed Communication", **Patrick Reynaert**, *Katholieke Universiteit Leuven, Belgium*
8. "Beyond Active Terahertz Imaging in Silicon Technology", **Richard Hadi**, *University of California, Los Angeles, USA*

WSB (Full Day): Sunday 08:00–17:00
5G Communications Innovations: Connectivity for the Next Decade

Sponsors: **RFIC, IMS**

Organizers: **Edward Niehenke**, *Niehenke Consulting, USA*
Nuno Borges Carvalho, *Universidade de Aveiro, Portugal*
Alberto Valdes-Garcia, *IBM T.J. Watson Research Center, USA*
Laurent Dussopt, *CEA-TECH, France*
Roberto Gomez-Garcia, *Universidad de Alcalá, Spain*

Abstract: 5G communication is a unifying connectivity fabric for the next decade empowering new user experiences, connecting new industries and devices, enabling new services and delivering new levels of efficiency. This workshop will focus on technologies leading the 5G connectivity. An overview of the 5G communication system will be presented showing usage scenarios, enhanced broadband mobile, mission critical services, massive internet of things, standards and spectrum. Propagation, system design and performance of 5G millimeter wave mobile communications will be presented.

Speakers:

1. "Communications Innovations: Connectivity for the Next Decade and Beyond to 2030", **Upkar Dhaliwal**, *Future Wireless Technologies, USA*
2. "Millimeter Wave Mobile Communications: Propagation, System Design and Performance", **Ashwin Sampath**, *Qualcomm, USA*
3. "CLOUD RAN Approaches and the Path to All Digital Radios", **Arnaldo Oliveira**, *Instituto de Telecomunicações Aveiro, Portugal*
4. "MiEdge: Fusion of mmWave Access and Mobile Edge Computing for 5G", **Keii Sakaguchi**, *Fraunhofer HHI, Germany*
5. "Architectures and Circuits for 5G Base Station Transmitters", **Christian Fager**, *Chalmers University of Technology, Sweden*
6. "Power Amplifier Innovations for 5G System", **Sergio Pires**, *Ampleon, The Netherlands*

7. "CMOS mm-Wave PAs for 5G Communication", **Patrick Reynaert**, *Katholieke Universiteit Leuven, Belgium*
8. "Millimeter-Wave Phased-Arrays for 5G Systems", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*
9. "Antennas for Integration in Miniaturized Wireless Communication", **Mario Pauli, Thomas Zwick**, *Karlsruhe Institute of Technology, Germany*

WSC (Full Day): Sunday 08:00–17:00
5G mm-Wave IC Front-End Co-Design with Antenna, Packaging, and Testing for Future SOC Solutions

Sponsors: **RFIC, IMS**

Organizers: **Yanjie Jay Wang**, *Intel, USA*
Didier Belot, *CEA-LETI, France*
Hua Wang, *Georgia Institute of Technology, USA*

Abstract: The 5th generation wireless systems (5G) is proposed as the next major revolution of mobile wireless technologies. mm-Wave carriers and MIMO systems are expected to be extensively employed in 5G systems to achieve significantly enhanced data rate, spectral/spatial diversity/efficiency, and minimized system latency. High-performance mm-wave front-end integrated circuit design has always been a major technical challenge, and the inflexible 50ohm interface with antenna and packaging adds to such existing circuit challenges. In this full-day workshop, the speakers will demonstrate/discuss their recent innovations in the mm-Wave antenna and low-cost packaging designs as well as their co-designs with mm-Wave front-end circuits. Moreover, the sophisticate mm-wave testing for future System-on-Chip solutions is also discussed, as the cost of such industrial applications will be shared between the die, the package and the testing.

Speakers:
1. "Millimeter-Wave Phased-Arrays for 5G Systems", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*
2. "mm-Wave SiGe Power Amplifiers for 5G", **Domine Leenaerts, Mark van der Heijden**, *NXP Semiconductors, The Netherlands*
3. "Ultra-Broadband mm-Wave ICs for Next (5th) Generation Wireless", **Jacques C. Rudell**, *University of Washington, USA*
4. "Multi-Feed Antenna and On-Antenna Power Combining for High-Power High-Efficiency mm-Wave Transmitter", **Hua Wang**, *Georgia Institute of Technology, USA*
5. "Silicon-Based ICs and Organic Packaging/Antenna Solutions for 5G mmWave", **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center, USA*
6. "mmW Antenna Integrated Front-End IC-Module Co-Design and Testing for 5G Applications", **Debabani Choudhury**, *Intel, USA*
7. "Non-Invasive mmW Built-In Test Techniques", **Jose Luis Gonzalez**, *CEA-LETI, France*

8. "mmW Industrial Test Trends", **Dorine Gurney**, *Tektronix, USA*
9. "Rethinking mm-Wave Multi-Antenna Transceiver Design to Accommodate Both Beamforming and Diversity", **Payam Heydari**, *University of California, Irvine, USA*

WSD (Full Day): Sunday 08:00–17:00
Advanced Concepts and Architectures for Future RF and mmW Transceivers in Nanoscale CMOS

Sponsor: **RFIC**

Organizers: **Francois Rivet**, *University of Bordeaux, France*
Gernot Hueber, *NXP Semiconductors, Austria*

Abstract: With the advent of nano-scale CMOS technology, exciting new developments have recently taken place in the field of RF and mm-wave transmitters, receivers and frequency synthesizers. The low-voltage, fast speed, fine feature-size and low cost of the new technology have forever changed the way we design circuits, architectures and systems. Not only the RF/mm-wave circuits have taken different shapes from what has been taught in textbooks but also their integration with digital processors have enabled new possibilities for digital assistant. The motivation of this workshop is to capture what is the state at the edge of technology, what is the demand of the industry in the context of high volume products, as well, what are circuit and architectural concepts that are demanded or enforced by the technology. Hence, the idea is to capture and summarize the trends and directions RF design is heading to, which makes it highly valuable from early researchers to long time experienced experts as well as technology scouts., for instance because there may be strong unwanted signals between the carrier aggregation spectrum segments. This leads to new requirements and causes problems, for instance with respect to nonlinearity, crosstalk and LO pulling. This workshop will discuss these requirements and will primarily focus on advancements in RFIC transceiver architectures and circuits that enable carrier aggregation. It will also address some related aspects like broadband front ends, blocker detection, linearization, interference cancellation, etc.

Speakers:

1. "Design by Mathematics: A Novel Approach for the Design of RFICs in Nanoscale CMOS", **Francois Rivet**, *University of Bordeaux, France*
2. "Designing Energy Efficient Radios for Emerging Low Power Standards", **Ramesh Harjani**, *University of Minnesota, USA*
3. "Principles of Noise-Cancelling Receivers with Wide Dynamic Range", **Asad Abidi**, *University of California, Los Angeles, USA*
4. "A Wideband Single-PLL Multi-Channel and Multi-Band Car Radio Receiver with High-Resolution DS ADCs", **Lucien Breems**, *NXP Semiconductors, The Netherlands*
5. "mmWave Transceivers in Nanoscale CMOS", **Khaled Khalaf**, *imec, Belgium*
6. "5G Race for 1–10Gb/s — Cellular and/or mmWave, Friends and/or Foes?", **Aleksandar Tasic**, *Qualcomm, USA*

7. "Gigabit/s Over-the-Air Throughput in Nanoscale CMOS", **Renaldi Winoto**, *Marvell Semiconductor, USA*
8. "Multi-Standard RF and mmW Transmitters Based on Semi-Digital FIR-DAC", **Antoine Frappé**, *IEMN, France*

WSE (Full Day): Sunday 08:00–17:00
CMOSpace: Challenges and Accomplishments of Designing Advanced CMOS SoC for Space Communication and Instrumentation

Sponsors: **RFIC, IMS**

Organizers: **Tim LaRocca**, *Northrop Grumman, USA*
Bryan Wu, *Northrop Grumman, USA*

Abstract: Affordability is critical now for all space based electronics including the military, commercial and science industries. There is tremendous need for reliable RF and millimeter-wave CMOS System-on-Chip designs that reduce SWAP and cost to either fit in a 1U CubeSat dimension or operate on picowatts of power. The RF and microwave design community need to become familiar with the challenges of designing in space, so this workshop will address this need. While the digital ASIC community already has rad-hard by design (RHBD) libraries, the RF CMOS is behind in general understanding and test. We believe everyone from the foundry to system level designers need to understand the effects of radiation and the environment on space, as well as the current state-of-the-art in design. This is a highly relevant topic for all attendees.

Speakers:
1. "Requirements and Capabilities of the Standardized CubeSat Platform for Supporting CMOS SoC Development", **Adam Gunderson**, *Northrop Grumman, USA*
2. "Utilizing Advanced Semiconductor Device Technologies in the Natural Space Environment", **Jonny Pellish**, *NASA, USA*
3. "CMOS-Compatible SOI MESFETs for Extreme Environment Electronics", **Trevor Thornton**, *Arizona State University, USA*
4. "Designing with CMOS for space applications", **Anthony Amort**, *Boeing, USA*
5. "CMOS Systems-on-Chip for NASA Millimeter-Wave & THz Space Instruments", **Adrian Tang**, *Jet Propulsion Laboratory, USA*
6. "RHBD for Space — Addressing the Spectrum of Applications", **Michael Bear**, *BAE Systems, USA*
7. "Advanced Millimeter-Wave Package for Space and Beyond", **Jean-Marc Rollin**, *Nuvotronics, USA*

WSF (Full Day): Sunday 08:00–17:00
Efficiency Enhancement Techniques for Linear and High Bandwidth Power Amplifiers

Sponsor: **RFIC**

Organizers: **Ali Afsahi**, *Broadcom, USA*
Patrick Reynaert, *Katholieke Universiteit Leuven, Belgium*

Abstract: Increasing demand for higher data rate has forced the communication standards to use higher bandwidth and more complex modulation schemes which require a very linear power amplifier. Operating at back off power to meet linearity degrades efficiency significantly. This workshop covers various efficiency enhancement and linearization techniques for linear and high bandwidth power amplifiers.

Speakers:

1. "Physical Foundations and Practical Implementations of Efficient RF Power Amplifiers", **Earl McCune**, *RF Communications Consulting, USA*
2. "Si Envelope Tracking Power Amplifiers for High Peak-to-Average Power (PAPR) Signals", **Donald Kimball**, *Maxentric, USA*
3. "Switched-Capacitor Power Amplifiers for Efficient Digital RF Transmission", **Jeffrey Walling**, *University of Utah, USA*
4. "Digital Outphasing Techniques for Wideband WLAN Radios", **Paolo Madoglio**, *Intel, USA*
5. "Doherty Architecture for Mixed-Signal Power Amplifiers and mm-Wave Power Amplifiers", **Hua Wang**, *Georgia Institute of Technology, USA*
6. "A Self-Destructive Phenomenon Affecting High Efficient and High Bandwidth PA's Performance, the Memory Effect", **Farbod Aram**, *ProjectFT, USA*
7. "Digital Signal Processing Techniques for Efficient Power Amplifiers", **Paul Draxler**, *Qualcomm, USA*

WSG (Full Day): Sunday 08:00–17:00
Energy-Efficient RF Transceiver IC and System Design for Healthcare Applications

Sponsor: **RFIC**

Organizers: **Yao-Hong Liu**, *imec, The Netherlands*
Gernot Hueber, *NXP Semiconductors, Austria*

Abstract: The RF transceiver is typically one of the most power consuming building blocks in wireless sensor devices for different wearable/implantable healthcare monitoring, e.g., heart-rate monitor, capsule endoscope, etc. On the other hand, the efficiency of the RF transceiver has been dramatically reduced in the past few years, thanks to both CMOS technology scaling and the development of the new low-power/low-voltage digital-intensive design approaches, which enables many new wireless healthcare applications. In this workshop, we will discuss several latest wireless technologies for these applications, including Bluetooth Low Energy, Medical Implantable Communication Services (MICS), Body channel communication, and wideband wireless interface for neural recording/stimulation. The experts from both industrial and academic will introduce the topics from market, potential market, to regulations. In addition, this workshop will especially focus on the discussion of various design challenges, system requirements and potential solutions in developing energy-efficient transceiver ICs for the healthcare applications.

Speakers:

1. "ULP Wireless Technologies in the Healthcare Domain", **Christian Bachmann**, *imec, The Netherlands*
2. "A Body Channel Communication (BCC) Transceiver Design for Wireless Body Area Network (WBAN)",**Hyunwoo Cho**, *KAIST, Korea*
3. "Radar-Based Health Monitoring: System Requirement, Recent Advances, and Design Challenges", **Marco Mercuri**, *imec, The Netherlands*
4. "Bluetooth Low Energy Communication for Implantable Medical Devices", **Perry Li**, *St. Jude Medical, USA*
5. "Ultra-Low Power Radio and Antenna Design for Cubic-mm Sensor Nodes", **David Wentzloff**, *University of Michigan, USA*
6. "An Ultra-Low-Power IEEE802.15.6/Proprietary Mode Radio SoC for Medical Applications",**Kazuaki Oishi**, *Fujitsu Laboratories, Japan*
7. "Wireless Bioelectronics", **Ada Poon**, *Stanford University, USA*

WSH (Full Day): Sunday 08:00–17:00
Frequency Synthesis and Clock Distribution for Massive MIMO and Phased-Arrays in 5G Communication Systems and Beyond

Sponsor: **RFIC**

Organizers: **Jeyanandh Paramesh**, *Carnegie Mellon University, USA*
Xiang Gao, *Credo Semiconductor, USA*
Jaber Khoja, *IDT, USA*

Abstract: Next generation communication systems (5G and beyond) seek to bridge the gap between the projected demand and supply of mobile data traffic through a combination of new system techniques and access to new spectrum below 6 GHz and especially in several millimeter-wave bands from 15 GHz to 86 GHz. In these systems, the design of frequency synthesizers that can access several such bands with low phase noise, spur levels and frequency granularity remains a critical block. Furthermore, "Massive MIMO" — which consists of a large number of antennas at the access point — is a promising technology to meet the high data rate and quality of service requirements of 5G wireless systems. Achieving stringent phase-noise specifications and scalable LO distribution to maintain phase coherence across the different units in the MIMO array is a critical challenge. This workshop will present the latest trends in the design of such synthesizers

Speakers:

1. "Phase Noise Limits of On-Chip mm-Wave Oscillators", **Hossein Hashemi, Alireza Imani**, *University of Southern California, USA*
2. "A 2–26 GHz Highly Flexible Synthesizer in 32nm SOI CMOS", **Bodhisatwa Sadhu**, *IBM T.J. Watson Research Center, USA*
3. "On CMOS Clock Generation with Low Phase Error", **Eric Klumperink**, *University of Twente, The Netherlands*
4. "Design Consideration of Integrated Frequency Synthesizers in CMOS SOCs", **Sheng Ye**, *MaxLinear, USA*
5. "Frequency Synthesis and Clock Distribution Techniques for Phased-Array Technology and Massive MIMO", **Arun Natarajan**, *Oregon State University, USA*
6. "CMOS mm-Wave Phased-Array Frequency Synthesis", **Howard Luong**, *HKUST, China*
7. "All-Digital PLL Based Frequency Synthesis", **Ashoke Ravi**, *Intel, USA*
8. "Digital Loop Filter Architectures for Millimeter Wave Frequency Synthesizers Based on ALL Digital PLL Single Bit Binary Phase Detection", **Pasquale Lamanna**, *Huawei Technologies, France*
9. "Component Design for Millimeter-Wave All-Digital Phase-Locked Loops", **Jeyanandh Paramesh**, *Carnegie Mellon University, USA*

WSI (Half Day): Sunday 08:00–12:00
Frontiers of Superconducting and Cryogenic Microwave Electronics

Sponsors: **RFIC, IMS**

Organizers: **Michael C. Hamilton**, *Auburn University, USA*
Daniel E. Oates, *MIT Lincoln Laboratory, USA*

Abstract: Recent years have seen renewed interest and increase in efforts directed towards development of technology for high-frequency (microwave and beyond) and high-speed superconducting and cryogenic electronics systems. The discovery of superconductivity is recognized as an IEEE Milestone in Electrical and Computer Engineering and has made possible many important applications across a wide range of disciplines. Cryogenic electronics holds the promise of high performance and super-low energy per operation for computing applications, that can take us beyond the end of the semiconducting technology roadmap. Driven by goals of ultra-high speed computing and signal processing, super-sharp and low-loss filters, higher performance MRI/NMR systems and integration with computing or imaging systems that must be cryogenically cooled due to noise constraints, there is a growing interest in active and passive microwave components designed for operation at low temperatures. Historically, despite the potential of higher performance from cryogenic components and systems, conventional technologies have provided sufficient performance. There are, however, reasons to believe that this situation may change in the near future. As one example, consider the case of superconducting quantum computing, where communication between qubits occurs through signals in the microwave regime and where the noise constraints are of utmost importance. Proper communication, control and integration of systems such as this will require superconducting and cryogenic microwave technology advancements that are now in development. This workshop aims to provide a sufficiently detailed description and platform for discussion of the current status and future of superconducting and semiconducting electronics for cryogenic systems. Talks in this workshop will cover: RF MEMS + superconducting filters, HTS filters, superconducting filters for resonance imaging systems, advances in superconducting microwave technology in Japan and China, superconducting microwave interconnect technology, recent superconducting device technology developments for mixed-signal circuits, recent cryogenic semiconducting device technology developments and cryogenic electronics for quantum computing systems.

Speakers:

1. "Prospect of Cryogenic Digital Technology", **Akira Fujimaki**, *Nagoya University, Japan*
2. "Superconducting Microwave Mixed-Signal Circuits", **Deepnarayan Gupta**, *HYPRES, USA*
3. "Developments in China for the Design and Application of High Temperature Superconducting (HTS) Filters", **Yusheng He**, *Chinese Academy of Sciences, China*
4. "MEMS-Based Superconductor Tunable Filters", **Raafat R. Mansour**, *University of Waterloo, Canada*
5. "Microwave Surface Resistance of Ion-Implanted YBCO Thin Films in High Magnetic Field and Development of NMR Pickup Coils Using YBCO Thin Films", **Shigetoshi Ohshima**, *Yamagata University, Japan*

6. "Cryogenic Hardware at the Quantum-Classical Interface", **David Reilly**, *University of Sydney, Australia*
7. "Flexible Superconducting Microwave Transmission Line Interconnects", **Michael C. Hamilton**, *Auburn University, USA*

WSJ (Half Day): Sunday 13:00–17:00
High Performance Power Efficient Clock Generation for Internet of Things Applications

Sponsor: **RFIC**

Organizers: **Hiva Hedayati**, *Applied Micro, USA*
Salvatore Levantino, *Politecnico di Milano, Italy*

Abstract: Internet of Things (IoT) applications are becoming a reality that will sense and actuate the world around us. IoT presents semiconductor industries with a market opportunity that may exceed that of all previous processing classes. In many cases battery-operated satellite nodes face a performance and power paradox challenge that is driving the need for a new type of low-power clock generation. The workshop will introduce various timing technologies to enable the lowest power consumption with acceptable accuracy and smaller size. Fully integrated phase-lock loop (PLL) solutions are considered more attractive compared to expensive bulky crystal oscillators. The workshop will also focus on MEMS timing solutions or other leading technologies to enable far more compact high performance designs.

Speakers:
1. "Energy-Efficient Radio Links for IoT Applications", **Jagdish Pandey**, *Qualcomm, USA*
2. "Scalable Synchronization for Duty-Cycled Radio Networks", **Rajeev Dokania**, *Intel, USA*
3. "Efficient Clock Multiplication", **Ahmed Elkholy**, *Univeristy of Illinois at Urbana-Champaign, USA*
4. "Ultra-Low-Power RC Oscillators", **Patrick Mercier**, *University of California, San Diego, USA*
5. "Fast Startup Techniques", **Christian Enz**, *EPFL, Switzerland*

WSK (Half Day): Sunday 08:00–12:00
Highly Digital CMOS Transmitters with Embedded Power Amplifiers

Sponsors: **RFIC, IMS**

Organizers: **Jeffrey Walling**, *University of Utah, USA*
Hua Wang, *Georgia Institute of Technology, USA*

Abstract: In recent years, RF front-end transmitters with direct digital interfaces have become common for low-to-moderate power wireless systems (e.g. Bluetooth, Wi-Fi, etc.). These transmitters include up-conversion, filtering and output power amplifier stages. They are capable of generating ~1 W of output power with very good total system efficiency. Furthermore, they provide flexibility for software defined systems that allow quick re-configuration via software programming. Additionally, they are compact, often requiring areas less than 1mm2. In this workshop, we will examine three main types of digital transmitters: outphasing based pulse-width modulation, switched-capacitor power amplifiers and current-mode digital power amplifiers. Additionally, there are many different architectures that utilize each of the above topologies, including class-G, polar, outphasing and multiphase. The presenters will provide examples of these architectures and provide insight into their designs and the scenarios in which their use is optimal.

Speakers:

1. "A Switched Capacitor Power Amplification Technique for Energy- and Area-Efficient Wireless Transmitters", **Sangmin Yoo**, *Michigan State University, USA*
2. "RF Transmitter Based on Cartesian RFDAC", **Bumman Kim**, *POSTECH, Korea*
3. "SCPAs and the (R)evolution from Polar to Multiphase Transmitters", **Jeffrey Walling**, *University of Utah, USA*
4. "Hybrid Broadband PA Architecture Leveraging RF Power DACs", **Hua Wang**, *Georgia Institute of Technology, USA*
5. "Impedance Modulation in Digitally Modulated Polar Power Amplifiers for Wireless Applications", **Debopriyo Chowdhury**, *Broadcom, USA*
6. "Digitally-Modulated CMOS Polar Transmitters for Highly-Efficient mm-Wave Wireless Communication", **Khaled Khalaf**, *imec, Belgium*
7. "Pulse-Width Modulation Based Transmitter Architectures for Wireless Applications", **Ranjit Gharpurey**, *University of Texas, USA*

WSL (Half Day): Sunday 08:00–12:00
Microwave thru Sub-THz Imaging and Sensor Array Technology for Security, Industrial, Commercial and Medical applications

Sponsor: **RFIC**

Organizers: **Ed Balboni**, *Analog Devices, USA*
Brian Floyd, *North Carolina State University, USA*

Abstract: Advances in silicon technology now provides the ability to economically build large arrays operating in the microwave to THz frequencies supporting bandwidths in the 10GHz-100GHz range. This workshop will include presentations on state of the art sensor arrays. Included will be systems targeted toward security, industrial, commercial and medical applications.

Speakers:

1. "THz Medical Imaging with RF technology", **Zackary Taylor**, *University of California, Los Angeles, USA*
2. "Wideband Transmitters and Receivers for High Resolution Imaging", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*
3. "Rotational Spectroscopy with Low Cost CMOS mmW Sensors", **Navneet Sharma**, *University of Texas at Dallas, USA*
4. "Carrier Distribution and Synchronization for Radar and Imaging Arrays", **Adrian Tang**, *Jet Propulsion Laboratory, USA*
5. "Advances on Spectro and Terahertz Imaging: from Sources to Applications", **Patrick Mounaix**, *University of Bordeaux, France*

WSM (Full Day): Sunday 08:00–17:00
Millimeter Wave for 5G: Which Systems with Which Frequency Band – 5G RF Transceiver Design and System Aspects

Sponsor: **RFIC**

Organizers: **Pierre Busson**, *STMicroelectronics, France*
Andre Hanke, *Intel, Germany*

Abstract: In the last two decades data-rates in wireless communication systems have been increasing exponentially. This trend is continuing with the fifth generation of wireless systems (5G) that will require peak rates in excess of Gb/s for many users, several hundred thousands of simultaneous connections for massive sensor deployments, and substantially improved spectral efficiency. This Workshop is focused on current state-of-the-art of 5G band and future directions of the key circuit techniques and system architectures for base station or between the Handset, or other portable devices, and the cell, or mini-cell, micro-cell, pico-cell base stations. All aspects covering

normalization Systems, Architecture, and low power design solutions for beam orientation will be discussed.

Speakers:

1. "Why Should 5G Go for mmWave (e.g. 28GHz)?", **Uwe Rüddenklau**, *Infineon Technologies, Germany*
2. "Millimeter-Wave Systems for 5G", **Brian Floyd**, *North Carolina State University, USA*
3. "5G System and Design by Intel", **Jonathan Jensen**, *Intel, USA*
4. "Requirements on Power Amplifiers and PLLs for 5G at mmW Frequencies", **Lars Sundstrom**, *Ericsson, Sweden*
5. "Industrial Packaging & Antenna for Consumer Grade mm-Wave Products", **Frederic Gianesello**, *STMicroelectronics, France*
6. "Phased Arrays for 5G Systems at 28 GHz and 60 GHz", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*
7. "Millimeter-Wave Transceiver System Design for 5G Mobile Network", **Kenichi Okada**, *Tokyo Institute of Technology, Japan*
8. "5G Operator Vision by Samsung UK", **Maziar Nekovee**, *University of Sussex, UK*

WSN (Full Day): Sunday 08:00–17:00
Passive Integrated Circuits

Sponsors: **RFIC, IMS**

Organizers: **Xun Luo**, *UESTC, China*
Roberto Gomez-Garcia, *Universidad de Alcalá, Spain*
Guoan Wang, *University of South Carolina, USA*

Abstract: With the ever-increasing advances on the field of modern wireless communications technologies-e.g., 5G and internet-of-things (IoT)-, the design of compact and multi-functional transceivers to meet the stringent requirements demanded by such systems remains as a great challenge. In this context, high-performance integrated passive devices (IPDs) are considered key building circuits for their development. These components are based on novel miniaturized structures and specific technologies that can be utilized for the implementation of RF, microwave, millimeter-wave, and THz communication systems. This unique workshop focuses, for the first time, on the area of IPDs and their applications in the context of wireless-communications and sensing scenarios by reporting recent research findings in this exciting field. This includes current progresses about fully-electrically tunable RF passives based on the nano-patterned ferroelectric and ferromagnetic thin films technology, as well as new high-Q micro-electromechanical-system (MEMS) for spectrally-agile filter implementations with wide-band operation, switches, and phase shifters. Miniaturized passive circuits that are integrated with BST technology for the development of reconfigurable IPDs are presented. Furthermore, novel on-chip passive circuits for performance improvement of active circuits using advanced CMOS and SiGe processes are reviewed. Their practical application goes from RF-to-THz bands. Metamaterial-inspired and plasmonic devices are also introduced for compact CMOS passive integration. In addition, multi-function filtering components and integrated antenna

sub-system, along with hybrid acoustic-wave-lumped-element-microwave-resonator technologies for the realization of advanced compact microwave filtering devices, are described. Finally, the last advances in the area of RF and microwave passive microsystems for gas/chemical, biological, and nanomaterial-characterization sensing applications are also expounded.

Speakers:

1. "Integration of Nano-Patterned Ferroelectric and Ferromagnetic Thin Films for Fully Electrically Tunable RF Passives", **Guoan Wang**, *University of South Carolina, USA*
2. "On-Chip Integrated Passive Circuits for RF, Microwave, mm-Wave, and THz Application", **Xun Luo**, *UESTC, China*
3. "Towards CMOS THz Electronics: Metamaterial and Plasmonic Devices", **Hao Yu**, *Nanyang Technological University, Singapore*
4. "How Can RF MEMS be as Successful as Other MEMS?", **James C.M. Hwang**, *Lehigh University, USA*
5. "High-Power Handling Hot-Switching RF-MEMS Switches", **Xiaoguang Liu**, *University of California, Davis, USA*
6. "High-Q Miniature Integrated Passive Devices", **Raafat R. Mansour**, *University of Waterloo, Canada*
7. "Hybrid Acoustic-Wave-Microwave-Resonator Technologies for High-Performance Microwave Filters", **Dimitra Psychogiou**, *University of Colorado Boulder , USA*
8. "Dielectric Spectroscopy and RF and Microwave Passive Microsystems for Biological Application and Discrimination of Cells", **Arnaud Pothier**, *XLIM, France*
9. "Microwave Resonators for Sensing Applications", **Mojgan Daneshmand**, *University of Alberta, Canada*

WSO (Half Day): Sunday 13:00–17:00
Polar, ET, Outphasing, Doherty, Predistortion…: Which One Survives at mm-Wave Frequencies?

Sponsor: **RFIC**

Organizers: **Patrick Reynaert**, *Katholieke Universiteit Leuven, Belgium*
Ali Afsahi, *Broadcom, USA*

Abstract: Various PA linearization and efficiency enhancement techniques exist. Their applicability in a certain situation depends on various factors such as operating frequency, power level, thermal constraints, operating voltage, dynamics of the signals, bandwidth, … Today, there is a clear shift towards higher frequencies and the importance of communication systems operating above 20GHz is rising. At these frequencies, the goal is to exploit the high available bandwidths to achieve very high data rates. Within this context, this workshop will have a closer look into mm-wave systems and Silicon technologies, and then explore which PA techniques are most suited for wideband mm-wave systems. It will give the audience an excellent overview of the pros and cons of each technique.

Speakers:

1. "Comparison of PA Efficiency Enhancement Techniques at RF and mm-Wave Frequencies", **Dixian Zhao**, *Southeast University, China*
2. "mmW RF Pre-Distortion Linearization for Multi-GHz Broadband PA Applications", **Tian-Wei Huang**, *National Taiwan University, Taiwan*
3. "CMOS Doherty PAs at mm-Wave Frequencies", **Patrick Reynaert**, *Katholieke Universiteit Leuven, Belgium*
4. "mm-Wave Switching Power Amplifiers", **Hossein Hashemi**, *University of Southern California, USA*

WSP (Half Day): Sunday 13:00–17:00
Recent Advances in Microwave Noise: From Device Modeling to Network Design and Characterization

Sponsors: **RFIC, IMS**

Organizer: **Luciano Boglione**, *Naval Research Laboratory, USA*

Abstract: This workshop introduces and thoroughly reviews recent advances made in the broad field of microwave noise, from device modeling to measurement techniques. In the first talk, for the purpose of comparison of different technologies such as HFETs, CMOS, HBTs their noise models are reviewed with emphasis on their common noise properties. Certain limits on the allowable values of transistor noise parameters are established and possible limits of low noise performance upon further scaling of gate or emitter size discussed. Widely published concepts in the treatment of noise in transistors and amplifiers, amongst those "gate induced noise" in FETs, wideband low noise amplifier design, CMOS "noise cancelling" amplifiers, are critically examined. The second talk reviews standard techniques to determine the noise performance of 2 port microwave networks, including a recent procedure extending the noise parameters characterization to N port linear networks. The implications to the measurement of differential amplifiers will be addressed. Then, the talk will focus on a novel, tuner-less procedure particularly suited for the determination of on-wafer microwave transistor noise parameters because solely based on transistor size. The third talk discusses the paradoxes of mixer noise characterization, shows how well established noise characterization methods can be applied to mixers, and presents established and advanced methods for optimizing mixer noise figure in both passive and active mixer circuits. Finally, the last talk addresses the question of how to simulate noise in nonlinear circuits. After an introduction on how nonlinear effects such as upconversion of 1/f noise are simulated in time and frequency domains, special emphasis is placed on modeling GaAs and InP HBTs and GaN HEMTs. The talk will also discuss how nonlinear excitations may impact the properties of flicker and white noise sources from the physical standpoint, and how to reflect this behavior in a large-signal transistor model.

Speakers:

1. "On the General Noise Properties of Low Noise Microwave Transistors and Amplifiers", **Marian Pospieszalski**, *National Radio Astronomy Observatory, USA*
2. "Measuring Microwave Noise: From Standard to Advanced Techniques", **Luciano Boglione**, *Naval Research Laboratory, USA*
3. "Noise in Mixers", **Steve Maas**, *Nonlinear Technologies, USA*
4. "Simulating Noise in Nonlinear Circuits", **Fabrizio Bonani**, *Politecnico di Torino, Italy*

WSQ (Full Day): Sunday 08:00–17:00
RFIC Design Challenges for the IoT at Scale

Sponsor: **RFIC**

Organizers: **Nathan Roberts**, *PsiKick, USA*
Haolu Xie, *ZTE, USA*

Abstract: In 2008 the number of "things" connected to the internet surpassed the number of people living on earth and by 2020 the number of "things" is predicted to reach beyond 50 billion on the way to trillions. The potential for the Internet of Things (IoT) and its ubiquitous computing reality is staggering, but limited in present day by many technical challenges. This workshop will look at two contradictory technical challenges to the IoT vision: wireless communication at scale and low power energy efficient circuit design. The workshop will begin with an overview of present day and upcoming wireless standards used for IoT and will discuss challenges as well as introduce novel approaches for supporting large scale sensor networks. The second part of the workshop will discuss the RFIC system and circuit design landscape for the IoT highlighting the intersection of challenges presented by the previous discussions and the need for low power and energy efficient systems. The workshop will help participants understand the complexity of the challenges presented by the IoT as well as an appreciation for the novelty that will arise from it.

Speakers:

1. "Cross-Layer Optimized, Ultra-Low Power Wireless Communication Solutions for Energy-Constrained Internet-of-Things", **Hun-Seok Kim**, *University of Michigan, USA*
2. "An Overview of Wireless Standards for the IoT", **Christian Bachmann**, *imec, The Netherlands*
3. "NB-IoT for a Better Connected World", **Sam Zhang**, *ZTE, China*
4. "Energy-Efficient Phase-Domain Receiver Design for IoT", **Yao-Hong Liu**, *imec, The Netherlands*
5. "RFICs for Energy Autonomous Sensor Nodes", **Nathan Roberts**, *PsiKick, USA*
6. "Battery-Free Computing and Communication", **Shyam Gollakota**, *University of Washington, USA*
7. "Design of Ultra-Low-Power Spectrally-Efficient Radios", **Patrick Mercier**, *University of California, San Diego, USA*

WSR (Full Day): Sunday 08:00–17:00
RFIC Design for Automotive Radar

Sponsor: **RFIC**

Organizers: **Franz Dielacher**, *Infineon Technologies, Austria*
Gernot Hueber, *NXP Semiconductors, Austria*

Abstract: Recent advances in microwave and millimeter-wave silicon technology have drawn strong interest in the RF community for applications like safety, radar, and communications systems. The goal of this workshop is to provide an in-depth coverage of state of the art and future development trends specifically for FMCW and pulse radars, MIMO and novel CMOS-based architectures and solutions. This includes silicon solutions from 24GHz to 240GHz with an emphasis on automotive radar in the 77 to 79GHz frequency range as highest volume example of commercial millimeter-wave application. Distinguished speakers from industry and academia will highlight system requirements, technology advances, challenges and solutions for implementations on system and silicon level.

Speakers:

1. "System Architecture Concepts of ADAS Systems for Autonomous Vehicles", **Holger Meinel**, *Consultant (Daimler), Germany*
2. "RFIC Concepts for Future Integrated Automotive Radar Sensors", **Rainer Stuhlberger[1,2]**, *[1]DICE, Austria, [2]Infineon Technologies, Austria*
3. "CMOS Circuit and System Techniques for mmWave MIMO Radar", **Harish Krishnaswamy**, *Columbia University, USA*
4. "Phased-Arrays for High-Resolution Automotive Radar Systems", **Gabriel M. Rebeiz**, *University of California, San Diego, USA*
5. "Circuits and Systems of Millimeter-Wave Automotive Radars", **Jri Lee**, *National Taiwan University, Taiwan*
6. "Transceiver for Automotive Radar Applications", **Angelo Scuderi**, *STMicroelectronics, Italy*
7. "GHz Radar SoC Integration in 28nm CMOS", **Andre Bourdoux**, *imec, Belgium*
8. "28nm CMOS mmWave Building Blocks for Wideband Automotive Radar Applications", **Nader Rohani, Sergio Pacheco**, *NXP Semiconductors, USA*

WSS (Full Day): Sunday 08:00–17:00
RFIC Design in CMOS FinFET and FD-SOI

Sponsor: **RFIC**

Organizers: **Magnus Wiklund**, *Qualcomm, USA*
Gernot Hueber, *NXP Semiconductors, Austria*

Abstract: Both, CMOS FinFET and FD-SOI are the enabling technology that allows nanoscale CMOS beyond 20nm. This technological revolution does not only allow highest integration density for high volume products at low cost. Due to the fundamental change how a transistor is built, there is impact on its characteristics as e.g., Ft, Vt, VDD. Considering this change, traditional and well-known circuits and architectures need to adapted or even be invented for FinFET. This workshop shall give an overview of novel architectures and designs in the context of RF that benefit from latest CMOS FinFET and FD-SOI technology. In several presentations trends, design challenges, and how these are overcome supported by application/circuit examples shall be shown.

Speakers:

1. "CMOS FD-SOI Technology and Benefits for RF", **David Harame**, *GLOBALFOUNDRIES, USA*
2. "GPS SoC's in FD-SOI", **Ken Yamamoto**, *Sony Semiconductor Solutions, Japan*
3. "Analog RF mmW Design with FD-SOI", **Andreia Cathelin**, *STMicroelectronics, France*
4. "Ultra-Low-Voltage Wideband Transmitter and LNA in FD-SOI", **David Bol**, *Université catholique de Louvain, Belgium*
5. "RF Synthesizers for Wide Area IoT SoC's in FD-SOI", **Stephen Allott, Chi Zhang**, *GLOBALFOUNDRIES, USA*
6. "RF and mm-Wave Design in FD-SOI CMOS Technologies", **Sorin P. Voinigescu,** *University of Toronto, Canada*
7. "RF Data Converters in 16nm FinFET for Wireless and Wired Infrastructure Applications", **Brendan Farley**, *Xilinx, Ireland*
8. "Design Challenges of RF/Analog Circuits Operating in a Hostile Digital Environment — Case Study of a Low Jitter PLL in 10nm FinFET", **Philip Kwan**, *Oracle, USA*
9. "Noise Cancelling LNAs in FinFET Technology", **Stephen Weinreich**[1,2], [1]*Stanford University, USA,* [2]*GLOBALFOUNDRIES, USA*
10. "RF Circuits in 14nm FinFET", **Edwin Thaller**[1], **Yorgos Palaskas**[2], [1]*Intel, Austria,* [2]*Intel, USA*

WST (Half Day): Sunday 13:00–17:00
RF-Inspired Silicon Photonic

Sponsor: **RFIC**

Organizer: **Hossein Hashemi**, *University of Southern California, USA*

Abstract: Advancements in silicon semiconductor processing enables silicon photonics integrated circuits (PIC) for applications including communication, imaging, sensing, and display. The level of integration and complexity in PICs has lacked those of RF and microwave integrated circuits (IC). This workshop brings leading researchers to cover the latest developments in the design and implementation of complex PICs that are inspired by the systematic design and verification of RFICs.

Speakers:

1. "Silicon-Photonics for Energy-Efficient Data Communication", **Azita Emami**, *California Institute of Technology, USA*
2. "Linear Microwave Photonic Techniques for Silicon Photonic Integrated Circuits", **James Buckwalter**, *University of California, Santa Barbara, USA*
3. "Electronically Assisted Optical Synthesis, Stabilization, and Phase Noise Reduction", **Firooz Aflatouni**, *University of Pennsylvania, USA*
4. "Examples of Hybrid Electronics and Photonics ICs: Optical Phased Arrays, Equalization, and RF Power Generation", **Ali Hajimiri**, *California Institute of Technology, USA*
5. "Monolithic Optical Phased Arrays", **Hossein Hashemi**, *University of Southern California, USA*

WSU (Half Day): Sunday 08:00–12:00
The Many Flavors of CMOS/Bipolar RF Harmonic Oscillators

Sponsor: **RFIC**

Organizers: **Pietro Andreani**, *Lund University, Sweden*
Mohyee Mikhemar, *Broadcom, USA*

Abstract: Recent developments in the art of integrated CMOS/bipolar oscillator design have witnessed the introduction of new topologies — class-C, class-F, class-F2, clip and restore, and other still unnamed – that complement well-known and much appreciated architectures such as the beloved class-B (in its many variations) and Colpitts. This workshop offers an overview of all these oscillators, bringing some clarity on the pros and cons of each.

Speakers:

1. "Common-Mode Resonance in LC Oscillators", **David Murphy**, *Broadcom, USA*
2. "Class-F and Switching Current-Source CMOS Oscillators", **Masoud Babaie**, *Technische Universiteit Delft, The Netherlands*

3. "The Good, the Bad and the Ugly of Bipolar Voltage-Controlled Oscillators", **Andrea Bevilacqua**, *University of Padova, Italy*
4. "Fundamental Limitations in RF and mm-Wave Harmonic Oscillators", **Danilo Manstretta**, *University of Pavia, Italy*
5. "The Insider Guide to Designing mm-Wave Silicon VCOs", **Waleed Khalil**, *Ohio State University, USA*

SUNDAY SHORT COURSE – 4 JUNE 2017

SSA (Full Day): Sunday 8:00–17:00
Introduction to Solid-State Power Amplifier Design and Considerations for Space-Borne Applications

Sponsor: **IMS**

SSB (Half Day): Sunday 8:00–12:000
Principles of Solid-State Microwave and RF Control for Circuit Reconfigurability

Sponsor: **IMS**

SSC (Full Day): Sunday 8:00–17:000
From Bits to Waves: Building a Modern Digital Radio in 1 Day

Sponsor: **IMS**

MONDAY WORKSHOPS – 5 JUNE 2017

WMA (Full Day): Monday 08:00–17:00
Advanced Microwave Technologies for Internet of Space Applications

Sponsor: **IMS**

WMB (Half Day): Monday 13:00–17:00
Digital-Intensive Wireless Transmitters for 4G/5G Broadband Mobile Communications

Sponsors: **RFIC, IMS**

Organizers: **Rui Ma**, *MERL, USA*
SungWon Chung, *University of Southern California, USA*

Abstract: Multiband multimode operation and massive multi-input multi-output (MIMO) technology are essential to 4G/5G mobile communications. As an alternative to conventional RF/analog transmitters, all or almost-all digital transmitters are gaining increasing interests since they enable low-cost implementation in a compact form-factor for broadband and flexible operation. Conventionally, the implementations of digital transmitters and digital power amplifiers were mostly limited to silicon based technologies. In recent times, several new attempts using advanced signal processing techniques have been reported, with all-digital high-efficiency power amplifiers in compound semiconductors as well as in silicon. This workshop overviews these recent advancements on digital-intensive wireless transmitter R&D for both base-stations and mobile devices. The focus will be on the digital signal processing techniques and related digital-intensive transmitter circuits and architectures for advanced modulation, linearization, spur cancellation, high efficiency encoding, and parallel processing.

Speakers:

1. "Digital Transmitters for the Wireless Infrastructure", **Wolfgang Heinrich**, *FBH, Germany*
2. "Linear and Efficient Digital Transmitters for Future Mobile Communication", **Shinichi Hori**, *NEC, Japan*
3. "Advanced Power Encoding and Non-Contiguous Multi-Band Digital Transmitter Architectures", **Rui Ma[1], SungWon Chung[2]**, *[1]MERL, USA, [2]University of Southern California, USA*
4. "All Digital Antenna Array Transmitter for Massive MIMO", **Jose Vieira**, *Universidade de Aveiro, Portugal*
5. "Digital Transmitter Architectures for Wireless Handsets — Trends, Opportunities and Challenges", **Chih-Ming Hung**, *MediaTek, Taiwan*

6. "28GHz PAs and RF-DAC in UTBB 28nm FD-SOI CMOS for Massive MIMO Systems", **Markus Törmänen**, *Lund University, Sweden*
7. "Capacitive-DAC Based Transmitter Architectures: Modeling and Digital Pre-Processing", **Mario Huemer**, *Johannes Kepler Universität Linz, Austria*
8. "Encoding Mobile Communication Signals for Switch-Mode Systems", **Daniel Markert**, *FAU Erlangen-Nürnberg, Germany*

WMC (Full Day): Monday 08:00–17:00
Emerging Applications of THz

Sponsor: **IMS**

WMD (Half Day): Monday 13:00–17:00
FFlexible Devices, Circuits and Systems Solutions to RF and mmW Front-Ends for 5G Cellular Communications

Sponsor: **IMS**

WME (Half Day): Monday 08:00–12:00
Front End Module (FEM) for 5G

Sponsors: **RFIC, IMS**

Organizers: **Roberto Quaglia**, *Cardiff University, UK*
Vittorio Camarchia, *Politecnico di Torino, Italy*
Anh-Vu Pham, *University of California, Davis, USA*

Abstract: In this workshop, speakers from leading industries and universities will present state-of-the-art results in the framework of 5th mobile generation (5G) front-end modules (FEMs). Several aspects regarding FEMs will be covered, from the motivations that drive their development to advanced testing. In the first talks, the main trends and challenges for FEMs will be shown from the stand-point of a regulatory body and commercial aspects will be highlighted. Results regarding the design of energy efficient FEMs will be presented considering both compound and silicon technologies, focusing on the pros- and cons- deriving from integration. Integrated solutions for millimetre-wave integrated circuits will be described, carefully evaluating the consequences of increasing centre frequency and bandwidth. Some aspects regarding packaging technologies will be also presented. The important aspect of RX/TX isolation will be also faced, with a description of integrated circulator/isolator solutions based on linear periodic time-varying circuits.

Speakers:

1. "The Trends and Challenges of Microwave/Millimeter-Wave in Future 5G Wireless Communication Networks", **Maurizio Pagani**, *Huawei Technologies, Italy*
2. "High Efficiency Power Amplifiers and Front-End Module Circuits for 5G Wireless Communications", **Anh-Vu Pham**, *University of California, Davis, USA*
3. "Advances in High Performance Cost Effective MMIC and SMD from V to D-Band", **Marcus Gavel**, *Gotmic, Sweden*
4. "Analog Front End Modules for 5G", **Peter Singerl**, *Infineon Technologies, Austria*
5. "RF SOI Technology for PA/FEM Integration", **Alexandre Giry**, *CEA-LETI, France*
6. "Breaking Lorentz Reciprocity: Non-Reciprocal Integrated Front-End Circulators and Isolators Based on Linear Periodic Time-Varying (LPTV) Circuits", **Harish Krishnaswamy**, *Columbia University, USA*

WMF (Half Day): Monday 13:00–17:00
High Power WPT

Sponsor: **IMS**

WMG (Full Day): Monday 08:00–17:00
New Developments in Microwave Measurements for Planar Circuits and Components

Sponsors: **IMS, ARFTG**

WMH (Half Day): Monday 08:00–12:00
Non-Doherty Load-Modulated PAs

Sponsor: **IMS**

WMI (Full Day): Monday 08:00–17:00
Novel 5G Applications of Nonlinear Vector Network Analyzer for Broadband Modulation and Millimeter Wave Characterization

Sponsors: **IMS, ARFTG**

WMJ (Full Day): Monday 08:00–17:00
PAs for 5G Mobile Communication: Technologies and Challenges

Sponsor: **IMS**

WMK (Full Day): Monday 08:00–17:00
RF and Optical Techniques for Non-Contact and Wearable Health Monitoring

Sponsor: **IMS**

WML (Half Day): Monday 08:00–12:00
RF to/from Bits: Challenges in High Frequency Mixed Signal Measurements and Design

Sponsor: **IMS**

WMM (Full Day): Monday 08:00–17:00
Silicon Technologies for mmWave Applications

Sponsors: **RFIC, IMS**

Organizers: **David Harame**, *GLOBALFOUNDRIES, USA*
Ned Cahoon, *GLOBALFOUNDRIES, USA*
Anirban Bandyopadhyay, *GLOBALFOUNDRIES, USA*

Abstract: Silicon technologies have made great strides and are now mainstream for most mmWave applications. They are pervasive in all but the higher power applications. The breadth of silicon technologies includes bulk RF CMOS, SiGe BiCMOS, Partially-Depleted (PD) RF SOI, and Fully-Depleted (FD) SOI. However, the market opportunity for silicon mmWave technologies has until recently been primarily relegated to lower volume wireless infrastructure and optical networking applications. With the push towards 5G standards at 28 GHz and above, broadband WTTx (Wireless-fiber-To-The-X) at 28 GHz, broadband satellite communications at Ku and Ka band, wireless backhaul at 60 GHz, licensed E-band at 71–76 GHz and 81–86 GHz, vehicular radar at 77 GHz, and photonics, many large volume opportunities have arrived. Designers are interested in understanding: 1) the current status of silicon technologies for mmWave, 2) innovations in models, design kits (DKs) and simulation/design tools, and 3) R&D and the transistor technology roadmap for the future. Designers need to know the impact of these technology developments on the performance and cost of mmWave circuits and systems. This workshop will explore these questions in detail. Our invited speakers will present a technology and argue for its merits against other technology choices given its status, roadmap, R&D, maturity and cost. Each section will include presentations on the

technology, models, circuits and systems. After a brief introduction the workshop will have three sections: RFCMOS, SiGe BiCMOS, and RFSOI (PDSOI and FDSOI). Topics will include the following: analog versus digital, SOC with low power logic and integrated RF, partitioned systems with higher performance and more mature RF technologies, and low-cost bulk CMOS versus SOI and SiGe. The workshop will conclude with a panel of the technologists. Each panel member will advance their position and answer the question: "Has RF performance peaked in silicon technology?".

Speakers:

1. "An Overview of Silicon Technologies for mmWave Applications", **Lawrence Larson**, *Brown University, USA*
2. "RF CMOS Technology for mmWave Applications", **Peter Baumgartner**, *Intel, Germany*
3. "RF CMOS Modelling", **Christian Enz**, *EPFL, Switzerland*
4. "No Waves, No Glory: The Renewal of RF CMOS for 5G mm-Wave Applications", **Michael Reiha**, *Nokia Networks, USA*
5. "High Performance SiGe HBT BiCMOS Technology", **Holger Rucker**, *IHP, Germany*
6. "High-Performance SiGe BiCMOS for Millimeter-Wave Applications", **Alvin Joseph**, *GLOBALFOUNDRIES, USA*
7. "Compact HBT Modeling for mm- and Sub-mm-Wave Applications", **Michael Schroeter**, *Technische Universität Dresden, Germany*
8. "RF and Wideband Circuit Benchmarks in SiGe-BiCMOS", **John Long**, *University of Waterloo, Canada*
9. "Millimeter-Wave Circuit and System Capabilities and Trade-Offs for SiGe BiCMOS", **Brian Floyd**, *North Carolina State University, USA*
10. "RFSOI (PDSOI and FDSOI) Technology for mmWave Applications", **David Harame**, *GLOBALFOUNDRIES, USA*
11. "RFSOI (PDSOI and FDSOI) Compact Models", **Josef Watts[1], Jean Charles Barbee[2]**, *[1]GLOBALFOUNDRIES, Germany, [2]LETI, Germany*
12. "RF and mm-Wave Design in FD-SOI CMOS Technologies", **Sorin P. Voinigescu**, *University of Toronto, Canada*
13. "mmWave Transceiver Design in RF PD SOI CMOS", **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center, USA*
14. "Panel: Has RF Performance Peaked? Are the Glory Days Behind Us?", **Larry Larson**, *Brown University, USA*

WMN (Full Day): Monday 08:00–17:00
System Requirements and Technologies for Tunable Filters

Sponsor: **IMS**

WMO (Full Day): Monday 08:00–17:00
Technologies for 5G Backhaul and Infrastructures

Sponsor: **IMS**

MONDAY SHORT COURSES – 5 JUNE 2017

SMA (Full Day): Monday 8:00–17:00
Coupling-Matrix-Based Design of RF/Microwave Filters

Sponsor: **IMS**

SMB (Full Day): Monday 08:00–17:00
Fundamentals of Microwave Imaging

Sponsor: **IMS**

SMC (Full Day): Monday 08:00–17:00
SOI, from Basics to Applications

Sponsor: **IMS**

FRIDAY WORKSHOPS – 9 JUNE 2017

WFA (Full Day): Friday 08:00–17:00
Acoustic Multiplexer for Carrier Aggregation

Sponsor: **IMS**

WFB (Full Day): Friday 08:00–17:00
Additive Manufacturing of Radio-Frequency Components

Sponsor: **IMS**

WFC (Half Day): Friday 08:00–12:00
Amateur Radio as a Low-Cost Means of Providing Students with Practical RF Experience

Sponsor: **IMS**

WFD (Full Day): Friday 08:00–17:00
Efficiency Enhancement and Linearization Techniques for Future Wireless Telecommunication Systems

Sponsor: **IMS**

WFE (Half Day): Friday 08:00–12:00
Electromagnetic Theranostics: From Diagnostics to Treatment with Micro- and Millimeter Wave Sensors and Systems

Sponsor: **IMS**

WFF (Full Day): Friday 08:00–17:00
Emerging Transmission Line Technologies for Interconnect, Components, Circuits and Systems

Sponsor: **IMS**

WFG (Full Day): Friday 08:00–17:00
GNSS Frontends, Antennas and Services

Sponsor: **IMS**

WFH (Half Day): Friday 08:00–12:00
Localization in Wireless Sensor Networks

Sponsor: **IMS**

WFI (Full Day): Friday 08:00–17:00
Low Cost Technology for Space Satellites

Sponsor: **IMS**

WFJ (Half Day): Friday 08:00–12:00
Low-Cost CMOS mm-Wave Front-Ends for 5G Wireless Terminals

Sponsor: **IMS**

WFK (Full Day): Friday 08:00–17:00
Massive MIMO and its 5G Related Applications

Sponsor: **IMS**

WFL (Full Day): Friday 08:00–17:00
Materials and Devices for
Next-Generation High-Q RF Resonators and Filters

Sponsor: **IMS**

WFM (Half Day): Friday 08:00–12:00
Microwave Circuit Design for the Next-Generation Radar: 5G and Beyond

Sponsor: **IMS**

WFN (Half Day): Friday 08:00–12:00
Microwave Nano-Biotechnology

Sponsor: **IMS**

WFO (Full Day): Friday 08:00–17:00
Multi-Physics Based Microwave Modeling and Design

Sponsor: **IMS**

WFP (Full Day): Friday 08:00–17:00
Plug and Play S-Parameter Measurements and Models for Broadband Interconnects

Sponsors: **IMS, ARFTG**

WFQ (Full Day): Friday 08:00–17:00
Recent Progresses in mmW Multilayer Circuit and System Design and Packaging (MCM/SoP)

Sponsor: **IMS**

WFR (Full Day): Friday 08:00–17:00
RFID Components and Devices for the Next Generation of 5G IoT Devices

Sponsor: **IMS**

WFS (Half Day): Friday 08:00–12:00
Thermal vs Non-Thermal Effects of
Electromagnetic Waves for Biomedical Applications

Sponsor: **IMS**

WFT (Full Day): Friday 08:00–17:00
Towards 5G: New Trends in Microwave Filters

Sponsor: **IMS**

FRIDAY SHORT COURSES – 9 JUNE 2017

SFA (Full Day): Friday 08:00–17:00
Multi-Beam Antennas and Beam-Forming Networks

Sponsor: **IMS**

SFB (Half Day): Friday 08:00–12:00
RF Sampling Architecture for
High Bandwidth Communication Systems

Sponsor: **IMS**

SFC (Full Day): Friday 08:00–17:00
The Dynamics, Bifurcation, and Practical Stability Analysis/Design of Nonlinear Microwave Circuits and Networks

Sponsor: **IMS**

REGISTRATION

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration which provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird Registration is the 2nd tier or Advance Registration which ends just prior to the start of Microwave Week. The 3rd and final tier is the On-Site Registration.

Early Bird Registration: 6 February – 8 May 2017 (through midnight Hawaii Standard Time)

Advance Registration: 9 May – 2 June 2017 (through midnight Hawaii Standard Time)

On-Site Registration: 3 June – 9 June 2017

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit http://www.ieee.org/services/join or or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Registration Categories

Register online: https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=220

Symposia

Microwave Week includes the IMS technical program and exhibit, as well as the RFIC Symposium (http://rfic-ieee.org/), ARFTG Conference (http://www.arftg.org/).

Select the conference(s) you wish to attend.

- **SUPERPASS** registrants can attend as many technical sessions as they can from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend **One** full-day workshop (or half-day workshops, to equal one full-day), the Proceedings for IMS, RFIC, ARFTG, Workshop Electronic Proceedings for all three days and admission to the exhibits. In addition, the SUPERPASS will allow you to attend the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, the Kick-Off Reception on Monday, and the Awards Banquet on Wednesday.
- **RFIC Technical Sessions** are held on Monday and Tuesday. Registration includes admission to the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, exhibits, and the electronic proceedings.
- **IMS Technical Sessions** are held on Tuesday, Wednesday and Thursday. Registration includes admission to the exhibits, the electronic proceedings, and the Kick-Off Reception on Monday.
- **ARFTG Technical Sessions** are held on Friday. Registration includes breakfast, lunch, electronic proceedings, and admission to the ARFTG exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE members.
- **5G Summit** is held on Monday and Tuesday afternoon. The registration cost is the same as that of a full-day workshop and it includes admission to the Executive Forum on 5G, as well as the 5G Demos area in the 5G/IoT Pavilion on the exhibition floor.

Exhibit Only Registration

Microwave Week hosts the largest exhibition of its kind with over 400 companies.

Exhibit only registration is available.

Additional Items to Add to Your Registration

1) Guest Registration

Attendees registered for the technical portion of the conference (SUPERPASS, IMS, RFIC, ARFTG) may add a Guest to their registration. Guest Registration includes access to the Plenary Session and Exhibit Hall, but does not allow access to Technical Sessions and Workshops. Select the Guest Registration tab to add this to your registration. The name of the guest is added on the checkout page.

2) Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 7 June from 18:30–21:30 at the Hilton Hawaiian Village Waikiki Beach Resort Coral Ballroom. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

3) Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

4) Two Full-Day Workshop Registration

Purchase two full-day workshops by selecting the option titled "***Two Full-Day Workshop Registration***" and receive the electronic proceedings for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop electronic proceedings are not available for individual sale.

5) Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. Workshop notes will be available electronically.

Full-day workshops include a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a morning refreshment break and a lunch. Afternoon workshops include a lunch and an afternoon refreshment break.

6) Short Courses

The short course fee includes access to the short course selected and any materials that the short course organizers may provide.

Full-day short courses include a morning refreshment break, a lunch, and an afternoon refreshment break. Morning short courses include a morning refreshment break and a lunch. Afternoon short courses include a lunch and an afternoon refreshment break.

7) Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are not accepted and will be returned. Please make checks payable to "2017 IEEE MTT-S". Written requests for refunds will be honored if received by 8 May 2017. Refer to the Refund Policy for complete details.

8) Refund Policy

Written requests received by 8 May 2017 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email when requesting a refund. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027, USA

nannette@mpassociates.com

ON-SITE REGISTRATION

On-site registration for all Microwave Week events will be available in the Hawaii Convention Center, Main Lobby:

Date	Time
Saturday, 3 June	08:00–19:00
Sunday, 4 June	07:00–19:00
Monday, 5 June	07:00–19:00
Tuesday, 6 June	07:00–18:00
Wednesday, 7 June	07:00–18:00
Thursday, 8 June	07:00–16:00
Friday, 9 June	07:00–09:00

Exhibit Only Registration

Exhibit only registration is available.

Press Registration

Qualified journalists are invited to register for press credentials. Please see the IMS Press Credentials Guidelines page at http://ims2017.org/press/press-credential-guidelines for qualification requirements. All requests for press credentials are subject to review and approval.

ARFTG Registration

Late on-site registration will be available in the Hawaii Convention Center, Main Lobby on Friday from 07:00–09:00. If at all possible, please pre-register earlier in the week to reduce the on-site workload.

Registration Rates in USD	Early Bird (6 Feb–8 May)		Advance (9 May–2 June)		On-site (3–9 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Superpass	$1,090	$1,645	$1,270	$1,900	$1,475	$2,195
IEEE Life Member (Retiree)	$650		$760		$925	
Student	$650	$670	$760	$780	$925	$940
RFIC Sessions	$255	$360	$290	$420	$310	$455
IEEE Life Member (Retiree)	$180		$200		$220	
Student	$180	$200	$200	$220	$220	$240
IMS Sessions	$475	$700	$545	$815	$630	$935
IEEE Life Member (Retiree)	$85		$95		$115	
Student	$85	$145	$95	$160	$115	$185
Single Day Registration	$240	$350	$280	$405	$320	$485
ARFTG Sessions	$240	$360	$285	$420	$320	$485
IEEE Life Member (Retiree)	$170		$195		$215	
Student	$170	$195	$195	$220	$215	$240
Exhibit Only Pass	$25	$25	$25	$25	$30	$30
Wednesday Exhibition Only Pass	free	free	free	free	free	free
Guest Badge	N/A	N/A	N/A	N/A	N/A	N/A

Registration Rates in USD	Early Bird (6 Feb–8 May)		Advance (9 May–2 June)		On-site (3–9 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
5G Summit	$185	$270	$200	$295	$245	$370
IEEE Life Member (Retiree)	$140		$150		$175	
Student	$140	$160	$150	$170	$175	$190
Full Day Short Course	$315	$465	$370	$550	$430	$645
IEEE Life Member (Retiree)	$220		$255		$295	
Student	$220	$245	$255	$280	$295	$315
Half Day Short Course	$220	$330	$255	$390	$295	$445
IEEE Life Member (Retiree)	$160		$185		$210	
Student	$160	$175	$185	$200	$210	$225
Full Day Workshop	$185	$270	$200	$295	$245	$370
IEEE Life Member (Retiree)	$140		$150		$175	
Student	$140	$160	$150	$170	$175	$190
Half Day Workshop	$95	$140	$110	$160	$130	$190
IEEE Life Member (Retiree)	$75		$80		$90	
Student	$75	$90	$80	$95	$90	$110
2 Full Day Workshops (includes all workshop proceedings: Sun Mon Fri)	$475	$690	$515	$760	$645	$955
IEEE Life Member (Retiree)	$350		$385		$435	
Student	$350	$375	$385	$405	$435	$460

Registration Rates in USD	Early Bird (6 Feb–8 May)		Advance (9 May–2 June)		On-site (3–9 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Proceedings Electronic Download						
RFIC	$50	$75	$60	$90	$70	$105
IMS	$50	$75	$60	$90	$70	$105
ARFTG	$50	$75	$60	$90	$70	$105
Evening Events						
RFIC Sunday Evening Only (includes: RFIC Plenary Session, Industry Showcase and Reception)	$50	$75	$60	$90	$70	$105
Award Banquet (Wednesday Night)	$75	$75	$75	$75	$75	$75
Lunch						
Monday Boxed Lunch	$30	$30	$30	$30		
Tuesday Boxed Lunch	$30	$30	$30	$30		
Wednesday Boxed Lunch	$30	$30	$30	$30		
Thursday Boxed Lunch	$30	$30	$30	$30		

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning — if required — and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 38 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Currently, 38 countries participate in the Visa Waiver Program, as shown below:

Andorra	France	Lithuania	Slovakia
Australia	Germany	Luxembourg	Slovenia
Austria	Greece	Malta	South Korea
Belgium	Hungary	Monaco	Spain
Brunei	Iceland	the Netherlands	Sweden
Chile	Ireland	New Zealand	Switzerland
Czech Republic	Italy	Norway	Taiwan
Denmark	Japan	Portugal	United Kingdom
Estonia	Latvia	San Marino	
Finland	Liechtenstein	Singapore	

For more information, see http://travel.state.gov/content/visas/en/visit.html.

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, http://www.cbp.gov/, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. To allow sufficient time for processing, please submit your requests for letters of support well in advance of your interview dates, to ims2017.visa@gmail.com. All requests should include complete name (as in your passport) and current mailing address as this information is to be included in the letter for submission to the US Consulate. Also please contact ims2017.visa@gmail.com for additional visa assistance queries.

Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (currently posted on the IMS2017 website).

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative source of information is the U.S. Government website at http://travel.state.gov/content/visas/en/visit.html.

SOCIAL/NETWORKING EVENTS

SUNDAY, 4 June 2017

RFIC Reception: 19:30–21:30

The RFIC Reception features the Joint Industry Showcase & Interactive Forum. Drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest developments in the wireless industry.

MONDAY, 5 June 2017

Welcome Event: 19:00–20:30

IMS2017 starts with a welcome event on Monday for all attendees, which will be hosted at the Hilton Hawaiian Village on the Great Lawn immediately following the IMS2017 Plenary Session.

TUESDAY, 6 June 2017

Young Professionals Panel Session and Networking Event

The Young Professionals are planning a panel session and networking event at the Hawaii Convention Center. Please refer to the conference website for detailed information on the panel session.

WEDNESDAY, 7 June 2017

Industry-Hosted Cocktail Reception: 17:00–18:00

The Industry-Hosted Reception is scheduled in the exhibition hall on Wednesday, 7 June 2017 right before the MTT-S Awards Banquet.

Awards Banquet: 18:30–21:30

The MTT-S Awards Banquet will be hosted at the Hilton Hawaiian Village and will feature exciting entertainment.

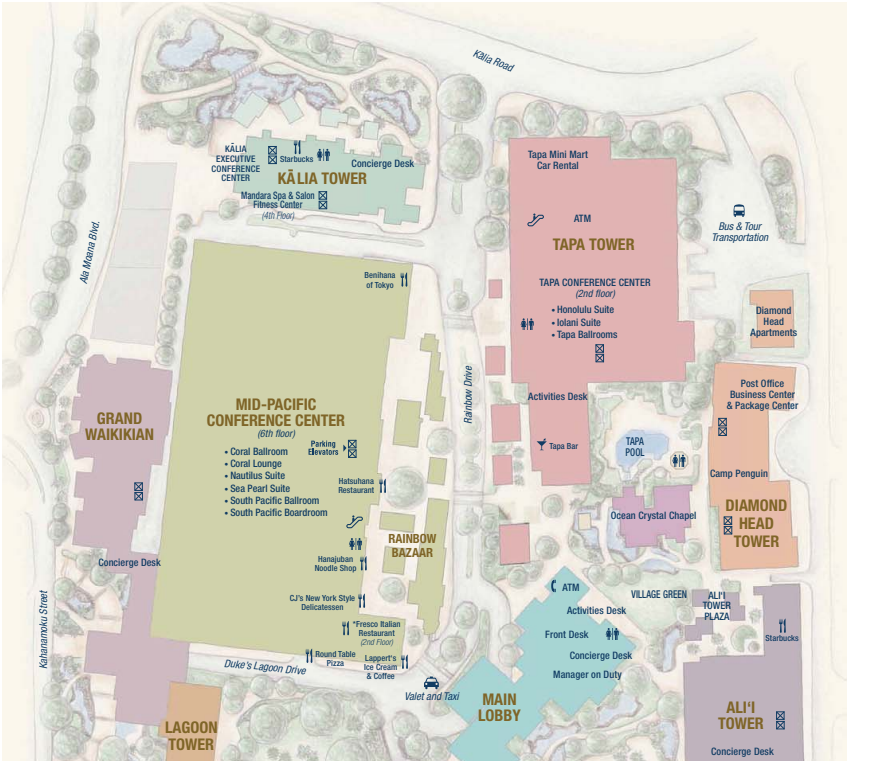
THURSDAY, 8 June 2017

Women in Microwaves Reception

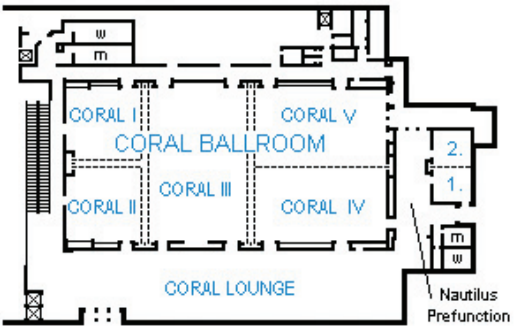
The Women in Microwaves Reception will be held at the Hawaii Convention Center immediately following the WIM Session.

HILTON MID-PACIFIC CONFERENCE CENTER MAPS

RFIC Plenary, Reception, Joint Industry Showcase & Interactive Forum



HILTON HAWAIIAN VILLAGE - 6th FLOOR

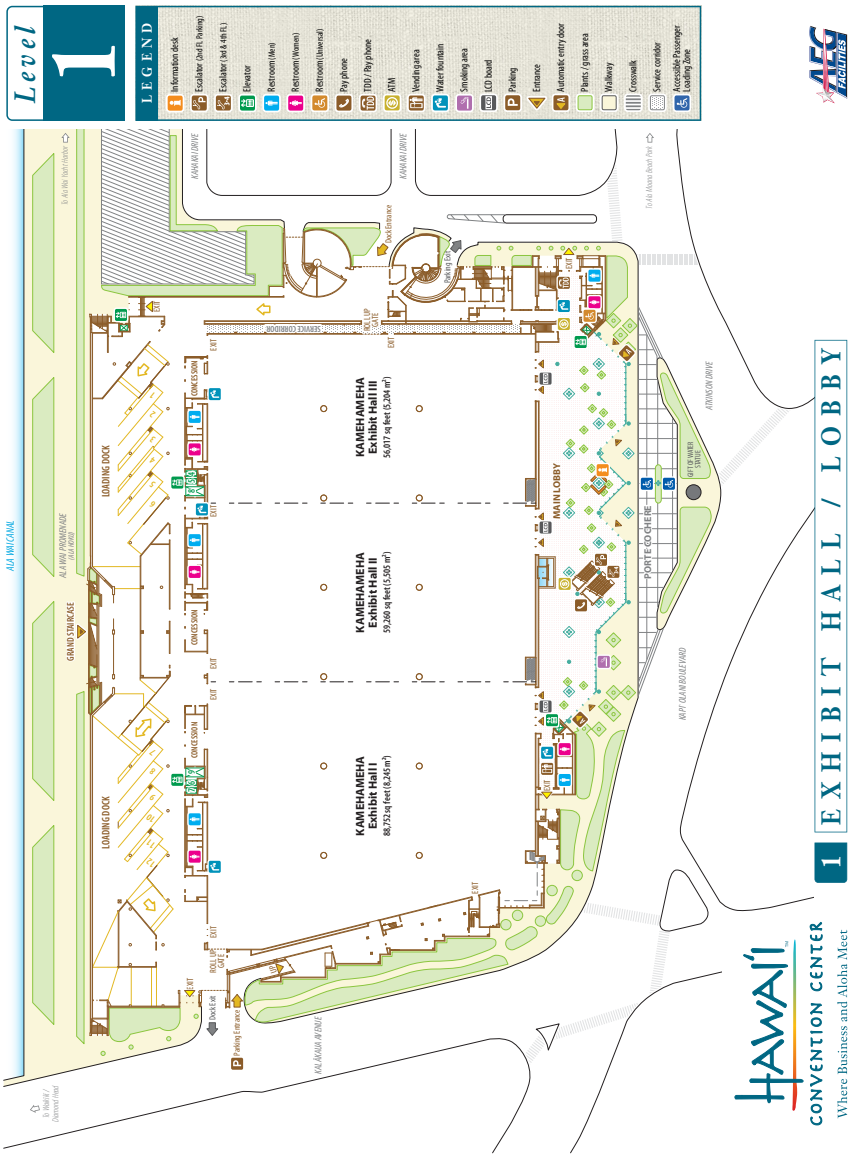


1. NAUTILUS I
2. NAUTILUS II

HAWAII CONVENTION CENTER MAPS

RFIC Technical Sessions and IMS Workshops

IMS Exhibits



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2017 RFIC Symposium
Honolulu, Hawaii, USA
4–6 June 2017

PROGRAM