

2015 IEEE Radio Frequency Integrated Circuits Symposium

Phoenix, Arizona, USA 17–19 May 2015



PROGRAM

Phoenix Convention Center and Sheraton Hotel

Sponsored by

IEEE Microwave Theory and Techniques Society IEEE Electron Devices Society and IEEE Solid-State Circuits Society







RFIC Plenary, Industry Showcase and Reception

Sunday Evening, 17 May 2015 Phoenix Convention Center (PCC) North Building Ballroom 120AB

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in the Phoenix Convention Center (PCC), North Building Ballroom 120AB.

17:30–19:00, PCC North Building Ballroom 120AB — **The Plenary Session** kicks off the evening with the Student Paper Awards, RFIC Industry Best Paper Award, and RFIC Tina Quach Service Award ceremony followed by two outstanding plenary speakers, Dr. Peter H. Siegel, Director, Submillimeter Wave Advanced Technology Team, Jet Propulsion Laboratories, and Dr. Hermann Eul, Corporate Vice President at Intel.

19:00–21:00, PCC North Building Ballroom Foyer — "Hot Chips and Cold Drinks" **Industry Showcase and Reception:** Immediately following the Plenary Session is the RFIC Reception held in the foyer just outside the ballroom. Drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest news in the wireless industry.

The Industry Showcase session, held concurrently with the plenary reception, will highlight 11 selected papers submitted by authors from the industry. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. This year, for the first time, a Best Industry Paper Award will be awarded to the author of one selected paper among these.

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and Superpass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but want don't want to miss these great events. Please see http://rfic-ieee.org/ for more details.

The RFIC Reception is sponsored by the RFIC Steering Committee, and through generous support of our cooperate sponsors: Qorvo (Platinum Level), Intel (Platinum Level), Analog Devices (Gold Level), Skyworks (Silver Level) and Qualcomm (Silver Level).



Event	Location	Saturday 16 May	Sunday 17 May	Monday 18 May	Tuesday 19 May
Registration	PCC North Bld.	08:00 - 18:00	02:00-	-19:00	$07:00{-}18:00$
Speakers' Breakfast	PCC North Bld.120C			07:00-08:30	
Workshop Breakfast	PCC North Bld.120D		02:00-	-08:30	
Workshops & Short Courses	PCC 121–122 (Sunday) PCC 125–132 (Sunday) PCC 125–132 (Monday)		08:00-	-17:00	
Workshop Lunch	PCC North Bld.120D		12:00-	-13:30	
Panel Sessions	PCC 122 (Monday) PCC 129 (Tuesday)			12:00-	-13:15
Technical Sessions	PCC 121–122 (Monday) PCC 125–126 (Tuesday)			08:00–09:40 10:10–11:50 13:30–15:10 15:40–17:20	08:00-09:40 10:10-11:50
Interactive Forum	PCC North Bld. Hall 6				13:30–16:00
Plenary Session	PCC North Bld. 120AB		17:30–19:00		
Industry Showcase & Reception	PCC North Bld. Foyer		19:00–21:00		

RFIC Symposium Schedule (16–19 May 2015)



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Welcome Message from Chairs

We invite you to participate in the 2015 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held in Phoenix, Arizona on 17–19 May 2015. RFIC Symposium is the premier IC design conference focused exclusively on the latest developments in RF, Microwave, and Millimeter Wave Integrated Circuit technology and high frequency analog/mixed-signal design and innovation.

RFIC Symposium, the International Microwave Symposium (IMS), ARFTG, and the IMS Industry Exhibition make up the "Microwave Week", the largest worldwide RF/microwave meeting of the year. Come to Microwave week to learn from the world's experts through a wide variety of technical sessions, interactive forums, panel sessions, workshops, short courses, industrial exhibits, application seminars and historical exhibits. Share your knowledge with others by presenting your latest results. Expand your network. Catch up with old friends and colleagues. Return invigorated with new ideas and enthusiasm.

RFIC Symposium will continue to offer a number of initiatives specifically geared towards the RFIC industry. The 2-page industry brief format, which was introduced in 2014, allows the latest state-of-the-art RF IC design results to be presented, without requiring die photos and detailed schematics (as required in full-length, 4-page, submissions), and will be continued in 2015. The most innovative and highly-rated industrial papers, both 2- and 4-page, will be invited to present a poster (and optional demo) at a special Industry Showcase Session to be held during the popular evening RFIC Reception on Sunday, 17 May 2015. As a new initiative in 2015, there will be a Best Industry Paper Award that would be selected from the industry showcase papers and will be presented during the RFIC Plenary.

To enhance academic submission experiences, all of the RFIC student paper finalists will now receive complementary RFIC registration. In addition, the lead authors of the top 3 student papers will receive a \$500 honorarium along special recognition at the RFIC Plenary Session, where these awards will be announced. Students can also volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complementary conference registration, meals, T-shirts, and other benefits. First and second-year RFIC PhD students may also participate in the PhD Student Sponsorship Initiative Program, joint with IMS. This program, established and sponsored by the MTT-S Administrative Committee, aims to engage these PhD students in the conference by having them complete technical assignments during the conference and report on them later in the week. Sponsorship includes complementary conference registrations (RFIC and IMS), lodging, and meals.

The 2015 RFIC Symposium will open on Sunday, 17 May 2015 with a lineup of ten full-day and one half-day workshop, six of which will be co-sponsored by IMS. One additional RFIC and four additional joint RFIC/IMS workshops will be held on Monday. RFIC and RFIC/IMS joint workshops cover a wide array of topics with presentations from experts in their respective fields, and historically have been highly attended and well received. This year's workshops cover some of the hottest topics in RFIC designs.

The Plenary Session will be held in Sunday evening, at the Phoenix Convention Center. It will begin with conference highlights, followed by presentation of the Student Paper Awards, the inaugural Industry Best Paper Award. The Plenary continues with two outstanding keynote talks, given by two renowned leaders in the RF/Microwave Community. The first speaker is Prof. Siegel of Jet Propulsion Laboratories who founded the Submillimeter Wave Advanced Technology (SWAT) Research center for 25 years. The topic of his talk is *"From THz Imaging to Millimeter-Wave Stimulation of Neurons: Is There a Killer Application for High Frequency RF in the Medical Community?"*. The second speaker is Dr. Hermann Eul who is a Corporate Vice President at Intel Corporation. Dr. Eul leads a worldwide organization focused on the development of hardware, software and connectivity ingredients for phones, tablets, UltrabookTM and other mobile devices, and complete system solutions. His talk is titled *"RF as the Differentiator"*. Be sure not to miss these engaging presentations!

Immediately following the Plenary Session is the Industry Showcase Session embedded in the RFIC Reception, providing a mix of "hot chips" and cold drinks. These events will be held in the Phoenix Convention Center. You won't want to miss the RFIC Reception!

Technical papers will be presented during oral sessions throughout Monday and in Tuesday morning, followed by the RFIC Interactive Forum in Tuesday afternoon. The Interactive Forum features papers presented in poster format, giving the attendees a chance to speak directly with the authors.

During lunchtime on both Monday and Tuesday, the conference features Panel Sessions. We have two "sizzling" topics this year that are sure to spark lively debates among the panelists and audience. The first RFIC Panel Session is titled *"Research is Expensive, but Innovation Sells"* and will debate on the intricacies of how to successfully (or not !) conduct research in the industry: manage cost and resources, deal with the treacherous path from innovation to product, survive commoditization and succeed in IP protection. Directors and VPs from some of the most prestigious industry research labs in the world will share their views and opinions with the audience. The second Panel Session, is entitled *"Internet of Things: What's all the hype?"*. This panel brings together experts from across a wide range of industries, discussing the end user benefits, market opportunities, technical challenges and projected solutions for devices supporting Internet of Things (IoT). Will IoT be just an evolution of current connected devices or a real revolution? Come to the panel to find out !

Phoenix offers a unique and exciting experience for everyone. Phoenix is America's fifth largest city in the heart of Sonoran Desert, and it is the gateway to Grand Canyon. Phoenix offers a spectrum encompassing red-rock buttes and urban sophistication. The Heard Museum features Native American art and culture set and Phoenix Art Museum houses more than 17,000 works of classic and modern art. The artistic tapestry in Phoenix includes Native American, Hispanic, African and Asian influences. There are three mountains around Phoenix that provide the opportunity for hiking, biking and climbing. Horseback riding and water recreation are also popular.

On behalf of the entire RFIC Steering Committee, we would like to extend to all of you a warm welcome to attend the 2015 RFIC Symposium. We are looking forward to an exciting program and hope you can join us in Phoenix, Arizona! For more details, please visit our website http://rfic-ieee.org.



Bertan Bakkaloglu General Chair Arizona State University



Kevin Kobayashi TPC Co-Chair Qorvo



Albert Wang TPC Co-Chair UC Riverside

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RFIC 2015 Schedule

Saturday, 16 May 2015

08:00–18:00 Registration — Phoenix Convention Center (PCC) North Lobby

Sunday, 17 May 2015

- 07:00–19:00 Registration PCC North Lobby
- 07:00-08:00 Workshop Speakers' Breakfast PCC 120C
- 07:00-08:00 Workshop Breakfast --- PCC 120D
- 08:00–17:00 Workshops and Short Courses, PCC 121–122, 125–132
- 12:00–13:00 Workshops Lunch PCC 120D
- 17:30-19:00 RFIC Plenary PCC 120AB
- 19:00-21:00 Industry Showcase and Reception PCC Ballroom Pre-Function Area

Monday, 18 May 2015

- 07:00–19:00 Registration PCC North Building Lobby
- 07:00-08:00 Speakers' Breakfast PCC 120C
- 07:00–08:00 Workshop Breakfast PCC 120D
- 08:00–17:00 Workshops and Short Courses PCC 127-132
- 08:00–09:40 RM01B PCC 122ABC: Broadband mm-Wave Building Blocks
 - RMO1C PCC 125AB: Advances in mm-Wave Arrays and Transceivers
- RMO1D PCC 126AB: Heterogenous Integration of the III-V and CMOS Devices for Multi-Function RFIC 09:40-10:10 Break
- 10:10–11:50 RMO2A PCC 121ABC: Frequency Generation and Measurement Techniques RM02B — PCC 122ABC: *RF Front-End Techniques*
 - RMO2C PCC 125AB: Mixed-Signal Techniques for Transmit and Frequency Synthesis
- 12:00–13:00 Workshops Lunch PCC 120D
- 12:00-13:15 RFIC Panel PCC 122ABC
- 13:00–14:30 RFIC Steering Committee Lunch Meeting Sheraton Phoenix, Maryvale A
- 13:30–15:10 RMO3A PCC 121ABC: Millimeter-Waves and Terahertz Frequency Generation RM03B — PCC 122ABC: Linearized PAs for Cellular and Connectivity Services
 - RMO3C PCC 125AB: High Performance Wireless Mobile ICs
 - RMO3D PCC 126ABC: *Ultra-Low Power Transceivers*
- 15:10-15:40 Break
- 15:40–17:20 RMO4A PCC 121ABC: Techniques for High Tuning Range and Low Phase Noise RMO4B — PCC 122ABC: Wideband and Reconfigurable High Frequency Integrated PAs RMO4C — PCC 125AB: Wireless Connectivity Transceivers and Power Amplifier Techniques RMO4D — PCC 126ABC: Low-Power Wideband SoCs

Tuesday, 19 May 2015

- 07:00–19:00 Registration PCC North Lobby
- 07:00-08:00 Speakers' Breakfast PCC 120D
- 08:00–09:40 RTU1A PCC 121ABC: mm-Wave & THz Frequency Multipliers RTU1C — PCC 125AB: Reconfigurable and Interference-Tolerant Transceivers
 - RTU1D PCC 126ABC: Wireline Transceiver Circuits
- 09:40-10:10 Break
- 10:10–11:50 RTU2B PCC 122ABC: Software-Defined and Cognitive Radio Techniques RTU2C — PCC 125AB: *Mixed Signal Circuits for RF Receivers*
 - RTU2D PCC 126ABC: High Frequency and Non-Linear Device Modeling
- 12:00–13:15 RFIC Panel PCC 129AB
- 13:00-14:30 RFIC TPC Lunch Meeting Sheraton Phoenix, Encanto B
- 13:30–16:00 RTUIF Interactive Forum PCC Hall 6

Plenary, Industry Showcase and Reception Schedule Phoenix Convention Center, Ballroom 120AB

1**7:30**

RFIC Plenary Phoenix Convention Center, Ballroom 120AB Chair: Bertan Bakkaloglu, Arizona State University Co-Chair: Albert Wang, University of California at Riverside Co-Chair: Kevin Kobayashi, Qorvo

17:30 Welcome Message from General Chair and TPC Chairs, Student Paper Awards, Industry Best Paper Award, Tina Quach Service Award
18:00 From THz Imaging to Millimeter-Wave Stimulation of Neurons: Is there a Killer Application for High Frequency RF in the Medical Community? Peter H. Siegel, Caltech & THz Global
18:30 RF as the Differentiator Hermann Eul, Intel

19:00–21:00 "Hot Chips and Cold Drinks" Industry Showcase and Reception Phoenix Convention Center Ballroom Foyer

The Industry Showcase session, held concurrently with the plenary reception, will highlight 11 selected papers submitted by authors from the industry. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration. The media will cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. This year, for the first time, a Best Industry Paper Award will be awarded to the author of one selected paper among these.

Student Paper Award Finalists

Each year, the RFIC Symposium holds a student paper contest to select the top-three student papers. Additional information on the contest eligibility and judging procedure is provided below. First, second, and third prizes will be announced at the RFIC Plenary Session on 17 May 2015 in Phoenix, AZ. Each winner will receive a plaque and an honorarium. The 2015 Student Paper Finalists are as follows:

- A 60GHz Single-Chip 256-Element Wafer-Scale Phased Array with EIRP of 45dBm Using Sub-Reticle Stitching
 Samet Zihir¹, Ozan D. Gurbuz¹, Arjun Karroy², Sanjay Raman³, Gabriel M. Rebeiz¹
 ¹University of California at San Diego, USA, ²Jazz Semiconductor, USA, ³Virginia Tech, USA RM01C-2 08:20
- 2) A 60GHz Same-Channel Full-Duplex CMOS Transceiver and Link Based on Reconfigurable Polarization-Based Antenna Cancellation Tolga Dinc, Anandaroop Chakrabarti, Harish Krishnaswamy Columbia University, USA RM01C-4 09:00
- A Vertical Solenoid Inductor for Noise Coupling Minimization in 3D-IC Gilad Yahalom¹, Alice Wang², Uming Ko², Anantha P. Chandrakasan¹
 ¹MIT, USA, ²MediaTek, Taiwan RM01D-5 09:20
- A 192MHz Differential XO Based Frequency Quadrupler with Sub-Picosecond Jitter in 28nm CMOS
 Mohammad Mahdi Ghahramani¹, Yashar Rajavi², Alireza Khalili², Amirpouya Kavousian², Beomsup Kim², Michael P. Flynn¹
 ¹University of Michigan, USA, ²Qualcomm, USA RMO2A-1 10:10
- 5) A Wideband Fractional-N Synthesizer with Low Effort Adaptive Phase Noise Cancellation for Low-Power Short-Range Standards Ye Zhang, Jan Henning Mueller, Bastian Mohr, Lei Liao, Aytac Atac, Ralf Wunderlich, Stefan Heinen RWTH Aachen University, Germany RMO2A-4 11:10
- A Self-Interference Cancelling Front-End for In-Band Full-Duplex Wireless and its Phase Noise Performance
 Dirk-Jan van den Broek, Eric A.M. Klumperink, Bram Nauta
 University of Twente, The Netherlands
 RM02B-1 10:10
- 7) A 1.8GHz Wideband Open-Loop Phase Modulator with TDC Based Non-Linearity Calibration in 0.13μm CMOS Nitin Nidhi, Sudhakar Pamarti University of California at Los Angeles, USA RM02C-1 10:10

Sunday, 17 May 2015

17:30-18:00

PCC Ballroom 120AB

- A Class-C Self-Mixing-VCO Architecture with High Tuning-Range and Low Phase-Noise for mm-Wave Applications
 Amir Hossein Masnadi Shirazi, Amir Nikpaik, Reza Molavi, Shahriar Mirabbasi, Sudip Shekhar
 University of British Columbia, Canada
 RM03A-1
 13:30
- 9) Higbly Linear Envelope Tracking Power Amplifier with Simple Correction Circuit Kyunghoon Moon¹, Jooseung Kim¹, Sangsu Jin¹, Byungjoon Park¹, Yunsung Cho¹, Min Park², Bumman Kim¹
 ¹POSTECH, Korea, ²ETRI, Korea RM03B-2
 13:50
- 10) Digitally Intensive Transmitter Employing RF Pulse Width Modulation for IoT Applications Hyejeong Song, Ranjit Gharpurey University of Texas at Austin, USA RM03C-3 14:10
- 11) A 380µW Rx, 2.6mW Tx 433MHz FSK Transceiver with a 102dB Link Budget and Bit-Level Duty Cycling Nathan E. Roberts, Michael C. Kines, David D. Wentzloff University of Michigan, USA RM03D-3 14:10
- 12) A 0.7V 194μW 31dB FOM 2.3–2.5GHz RF Frontend for WBAN with Mutual Noise Cancellation Using Passive Coupling Mustafijur Rahman, Ramesh Harjani University of Minnesota, USA RM03D-4 14:30
- A 0.5V 0.5mW Switching Current Source Oscillator
 Masoud Babaie, Mina Shahmohammadi, Robert Bogdan Staszewski
 Technische Universiteit Delft, The Netherlands
 RM04A-1 15:40
- 14) A 4.6–5.35GHz Transceiver with 38dB On-Chip Self-Interference Cancelation at 10kHz Offset Frequency Xuebei Yang, Aydin Babakhani Rice University, USA RMO4C-5 17:00
- A 3.6cm² Wirelessly-Powered UWB SoC with -30.7dBm Rectifier Sensitivity and Sub-10cm Range Resolution
 Jian Kang, Patrick Chiang, Arun Natarajan
 Oregon State University, USA
 RMO4D-4
 16:40
- 16) An IF 8-Element 2-Beam Bit-Stream Band-Pass Beamformer Jaehun Jeong, Nicholas Collins, Michael P. Flynn University of Michigan, USA RTU1C-2 08:20

Sunday, 17 May 2015

17:30-18:00

PCC Ballroom 120AB

- 17) A Switched-Capacitor RF Front End with Embedded Programmable High Order Filtering and a +15dBm OB-B1dB Yang Xu, Peter R. Kinget Columbia University, USA RTU1C-3 08:40
- 18) An 80-GHz Low Noise Amplifier Resilient to the TX-Spillover in Phase-Modulated Continuous-Wave Radars
 Alaa Medra, Davide Guermandi, Kristof Vaesen, Qixian Shi, Piet Wambacq, Vito Giannini imec, Belgium
 RTU2B-2 10:30
- 19) A Wideband Under-Sampling Blocker Detector with a 0.7–2.7GHz Mixer-First Receiver Olli Viitala¹, Mikko Kaltiokallio², Marko Kosunen¹, Kari Stadius¹, Jussi Ryynänen¹
 ¹Aalto University, Finland, ²TDK, Finland RTU2C-1 10:10

Congratulations to the 19 finalists. I encourage all the finalists and their advisors to share this exciting moment made possible by all of your hard work. The committee thanks all the student authors for your contributions. We look forward for more students participating in this contest in the future RFIC Symposia.

<u>Student Paper Contest Eligibility</u>: To be considered for an award, the student must have been a full time student (9 hours/term graduate, 12 hours/term undergraduate) during the time the work was performed. The student must be the lead author of the paper and must present the paper at the Symposium. A memorandum will be automatically sent to the advisor to certify that the work was done by the student.

<u>Judging Procedure</u>: Student papers will be reviewed and admitted to the conference in the same manner as all other conference papers. A student paper contest committee consisting of one representative from each technical program subcommittee is formed to review all the finalists and select the top three papers. Papers accepted for the competition will be judged on content.

Walid Y. Ali-Ahmad Student Programs Chair Qualcomm

Plenary Speaker 1



Peter H. Siegel Caltech & THz Global

From THz Imaging to Millimeter-Wave Stimulation of Neurons: Is there a Killer Application for High Frequency RF in the Medical Community?

Abstract: As millimeter- and submillimeter-wave device and circuit technologies move from the laboratory into customized commercial components and instruments, the search for mainstream applications that might serve as a basis for significant capital investment has expanded. A plethora of hypothetical, and often unrealistic expectations for the technology, have been touted, mainly in biomedical imaging, defense and security, and communications applications, but most fail the comparison test for existing or competing alternatives, and some are based on false premises. This talk will briefly cover the advantages and limitations of millimeter- and submillimeter-wave technologies when applied in the biomedical field, and specifically highlight an application that the speaker believes fulfils at least one dream for broad-based disease control application — millimeter-wave mon-invasive monitoring of blood glucose levels.

About Peter H. Siegel

Peter H. Siegel (BA Colgate 1976, PhD Columbia, 1983, IEEE member since 1975) has held appointments as Faculty Associate in Electrical Engineering and Senior Scientist in Biology at the California Institute of Technology, and Senior Research Scientist at the NASA Jet Propulsion Laboratory, both in Pasadena, California. At JPL, he founded and led for 25 years, the Submillimeter Wave Advanced Technology (SWAT) team, a group of 20+ scientists and engineers developing THz technology for NASA's near and long term space missions. This included delivering key components for four major satellite missions and leading more than 75 smaller R&D programs for NASA and the US department of defense. At Caltech, Dr. Siegel has been involved in new biological and medical applications of THz, especially low power effects on neurons and most recently, millimeter-wave monitoring of blood chemistry. Among many other functions, he serves as founding Editor-in-Chief of the IEEE Transactions on Terahertz Science and Technology and the General Secretary of the International Society of Infrared, Millimeter, and Terahertz Waves, the world's largest society devoted exclusively to THz science and technology, which he founded in 2009. He is also an IEEE Fellow, and has served as an IEEE Distinguished lecturer, vice-chair and chair of IEEE MTTS Committee 4 - THz Technology, and an ad-hoc member of the MTTS AdCom. Dr. Siegel has published more than 300 articles on THz components and technology and has given more than 200 invited talks on this subject throughout his career of 40 years in THz.

Plenary Speaker 2



Hermann Eul Corporate Vice President, Intel

RF as the Differentiator

Abstract: There is an explosion in number of connected devices around us, driven by Mobility and Internet of things (IoT) adoption. By one estimate (Source: Gartner Research), there will be 25 billion connected devices by 2020. Smart RF design is the engine that enables these devices to get connected. Dr Eul has been a leading voice in the world of communications for the past 20 years and has played leadership roles through the multiple technology transitions. He will share his perspective on where the industry is headed and how the complexity of RF design is actually going to be a key strategic differentiator for players in the industry.

About Hermann Eul

Dr. Hermann Eul is Corporate Vice President at Intel Corporation. In his role, Dr. Eul leads a worldwide organization focused on the development of hardware, software and connectivity ingredients for phones, tablets, UltrabookTM and other mobile devices and complete system solutions. Dr. Eul joined Intel in February 2011 when the acquisition of Infineon's wireless solutions business was completed, forming Intel Mobile Communications, a subsidiary of the company. He was president and general manager of Intel Mobile Communications, responsible for developing wireless communication products for mobile phones, tablet computers and other connected devices. From 2005 to 2011 Dr. Eul was executive vice president and a member of the management board of Infineon Technologies, where he was responsible for research and development, as well as for sales and marketing, and prior to that served as president of Infineon's communications business. From 1991 to 2005, before being promoted into Infieon's executive board, Dr. Eul held numerous management positions at Infineon and at Siemens.

"Hot Chips and Cold Drinks" Industry Showcase

Chair: Oren Eliezer, EverSet Technologies

The Industry Showcase session, held concurrently with the plenary reception, will highlight 11 selected papers submitted by authors from the industry. Authors of these papers will be present to discuss their innovative work, summarized in poster format, and some will also show a demonstration during the showcase. The media will be present to cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. This year, for the first time, a Best Industry Paper Award will be awarded to the author of one selected paper among these. This year's Industry Showcase papers are:

- A 16-Element W-Band Phased Array Transceiver Chipset with Flip-Chip PCB Integrated Antennas for Multi-Gigabit Data Links Bell Labs, USA
 Shahramian, M.J. Holyoak, Y. Baeyens RM01C-3 08:40
- 2) InP HBT/GaN HEMT/Si CMOS Heterogeneous Integrated Q-Band VCO-Amplifier Chain Northrop Grumman Aerospace Systems, USA Yi-Cheng Wu, Monte Watanabe, Tim LaRocca RMO1D-1 08:00
- A Capacitance Boosted Full-Octave LC VCO Based 0.7 to 24GHz Fractional-N Synthesizer IBM, USA Bodhisatwa Sadhu, Mark Ferriss, Daniel Friedman RMO3A-2 13:50
- A Highly Integrated Multiband LTE SiGe Power Amplifier for Envelope Tracking Qorvo, USA Yan Li, Jeffery Ortiz, Eddie Spears RMO3B-3 14:10
- 5) Dual-Band Integrated Wi-Fi PAs with Load-Line Adjustment and Phase Compensated Power Detector MediaTek, Taiwan Yuan-Hung Chung, Po-Yu Chang, Meng-Hsiung Hung, Ming-Yeh Hsu, Che-Hung Liao, Chun-Wei Lin RMO4C-1 15:40
- 6) A Highly Integrated Single Chip 5–6GHz Front-End IC Based on SiGe BiCMOS That Enhances 802.11ac WLAN Radio Front-End Designs Skyworks Solutions, USA Chun-Wen Paul Huang, Kenny Christainsen, Sergey Nabokin, Rafik Mirzayantz, Justin Allum, Andrew Chen, Lui Lam, Mike McPartlin, Mark Doherty, Bill Vaillancourt RMO4C-2 16:00
- 7) The MATRICS RF-FPGA in 180nm SiGe-on-SOI BiCMOS BAE Systems, USA Lawrence J. Kushner, Kevin W. Sliech, Gregory M. Flewelling, Joseph D. Cali, Curtis M. Grens, Steven E. Turner, Douglas S. Jansen, Joseph L. Wood, Gary M. Madison RTU1C-1 08:00

Sunday, 17 May 2015

19:00-21:00

PCC Ballroom 120AB

- Besign of Lange Couplers with Local Ground References Using SiGe BiCMOS Technology for mm-Wave Applications
 ¹NXP Semiconductors, France, ²LaMIPS, France, ³ISAE, France, ⁴NXP Semiconductors, The Netherlands
 S. Wane¹, L. Leyssenne², O. Tesson¹, O. Doussin³, D. Bajon³, D. Lesénéchal², T.V. Dinh², M.P. van Heijden⁴, Ralf Pijper⁴, P. Magnée⁴, P. Descamps², A. Erdem¹
 RTU2D-1 10:10
- A 265mW, 225MHz Signal Bandwidth, and <1-dB Gain Step Software Defined Cable Receiver Front-End Enabling Ultra-HDTV in 28nm CMOS
 ¹Broadcom, USA, ²imec, Belgium, ³Broadcom, The Netherlands Silvian Spiridon¹, Davide Guermandi², Stefano Bozzola³, Han Yan³, Mattia Introini³, Dongsoo Koh¹ RTUIF-6 13:30
- 10) A Robust Low Phase Noise Ku Band VCO with 23.3% Tuning Range for E-Band and V-Band Backhaul Transceivers IBM, Israel
 Run Levinger, Oded Katz, Jakob Vovnoboy, Roee Ben Yishay, Roi Carmon, Benny Shienman, Nadav Mazor, Danny Elad RTUIF-8 13:30
- 20-GHz PLL-Based Configurable Frequency Generator in 180nm SiGe-on-SOI BiCMOS BAE Systems, USA Joseph D. Cali, Curtis M. Grens, Steven E. Turner, Douglas S. Jansen, Lawrence J. Kushner RTUIF-10 13:30

Monday, 18 May 2015 08:00–09:40 Room 122AB Session RMO1B: Broadband mm-Wave Building Blocks Chair: Domine Leenaerts, NXP Semiconductors Co-Chair: Frank Henkel, IMST

RMO1B-108:00Compact Broadband Amplifiers with up to 105GHz Bandwidth in SiGeBiCMOS

Faisal Ahmed¹, Muhammad Furqan¹, Klaus Aufinger², Andreas Stelzer¹; ¹Johannes Kepler Universität Linz, Austria, ²Infineon Technologies, Germany

Abstract: In this paper the design and measurements of a single-ended and a fully differential broadband amplifier are presented. The amplifiers are based on a lumped circuit design topology and are highly compact with an active chip area of around 0.02mm^2 . The amplifiers are fabricated in a 0.13-µm SiGe BiCMOS HBT technology. Wide bandwidth is achieved with a common-base input stage and an output cascode stage buffered with emitter followers. A 3-dB bandwidth of around 91 GHz and 105 GHz, and a small-signal gain of 13 dB and 12 dB are achieved for the single-ended and the differential-ended amplifiers, respectively. The differential-ended amplifier shows a superior performance with an input return loss greater than 10 dB from DC-110 GHz, ±1 dB in-band gain ripple and a low group delay variation of ±6 psec. Large signal measurements show a single-ended saturated power of around 2.8 dBm.

RMO1B-2 08:20 Compact 160-GHz Amplifier with 15-dB Peak Gain and 41-GHz 3-dB Bandwidth

S. Hara¹, K. Katayama², K. Takano², I. Watanabe¹, N. Sekine¹, A. Kasamatsu¹, T. Yoshida², S. Amakawa², M. Fujishima²; ¹NICT, Japan, ²Hiroshima University, Japan

Abstract: This paper presents a compact wideband amplifier at 160 GHz in 40-nm CMOS. Typical wideband amplifier design requires higher-order matching networks and more gain stages, both of which demand larger die area. The presented 8-stage amplifier uses a compact "fishbone" layout technique, and its core size is as small as $190 \times 123 \ \mu\text{m}^2$. A small-signal gain of 15 dB at 160 GHz and a 3-dB bandwidth of 41 GHz are achieved. It consumes 117 mW from a 0.9 V voltage supply.

RM01B-3 08:40 A 79GHz g_m-Boosted Sub-Harmonic Mixer with High Conversion Gain in 65nm CMOS

JinGyu Jang, JunTaek Oh, Songcheol Hong; KAIST, Korea

Abstract: In this paper, a 79 GHz g_m-boosted sub-harmonic mixer with high conversion gain is presented. As a g_m-boosting technique, a transformer based feedback network with an NMOS bleeding path is proposed to achieve high conversion gain. The differential LO-driven sub-harmonic mixer has a simple structure and operates at low LO power. The measurement results show a conversion gain of 1.6 dB at a LO power of -5 dBm, a noise figure of 13 dB, and a 2LO-to-RF isolation of 38 dB. The power consumption of the sub-harmonic mixer is 12 mW. The circuit was fabricated using 65-nm CMOS technology with a chip area of 0.69×0.45 mm².

RM01B-4 09:00

A 54–84GHz CMOS SPST Switch with 35dB Isolation

Ran Shu¹, Adrian Tang¹, Brian Drouin², Qun Jane Gu¹; ¹University of California at Davis, USA, ²Jet Propulsion Laboratory, USA

Abstract: This paper presents a hybrid design based, CMOS millimeter-wave (mm-wave) singlepolar single-throw (SPST) switch. The circuit design starts from the analysis and optimization of a distributed structure, while implemented using coupled lump elements for performance improvement and area-efficient layout. Moreover, a specific bias scheme is used to further decrease insertion loss by more than 0.5 dB. This SPST switch achieves higher than 35 dB isolation over an ultra-wide frequency range, from 54 GHz to 84 GHz, a minimum 1.7 dB insertion loss, and <-10 dB return loss with 0.012 mm² chip area in 65 nm CMOS. This design achieves more than 10 dB enhancement of isolation by comparing with state-of-the-arts while maintaining similar insertion loss.

Monday, 18 May 2015 08:00-09:40 Room 125AB

Session RMO1C: Advances in mm-Wave Arrays and Transceivers Chair: Mona Hella, Rennselaer Polytechnic Institute Co-Chair: Ed Balboni, Analog Devices

RM01C-1 08:00

A 312GHz Antenna Array Receiver in 65nm CMOS Utilizing Self-Oscillating 3X Subharmonic Mixer Frontend

Yen-Ju Chen, Ta-Shun Chu; National Tsing-Hua University, Taiwan

Abstract: A 312GHz antenna array receiver is presented in this paper. The receiver is a doubleconversion superheterodyne architecture. The first down-conversion is accomplished by a selfoscillating 3X subharmonic mixer frontend, and the second down-conversion is performed by a Gilbert-cell mixer and an LO. The receiver is co-designed and integrated with a 4-element loop antenna array. By mixing an RF input signal at 312 GHz with the 3rd harmonic of the 96GHz LO, the first IF of 24 GHz is produced ($f_{IFI}=f_{RF}-3f_{LOI}$). The second LO is at frequency of 22.3 GHz, and the second IF is 1.7 GHz ($f_{IF2}=f_{IFI}-f_{LO2}$). The antenna array receiver exhibits a measured conversion loss of 19 dB from 312GHz RF to 1.7GHz IF, and has a -3dB bandwidth of 1.2 GHz. It is implemented in 65nm CMOS. The chip occupies an area of 1.71 mm² and consumes DC power of 110 mW.

RM01C-2 08:20

A 60GHz Single-Chip 256-Element Wafer-Scale Phased Array with EIRP of 45dBm Using Sub-Reticle Stitching

Samet Zihir¹, Ozan D. Gurbuz¹, Arjun Karroy², Sanjay Raman³, Gabriel M. Rebeiz¹; ¹University of California at San Diego, USA, ²Jazz Semiconductor, USA, ³Virginia Tech, USA

Abstract: This paper presents a 60 GHz wafer-scale transmit phased-array with 256-elements spaced $\lambda/2$ apart in the x and y directions, and occupying an area of 4.14×4.2 cm² (1740 mm²). The phased array is built using independent RF, transmission-line and control circuit blocks which are stitched together to form an aggregate chip which is much larger than a standard reticle $(22 \times 22 \text{ mm}^2)$. This method allows for a wafer-scale design and can be extended to any size and any shape (rectangular, hexagonal, etc.) up to the edge of the wafer. The blocks include high-efficiency on-wafer antennas, phased-array channels with 3-bits amplitude and 5-bits phase control together with an amplifier having an output power of +3 dBm at 60 GHz. Also, a highly redundant RF distribution network is synthesized from several stitched blocks for improved yield, and the control blocks have redundant SPI control and power strips, also for improved yield. The 256-element array results in a half-power beamwidth of 6° in the E- and H-planes, a directivity of 29 dB, and scans to $+/-55^{\circ}$ in the E- and H-planes with near-ideal patterns and a cross-polarization level of <-25 dB. The measured EIRP is 45 dBm at 61 GHz and with a 3-dB bandwidth from 58 to 64 GHz. To our knowledge, this is the largest single-chip phased-array ever developed and allows the construction of large-scale (1000+ elements) phased-array systems, either on a single wafer or by assembling several of these chips together.

RM01C-3 08:40

A 16-Element W-Band Phased Array Transceiver Chipset with Flip-Chip PCB Integrated Antennas for Multi-Gigabit Data Links

S. Shahramian, M.J. Holyoak, Y. Baeyens; Bell Labs, USA

Abstract: This paper describes the design and implementation of a W-band phased array system with integrated PCB antennas capable of multi-gigabit spectrally-efficient wireless communication. The chipset is manufactured in a 0.18 μ m SiGe BiCMOS technology with f_T/f_{MAX} of 240/270GHz and is flip-chipped onto an organic PCB with integrated antenna arrays. Each chip is equipped with 16-transmit/4-receive or 16-receive/4-transmit calibrated phase shifter elements, direct up-and down-converters plus a half-rate phase locked loop. Each transceiver IC operates from 1.5V and 2.5V supplies and consumes 5.5W and 4.5W in transmit and receive mode respectively. The transmitter EIRP is 34dBm in each polarization. A 4.8Gb/s QPSK wireless link in each polarization is demonstrated at a distance of 20-meters.

RM01C-4 09:00

A 60GHz Same-Channel Full-Duplex CMOS Transceiver and Link Based on Reconfigurable Polarization-Based Antenna Cancellation

Tolga Dinc, Anandaroop Chakrabarti, Harish Krishnaswamy; Columbia University, USA

Abstract: This paper describes a direct-conversion 45nm SOI CMOS 60 GHz transceiver for samechannel full duplex applications. A novel polarization-based wideband self-interference cancellation (SIC) technique in the antenna domain is described that can be reconfigured from the IC. In order to achieve the high levels of required SIC, a second RF cancellation path from the transmitter output to the LNA output with >30 dB gain control and >360° phase control is also integrated. The TX and RX share the same LO to reduce the impact of phase noise on SIC. Antenna and RF cancellation together enable >70 dB of total self-interference suppression even in the presence of nearby reflectors. In conjunction with digital SIC implemented in MATLAB, a same-channel fullduplex link is demonstrated over 0.7 m. To the best of our knowledge, this work demonstrates the first fully-integrated full-duplex transceiver front-end and mm-wave link. While not our focus, the transceiver also achieves state-of-the-art saturated output power of +15 dBm, peak TX efficiency of 15.3% and RX NF of 4 dB.

RM01C-5 09:20

A 60-GHz CMOS Direct-Conversion Doppler Radar RF Sensor with Clutter Canceller for Single-Antenna Noncontact Human Vital-Signs Detection

Hsin-Chih Kuo, Chien-Chang Chou, Chien-Chih Lin, Chun-Han Yu, Tzuen-Hsi Huang, Huey-Ru Chuang; National Cheng Kung University, Taiwan

Abstract: This paper presents a 60-GHz CMOS direct-conversion Doppler radar RF sensor with a quasi-circulator (QC) and a clutter canceller circuit for single-antenna noncontact human vital-signs detection. A high isolation QC is designed to provide better detection sensitivity for the tiny vital-signs detection for the single-antenna Doppler radar architecture. The clutter canceller performs cancellation for the transmitting leakage power from the circulator and the background reflection clutter to enhance the detection sensitivity of weak vital signals. The measurement shows that the total transmitting power is 3 dBm while the conversion gain of the sub-harmonic receiver is 10.5 dB. In the human vital-signs detection measurement, at a distance of 75 cm, the detected heartbeat (1-1.3 Hz) and respiratory (0.35-0.45 Hz) signals can be clearly observed. The RF sensor is fabricated in 90-nm technology with a chip size of 2 mm × 2 mm and a consuming power of 217 mW. The presented CMOS vital-signs Doppler radar RF sensor will be very useful for the wireless remote physiological monitoring healthcare system and the tiny vibrations detection applications.

Monday, 18 May 2015 08:00–09:40 Room 126ABC Session RMO1D: A Heterogenous Integration of the III-V and CMOS Devices for Multi-Function RFIC Chair: Aditya Gupta, Northrop Grumman Co-Chair: Fujiang Lin, USTC

RMO1D-1 08:00 InP HBT/GaN HEMT/Si CMOS Heterogeneous Integrated Q-Band VCO-Amplifier Chain

Yi-Cheng Wu, Monte Watanabe, Tim LaRocca; Northrop Grumman Aerospace Systems, USA **Abstract:** A Q-band DAHI (Diverse Accessible Heterogeneous Integration) multi-technology VCOamplifier chain is presented. The DAHI integration process is composed of InP HBT, GaN HEMT and 65nm CMOS. The InP VCO demonstrated 2GHz of tuning range at 35GHz while the GaN amplifier provides 15dB gain.

RM01D-2 08:20

RF Performance of 28nm PolySiON and HKMG CMOS Devices

Kok Wai Johnny Chew¹, Aniket Agshikar², Maciej Wiatr², Jen Shuang Wong¹, Wai Heng Chow¹, Zhihong Liu¹, Ting Huang Lee¹, Jinglin Shi¹, Suh Fei Lim¹, Kumaran Sundaram¹, Lye Hock Kelvin Chan¹, Chye Huat Michael Cheng¹, Nicolas Sassiat², Yong Koo Yoo¹, Asha Balijepalli³, Amit Kumta³, Chi Dong Nguyen², Ralf Illgen², Arun Mathew², Christian Schippel², Alexandru Romanescu², Josef Watts³, David Harame³; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, Germany, ³GLOBALFOUNDRIES, USA

Abstract: The impact of scaling in advanced RF/MS-CMOS has been extensively discussed but there has not been a publication that compares the RF characteristics of 28nm high-K metal gate HKMG and PolySiON technologies fabricated in the same facility. In this work, we show that HKMG improves transistor f_{T} and increases varactor tunning range. However, it can actually decrease f_{max} . We examine how process features made to optimize cost and digital performance impact the RF performance. Process features which improve DC current and gm, including HKMG also give higher f_{T} . However, f_{max} is sensitive to gate resistance and PolySiON has an advantage here.

RM01D-3 08:40

A 130nm RFSOI Technology with Switch, LNA, and EDNMOS Devices for Integrated Front-End Module SoC Applications

Purakh Raj Verma¹, Shaoqiang Zhang¹, Rui Tze Toh¹, Jen Shuang Wong¹, Wei Gao¹, Kok Wai Johnny Chew¹, Rajesh Nair¹, David Harame², Josef Watts², Thomas Mckay²; ¹GLOBALFOUNDRIES, Singapore, ²GLOBALFOUNDRIES, USA

Abstract: The cellular frequency spectrum has become increasingly complex with over 50 frequencies in LTE standards. To reduce costs in the front end module the switch has migrated from a III-V PHEMT base to a silicon solution in RFSOI. While many providers have focused on a 180nm base technology node for the RFSOI there has been an increasing move to more advanced nodes to solution the logic requirements of the cellular standards. In addition there has been a strong interest in migrating to an SOC solution in RFSOI. In this paper a 130nm RFSOI technology is presented with high performance and low noise body tied 1.5V NMOS for LNA devices with a novel method of body contacting, low Ron*Coff NMOS for antenna switch and state of the art EDNMOS with $f_{\rm T}$ of 38GHz and BVdss of 14V BVdss for integrated PA application. Specific results presented include characterization of the switch, LNA, and Power Amplifier devices.

RM01D-4 09:00

High Resolution Thermal Characterization of a GaAs MMIC

Dustin Kendig¹, Kazuaki Yazawa², Ali Shakouri²; ¹Microsanj, USA, ²Purdue University, USA **Abstract:** We present the high resolution thermal characterization of a GaAs MMIC. The thermal imaging technique provides sub-microsecond temporal and sub-micron spatial resolutions. The results show that the gate area heats up in less than 3 us, much faster than the other area of the transistor. Also, the thermal cross talk between transistor arrays takes place in 100s us. This imaging method revealed unique thermal characteristics, not previously observed with traditional thermal measurement techniques.

RM01D-5 09:20

A Vertical Solenoid Inductor for Noise Coupling Minimization in 3D-IC

Gilad Yahalom¹, Alice Wang², Uming Ko², Anantha P. Chandrakasan¹; ¹MIT, USA, ²MediaTek, Taiwan **Abstract:** This paper presents the use of an integrated solenoid inductor in three dimensional integrated circuits (3D-IC) for improved noise mitigation. The structure is fabricated in a two-tier, stacked 28nm CMOS using through silicon vias (TSV). The structure is implemented as part of an LC voltage-controlled oscillator (VCO), and exhibits 6dB improvement in phase noise and 14dB less coupling from adjacent digital clock lines compared to a planar two-turn inductor.

Monday, 18 May 2015 10:10–11:50 Room 121ABC

Session RMO2A: Frequency Generation and Measurement Techniques Chair: Himanshu Arora, Texas Instruments Co-Chair: Hiva Hedayati, Xilinx

RM02A-110:10A 192MHz Differential XO Based Frequency Quadrupler with Sub-
Picosecond Jitter in 28nm CMOS

Mohammad Mahdi Ghahramani¹, Yashar Rajavi², Alireza Khalili², Amirpouya Kavousian², Beomsup Kim², Michael P. Flynn¹; ¹University of Michigan, USA, ²Qualcomm, USA

Abstract: A low jitter 192MHz crystal reference quadrupler leverages a new active inductor based 48MHz differential XO, two skewed inverters, a new duty cycle correction circuit, and a frequency doubler. The 192MHz quadrupler can serve as a fast, low jitter reference for a low phase noise PLL and requires far less power and area than reference multiplying PLL or MDLL circuits. The measured RMS jitter is 168fs for the XO, and 184fs for 96MHz output (192MHz divide by 2). The entire circuit, including the XO, draws 5.5mA from a 1V supply and occupies 0.045mm². To our best knowledge, this is the first reference frequency quadrupler with sub-picosecond jitter.

RM02A-2 10:30

A 10GHz Delay Line Frequency Discriminator and PD/CP Based CMOS Phase Noise Measurement Circuit with -138.6dBc/Hz Sensitivity at 1MHz Offset

Shilei Hao, Tongning Hu, Qun Jane Gu; University of California at Davis, USA

Abstract: This paper presents a delay line frequency discriminator (FD) and phase detector (PD)/ charge pump (CP) based phase noise measurement (PNM) circuit to achieve wide bandwidth, great sensitivity and reliable integration at 10 GHz. PD/CP based phase noise detection makes it insensitive to environment and coupling noises. A delay-locked loop (DLL) is designed to align the PD input phases and a DC offset cancellation circuit is embedded to overcome circuit mismatches, which make the PNM self-calibrated. This PNM demonstrates -61/-81 dBc single tone sensitivity and -110.35/-138.60 dBc/Hz phase noise sensitivity at 100 kHz/1 MHz offset, respectively. The phase noise measurement bandwidth is 200 MHz, which is determined by the off-chip SAW filter bandwidth. This proof-of-concept design is fabricated in a 65 nm CMOS technology with the chip area of 1.5 mm \times 1.3 mm. The core circuit consumes 15.2 mW power.

RM02A-3 10:50

A 3–10mW, 3.1–10.6GHz Integer-N QPLL with Reference Spur Reduction Technique for UWB-Based Cognitive Radios

Nam-Seog Kim, Jan M. Rabaey; University of California at Berkeley, USA

Abstract: An integer-N charge pump QPLL provides 3.168–10.56GHz lock range, -108.38dBc/Hz phase noise at 1MHz offset, and -59.42dBc reference spur with digital calibration technique for charge pump mismatch while consuming 10.1mW at 10.56GHz with 4-divider at the output. A wideband low power TSPC programmable divider supports 57 sub-bands. It is implemented in a 1V 65nm CMOS process. Active area is 0.12mm².

RM02A-4 11:10

A Wideband Fractional-N Synthesizer with Low Effort Adaptive Phase Noise Cancellation for Low-Power Short-Range Standards

Ye Zhang, Jan Henning Mueller, Bastian Mohr, Lei Liao, Aytac Atac, Ralf Wunderlich, Stefan Heinen; RWTH Aachen University, Germany

Abstract: This paper presents a wideband low-spur fractional-N synthesizer with an adaptive noise cancellation technique. By adopting the classical loop filter, the $\Sigma\Delta$ quantization noise as well as the spurs are compensated with simple calibration circuits. The synthesizer is fully integrated in 130nm CMOS technology, consuming 0.33mm² area and 8.3mW core power. It operates at 1.8 GHz carrier frequency with 1MHz bandwidth. The outband phase noise is -129 dBc/Hz at 3MHz offset, the reference spur is -68 dBc, and the worst inband fractional spur is -56 dBc.

Monday, 18 May 2015 10:10–11:50 Room 122AB Session RMO2B: RF Front-End Techniques Chair: Hongtao Xu, Intel Co-Chair: Kenjiro Nishikawa, Kagoshima University

RM02B-1 10:10 A Self-Interference Cancelling Front-End for In-Band Full-Duplex Wireless and its Phase Noise Performance

Dirk-Jan van den Broek, Eric A.M. Klumperink, Bram Nauta; University of Twente, The Netherlands **Abstract:** This paper describes a frequency-agile RF front-end in 65nm CMOS targeting short-range full-duplex wireless communication. Complementing previous work on a self-interference cancelling receiver, this work describes the co-integrated transmitter and reports the phase noise advantages of using correlated clock resources to clock all up- and downconverters present in the system. The hardware is capable of frequency-agile operation from 0.15 to 3.5GHz carrier frequency. Measurements at 2.5 GHz indicate that the RX noise floor is only 1 dB degraded by phase noise when operated from a commercial PLL with \sim -38 dBc phase noise.

RM02B-2 10:30

A Positive Feedback Passive Mixer-First Receiver Front-End

Anders Nejdel, Mohammed Abdulaziz, Markus Törmänen, Henrik Sjöland; Lund University, Sweden **Abstract:** This paper presents a technique to reduce the noise figure of a passive mixer-first receiver front-end. By using lower than 50 Ω switch resistance in the current-mode passive mixer and introducing a positive feedback from baseband to the RF-input, it can be well matched close to f_{10} while achieving a noise figure below 3dB, which is otherwise a fundamental limit. A quadrature front-end prototype for a direct conversion receiver has been implemented in 65nm CMOS, occupying an active area of 0.23mm² with a frequency operation ranging from 0.7 to 3.8GHz. The prototype achieves a minimum noise figure of 2.5dB, an out-of-band 1dB compression point of +3dBm, with IIP3 and IIP2 exceeding +26 and +65dBm, respectively. The current consumption from a 1.2V supply is between 22.8 and 62.8mA, depending on frequency operation.

RMO2B-3 10:50 Design of All-Passive Higher-Order CMOS N-Path Filters

Negar Reiskarimian, Harish Krishnaswamy; Columbia University, USA

Abstract: In this paper, a methodology for designing all-passive higher-order N-path filters is described. The methodology extends known filter synthesis techniques for LC filters to N-path filters through the use of lumped quarter-wave transmission-line (t-line) equivalents that enable series-LC-like N-path structures. The quarter-wave t-line equivalents also isolate N-path filters from each other, allowing N-path sections to be cascaded to realize filters of arbitrary order. A tunable, nominally 6th-order, high-Q N-path bandpass filter based on this methodology has been implemented in 65nm CMOS. The filter has an insertion loss of 4.7–6.2dB, a tuning range of about 35% from 600MHz to 850MHz, and bandwidth that ranges from 9–15MHz, resulting in a Q that ranges from 40–90. The filter achieves an out-of-band (OOB) rejection of 30–50 dB, input-referred in-band (IB) and OOB 1dB compression point of 0dBm and +14dBm, and input-referred IB and OOB IIP3 of +7 and +17.5dBm respectively. The clock path DC power consumption at 700MHz is 75mW from a 1.2V supply.

RM02B-4 11:10 A 2.4GHz 72dB-Variable-Gain 100dB-DR 7.8mW 4th-Order Tunable Q-Enhanced LC Band-Pass Filter

Nicolo Testi¹, Roc Berenguer², Xuejun Zhang², Sara Munoz², Yang Xu¹; ¹Illinois Institute of Technology, USA, ²Innophase, USA

Abstract: This paper presents a 2.4GHz two-stage Q-enhanced 4th-order active band-pass filter with 72dB variable gain and 12MHz 3-dB bandwidth. The center frequency of the filter can be tuned from 2.35GHz to 2.48GHz with a frequency step of 0.4MHz. An RF linearization technique is proposed to enhance the dynamic range (DR) to 100dB, and a robust Q of 400 is achieved for each of the two filter stages allowing RF channel selection. An EM isolation structure is implemented to reduce the mutual coupling between the two inductors to -76dB. This RF BPF is fabricated in 55nm CMOS technology and consumes only 7.8mW.

Monday, 18 May 2015 10:10-11:50

Room 125AB Session RMO2C: Mixed-Signal Techniques for Transmit and Frequency Synthesis

Chair: Eric Fogleman, MaxLinear Co-Chair: James Wilson, US Army Research Laboratory

RMO2C-110:10A 1.8GHz Wideband Open-Loop Phase Modulator with TDC Based Non-
Linearity Calibration in 0.13μm CMOS

Nitin Nidhi, Sudhakar Pamarti; University of California at Los Angeles, USA

Abstract: A non-linearity calibration technique is proposed for an open loop RF phase modulator. The phase modulator integrates a digital phase-locked loop, LO distribution network and digital calibration. A prototype was implemented in 0.13- μ m CMOS 1.8-GHz GFSK transmitter integrated circuit. Measurements on the prototype show that out-of-band quantization noise is 56-dB lower than the signal when transmitting 20-Mb/s GFSK signal and the r.m.s. error is only 3.2%. The power consumption of the phase modulator is 18 mW.

RM02C-2 10:30

A 103fs_{rms} 1.32mW 50MS/s 1.25MHz Bandwidth Two-Step Flash- $\Delta\Sigma$ Time-to-Digital Converter for ADPLL

Ying Wu¹, Ping Lu², Robert Bogdan Staszewski¹; ¹Technische Universiteit Delft, The Netherlands, ²Lund University, Sweden

Abstract: A 50-MS/s two-step flash- $\Delta\Sigma$ time-to-digital converter (TDC) using a 2-channel timeinterleaved time-domain register with an implicit adder/subtractor demonstrates a 3rd order noiseshaping. The TDC is fabricated in 40-nm CMOS and consumes 1.2 mA from a 1.1 V supply. At frequencies below 1.25 MHz, the TDC error integrates to 103 fs_{rms}, which is equal to an equivalent resolution of 1.6 ps.

RM02C-3 10:50 Digital Pulse-Width Pulse-Position Modulator in 28nm CMOS for Carrier Frequencies up to 1GHz

Johannes Digel¹, Markus Grözing¹, Martin Schmidt¹, Manfred Berroth¹, Christoph Haslach²; ¹Universität Stuttgart, Germany, ²Bell Labs, Germany

Abstract: A fully digital pulse-width pulse-position modulator (D-PWPM) is proposed that is capable of providing pulse sequences for a switching-mode power amplifier. The pulse sequences are generated according to 6-bit digital input words defining the positions of the rising and falling edges without the need for tunable analog delay cells. All possible edge positions are derived by division and phase interpolation of a digital input clock signal that is a multiple of the carrier frequency. CMOS selectors provide two signals which carry the actual rising and falling edge positions to special symmetric CMOS NOR and NAND gates. They finally generate the modulated pulse sequence.

The D-PWPM is fabricated in a 28 nm low-power CMOS technology and the circuit core dissipates 53mW from a 1 V supply. Sinusoidal double-sideband suppressed-carrier modulation of a 1 GHz carrier demonstrates the capability of the D-PWPM to operate as an RF bandpass mode DAC. With a carrier frequency of 983.04MHz, an SFDR of 45.6 dB is achieved for a low-frequency modulation and 33.4 dB near Nyquist frequency. Data transmission at 491.52MBit/s is demonstrated with a 16-QAM.

RM02C-4 11:10

A Time-Interleaved Multi-Mode $\Delta\Sigma$ RF-DAC for Direct Digital-to-RF Synthesis

Jamin J. McCue¹, Brian Dupaix¹, Lucas Duncan¹, Vipul J. Patel², Tony Quach², Waleed Khalil¹; ¹Ohio State University, USA, ²AFRL, USA

Abstract: A multi-mode delta-sigma ($\Delta\Sigma$) RF digital-to-analog converter (RF-DAC) is proposed for direct digital-to-RF synthesis. Unlike embedded-mixer $\Delta\Sigma$ RF-DACs which require analog I/Q combining and precise alignment of the local oscillator (LO) and data clock, the proposed circuit is fully digital with only one clock frequency (f_s). This architecture eliminates the need for a widelytuned LO by reconfiguring the $\Delta\Sigma$ modulator (DSM) for a variety of output frequencies, thus making it suitable for software-defined radio. Both a band-pass (BP) and high-pass (HP) DSM are used to synthesize signals at $f_g/4$, $f_g/2$, or $3f_g/4$. Interleaving is used to reject the first DAC image, doubling the usable bandwidth of the HP DSM while reducing reconstruction filter requirements. The proposed RF-DAC is implemented in 130 nm SiGe BiCMOS. With an f_s of 2 GHz, the 0.18 mm² RF-DAC core consumes 55 mW with output powers of -4.5 dBm, -7.5 dBm, and -13.8 dBm at 0.5 GHz, 1 GHz, and 1.5 GHz, respectively. For the HP DSM, a signal-to-image rejection ratio (SIRR) of 72 dB, an SNR of 54.5 dB over a 50 MHz bandwidth, and an in-band SFDR of 58.5 dB are demonstrated.

Monday, 18 May 2015 13:30–15:10 Room 121ABC Session RMO3A: Millimeter-Waves and Terahertz Frequency Generation Chair: Fred Lee, Google

Co-Chair: Reynold Kagiwada, NGAS

RM03A-1 13:30

A Class-C Self-Mixing-VCO Architecture with High Tuning-Range and Low Phase-Noise for mm-Wave Applications

Amir Hossein Masnadi Shirazi, Amir Nikpaik, Reza Molavi, Shahriar Mirabbasi, Sudip Shekhar; University of British Columbia, Canada

Abstract: Achieving high tuning-range and low phase-noise simultaneously in mm-wave voltagecontrolled oscillators (VCO) has been a severe design challenge. Our architecture, referred herein as a self-mixing VCO (SMV), utilizes a Class-C push-push VCO topology to generate the first (f_0) and second harmonics ($2f_0$) and then mixes them together to obtain the desired third harmonic ($3f_0$) component. Compared to a fundamental-mode VCO operating at $3f_0$ in mm-wave band, the SMV architecture achieves superior frequency tuning range (FTR) and phase-noise (PN) performance. A Class-C topology enhances the second-harmonic content to improve mixing efficiency, decreases parasitic capacitance and reduces phase noise. A 52.8-to-62.5 GHz SMV prototype is designed and implemented in a 0.13-µm CMOS process. Measurement results show an FTR of 16.8% together with a PN of -100.57 dBc/Hz at 1 MHz offset — resulting in an FTR-inclusive figure-of-merit (FOM_r) of -190.85 dBc/Hz while consuming 7.6 mW from a 1.2 V supply voltage.

RM03A-2 13:50

A Capacitance Boosted Full-Octave LC VCO Based 0.7 to 24GHz Fractional-N Synthesizer

Bodhisatwa Sadhu, Mark Ferriss, Daniel Friedman; IBM, USA

Abstract: This paper describes a technique in which a series inductance is used with a varactor to increase the varactor maximum to minimum capacitance ratio, thus enabling increased tuning range in an LC VCO. This technique is demonstrated through the implementation of an LC VCO tunable over a range greater than an octave, specifically 10.5 to 24 GHz (78%). The VCO is implemented within a fractional-N synthesizer in 32nm SOI CMOS to achieve continuous tuning from a fixed reference and achieves -128 to -119 dBc/Hz phase noise at 10MHz offset from the carrier across the tuning range. Output divider circuits are used to obtain all frequencies down to 660MHz.

RM03A-3 14:10

Sub-Harmonic Wireless Injection Locking of a THz CMOS Chip Array

Samuel Jameson, Eliezer Halpern, Eran Socher; Tel Aviv University, Israel

Abstract: A novel concept is introduced for generating high power frequency locked THz radiating based on CMOS chips. The concept is based on an array of CMOS VCO chips with on-chip ring antennas. With fundamental mm-wave oscillation around 115 GHz, the 3^{rd} harmonic of 0.35 THz is radiated with record total radiated power (TRP) of -4.3 dBm, EIRP of +3.8 dBm, DC-to-THz efficiency of 1.4% and phase noise better than -95 dBc/Hz at 10 MHz offset. Using a buffer-less Colpitts topology both improves the output power and efficiency but also allows wireless locking of the VCO fundamental frequency using the on-chip antenna, which is an RF-choke for that frequency. This allows wireless coupling between array CMOS chip elements integrated on-board for mutual locking and also wireless locking to an external D-band reference. The concept is demonstrated using a 1×4 array of CMOS radiating chips. The sources can be tuned from 343 to 347 GHz and the injection locking range is around 80 MHz. The 1×4 array has an EIRP of +13.8 dBm, a TRP and DC-to-THz efficiency of +1 dBm and 1.2%, respectively. The 1×4 array locked signal follows the phase noise of the external reference (+9.5 dB) up to a locking range around 80 MHz. This new concept enables simple and cost effective locked CMOS THz scalable source arrays.

RM03A-4 14:30

A Dual-Band E-Band Quadrature VCO with Switched Coupled Transformers in 28nm HPM Bulk CMOS

M. Vigilante, P. Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents a quadrature VCO (QVCO) that employs gate-to-drain transformers to couple two fundamental oscillators to generate accurate quadrature phases and switched coupled inductors for tuning extension. Thanks to these techniques, it is possible to cover two bands with a single quadrature VCO, without jeopardizing phase noise or demanding extensive silicon area. The oscillator, realized in 28nm HPM bulk CMOS, occupies a core area of only 0.031mm² and is tunable from 71-to-76GHz and 85.6-to-90.7GHz, resulting in a total tuning range of 9.8GHz. The peak phase noise at 10MHz offset from the carrier is -117.7dBc/Hz in the lower band and -110dBc/Hz in the higher one and varies less than 3.5dB within each sub-band. The maximum phase error is 1.5° and 3.5° in the lower and higher band respectively.

Monday, 18 May 2015 13:30–15:10 Room 122AB Session RMO3B: Linearized PAs for Cellular and Connectivity Services Chair: Eddie Spears, Qorvo Co-Chair: Jeff Walling, University of Utah

RMO3B-1 13:30 A Dual Band (2G/5G) IEEE 802.11b/g/n/ac 80MHz Bandwidth AM-AM Envelope Feedback Power Amplifier with Digital Pre-Distortion

Sai-Wang Tam, Yuan Lu, Morteza Nick, Yi Zhao, Alden Wong, Renaldi Winoto, Li Lin; Marvell, USA **Abstract:** A dual band (2G/5G) IEEE 802.11b/g/n/ac wide-band AM-AM envelope feedback power amplifier with digital pre-distortion is demonstrated in 40nm CMOS. This architect effectively improves both EVM and spectrum mask up to 20.9dBm in 40MHz bandwidth at 2G and 17.2dBm in 80MHz bandwidth in 5G. In addition, comparing to the conventional class AB PA, the power consumption is significantly reduced by 33% at low output power (<6dBm) and 21% at high output power (>16dBm).

RM03B-2 13:50

Highly Linear Envelope Tracking Power Amplifier with Simple Correction Circuit

Kyunghoon Moon¹, Jooseung Kim¹, Sangsu Jin¹, Byungjoon Park¹, Yunsung Cho¹, Min Park², Bumman Kim¹; ¹POSTECH, Korea, ²ETRI, Korea

Abstract: In this paper, we propose an envelope tracking (ET) power amplifier (PA) with a simple correction circuit (SCC) for linear operation. The supply dependent AM-AM and AM-PM distortion of an ET PA is linearized by the SCC which is fabricated on chip. The PA and supply modulator are fabricated using I/O device of CMOS 40nm process. For the 9.35-dB peak-to-average-power ratio, 256-QAM IEEE 802.11ah signal, the ET PA delivers a power-added efficiency of 24%, an average output power of 19.4 dBm and an error vector magnitude of -30 dB.

RMO3B-3 14:10 A Highly Integrated Multiband LTE SiGe Power Amplifier for Envelope Tracking

Yan Li, Jeffery Ortiz, Eddie Spears; Qorvo, USA

Abstract: This paper presents a highly integrated SiGe power amplifier (PA) for multiband longterm evolution (LTE). Two different harmonic loadings are investigated for the PA to achieve the optimized efficiencies for the envelope tracking (ET) and average power tracking (APT), respectively. By adopting the proper PA structure, our ET PA delivers >39% overall power-added efficiency (PAE) at the maximum output power (P_{out}) of 26.5 dBm with ACLR_{EUTRA} below -42 dB and EVM below 1% for the LTE QPSK 10 MHz at 699–716 MHz, 824–915 MHz and 1710–1980 MHz. At the back-off more than 5 dB below the maximum P_{out} , the ET PA is reconfigured to APT for remaining high overall PAE and linearity across a broad P_{out} range.

RM03B-4 14:30

A Quadrature Switched Capacitor Power Amplifier in 65nm CMOS

Wen Yuan¹, Vladimir Aparin², Jeremy Dunworth², Lee Seward², Jeffrey S. Walling¹, ¹University of Utah, USA, ²Qualcomm, USA

Abstract: This paper presents a quadrature switched-capacitor power amplifier (SCPA) that achieves similar output power and efficiency as polar/EER based digital PAs. It combines in-phase (I) and quadrature (Q) signals on a shared capacitor array in the charge domain. The SCPA utilizes a class-G dual-supply architecture to improve efficiency at backoff. This counteracts losses associated with the signal combination. Unlike polar/EER counterparts, the quadrature SCPA requires no wideband phase modulator or delay matching circuitry. The SCPA delivers a peak output power of 20.5 dBm with a peak PAE of 20%.

RM03B-5 14:50

A 25.6dBm Wireless Transmitter Using RF-PWM with Carrier Switching in 130-nm CMOS

Kunhee Cho, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A wireless transmitter using RF pulse-width-modulation (PWM) with carrier switching is introduced. The proposed approach overcomes the dynamic range limitation of PWM at radio frequencies by utilizing carrier switching between fundamental and half-fundamental frequencies, depending on the signal level to be transmitted. This allows for transmission of signals with large peak-to-average power ratio (PAPR) such as OFDM. The efficiency is also improved in the power back-off region due to reduced switching losses in the half-fundamental mode. The transmitter has been implemented in a 130-nm CMOS process. The measured peak output power and power-added-efficiency (PAE) are 25.6 dBm and 34%, respectively. While driving 802.11g 64-QAM OFDM signals, the average output power is 18.3 dBm and the PAE is 16% with an EVM of -25.5 dB.

Monday, 18 May 2015 13:30–15:10 Room 125AB Session RMO3C: High Performance Wireless Mobile ICs Chair: Haolu Xie, ZTE USA Co-Chair: Magnus Wiklund, Qualcomm

RM03C-1 13:30

A Rel-12 2G/3G/LTE-Advanced 3CC Receiver

M. Mikhemar¹, Masoud Kahrizi¹, John Leete¹, B. Pregardier², N. Vakilian¹, A. Hadji-Abdolhamid³, Morteza Vadipour¹, P. Ye⁴, Janice Chiu¹, Behzad Saeidi¹, G. Theodoratos¹, M. Nariman⁵, Yuyu Chang¹, F. Etemadi¹, B. Nourani¹, A. Tarighat¹, P. Mudge¹, Z. Zhou¹, N. Liu¹, C. Guan¹, Kevin Juan¹, B. Zhao¹, Rahul Magoon¹, M. Rofougaran¹, R. Rofougaran¹; ¹Broadcom, USA, ²Ethertronics, USA, ³MaxLinear, USA, ⁴Skyworks Solutions, USA, ⁵Qualcomm, USA

Abstract: This work presents a cellular receiver capable of receiving three simultaneous channels with an aggregate bandwidth of 60 MHz, enabling a 300 Mbps downlink rate. The receiver has 16 RF LNA ports covering the cellular bands within the 572–2700 MHz frequency range. It supports LTE-advanced Rel-12 Cat6, HSPA+ Rel-11, TD-SCDMA Rel-9, and GSM/EDGE Rel-9. The 40 nm CMOS receiver consumes 13.7 mA and 17.6 mA of battery current in 3G and LTE modes, respectively, including the PLL, DCXO, and bia sing for a single channel.

RM03C-2 13:50

A Dynamically-Biased 2G/3G/4G Multi-Band Transmitter with >4dBm P_{out}, <-65dBc CIM3 and <-157dBc/Hz Out-of-Band Noise in 28nm CMOS

Siddharth Seth¹, Daehyun Kwon², Sriramkumar Venugopalan¹, Sang Won Son¹, Yongrong Zuo¹, Venumadhav Bhagavatula¹, Jaehyun Lim², Dongjin Oh², Thomas Cho²; ¹Samsung, USA, ²Samsung, Korea

Abstract: We present a highly-configurable, low-power, low-area, SAW-less TX architecture that is based on a dynamically-biased power mixer. All FDD/TDD bands for 4G LTE and 3G WCDMA/ HSPA are supported in addition to 2G quad bands. The power-mixer bias current is dynamically adjusted based on the instantaneous baseband signal swing using a fully-differential hybrid full-wave rectifier / envelope detector circuit. Implemented in 28nm CMOS technology, the TX shows better than -157dBc/Hz RX-band noise emission and -41dBc ACLR for output powers up-to 4dBm across all 3G/4G bands. In addition, the TX can be configured to provide better than -65dBc CIM3, allowing it to meet stringent spurious emission specifications when transmitting 1RB 4G LTE signals in B13 / B26 / B1.
RM03C-3 14:10

Digitally Intensive Transmitter Employing RF Pulse Width Modulation for IoT Applications

Hyejeong Song, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A CMOS RF-PWM transmitter with a Class-D power amplifier (PA) is proposed for Internet of Things (IoT) applications. The transmitter utilizes two PLL-based PWM generators to convert baseband signals into an RF-PWM signal without an upconverter. For an LTE signal with a 1.4 MHz bandwidth and a 6.4 dB peak-to-average ratio (PAR), the RF-PWM transmitter achieves a power-added efficiency (PAE) of 17.5%, an error vector magnitude (EVM) of -24.9 dB, and an adjacent channel leakage ratio (ACLR) of -31 dBc at an average output power of 16.1 dBm. The transmitter achieves a peak output power of 22.4 dBm with 46.6% PAE, and 38.8% efficiency for the full RF-PWM transmitter including PAs.

RM03C-4 14:30

A Passive-Mixer-First Receiver with LO Leakage Suppression, 2.6dB NF, >15dBm Wide-Band IIP3, 66dB IRR Supporting Non-Contiguous Carrier Aggregation

Charles Wu¹, Yanjie Wang², Borivoje Nikolic¹, Christopher Hull²; ¹University of California at Berkeley, USA, ²Intel, USA

Abstract: A passive-mixer-first receiver design in 28 nm CMOS is presented where the front-end 5-bit mixer DAC provides a wide-band tuneable impedance match to suppress the LO leakage as well as to improve image rejection performance. Baseband LNA together with the AC-boosting compensation amplifier provides a 50MHz baseband bandwidth, which allows support for non-contiguous carrier aggregation for LTE. The proposed design can suppress multiple LO harmonics down below -62dBm. The system achieves < 3dB NF, >15dBm IIP3 and an IRR > 66dB with 60mW power.

RM03C-5 14:50

A Rel-12 2G/3G/LTE-Advanced 2CC Transmitter

B. Mohammadi¹, Masoud Kahrizi¹, John Leete¹, B. Pregardier², Sining Zhou¹, Janice Chiu¹, Behzad Saeidi¹, Yuyu Chang¹, M. Nariman³, A. Mirzaei¹, A. Hadji-Abdolhamid⁴, B. Nourani¹, Dmitriy Rozenblit¹, V. Aggarwal¹, H. Eslami¹, N. Vakilian¹, P. Mudge¹, Z. Zhou¹, C. Guan¹, N. Liu¹, Kevin Juan¹, A. Tarighat Mehrabani¹, Rahul Magoon¹, M. Rofougaran¹, R. Rofougaran¹; ¹Broadcom, USA, ²Ethertronics, USA, ³Qualcomm, USA, ⁴MaxLinear, USA

Abstract: This work presents a cellular transceiver capable of transmitting two simultaneous channels with an aggregate bandwidth of up to 40 MHz, supporting a 100 Mbps uplink rate. The transmitter has 8 RF output ports covering the cellular transmit bands within the 572–2100 MHz frequency range. It can support TX LTE-advanced Rel-12 Cat7, HSPA+ Rel-11, TDSCDMA Rel-9, and GSM/EDGE Rel-9. The 40 nm CMOS transmitter consumes 22 mA and 27 mA in 3G and LTE modes (at 0 dBm antenna power), respectively, including the PLL, DCXO and biasing for a single channel.

Monday, 18 May 2015 13:30–15:10 Room 126ABC Session RMO3D: Ultra-Low Power Transceivers Chair: Li-Wu Yang, Jiao-Tong University Co-Chair: Gernot Hueber, NXP Semiconductors

RMO3D-1 13:30 A Low-Power FSK/OOK Transmitter for 915MHz ISM Band

M. Shahriar Jahan, Jeremy Langford, Jeremy Holleman; University of Tennessee, USA

Abstract: A PLL-based, low-power, 915 MHz FSK/OOK transmitter is presented. The PLL uses gain-boosted LC VCO and hybrid injection-locked divider topologies to reduce power consumption with acceptable phase noise. In FSK mode, the transmitter consumes 367μ W from a 1.2 V supply with -18.6 dBm output power and achieves maximum 3 Mbps speed (122.3 pJ/bit). In OOK, power consumption is 314μ W with maximum 20 Mbps speed (15.7 pJ/bit). The transmitter occupies 0.29 mm² of die area in a 130 nm CMOS process.

RM03D-2 13:50

A Fully-Integrated Reconfigurable Transceiver for Narrowband Wireless Communication in 180nm CMOS

Zheng Song¹, Xiliang Liu¹, Xiaokun Zhao¹, Qiongbing Liu¹, Zongming Jin¹, Yun Yin¹, Yichuang Sun², Baoyong Chi¹; ¹Tsinghua University, China, ²University of Hertfordshire, UK

Abstract: A fully integrated reconfigurable transceiver (TRX) in 180nm CMOS for 750–960MHz narrowband applications is presented. The low-cost TRX consists of a low-IF receiver with 180 kHz signal bandwidth, a digital polar transmitter with 3.75 kHz signal bandwidth and a fractional-N frequency synthesizer. The receiver features a passive current mode mixer to improve the linearity and avoid the noise degradation due to the 1/f noise. The on-chip I/Q mismatch calibration is introduced to improve the image rejection ratio (IRR). The Inverse Class-D power amplifier (PA) is integrated into the transmitter to achieve high output power and efficiency, and the pre-distortion is exploited to realize the DPA linearization. Besides, the digital transmitter performs the power output by digitally controlling the DPA unit array. In order to compensate for PVT variations, the DCOC, I/Q mismatch, AFC and filter frequency tuning are all integrated in the transceiver. The RX achieves 5.1dB NF, 48dB IRR and 60dB gain dynamic range with 1dB step. The DPA provides the maximum 24.2dBm output power with 28.9% PAE. Furthermore, the TX demonstrates 4.9% EVM for 891MHz DQPSK signals at 19.09dBm output power.

RMO3D-3 14:10 A 380μW Rx, 2.6mW Tx 433MHz FSK Transceiver with a 102dB Link Budget and Bit-Level Duty Cycling

Nathan E. Roberts, Michael C. Kines, David D. Wentzloff; University of Michigan, USA

Abstract: This paper presents a low-power, long-range 433MHz transceiver designed for 2-FSK modulation at 1kbps in 8 different physical channels capable of communicating with a Texas Instruments CC1101. Designed in a 130nm CMOS process with an area of 1.1mm², the transmitter's output power is 0dBm and the receiver has a sensitivity of -102dBm producing a link budget >100dB and a theoretical range >5km assuming $1/d^2$ path loss. Low transmitter power is achieved using a 0.5V Class-E PA and low receiver power is achieved by implementing a digitally-assisted demodulator with further power reduction achieved through bit-level duty cycling with an off power of 110nW.

RM03D-4 14:30

A 0.7V 194 $_\mu W$ 31dB FOM 2.3–2.5GHz RF Frontend for WBAN with Mutual Noise Cancellation Using Passive Coupling

Mustafijur Rahman, Ramesh Harjani; University of Minnesota, USA

Abstract: A low power low noise 0.7V mixer first RF frontend for an IEEE 802.15.6 narrowband receiver is presented which uses passive coupling based frequency translated mutual noise cancellation. Unlike traditional noise cancelling techniques we perform symmetrical noise cancellation of a fully differential structure where each path cancels the noise of the other at IF. This paper tackles the noise figure and power consumption problems of sub 1V mixers. The FOM is 10dB higher and power consumption is 194 μ W which is 0.5X lower than the state of the art. The LO power used is -14dBm.

RM03D-5 14:50

Auto-Calibrating Threshold Compensation Technique for RF Energy Harvesters

Kaveh Gharehbaghi, Özge Zorlu, Fatih Koçer, Haluk Külah; Middle East Technical University, Turkey

Abstract: This paper presents the design of a new threshold compensation technique for UHF Dickson rectifiers. The proposed solution addresses the efficiency reduction of previous architectures especially under large input powers. The measurements show that the proposed technique achieves very good efficiency within 10 dBm variation of the input power. Therefore, the technique is suitable for applications where the incident power is not constant. Thanks to the reduction in the reverse leakage current, a peak efficiency of 34% at 433 MHz was measured.

Monday, 18 May 2015 15:40–17:20 Room 121ABC Session RMO4A: Techniques for High Tuning Range and Low Phase Noise

Chair: Mohyee Mikhemar, Broadcom Co-Chair: Danielle Griffith, Texas Instruments

RMO4A-1 15:40

A 0.5V 0.5mW Switching Current Source Oscillator

Masoud Babaie, Mina Shahmohammadi, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: This paper proposes a new RF oscillator topology that is suitable for ultra-low voltage and power applications. By employing alternating current source transistors, the structure combines the benefits of low supply voltage operation of conventional NMOS cross-coupled oscillators together with high current efficiency of the complementary push-pull oscillators. In addition, the 1/f noise upconversion is also reduced. The 40nm CMOS prototype exhibits an average FoM of 189.5 dBc/ Hz over 4–5 GHz tuning range, dissipating 0.5mW from 0.5V power supply, while abiding by the technology manufacturing rules.

RM04A-2 16:00

A Temperature Compensated VCO Using Feed-Forward Gain Multiplication for Cellular Applications

Yuyu Chang, Dmitriy Rozenblit, Behzad Saeidi, John Leete, Masoud Kahrizi, Janice Chiu, Sining Zhou, Morteza Vadipour, Kevin Juan, Rahul Magoon; Broadcom, USA

Abstract: A new LC-tank VCO to minimize frequency drift due to temperature variations for cellular applications is presented. By employing the feed-forward VCO gain multiplication technique, frequency drift is reduced by 83% without resorting to conventional temperature dependent biases and circuits. Additionally, the compensation circuit retains the original VCO behavior with no degradation in performance. A fractional-N PLL fabricated in 40 nm CMOS shows that the VCO draws 9 mA and the temperature compensation circuit draws 200 µA. Measurements show that the VCO has a tuning range of 46% (from 2890 MHz to 4560 MHz) and a phase noise of -102 dBc/Hz at 200 kHz offset centered at 3960 MHz at the PLL output before the divide-by-two circuit for 3G/LTE Band I.

RMO4A-3 16:20

A 3-Band Switched-Inductor LC VCO and Differential Current Re-Use Doubler Achieving 0.7-to-11.6GHz Tuning Range

Bodhisatwa Sadhu, Sachin Kalia, Ramesh Harjani; University of Minnesota, USA

Abstract: This paper presents a 3-bit switched inductor, 8-bit switched capacitor VCO utilizing frequency aware switch sizing to achieve 157% tuning range (0.7–5.8 GHz). Implemented in 65nm CMOS, the VCO maintains phase noise between -128 and -116 dBc/Hz at 1MHz offset across the tuning range. A current reuse differential frequency doubler extends the tuning range to 0.7–11.6 GHz (177%). The FOM_r s of the stand alone VCO as well as that of the VCO-doubler combination vary between 191 to 209 dBc/Hz over their respective tuning ranges.

RMO4A-4 16:40

A 2.8-to-5.8GHz Harmonic VCO in a 28nm UTBB FD-SOI CMOS Process

Luca Fanori¹, Ahmed Mahmoud¹, Thomas Mattsson², Peter Caputa², Sami Rämö³, Pietro Andreani⁴; ¹Marvell, Italy, ²Ericsson, Sweden, ³Ericsson, Finland, ⁴Lund University, Sweden

Abstract: A 2.8-to-5.8GHz VCO designed in a 28nm UTBB FD-SOI CMOS process adopts a reconfigurable active core to save power at the lower oscillation frequencies, and to enable a trade-off between power consumption and phase noise at all frequencies. The UTBB FD-SOI CMOS process is instrumental to achieve a tuning range in excess of one octave at low power consumption, while the use of an 8-shaped tank coil yields a VCO that is highly insensitive to external magnetic fields. The VCO operates from 0.9V and has a figure-of-merit of 186–189 dBc/Hz, depending on the oscillation frequency and the configuration of the oscillator core. The active area of the VCO is 380 μ m × 700 μ m.

RM04A-5 17:00

A 6.39GHz–14GHz Series Resonator Mode-Switching Oscillator with 186–188dB FoM and 197dB FoMA in 65nm CMOS

Abhishek Agrawal, Arun Natarajan; Oregon State University, USA

Abstract: CMOS LC voltage-controlled oscillators (VCO) with octave frequency tuning-range (FTR) are attractive for wideband radios. An area and power-efficient resonant mode-switching approach is presented that enables wide-FTR oscillators without compromising inductor Q, resulting in low phase noise and high VCO Figure-of-Merit (FoM). The proposed series resonator mode-switching approach results in a 6.4GHz to 14GHz VCO (74.6% FTR) in 65nm CMOS that achieves 186dB–188dB FoM. The scalability of this approach towards achieving even larger FTR is also demonstrated by a triple-mode 2.2GHz to 8.7GHz (119% FTR) VCO.

Monday, 18 May 2015 15:40–17:20 Room 122AB

Session RMO4B: Wideband and Reconfigurable High Frequency Integrated PAs

Chair: Margaret Szymanowski, Freescale Semiconductor Co-Chair: Patrick Reynaert, Katholieke Universiteit Leuven

RMO4B-1 15:40 A 5.5-GHz Multi-Mode Power Amplifier with Reconfigurable Output Matching Network

Huan-Sheng Chen, Yi-Keng Hsieh, Liang-Hung Lu; National Taiwan University, Taiwan

Abstract: A 5.5-GHz multi-mode PA with a reconfigurable output matching network which enables near-optimal impedances for size-scaling MOS transistors is proposed. The required load adaption is realized by using two transformers along with stage-bypassing technique for impedance coarse tuning and a switched capacitor for impedance fine tuning. Using a 90-nm CMOS process, the proposed PA demonstrates a PAE enhancement of 2.2×, 3.0×, and 5.0× respectively at 6-dB, 9-dB, and 15-dB transmit power back-off.

RMO4B-2 16:00 Low Cost Ka-Band 7W GaAs PHEMT Based HPA with GaN PHEMT Equivalent Performance

Kohei Fujii; M/A-COM Technology Solutions, USA

Abstract: This paper describes a very low cost MMIC high power amplifier (HPA) with output power of over 7W. The MMIC was fabricated using a GaAs PHEMT process with a state-of-the-art compact die area of 13.7mm². The HPA MMIC contains a phase and amplitude compensated output power combiner and super low loss phase compensated inter-stage matching networks. A four stage amplifier demonstrated commercially available GaN PHEMT based HPA equivalent performance with 7W saturated output power and 24dB small signal gain from 27.5GHz to 30GHz with peak output power of 8.3W and power added efficiency (PAE) of 27%. This low cost MMIC HPA achieved approximately 10-times lower production cost than GaN PHEMT based MMIC HPAs.

RMO4B-3 16:20

A 38GHz Inverse Class-F Power Amplifier with 38.5% Peak PAE, 16.5dB Gain, and 50mW $P_{\sf sat}$ in 0.13- μm SiGe BiCMOS

Seyed Yahya Mortazavi, Kwang-Jin Koh; Virginia Tech, USA

Abstract: This paper presents a 38 GHz 2-stage harmonic-tuned power amplifier consisted of a class-F⁻¹ output power amplifier proceeded by a class-AB driving stage in 0.13 μ m SiGe BiCMOS technology. In order to shape highly efficient class-F⁻¹ current and voltage waveforms, the PA adopts multi-resonance series and parallel load networks that modulate load impedance to generate an optimum 50- Ω for signal band, high impedance at the 2nd harmonic band and low impedance at the 3rd harmonic band. Inter-stage matching between the driver and output stage is also applied to deliver optimal power to the output stage with a maximum PAE, resulting in 38.5% of peak PAE with 50 mW P_{sat} at 38 GHz, which is one of the highest PAEs in silicon technology at mm-wave. The chip size is 0.9×0.55 μ m² including all pads.

RMO4B-4 16:40

A Wideband 60GHz Class-E/F, Power Amplifier in 40nm CMOS

Masoud Babaie, Robert Bogdan Staszewski, Luca Galatro, Marco Spirito; Technische Universiteit Delft, The Netherlands

Abstract: This paper presents a fully integrated 60 GHz power amplifier in 40nm CMOS that reaches the highest reported product of power-added efficiency and bandwidth. It is achieved through low/ moderate coupling-factor transformers in the preliminary stages and a proper second harmonic termination of the output stage, such that it can operate as a class- E/F_2 switched-mode PA at the saturation point. The three-stage PA delivers 17.9dBm saturated output power with 20% peak PAE. It demonstrates a bandwidth of 9.7 GHz with a peak gain of 21.6 dB.

RMO4B-5 17:00

A 2×2 Dynamic Polarization-Controlling Integrated Phased Array

Amirreza Safaripour, Steven M. Bowers, Kaushik Dasgupta, Ali Hajimiri; Caltech, USA

Abstract: Radiator arrays with Dynamic Polarization Control (DPC) and 2D beam steering enable polarization matching to the receiver antenna regardless of its polarization, orientation, and location. A fully integrated 122.9 GHz 2×2 DPC multi-port driven phased array radiates all linear polarizations (0°–180° polarization angles) with axial ratios above 14 dB, and controls the axial ratio from 1.2 dB (circular) to 17.8 dB (linear) with a maximum EIRP of +12.3 dBm and 2D beam steering of up to 15°.

Monday, 18 May 2015 15:40–17:20 Room 125AB Session RMO4C: Wireless Connectivity Transceivers and Power Amplifier Techniques Chair: Julian Tham, Broadcom Co-Chair: Renaldi Winoto, Marvell

RM04C-1 15:40 Dual-Band Integrated Wi-Fi PAs with Load-Line Adjustment and Phase Compensated Power Detector

Yuan-Hung Chung, Po-Yu Chang, Meng-Hsiung Hung, Ming-Yeh Hsu, Che-Hung Liao, Chun-Wei Lin; MediaTek, Taiwan

Abstract: A load-line adjusted 2.4GHz PA is designed to operate in full power (18dBm/150mA) & mid power (7dBm/19mA) in OFDM with ~130mA saving. To improve network throughput in dense environment with per-packet TX power control, the phase-compensated power detector achieves ± 0.6 dB accuracy for the entire 5GHz band over 2:1 VSWR and 16dBm ± 0.25 dB over channel flatness in VHT80MCS9. The chip area is 0.21mm² for load-line adjusted 2.4GHz PA and 0.13 mm² for 5GHz PA with power detector.

RM04C-2 16:00

A Highly Integrated Single Chip 5–6GHz Front-End IC Based on SiGe BiCMOS That Enhances 802.11ac WLAN Radio Front-End Designs

Chun-Wen Paul Huang, Kenny Christainsen, Sergey Nabokin, Rafik Mirzayantz, Justin Allum, Andrew Chen, Lui Lam, Mike McPartlin, Mark Doherty, Bill Vaillancourt; Skyworks Solutions, USA **Abstract:** A highly integrated 4.9–5.9 GHz single chip front-end IC (FEIC) is presented, which is based on SiGe BiCMOS, realized in a 1.6 mm2 chip area and in an ultra-compact $1.7 \times 2.0 \times 0.33$ mm3 package. The Tx chain has >30 dB gain and meets -40 dB DEVM up to Pout of 15 dBm and -35 dB DEVM up to Pout of 17 dBm with a 3.3 V supply, insensitive to modulation bandwidths and duty cycle. The ultra-low back-off DEVM enables the emerging 1024-QAM applications. The integrated log detector enhances the dynamic range for the transmit power control. The Rx chain features <2.8 dB NF and 15 dB gain with 3 dBm IIP3 and 10 dB bypass attenuator with 23 dBm IIP3. All the unique features enhance the front-end circuit designs of complex radios based on the 802.11ac standard.

RM04C-3 16:20

A Sub-GHz Low-Power Transceiver with PAPR-Tolerant Power Amplifier for 802.11ah Applications

Xiaobao Yu¹, Meng Wei¹, Yun Yin¹, Ying Song¹, Zhihua Wang¹, Yichuang Sun², Baoyong Chi¹; ¹Tsinghua University, China, ²University of Hertfordshire, UK

Abstract: A fully-integrated Sub-GHz low-power transceiver (TRX) for 802.11ah applications is presented. The receiver takes both advantages of Low-IF/Zero-IF architectures while supporting 1/2/8MHz reconfigurable signal bandwidth. A Σ - Δ fractional-N PLL with Class-C VCO is employed to provide the LOs. In order to enhance the power amplifier (PA) back-off efficiency, a Peak-to-Average-Power-Ratio (PAPR) tolerant technique is proposed with the aid of a power control loop to dynamically detect the input signal PAPR and flexibly reconfigures the PA's operation modes. With digitally-assisted self-calibrations for LO leakage and image rejection, the transmitter obtains -51.6dBc LO leakage and 51.2dBc image rejection ratio (IRR). A JESD207 interface is also included to communicate with the digital baseband. Implemented in 180nm CMOS, the receiver achieves 4dB NF and dissipates 18.9mW from a 1.7V supply. The CMOS PA achieves 13.6dBm output P1dB with 25.5% PAE in high power mode (HPM) and ×2.61 PAE improvement at 7dB back-off power in low power mode (LPM).

RM04C-4 16:40

A Pulsed UWB Transmitter and Receiver with 4-Element Beamforming for 1-Gbps Meter-Range WPAN Applications

Jaegan Ko, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A UWB transceiver that employs pulsed, multiband signaling with frequency-hopping is demonstrated in a 65nm CMOS process. The transceiver satisfies ECC requirements and operates in the frequency range 6–8.5 GHz. The proposed signaling scheme provides flexibility to satisfy regulations across multiple regions with low implementation complexity. The receiver employs 4-element beamforming at IF to enhance sensitivity. The beamforming architecture does not require a wideband delay circuit at the RX. The prototype demonstrates 1 Gbps data rate over 2 meters, while consuming 221 mW in the TX and 211 mW in the receiver.

RM04C-5 17:00

A 4.6–5.35GHz Transceiver with 38dB On-Chip Self-Interference Cancelation at 10kHz Offset Frequency

Xuebei Yang, Aydin Babakhani; Rice University, USA

Abstract: A 4.6–5.35GHz transceiver with active self-interference cancelation is reported. The active cancelation circuit cancels up to 38dB of TX leakage at 10kHz offset from the RX signal. It increases the interference P1dB from -25dBm to -8dBm, and RX gain by 15dB. When the transceiver is utilized in a magnetic resonance spectroscopy system, the SNR improves by 15dB. Furthermore, in addition to the traditional method of B_n -sweep, for the first time, the method of frequency-sweep is demonstrated.

Monday, 18 May 2015 15:40–17:20 Room 126ABC Session RMO4D: Low-Power Wideband SoCs Chair: David Wentzloff, University of Michigan Co-Chair: Jenshan Lin, University of Florida

RMO4D-1 15:40 A Symbol-Duty-Cycled 440pJ/b Impulse Radio Receiver with 0.57aJ Sensitivity in 130nm CMOS

Daniele Vogrig, Andrea Bevilacqua, Andrea Gerosa, Andrea Neviani; Università di Padova, Italy **Abstract:** A non-coherent 130nm CMOS UWB impulse radio receiver for ultra-low energy consumption applications is presented. The receiver supports a 4.4 Mb/s data rate employing 2-PPM modulation, with a sensitivity of 0.57 aJ. Implementing symbol-level duty-cycling, such an outstanding performance is attained at an energy consumption of only 440 pJ/b.

RMO4D-2 16:00

A Fully Integrated $0.18\mu m$ CMOS UWB SoC for Wireless Body Area Network Applications

Myung Cheol Park¹, Won Il Chang², Kyoung Hak Lee¹, Dong-Sun Kim³, Tae-Ho Hwang³, Yun Seong Eo¹; ¹Silicon R&D, Korea, ²Kwangwoon University, Korea, ³KETI, Korea

Abstract: A fully integrated 3–5GHz CMOS transceiver SoC for WBAN is presented in this paper. To achieve the low power and low complexity, OOK receiver architecture and the digital impulse generator are employed. For the rejection of the undesired interferers, the tunable RF notch filter is integrated and measured results show more than 9 dB improvement of the sensitivity. The measured energy efficiency of transmitter and the receiver sensitivity are 20.6 pJ/bit and -86.5 dBm, respectively.

RMO4D-3 16:20

A 65nm CMOS Low Power Impulse Radar for Respiratory Feature Extraction Shao-Ting Tseng¹, Yu-Hsien Kao¹, Chun-Chieh Peng¹, Jinn-Yann Liu¹, Shao-Chang Chu¹, Guo-Feng Hong¹, Chi-Hsuan Hsieh¹, Kung-Tuo Hsu¹, Wen-Te Liu², Yuan-Hao Huang¹, Shi-Yu Huang¹, Ta-Shun Chu¹; ¹National Tsing-Hua University, Taiwan, ²Taipei Medical University, Taiwan

Abstract: This paper presents a wireless sensor system for monitoring human respiratory activities. The sensor is composed of a fully-integrated CMOS impulse radar chip and a DSP platform that is used for human respiratory feature extraction. The proposed and implemented radar chip was fabricated using in the TSMC 65nm CMOS technology. It can achieve the 1.5mm scanning resolution over the 15m scanning range with total 21mW power consumption. Moreover, the timing circuitry supporting range gated sensing and the pulse generator are all digital standard cell-based design which is very favorable to the technology scaling. The real-time DSP platform captures the wireless data via the CMOS radar chip and processes that through a human respiratory feature extraction algorithm. The entire system can fully operate to validate the performance of the wireless sensor

system. Furthermore, the clinical trial was carried on and the system was proved helpful in rapid screen for respiratory diseases.

RMO4D-4 16:40

A 3.6cm² Wirelessly-Powered UWB SoC with -30.7dBm Rectifier Sensitivity and Sub-10cm Range Resolution

Jian Kang, Patrick Chiang, Arun Natarajan; Oregon State University, USA

Abstract: This paper discusses the design of a battery-less wirelessly-powered UWB system-ona-chip (SoC) tag for area-constrained localization applications. An antenna-rectifier co-design methodology optimizes sensitivity and increases range under tag area constraints. A low-voltage (0.8-V) UWB TX enables high rectifier sensitivity by reducing required rectifier output voltage. The 2.4GHz rectifier, power-management unit and 8GHz UWB TX are integrated in 65nm CMOS and the rectifier demonstrates state-of-the-art -30.7dBm sensitivity for 1V output with only 1.3cm² antenna area, representing a 2.3x improvement in sensitivity over previously published work, at 2.6x higher frequency with 9x smaller antenna area. Measurements in an office corridor demonstrate 20m range with 36dBm TX EIRP. The 0.8-V 8GHz UWB TX consumes 64pJ/pulse at 28MHz pulse repetition rate and achieves 2.4GHz -10dB bandwidth. Wireless measurements demonstrate sub-10cm range resolution at range > 10m.

RM04D-5 17:00

Low-Power Injection-Locked Zero-IF Self-Oscillating Mixer for Self-Powered Millimeter-Wave Identification (MMID) Active Tag in 65-nm CMOS

Pascal Burasa¹, Nicolas Constantin², Ke Wu¹; ¹École Polytechnique de Montréal, Canada, ²Université du Québec, Canada

Abstract: In this paper, a 40 GHz zero-IF self-oscillating mixer (SOM) with low-power consumption, is proposed and demonstrated for the next generation of battery-free yet active mm-wave identification (MMID) tag. It exploits the mixing property of LC cross-coupled VCO, and by injection-locking the SOM to the reader's carrier frequency, it enables a direct-conversion to the baseband. It, therefore, does not require any external LO source (self-mixing) nor RF frequency conversion into IF frequency. A chip was designed using 65-nm CMOS process, and experimental results exhibit a conversion loss of about 29 dB, with a power consumption of only 280 μW.

Tuesday, 19 May 2015 08:00-09:40 Room 121ABC

Session RTU1A: mm-Wave & THz Frequency Multipliers Chair: Kamran Entesari, Texas A&M University Co-Chair: Timothy Hancock, MIT Lincoln Laboratory

RTU1A-1 08:00 A +2.3dBm 124–158GHz Class-C Frequency Quadrupler with Folded-Transformer Based Multi-Phase Driving

Taiyun Chi, John Papapolymerou, Hua Wang; Georgia Institute of Technology, USA

Abstract: This paper presents a D-band frequency quadrupler from 124GHz to 158GHz. The design leverages a folded-transformer based passive network to generate high-quality and broadband differential quadrature driving signals with low loss for the input tone centered at 35GHz. Then, the four-phase signals drive the 1st-stage frequency doublers to yield fully differential signals at the 2nd harmonic frequency (70GHz), which feed another push-push frequency doubler and generate the desired 4th harmonic output at 140GHz. The push-push doublers are designed based on 2nd harmonic load-pull with Class-C operation for optimized output power and efficiency. The quadrupler is implemented in a 32nm CMOS SOI process occupying only 530µm-by-550µm. It achieves the state-of-the-art output power of +2.3dBm, a peak DC-to-RF efficiency of 5.3%, and the best reported -3dB bandwidth of 24% at D-band under 1.1V supply.

RTU1A-2 08:20

A 55-GHz Power-Efficient Frequency Quadrupler with High Harmonic Rejection in $0.1\mathchar`umu$ SiGe BiCMOS Technology

Yi-Shin Yeh, Brian A. Floyd; North Carolina State University, USA

Abstract: This paper presents a V-band frequency quadrupler in 0.1-µm SiGe BiCMOS technology with 3-dB bandwidth from 44.8 to 57.2 GHz. The circuit employs cascode stacks comprising in-phase class-C common-emitter and anti-phase class-AB cascode devices to obtain current pulses at ×4 frequency. Four such cascodes driven with differential and tunable quadrature increase the 4th harmonic output power while suppressing all other harmonics 22 dB or more. Measurements show >7.4-dBm 4th harmonic output power, and >5.2% power efficiency for the core of the multiplier.

RTU1A-3 08:40

Frequency Doublers with 10.2/5.2dBm Peak Power at 100/202GHz in 45nm SOI CMOS

Gang Liu, Jefy Jayamon, James F. Buckwalter, Peter Asbeck; University of California at San Diego, USA

Abstract: This paper presents frequency doublers with high output power for millimeter-wave applications. The circuits are fabricated using a 45nm SOI CMOS technology. A new circuit topology, combining a push-push doubler core with a cascaded stacked amplifier, has been implemented to increase the output power. The first doubler delivers 10.2 dBm peak power at 100 GHz output, with a 3-dB bandwidth from 88 to 104 GHz and DC-RF efficiency of 4.1%, while the second doubler has 5.2 dBm peak power at 202 GHz, with a 3-dB bandwidth from 180 to 212 GHz and DC-RF efficiency of 3.3%. To the authors' knowledge, these are the highest powers reported for silicon frequency doublers in similar frequency ranges to date. The 200 GHz doubler also provides the highest on-chip power from a single-element signal generation circuit without power combining.

RTU1A-4 09:00

0.39-0.45THz Symmetric MOS-Varactor Frequency Tripler in 65-nm CMOS

Zeshan Ahmad¹, Insoo Kim², Kenneth K. O¹; ¹University of Texas at Dallas, USA, ²Samsung, USA **Abstract:** A broadband passive frequency tripler using an accumulation-mode symmetric MOS varactor (SVAR) in 65-nm bulk CMOS process is demonstrated. The measured output power (P_{out}) is >-15dBm over a 57GHz band. This tripler incorporating an on-chip patch antenna operates at frequencies between 390 and 456GHz, and achieves a peak Effective Isotropically Radiated Power (EIRP) of -5dBm. The measurement setup limited peak P_{out} and conversion loss is -3.2dBm and 15.2dB, respectively at 447GHz after antenna gain de-embedding. This is the highest reported output power for all CMOS sources operating above 350GHz and can be integrated with an on-chip input driver amplifier.

RTU1A-5 09:20

A 60GHz 25% Tuning Range Frequency Generator with Implicit Divider Based on Third Harmonic Extraction with 182dBc/Hz FoM

Zhirui Zong, Masoud Babaie, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: A 60 GHz frequency generator with implicit \div 3 divider is proposed in this work to improve the system-level efficiency and phase noise. A third-harmonic boosting technique is utilized to simultaneously generate 20GHz and sufficiently strong 60 GHz signals in order to avoid any divider operating at 60 GHz. The prototype is fabricated in 40nm CMOS and exhibits a phase noise of -100 dBc/Hz at 1MHz offset from 60 GHz carrier and 25% tuning range. The phase noise and FoM_r (figure-of-merit with tuning range) are improved by 5 dB and 4.6 dB, respectively, compared to state-of-the-art.

Tuesday, 19 May 2015 08:00-09:40 Room 125AB

Session RTU1C: Reconfigurable and Interference-Tolerant Transceivers Chair: Vito Giannini, Texas Instruments Co-Chair: Ramesh Harjani, University of Minnesota

RTU1C-1 08:00 The MATRICs RF-FPGA in 180nm SiGe-on-SOI BiCMOS

Lawrence J. Kushner, Kevin W. Sliech, Gregory M. Flewelling, Joseph D. Cali, Curtis M. Grens, Steven E. Turner, Douglas S. Jansen, Joseph L. Wood, Gary M. Madison; BAE Systems, USA

Abstract: MATRICs (Microwave Array Technology for Reconfigurable Integrated Circuits) is a DCto-20 GHz general purpose reconfigurable array of RF circuits embedded in a flexible switch fabric. Fabricated in a commercial SiGe-on-SOI BiCMOS process, the MATRICS IC employs SiGe HBTs for high-linearity (> + 10 dBm IIP3) amplification and low phase-noise frequency generation, and SOI FETs for low-loss switching. It achieves high on-chip RF isolation (>80 dB at 16 GHz) due to the high-resistivity SOI substrate, differential signalling, and chip-scale flip-chip bump packaging. MATRICs will allow fixed-function RF systems to have the size, weight, and power benefits of a custom RF ASIC without the associated long development cycle and high NRE, and enable future RF subsystems to be dynamically reconfigured on-the-fly, adapting to changing environments.

RTU1C-2 08:20

An IF 8-Element 2-Beam Bit-Stream Band-Pass Beamformer

Jaehun Jeong, Nicholas Collins, Michael P. Flynn; University of Michigan, USA

Abstract: We introduce a new ADC-digital co-design approach to IF digital beamforming (DBF) that combines continuous-time band-pass $\Delta\Sigma$ modulators (CTBPDSMs) and bit-stream processing (BSP) to achieve highly flexible and low-cost DBF. Our prototype DBF IC digitizes eight 260MHz IF signals at 1040MS/s with band-pass ADCs, and performs DBF directly on the over-sampled, undecimated ADC outputs, achieving band-pass filtering in both spatial and frequency domains. With 12b programmable complex weights, the prototype generates two simultaneous beams, and achieves an SNDR of 63.3dB with an 8.9dB array improvement over a 10MHz bandwidth. Fabricated in 65nm CMOS, the prototype is the first IC implementation of IF DBF, occupies 0.28mm², and consumes 124mW.

RTU1C-3 08:40

A Switched-Capacitor RF Front End with Embedded Programmable High Order Filtering and a +15dBm OB-B1dB

Yang Xu, Peter R. Kinget; Columbia University, USA

Abstract: A 0.1–0.7GHz switched-capacitor RF front end features tunable center frequency and programmable filter order as well as very high tolerance for out-of-band (OB) blockers. RF input impedance matching, N-path filtering, down-conversion, and high order IIR filtering are implemented using highly linear switches and capacitors only. The 3.24mm² 40nm CMOS front-end prototype consumes 38.5–76.5mA, achieves 24dBm OB-IIP3 and 14.7dBm B1dB for a 30MHz offset, 6.8 to 9.7dB NF, and >66dB calibrated harmonic rejection ratio.

RTU1C-4 09:00

An Interferer-Tolerant Receiver with Active Feedback for Cognitive Radio Applications

Vahid Dabbagh Rezaei, Masoud Moslehi Bajestan, Hajir Hedayati, Kamran Entesari; Texas A&M University, USA

Abstract: A receiver architecture covering 54–864 MHz and suitable for tolerating large interferers is presented in 0.18 μ m CMOS. It alleviates the problem of LO harmonics mixing with the aid of a heterodyne conversion, and by employing an active feedback, provides an IIP3 of better than +13.4 dBm, comparable with state-of-the-art. Noise canceling techniques are used to improve the NF of the receiver so that the receiver achieves NF of 8.6 and 18 dB in the absence, and presence of an interferer, as strong as 0 dBm, respectively.

RTU1C-5 09:20

0.4–6GHz, 17-dBm B1dB, 36-dBm IIP3 Channel-Selecting, Low-Noise Amplifier for SAW-Less 3G/4G FDD Receivers

Cheng-kai Luo¹, Prasad S. Gudem², James F. Buckwalter³; ¹University of California at San Diego, USA, ²Qualcomm, USA, ³University of California at Santa Barbara, USA

Abstract: A channel-selecting, low-noise amplifier (CS-LNA) is presented that meets the requirements for a SAW-less diversity path receiver in frequency-division duplexing (FDD) cellular systems. An N-path filter is incorporated into the LNA feedback network to tune from 400 MHz to 6 GHz. The proposed CS-LNA creates close-in stopbands around the passband to suppress transmit (TX) blockers up to 17 dBm. This work reports an out-of-band (OOB) IIP3 of 36 dBm and IB IIP3 of 10 dBm with the maximum rejection larger than 60 dB. To the author's knowledge, this is the highest blocker rejection, power-handling capability and IIP3 for an LNA that is tunable over more than a decade.

Tuesday, 19 May 2015 08:00–09:40 Room 126ABC Session RTU1D: Wireline Transceiver Circuits Chair: Amin Arbabian, Stanford University Co-Chair: Ping Gui, Southern Methodist University

RTU1D-1 08:00 A 25-Gb/s FIR Equalizer Based on Highly Linear All-Pass Delay-Line Stages in 28-nm LP CMOS

F. Loi¹, E. Mammei², F. Radice², M. Bruccoleri², S. Erba², Matteo Bassi¹, Andrea Mazzanti¹; ¹Università di Pavia, Italy, ²STMicroelectronics, Italy

Abstract: FIR filters are attractive to enhance the equalization performances of high speed wireline receivers, providing high flexibility to match the channel frequency response and compatibility with simple adaptation techniques. This paper presents a 25-Gb/s 4-tap FIR equalizer in 28-nm LP CMOS. To keep high SNR and not compromise equalization performances, a new all-pass stage is proposed to realize a delay line accommodating large input signal amplitude. The chip draws 25 mA from 1V supply and measurements with 900 mV_{pk-pk} input signal prove equalization of a 20-dB loss channel with 50% horizontal eye opening at BER=10⁻¹². Experimental results compare favorably against state of the art.

RTU1D-2 08:20

A Low-Voltage Low-Power 25Gb/s Clock and Data Recovery with Equalizer in 65nm CMOS

Shita Guo¹, Tianwei Liu¹, Tao Zhang¹, Tianzuo Xi¹, Guoying Wu¹, Ping Gui¹, Yanli Fan², Win Maung², Mark Morgan²; ¹Southern Methodist University, USA, ²Texas Instruments, USA

Abstract: A novel low-power low-jitter 25 Gb/s clock and data recovery (CDR) circuit with equalizer that can work at an ultra-low supply voltage of 0.6 V is proposed and implemented in a 65 nm CMOS process. A two-tank transformer-feedback technique is proposed in the 25 GHz LC-tank VCO to improve the phase noise performance at low supply voltage. Forward-body biasing (FBB) technique is proposed in the low-voltage signal path to reduce the threshold voltage of the transistors, thus increasing the signal amplitude and achieving low BER. The measurement results show that the CDR and equalizer can work under 0.6 V with 0.23ps/4.62ps (rms/pk-pk) of recovered clock jitter. The measured power consumption of the CDR with the equalizer is 48.8 mW (1.95 mW/Gb/s).

RTU1D-3 08:40

A 30Gb/s CMOS Driver Integrated with Silicon Photonics MZM

Ke Li, Dave J. Thomson, Shenghao Liu, Peter Wilson, Graham T. Reed; University of Southampton, UK

Abstract: A voltage mode modulator driver is proposed in the TSMC 65nm low power CMOS process. In the electrical testing, the driver itself can achieve a bit rate of 40Gb/s with the single-ended output swing of 1.65V. Unlike equivalent CML modulator drivers, when the proposed driver is integrated with the silicon photonic MZM, it does not require an additional biasing network. The integrated electro-optic transmitter can achieve 30Gb/s with an extinction ratio of 4.05dB, with the power consumption of main driver being 323mW.

RTU1D-4 09:00

A Low-Power 40Gb/s Optical Receiver in Silicon

Zhe Xuan¹, Ran Ding², Yang Liu², Tom Baehr-Jones², Michael Hochberg², Firooz Aflatouni¹; ¹University of Pennsylvania, USA, ²Coriant Advanced Technology Group, USA

Abstract: A low-power 40 Gb/s optical receiver is reported. The receiver consists of a broadband photodiode followed by a low-noise transimpedance amplifier front-end, a 3-stage Cherry-Hooper limiting amplifier, an output driver, and an offset cancellation network. The photodiode is fabricated in a 0.18 μ m Ge-on-SOI process and the electronic chip is fabricated in a 0.13 μ m SiGe BiCMOS process. The receiver consumes 77 mW. The output eye diagram has a 100 mV single-ended opening with input photocurrents as low as 120 μ A_m.

Tuesday, 19 May 2015 10:10–11:50 Room 122ABC Session RTU2B: mm-Wave LNAs and Beamformers Chair: Yanjie Wang, Intel Co-Chair: Hua Wang, Georgia Institute of Technology

RTU2B-1 10:10 A 18mW, 3.3dB NF, 60GHz LNA in 32nm SOI CMOS Technology with Autonomic NF Calibration

J.-O. Plouchart¹, F. Wang², A. Balteanu¹, B. Parker¹, M.A.T. Sanduleanu¹, M. Yeck¹, V.H.-C. Chen¹, W. Woods¹, Bodhisatwa Sadhu¹, A. Valdes-Garcia¹, X. Li², Daniel Friedman¹; ¹IBM, USA, ²Carnegie Mellon University, USA

Abstract: A self-healing mmWave SoC integrating an 8052 microcontroller with 12kB of memory, an ADC, a temperature sensor, and a 3-stage cascode 60GHz LNA, implemented in a 32nm SOI CMOS technology exhibits a peak gain of 21dB, an average 3.3dB NF from 53 to 62GHz and 18mW power consumption. An indirect NF sensing algorithm was implemented on the integrated uC, which enables an adaptive biasing algorithm to reduce the 60GHz NF sigma and LNA power consumption by 37 and 40%, respectively, across P,V,T.

RTU2B-2 10:30

An 80-GHz Low Noise Amplifier Resilient to the TX-Spillover in Phase-Modulated Continuous-Wave Radars

Alaa Medra, Davide Guermandi, Kristof Vaesen, Qixian Shi, Piet Wambacq, Vito Giannini; imec, Belgium

Abstract: We propose an 80GHz low noise amplifier capable of linearly handling and canceling a TX spillover up to -20dBm. The cancellation circuit is mainly intended for phase-modulated continuous-wave radar. The circuit is implemented in a 28nm CMOS technology and achieves a gain, NF and iP1dB of 15.2dB, 5.5dB and -15.5dBm respectively, while attenuating the TX spillover by 13.5dB.

RTU2B-3 10:50

A 40GHz to 67GHz Bandwidth 23dB Gain 5.8dB Maximum NF mm-Wave LNA in 28nm CMOS

Kambiz Hadipour, Andrea Ghilioni, Andrea Mazzanti, Matteo Bassi, Francesco Svelto; Università di Pavia, Italy

Abstract: Wide-band receivers at mm-waves enable several Gbit/s communications with simple modulation. This work presents the design of an ultra wide-band LNA in 28nm CMOS. Common source stages are stacked in a current-sharing configuration and coupled through third-order L-C band-pass networks. In addition, the stages are stagger-tuned to maximize bandwidth and gain flatness. Realized prototypes show 23dB peak gain over 40–67GHz with 5.8dB maximum in-band noise figure and 25.3mW power consumption.

RTU2B-4 11:10 Dual-Vector Phase Rotator for Doherty Beamformers

Kevin Greene, Brian A. Floyd; North Carolina State University, USA

Abstract: A 28-GHz dual-vector phase rotator is introduced, having the capability of generating two quadrature output signals that track one another in phase. The 4-bit dual-vector rotator was implemented in IBM 0.12- μ m SiGe BiCMOS technology and achieves full 360° phase shifting, RMS phase and amplitude errors of < 5 degrees and < 0.8 dB, respectively for both output vectors, and 10–12 dB of gain. Output 1-dB compression points for both quadrature outputs is -6.5 to -4.4 dBm, suitable for directly driving a Doherty amplifier in a 28-GHz beamformer.

Tuesday, 19 May 2015 10:10–11:50 Room 125AB Session RTU2C: Mixed Signal Circuits for RF Receivers Chair: Ayman Fayed, Iowa State University Co-Chair: Jennifer Kitchen, Arizona State University

RTU2C-1 10:10 A Wideband Under-Sampling Blocker Detector with a 0.7–2.7GHz Mixer-First Receiver

Olli Viitala¹, Mikko Kaltiokallio², Marko Kosunen¹, Kari Stadius¹, Jussi Ryynänen¹; ¹Aalto University, Finland, ²TDK, Finland

Abstract: This paper presents a low power wideband blocker detector consisting of an undersampling SAR ADC connected to the RF input node of a wideband mixer-first receiver. The original carrier frequency of the blocker is determined from folded spectra by using three FFTs sampled at different rates whose ratios correspond to prime numbers. The detector is targeted for blocker power levels between 0 and -30 dBm within frequency range of 0.7–2.7 GHz. The achieved ADC maximum SNDR of 28 dB, together with 10 dB input buffer gain control, provide sufficient blocker detection sensitivity in the desired range. The measured sampled input signal spectra show the designed circuits capability to simultaneously detect narrowband and wideband blockers. The reconstructed folded spectrum shows the original blocker frequencies. The power consumption of the wideband detector is only 7 mW, while the receiver consumes 42 mW.

RTU2C-2 10:30

Gain and Noise Optimization of a Passive Sliding IF Architecture

S. Vahid M. Bonehi, Christoph Beyerstedt, Zhimiao Chen, Lei Liao, Ralf Wunderlich, Stefan Heinen; RWTH Aachen University, Germany

Abstract: This paper presents gain and noise optimization of a passive Sliding IF downconverter as a promising choice for Zero-IF and Low-IF receivers. With detailed mathematical analysis of the architecture we propose a new design that provides 7.6 dB improvement of relative conversion gain with profound noise figure and IIP3 performance. The results of the mathematical derivation are supported by modeling, circuit simulation and measurement of a prototype chip fabricated on a standard 130nm CMOS technology. The chip operates under supply voltage of 1.2V and occupies 750 μ m × 200 μ m active area.

RTU2C-3 10:50

A 54.4-mW 4th-Order Quadrature Bandpass CT $\Sigma\Delta$ Modulator with 33-MHz BW and 10-Bit ENOB for a GNSS Receiver

Junfeng Zhang¹, Zehong Zhang¹, Yang Xu¹, Yichuang Sun², Baoyong Chi¹, ¹Tsinghua University, China, ²University of Hertfordshire, UK

Abstract: A 4th-order quadrature bandpass continuous-time sigma-delta modulator for a GNSS receiver is presented. With significantly wide bandwidth, the modulator is able to digitalize the down-conversed GNSS signals in two adjacent signal bands simultaneously. This makes it possible to realize simultaneous dual-frequency reception from two satellite systems with one receiver channel instead of two independent channels. A direct RZ feedback is introduced into the input of the last integrator to realize ELD compensation. Power-efficient amplifiers are employed in the active RC integrators, and self-calibrated comparators are used to implement the low-power 3-bit quantizers. Implemented in 180nm CMOS, the modulator achieves 62.1dB peak SNDR, 64dB DR and 59.3dB image rejection ratio (IRR), and consumes 54.4mW from a 1.8V power supply.

RTU2C-4 11:10 A 24GS/s Single-Core Flash ADC with 3 Bit Resolution in 28nm Low-Power Digital CMOS

G. Tretter, M. Khafaji, D. Fritsche, C. Carta, F. Ellinger; Technische Universität Dresden, Germany **Abstract:** This paper presents the design and characterization of a 24 GS/s, 3 bit flash ADC in 28nm low-power (LP) digital CMOS. The circuit was designed with the goal of achieving speed performance above state of the art for a single ADC core. The ADC is capable of delivering its full sampling rate without time interleaving, which makes it the fastest single core ADC in CMOS reported to date to the best of our knowledge. With a power consumption of 406mW and an effective number of bits (ENOB) of 2.2 at 24 GS/s, the ADC achieves a figure of merit (FOM) of 3.6 pJ per conversion step, which is the lowest reported value for single-core ADCs operating above 15 GHz. The very high sampling rate of the presented ADC enables ultra-high-speed ADC systems through moderate time interleaving.

Tuesday, 19 May 2015 10:10–11:50 Room 126ABC

Session RTU2D: High Frequency and Non-Linear Device Modeling Chair: Tzung-Yin Lee, Skyworks Solutions Co-Chair: Vipul Jain, Anokiwave

RTU2D-1 10:10 Design of Lange Couplers with Local Ground References Using SiGe BiCMOS Technology for mm-Wave Applications

S. Wane¹, L. Leyssenne², O. Tesson¹, O. Doussin³, D. Bajon³, D. Lesénéchal², T.V. Dinh², M.P. van Heijden⁴, Ralf Pijper⁴, P. Magnée⁴, P. Descamps², A. Erdem¹; ¹NXP Semiconductors, France, ²LaMIPS, France, ³ISAE, France, ⁴NXP Semiconductors, The Netherlands

Abstract: SiGe BiCMOS design solutions for Lange Couplers operating in the mm-Wave domain are proposed. Various circuit topologies are designed, fabricated, and experimentally compared in terms of their RF performances. Effect of grounding strategies and influence of DTI pattering are studied both for CPS and CPW topologies to evaluate dependence of obtained RF performances on Die back-side grounding strategies. Perspectives for physics-based broadband equivalent circuit model extraction are proposed for lumped elements implementation of Lange Couplers using custom variation-aware RLC library elements.

RTU2D-2 10:30

4-Port RF Performance Assessment and Compact Modeling of UTBB-FDSOI Transistors

Jean-Charles Barbé, Luca Lucci, Alexandre Siligaris, Pierre Vincent, Olivier Faynot; CEA-LETI, France

Abstract: RF small-signal performances of Ultra-Thin Body and Box FDSOI transistors are evaluated using state-of-the-art 4-port characterization in the 100MHz–24GHz frequency range. Front-Gate cut-off frequencies and related figures of merit are extracted to assess the capabilities of the technology at 28 nm technology node for RF applications. Back-Gate cut-off frequency is also extracted and shown to be in the 80GHz range, while front-gate cut-off is higher than 380GHz. A 4-port S-parameter RF extraction for a SPICE model featuring gate width scalability is described.

RTU2D-3 10:50

4-Terminal Angelov Model for SOI CMOS MESFETs

Seth J. Wilk, William Lepkowski, Payam Habibimehr, Trevor J. Thornton; Arizona State University, USA

Abstract: This work describes an improved Angelov/Chalmers MESFET model which includes substrate bias effects. The 4-terminal model employs a new and simplified gate current extraction method based on a forward and reverse diode equation which can be independently modified. The improved model is applied to a silicon metal-semiconductor-field-effect-transistor (MESFET) that was fabricated using a 45nm SOI CMOS process and designed for RF power amplifier applications. The model fits across DC and RF parameters and also shows a good fit to a 2.5GHz load pull measurement used for verification.

RTU2D-4 11:10 Behavioral Modeling for Fast Characterization and Design Optimization of Doherty Power Amplifiers

Abdellah Nabil¹, Frédéric Fernez¹, Edouard Ngoya²; ¹Freescale Semiconductor, France, ²XLIM, France

Abstract: As the complexity of modern RF front-end systems grows, the need for accurate models that allow effective emulation of the amplifying unit has become a key issue in analyzing, optimizing and designing high efficiency power amplifiers. These models must accurately predict both high and low frequency memory effects to fully characterize the device under test. In this context, a state-of-the-art behavioral modeling approach based on Volterra series is experimented onto an industry standard Doherty power amplifier, and validated successfully by comparing with circuit level simulations.

Tuesday, 19 May 2015 13:30–16:00 Room Hall 6 Session RTUIF: Interactive Forum

Chair: Luciano Boglione, Naval Research Laboratory Co-Chair: Freek van Straten, NXP Semiconductors

RTUIF-1 13:30 A Wideband Envelope-Tracking CMOS Linear Transmitter Without Digital Predistortion

Jung-Lin Woo, Sunghwan Park, Youngwoo Kwon; Seoul National University, Korea

Abstract: In this work, an effective linearization technique to linearize both AM-PM and AM-AM distortions in CMOS envelope tracking (ET) transmitter is developed using dual shaping tables. AM-AM response is linearized using iso-gain shaping table. A variable phase shifter is integrated with the RF power amplifier (RF PA), which linearizes AM-PM response of CMOS ET PA in conjunction with the iso-gain shaping table. In this way, no additional digital predistortion (DPD) is required to linearize the CMOS ET PA. The 2-stage RF PA with the integrated phase compensation circuit is fabricated in 0.28- μ m SOI CMOS process. The ET transmitter system demonstrated using the CMOS envelope amplifier (EA) shows an overall system PAE of 42.2% with -34.5 dBc E-UTRA ACLR with 40 MHz BW LTE signal centered at 0.837 GHz. The proposed method overcomes the bandwidth limitation of the conventional methods relying on DPD and/or feedback loops, and can be applied to wide bandwidth LTE signals.

RTUIF-2 13:30

Design Methodology for Controlled-Q Resonators in OTA-Based Filters

Saeed Ghamari, Gabriele Tasselli, Cyril Botteron, Pierre-André Farine; EPFL, Switzerland

Abstract: This paper presents a design methodology for high quality factor resonators based on operational transconductance amplifier (OTA) employed in active filters. The quality factor of a resonator, as its main specification, is translated to the requirements of the OTA. Moreover, the effects of the OTA's finite output resistance and internal poles are investigated. The results provide a useful chart and a simple methodology to design a resonator with a desired quality factor. The design methodology has been validated by fabricating a resonator with 8 MHz resonance frequency and a quality factor of around 10 using UMC 180-nm CMOS technology.

RTUIF-3 13:30

C-Band Bidirectional Amplifier with Switchable Matching Circuits

Doojung Kim, Byung-Wook Min; Yonsei University, Korea

Abstract: This paper presents a CMOS bidirectional amplifier for time division duplexing systems. By switching supply and ground voltages of a common gate amplifier, the bias current and amplification direction can be switched between forward and backward modes. Depending on the amplification direction, CMOS switches parallel with matching inductors perform switchable matching circuits. The source and drain voltages of CMOS switches are switched by the bias direction, and the CMOS

switches can be automatically turned on and off with a fixed gate voltage. The measured peak gain is 9.8 dB at 7.4 GHz with input and output return losses lower than -6.4 dB. The measured output 1-dB power compression point and average noise figure are 4.2 dBm and 7.7 dB including probe loss, respectively. The designed circuit and layout are directional input-output symmetric, and therefore the amplification characteristics of the forward and backward modes are identical. The measured insertion phase difference between forward and backward modes is <6°. The chip measures 470×544 μm^2 without pads.

RTUIF-4 13:30

An Impedance Sensor for MEMS Adaptive Antenna Matching

Armin Tavakol, Robert Bogdan Staszewski; Technische Universiteit Delft, The Netherlands

Abstract: We propose a new calibration mechanism for passive adaptive cellular antenna matching network containing MEMS-based tunable devices. To avoid expensive and bulky couplers and reference circuitry, the tuner contains voltage and current sensors inserted before the antenna matching network. The sensed complex impedance generates 2-bit update controls for the tuning algorithm, which drives the MEMS-based tunable devices. The impedance sensing IC is designed to operate in the frequency range of 1.7–2.7 GHz and the clock frequency is 50 kHz.

RTUIF-5 13:30

An Active Interference Canceler with Reduced Harmonic Response and Synthesizer Tuning Range

Wei-Gi Ho, Vineet Singh, Travis Forbes, Ranjit Gharpurey; University of Texas at Austin, USA **Abstract:** A feedback-based active interference cancellation technique for reducing interference in a broadband LNA is described. The interference is down-converted to baseband, low-pass filtered, then up-converted and subtracted from the input. Harmonic response in the active canceler is eliminated by using harmonic rejection mixers (HRMs). Furthermore, by configuring the HRMs to provide frequency translation while using the LO fundamental or its harmonics, the span required of the frequency synthesizer for driving the HRMs is reduced. Implemented in a 65 nm process, the proposed technique shows 8–13 dB improvement in blocker 1-dB compression.

RTUIF-6 13:30

A 265mW, 225MHz Signal Bandwidth, and <1-dB Gain Step Software Defined Cable Receiver Front-End Enabling Ultra-HDTV in 28nm CMOS

Silvian Spiridon¹, Davide Guermandi², Stefano Bozzola³, Han Yan³, Mattia Introini³, Dongsoo Koh¹; ¹Broadcom, USA, ²imec, Belgium, ³Broadcom, The Netherlands

Abstract: A 28 nm CMOS software-defined receiver front end (SDRX) for the analog signal conditioning of high-speed data streams on cable is presented. By making efficient use of the available cable bandwidth, the presented SDRX is, to the authors' knowledge, the first reported receiver front end to enable high-speed data and Ultra-HDTV video streaming within home cable networks. This paper focuses on the SDRX system-level design methodology as the key factor in finding the most effective circuit-level solutions for power and area optimization. Its direct result is that we have implemented the most power-efficient SDRX architecture for the 28 nm CMOS process, and we have developed enhanced building blocks to optimize further the system performance. The optimal

filtering strategy defines the harmonic rejection feature to reduce the external filter complexity and cost, and it also finds the appropriate ADC resolution and speed to reduce the baseband low-pass filter power and area. The SDRX gain partitioning strategy maximizes the output SNR by making sure both the mixer and baseband ADCs are fully loaded. Thus, enhanced gain blocks have been designed to accommodate a < 1 dB gain step. The presented monolithic SDRX is embedded in 28 nm CMOS multimedia SoCs, and it can cover frequency bands up to 1800 MHz and channel bandwidths up to 225 MHz. The success of the top-down design approach is validated by the 265/180 mW power consumption for 225/100 MHz signal bandwidth.

RTUIF-7 13:30 A 17.8dBm 110–130GHz Power Amplifier and Doubler Chain in SiGe BiCMOS Technology

Roee Ben Yishay, Danny Elad; IBM, Israel

Abstract: A D-Band $\times 2$ frequency multiplier-amplifier chain implemented in a $f_{T}/f_{MAX} = 250/330$ GHz 0.12 μ m SiGe BiCMOS technology is presented. The chain achieves a peak output power of 17.8 dBm at 115 GHz and consists of input balun and push-push frequency doubler which drives a balanced three stages Power Amplifier (PA). It operates from 110 GHz to 130 GHz (3 dB power bandwidth) with -2 dBm input power at V-Band and consumes a total DC power of 600 mW. The PA achieves output 1 dB compression point and saturated power of 13.5 and 17.6 dBm, respectively, at 120 GHz and peak small signal gain of 32 dB.

RTUIF-8 13:30

A Robust Low Phase Noise Ku Band VCO with 23.3% Tuning Range for E-Band and V-Band Backhaul Transceivers

Run Levinger, Oded Katz, Jakob Vovnoboy, Roee Ben Yishay, Roi Carmon, Benny Shienman, Nadav Mazor, Danny Elad; IBM, Israel

Abstract: This paper presents a K_u band G_m boosted Colpitts VCO designed in IBM 0.13µm SiGe BiCMOS8hp technology for E-Band and V-band backhaul transceivers. The VCO achieves 23.3% tuning range, covering 15.2–19.2 GHz while maintaining low phase noise. Measured phase noise at 10 MHz is lower than -133 dBc/Hz at 25°C. The VCO shows robust behaviour to temperature variations, with a measured frequency drift of less than 15 ppm/°C. The power consumption is 51.4mW and calculated FOM is -183.5 dBc/Hz.

RTUIF-9 13:30

A 0.68V 0.68mW 2.4GHz PLL for Ultra-Low Power RF Systems

Arun Paidimarri, Nathan Ickes, Anantha P. Chandrakasan; MIT, USA

Abstract: A 2.4GHz PLL consuming 0.68mW has been implemented in 65nm LPCMOS for use in ultra-low power Bluetooth Low Energy (BLE) applications. VCO, charge pump and dynamic flip-flop design optimization allow low voltage operation at 0.68V, bringing down dynamic power. The integer-N PLL covers all BLE channels and has a phase noise of -110dBc/Hz at 1MHz offset. To extend operation to extremely low duty cycles, extensive power gating is applied to bring the leakage power down to 170pW.

RTUIF-10 13:30

20-GHz PLL-Based Configurable Frequency Generator in 180nm SiGe-on-SOI BiCMOS

Joseph D. Cali, Curtis M. Grens, Steven E. Turner, Douglas S. Jansen, Lawrence J. Kushner; BAE Systems, USA

Abstract: This paper presents a configurable frequency generator (CFG) capable of synthesizing frequencies between 10 MHz and 20 GHz with superior far-out phase noise of less than -150 dBc/Hz at 100 MHz offset when synthesizing >10 GHz, reference spurs less than -70 dBc, settling times of less 3 μ s, and support for multiple reference frequencies through the use of a programmable bandwidth on-chip loop filter. The CFG is implemented in a 180nm SiGe-on-SOI BiCMOS process that enables high-frequency oscillation in the voltage-controlled oscillator (VCO), low parasitic switches for programmable passives, low phase noise HBTs, and excellent isolation between components sharing the same substrate.

RTUIF-11 13:30

Power Supply Bypass Capacitors – Myths and Realities

William B. Kuhn, Andrew D. Fund; Kansas State University, USA

Abstract: Power supply bypass capacitors are critical to the operation of high-frequency analog and digital circuits, yet are seldom considered in the depth they deserve. This paper investigates their use and the resulting power integrity effects as seen from an RFIC bondpad looking out to a host PCB. We show how designs can be either successful or unsuccessful depending on the capacitor values selected and the frequencies involved. In particular, the common practice of placing two or three graduated-size capacitors in an attempt to create a broadband AC ground may actually be counterproductive and potentially damaging to circuit operation. The associated problem of placing partial bypassing on-chip with larger bypass capacitors off-chip is also studied and guidance for avoiding hidden dangers is given.

RTUIF-12 13:30

Comprehensive ESD Co-Design with High-Speed and High-Frequency ICs in 28nm CMOS: Characterization, Behavioral Modeling, Extraction and Circuit Evaluation

Fei Lu, Zongyu Dong, Li Wang, Rui Ma, Chen Zhang, Hui Zhao, Albert Wang; University of California at Riverside, USA

Abstract: This paper reports a comprehensive electrostatic discharge (ESD) protection circuit co-design and analysis approach for high-frequency and high-speed ICs. Implemented in a 28nm CMOS, the ESD co-design flow includes ESD device optimization and characterization, ESD behavioral modeling, parasitic ESD parameter extraction and ESD circuit evaluation for up to 40Gbps I/O circuits. This practical ESD co-design technique can be applied to high-performance, high-frequency and high-speed ICs.

RTUIF-13 13:30

Design of ESD Protection for Large Signal Swing RF Inputs Operating to 24GHz in $0.18\mu m$ SiGe BiCMOS Process

Srivatsan Parthasarathy, Rodrigo Carrillo-Ramirez, Javier Salcedo, J.-J. Hajjar, Analog Devices, USA **Abstract:** The performance degradation resulting from the addition of ESD protection devices to very high speed Analog/RF designs is the main reason for low ESD robustness in these applications. This paper introduces an ESD methodology that combines device development and characterization as well as simulation, for high speed Analog/RF products. In this work a special ground referenced ESD network is introduced for protecting RF ports with asymmetrical signal swings in the range of +3.5V/-3.5V operating from 6-24GHz.

RTUIF-14 13:30

High-Performance 81–86GHz Transceiver Chipset for Point-to-Point Communication in SiGe BiCMOS Technology

Roee Ben Yishay, Oded Katz, Benny Sheinman, Roi Carmon, Run Levinger, Nadav Mazor, Danny Elad; IBM, Israel

Abstract: Fully integrated chipset at E-band frequencies in a superheterodyne architecture covering the 81–86 GHz band was designed and fabricated in 0.13 μ m SiGe technology. The receiver chip includes an image-reject low-noise amplifier (LNA), RF-to-IF mixer, variable gain IF amplifier, quadrature IF-to-baseband de-modulators, tunable baseband filter, phase-locked loop (PLL), and frequency multiplier by four (quadrupler). The receiver chip achieves maximum gain of 73 dB, 6 dB noise figure, better than -12 dBm IIP3, with more than 65 dB dynamic range, and consumes 600 mW. The transmitter chip includes a power amplifier (PA), image-reject driver, variable RF attenuators, IF-to-RF up-converting mixer, variable gain IF amplifier, quadrature baseband-to-IF modulator, PLL, and frequency quadrupler. It achieves output power at P1dB of 16.6 dBm, P_{sat} of 18.8 dBm on a single-ended output and consumes 1.8 W.

RTUIF-15 13:30

A 15-mW 7-GHz Inductorless Transimpedance Amplifier and a 1-THz+ GBP Limiting Amplifier for 10GbE Optical Receivers

Sagar Ray, Mona M. Hella; Rensselaer Polytechnic Institute, USA

Abstract: An inductorless 10 Gb/s optical receiver including a novel transimpedance amplifier (TIA) with dual feedback loop and a limiting amplifier (LA) with third-order nested feedback is presented. The current-buffer based TIA employs an active Cherry-Hooper (CH) stage in the auxiliary amplifier and reuses the tail current source to achieve 10 Gbps operation in the presence of a 1pF photodiode input capacitance. The use of nested feedback in the four stage limiting amplifier enables a gainbandwidth-product (GBP)>1THz without the use of area-consuming inductors. Implemented in IBM 130nm CMOS technology, the optical receiver achieves a BER<10⁻¹² at 10 Gbps for an input current of 30 μ A, delivering 600 mV p-p at the output of the 50 Ω buffer. Optical testing confirmed a -13.8 dBm sensitivity for a data rate of 7.5 Gbps, mainly limited by the 850nm source used for measurement. The receiver dissipates 108mW from a 1.2V supply, while occupying a core area of only 0.08 mm².

RFIC 2015 Panel Sessions

Monday, 18 May 2015 12:00–13:15 PCC 122ABC

Research is Expensive, but Innovation Sells!

Panel Orga	nizers and Moderators:
0	Stefano Pellerano, Intel, USA
	Brian Floyd, North Carolina State University, USA
Panelists:	Robert Gilmore, Director, Engineering, Qualcomm, USA
	Farooq Khan, President, Samsung R&D America, USA
	Aarno Parssinen, Research Director, University of Oulu, Finland
	Bernard Tenbroek, Director, RF IC Design, MediaTek, UK
	Wim Van Thillo, Program Director, Perceptive Systems, imec, Belgium
	Wen-Hann Wang, VP & Managing Director, Intel Labs, Intel, USA

Abstract: Technology is evolving at an amazingly fast pace. A key differentiator in commoditized markets is innovation. Users expect to pay less for the same functionality, but they might be willing to pay the same or more if their experience is enriched. Commercializing innovation, however, is: certainly not an easy task. This panel will discuss the intricacies of how to successfully (or not!) conduct research in the industry and answer some of the following questions. What is the right balance between blue-sky research and product development? How should profit from previous product cycles best be used to fuel research activity and survive commoditization? What role should university investment play in this process? Should the path from idea to product be laid by the same team or by different teams with a handoff along the way? Directors and VPs from some of the most prestigious research laboratories in the industry and academia will share their views and opinions on how to successfully drive innovation into products that may enrich the life of every one of us.

RFIC 2015 Panel Sessions

Tuesday, 19 May 2015 12:00–13:15 PCC 129AB

The Internet of Things (IoT) – What's All the Hype?

Panel Organizers and Moderators:

Oren Eliezer, EverSet Technologies & TallannQuest, USA Hossein Hashemi, University of Southern California, USA

 Panelists: Gangadhar Burra, Senior Director of Technology, Qualcomm, USA Baher Haroun, Director, Embedded Processing Systems Labs, TI, USA Larry Larson, Dean of Engineering, Brown University, USA Ravi Subramanian, GM, Analog/RF/Mixed-Signal, Mentor Graphics, USA Gang Gary Xu, Director, Samsung R&D America, USA Conan Zhan, Deputy Director, RF Division, MediaTek, Taiwan

Abstract: The "Internet of Things" (IoT) is already here, with sophisticated lighting and irrigation systems, thermostats, doorbells, and many other devices being connected and controlled via the internet. Many billions of such IoT devices will rely on wireless technologies, which is great for us RF engineers! Where is this going? What technologies and products can we expect to see going forward? What standards will prevail? Who will be the big players in this market? What research opportunities does this create for industry and academia? Our distinguished panelists from industry and academia will debate all these and respond to the audience's questions in this informative and entertaining lunchtime panel.

WORKSHOPS AND SHORT COURSES

Workshops and Short Courses are offered on Sunday, Monday and Friday of Microwave Week. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 17 MAY 2015

WSA (Full Day): Sunday 08:00–17:00, 121AB RF Interference Mitigation Techniques

Sponsors: RFIC

Organizers: Ranjit Gharpurey, University of Texas at Austin, USA Jacques C. Rudell, University of Washington, USA

Abstract: This full-day workshop will consist of speakers that address a wide range of problems related to transceiver interference management and suppression. Topics will include general techniques to improve receiver selectivity and reduce transmitter unwanted spurious spectrum. Speakers will come from a diverse set of backgrounds which include system, circuit, and technology design all with the goal of interference mitigation either through filtering or cancellation techniques. Presentations will focus on transceiver circuit design to enhance linearity, dynamic range, improve synthesizer phase noise, and cancellation methods, all for improved selectivity performance. Other topics which address emerging areas that attempt to improve overall spectral efficiency by realizing full-duplex systems capable of simultaneous transmit and receive (STARS) on the same frequency are also discussed. In addition, some speakers will focus on new MEMs technologies to improve transceiver interference mitigation. Further presentations on system/networking strategies related to integrating radios in the context of interference mitigation will be given.

- 1. "Electrical-Balance Duplexing for RF Self-Interference Cancellation to Enable In-Band Full-Duplex", **Barend van Liempd**, *imec*, *Belgium*
- 2. "Micromechanical Filters: Fundamentals and Application to Interference Mitigation", **Roy H. Olsson III**, *DARPA*, *USA*
- 3. "Interference Rejection Exploiting Switched-R-C Techniques Compatible with CMOS", **Erik Klumperink**, *University of Twente, The Netherlands*
- 4. "Broadband Channelizer Architectures with Dynamic Range Relaxation", **Ranjit Gharpurey**, *University of Texas at Austin, USA*
- 5. "Self-Interference Cancellation for Reconfigurable Frequency-Division-Duplex/Full-Duplex/Co-Existing Radios", **Harish Krishnaswamy**, *Columbia University, USA*
- 6. "Self-Interference Cancellation", Sachin Katti, Stanford University, USA
- 7. "Interference in Near-Field Communications (NFC) Circuits for Mobile Handsets", Magnus Wiklund, *Qualcomm, USA*
- 8. "Strategies for Transmitter Self-Interference Management & Mitigation", **Chris Rudell**, *University of Washington, USA*

WSB (Full Day): Sunday 08:00–17:00, 122AB Digital and Analog Techniques for Power-Efficiency Enhancement in Wireless Transmitters

Sponsor: RFIC

Organizers: Oren Eliezer, EverSet Technologies, USA & TallannQuest, USA Ayman Fayed, Iowa State University, USA

Abstract: Transmitter power-efficiency has always represented a significant challenge in wireless devices, whether these are for battery-operated mobile devices or infrastructure applications. As the targeted bandwidths become wider and the spectral efficiencies higher, it is becoming even more challenging to develop power-efficient transmitters that meet all the requirements of the wireless systems they serve. This workshop, involving experts from industry and academia, will cover various architectures and techniques for power-efficient transmitters, including both analog and digital approaches.

- 1. "Operating Modes of Dynamic-Power-Supply Transmitter Amplifiers", **Earl McCune**, *RF Communications Consulting, USA*
- 2. "Integrated and Non-Integrated Envelope Tracking Solutions", Jerry Lopez, NFR, USA
- "Design Challenges of Envelope Tracking and Polar Architectures as Supply Modulation Based Techniques", Jennifer Kitchen, Bertan Bakkaloglu, Arizona State University, USA
- 4. "Outphasing Techniques for High-PAPR Signals", **Taylor Barton**, *University of Texas at Dallas, USA*
- 5. "Power Supply Noise Mitigation Techniques for RF PAs", **Ayman Fayed**, *Iowa State University, USA*
- 6. "A Fully Integrated High-Efficiency Digital Transmitter Based on PWM and Class-D PA", Lei Ding, Rahmi Hezar, *Texas Instruments, USA*
- 7. "Linearizing Power Amplifiers with Class-G Analog Voltage-Supply Modulators", **Jeffery Walling**, *University of Utab*, *USA*
- "Digital Approaches for Power Efficiency Enhancement in Transmitters", Oren Eliezer^{1,2}, Sankalp Modi³, ¹EverSet Technologies, USA, ²TallannQuest, USA, ³University of Texas at Dallas, USA

WSC (Full Day): Sunday 08:00–17:00, 125 Highly Efficient RF Frequency Generation in Nanometer CMOS Technologies

Sponsor: RFIC

Organizers: Salvatore Levantino, Politecnico di Milano, Italy Stefano Pellerano, Intel, USA

Abstract: The energy efficiency of RF frequency synthesizers is essential in high-performance mobile radios that pose stringent phase-noise requirements, as well as in emerging wireless applications that feature extremely low power budgets (sensors, wearables, internet of things). Unfortunately, improving spectral purity in conventional phase-locked loops is obtained at the price of higher power consumption. This workshop will discuss the most relevant directions that have been investigated in recent years to break this trade-off by both circuit design and architectural innovations. The workshop will begin by reviewing the fundamental limitations of the phase-noiseversus-power trade-off in oscillators and the recent advances in the design of highly efficient LC oscillators. Then, it will move to discuss the main architectural innovations relaxing the noise-power trade-off in fractional-N PLLs: (i) adaptive phase-noise cancellation, (ii) nested-and-cascaded architectures, (iii) sub-sampling, (iv) injection-locking PLLs. As CMOS technologies scale down, traditional analog PLLs are also moving towards mostly digital designs, which are demonstrating better efficiency and scalability, and even towards fully digital designs, achieved via automatic synthesis-and-layout flow. In the second half of the workshop, the most recent realizations of analog, hybrid and digital frequency synthesizers will be critically compared from the efficiency and the scalability points of view.

- 1. "Fundamental Limitations in LC Oscillators Noise-Power Efficiency", **Danilo Manstretta**, *University of Pavia, Italy*
- 2. "Fully Integrated Phase Noise Extraction and Cancellation Techniques for Ring Oscillator Based Fractional-N PLLs", **Bertan Bakkaloglu**, *Arizona State University, USA*
- 3. "Low-Noise High-OSR Sigma-Delta Fractional-N Frequency Synthesis", **SeongHwan Cho**, *KAIST, Korea*
- 4. "High-Performance Fractional-N Frequency Synthesizers with Large Divided Ratios", **Tai-Cheng Lee**, *National Taiwan University, Taiwan*
- 5. "Synthesizable Digital PLL Using Injection-Lock Architecture", **Kenichi Okada**, *Tokyo Institute of Technology, Japan*
- 6. "Ring-Based RF Digital Frequency Synthesizers", Amr Elshazly, Intel, USA
- 7. "Toward Area Efficient Analog Synthesizer in Wireless Transceivers", **Jing-Hong Conan Zhan**, *MediaTek, Taiwan*
- 8. "The Best of Both Worlds: Combining Digital and Analog Techniques in High Performance PLLs", **Mark Ferriss**, *IBM, USA*
- 9. "Ultra-High Speed Direct Digital Frequency Synthesis", **Foster Dai**, *Auburn University*, USA

WSD (Half Day): Sunday 08:00–12:00, 126 Multi-Gbps Wireline Transceivers: Inching Closer to RF/mm-Wave IC Domain

Sponsor: RFIC

Organizers: Hiva Hedayati, Xilinx, USA Mona Hella, Rensselaer Polytechnic Institute, USA Burak Catli, Broadcom, USA

Abstract: High Performance Computing (HPC) installations and exaFLOP supercomputing require high bandwidth chip-to-chip and system-to-system communication links. One critical block in such systems is the Serializer/Deserializer (SerDes) which formats and transfers data over either electrical or optical links. Moving data transfer rates beyond 32Gb/s and 64Gb/s clearly places some of the SerDes design challenges into the RF/Microwave domain. The high data rate coupled to the limits on the transfer medium, require relatively complex modulation techniques. The cost and power consumption have also become more pronounceable, particularly with super data centers employing several thousand of such transceivers. A number of high speed circuit techniques are employed to meet the evolving transceiver design requirements; including ADC/DAC based architectures, and complex digital calibration techniques. This workshop presents an overview of recent advances and ongoing research in Multi-Gbp/s serial links from industry and academia as it relates to the world of RF/ Microwaves. The workshop will cover wideband microwave clock generation schemes, clock and data recovery circuits along with various equalization techniques. In addition 30+GS/s ADC architectures for 60+Gb/s wireline receiver applications will be discussed. We will also explore low-power circuit implementations.

- 1. "Design Techniques for Scalable, Sub-pJ/b Serial I/O Transceivers", **Samuel Palermo**, *Texas A&M University, USA*
- 2. "Design Techniques for 25G+ Analog & Digital I/O Implementations", **Thomas Toifl**, *IBM, Switzerland*
- 3. "ADC-Based Receivers and Their Challenges Beyond 40Gb/s", Ali Sheikholeslami, *University of Toronto, Canada*
- 4. "Transceivers for 40Gbps and 100Gbps Wireline Connections", **Jun Cao**, *Broadcom*, USA
- 5. "A 40nm Mixed NRZ/Multi-Tone Serial Data Transceiver for Multi-Drop Memory Interfaces", **Yusuf Leblebici**, *EPFL*, *Switzerland*

WSE (Full Day): Sunday 08:00–17:00, 127 Mixed-Signal Power Amplifiers and RF-DACs

Sponsors: RFIC

Organizers: Hua Wang, Georgia Institute of Technology, USA R. Bogdan Staszewski, University College Dublin, Ireland Renaldi Winoto, Marvell Semiconductor, USA

Abstract: The growing demand for a higher data-rate and longer battery life poses stringent requirements on the power amplifiers (PAs) in mobile handset transceivers. Silicon-based PAs, e.g., in CMOS or SiGe HBT processes, have recently emerged as competitive solutions for many applications. Besides low-cost and high integration, silicon-platforms offer unparalleled signal processing/ computation capabilities, which can be exploited for PA performance enhancement with low overhead. RF-DAC is one perfect example of this new PA paradigm-shift. It merges digital operation/ processing with RF PA operation. Other analog/mixed-signal techniques can be leveraged to achieve efficiency/linearity enhancement, performance self-healing, and antenna load compensation, etc. As a result, advanced silicon PA has expanded from a standalone RF building block to a complex mixed-signal/mixed-mode system with orchestrated collaboration among analog, digital, and large-signal RF operations. This workshop reviews this recent wave of innovations on "Mixed-Signal PAs and RF-DACs" and brings the state-of-the-art technologies to the attendees.

- "Next Generation Base Station Transmitters / RF DACs", L. de Vreede¹, S. M. Alavi^{2,1}, R. Bogdan Staszewski^{3,1}, ¹Delft University of Technology, The Netherlands, ²DitIQ, The Netherlands, ³University College Dublin, Ireland
- 2. "Leveraging RF-DACs to Enhance the Doherty PA Architectures", **Hua Wang**, *Georgia Institute of Technology, USA*
- 3. "Class-G PAs: From Analog to Digital Implementations", **Jeff Walling**, *University of Utab, USA*
- 4. "Polar Antenna Impedance Detection in a CMOS Power Amplifier and Impedance Tuning with an SOI Switch Based Impedance Tuner", **Shouhei Kousai**, *Toshiba, Japan*
- 5. "Self-Healing for mm-Wave Power Amplifiers", **Steven Bowers**, *University of Virginia*, *USA*
- 6. "Holistic Design Approach for Millimeter-Wave Digitally-Assisted Power Amplifiers (DAPA) on CMOS and GaN", **Tim LaRocca**, *Northrop Grumman*, *USA*
- 7. "Switched-Mode Power Amplifiers and RF DAC's", **R. Bogdan Staszewski**^{1,2}, ¹University College Dublin, Ireland, ²Delft University of Technology, The Netherlands
- "Digital Transmitters and RF-DACs for CMOS Transceiver SoCs with Self-Compensation/ Predistortion", Oren Eliezer^{1,2}, 'EverSet Technologies, USA, ²TallannQuest, USA

WSF (Full Day): Sunday 08:00–17:00, 128 Next Generation 77–81GHz Automotive Radars

Sponsors: RFIC, IMS

Organizers: Gabriel M. Rebeiz, University of California at San Diego, USA Juergen Hasch, Robert Bosch, Germany

Abstract: Automotive radars at 77 GHz are being shipped at more than 1 million units per year for long-range radars (LRR) and medium range radars (MRR) with applications in automatic cruise control (ACC), collision avoidance, and in imaging/tracking radars for autonomous driving. Radar topologies include lens-based systems, digital beamforming and RF-beamforming systems. Millimeter-wave radars are essential for autonomous driving, and new systems with wider bandwidths, better tracking and imaging software, and better scanning techniques are being developed to meet this need. This workshop assembles a mix of industry and universities to present the latest techniques in automotive radars, both from the systems/application perspective and from the mm-wave electronics and hardware perspective (antennas, packaging, etc.). The workshop will have a mix of users (Daimler Benz, Toyota), chip/electronic developers (Freescale, Infineon), and Universities, and promises to be comprehensive with a wide but in-depth view of this area.

- 1. "Active Sensing in Intelligent Transportation", Stephen H. Bayless, ITS America, USA
- 2. "High-Resolution Phased-Array Automotive Radars", **Jae Lee**, *Toyota Technical Center, USA*
- 3. "Automotive Radar Technology Trends", Juergen Dickman, Robert Bosch, Germany
- 4. "Digitally Centric Modulation Schemes on a Software Defined Radar (SDR) Platform", Andreas Stelzer, Johannes Kepler University Linz, Austria
- 5. "Packaging Technology and Production Testing: Key Differentiators for Automotive Radar Front-End Products", **Sergio Pacheco**, *Freescale Semiconductor, USA*
- 6. "How Can Semiconductor Technology and MMIC Packaging Contribute to Future Success of Automotive Radar?", **Rudolf Lachner**, *Infineon, Germany*
- 7. "Antennas Concepts for Automotive Radar Sensors", **Wolfgang Menzel**, *University of Ulm, Germany*
- 8. "Towards Lower-Cost Phased Array Chips Using Built-In-Self-Test", **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
WSG (Full Day): Sunday 08:00–17:00, 129A Performance Metrics for mm-Wave Devices and Circuits from the Perspective of the International Technology Roadmap for Semiconductors (ITRS)

Sponsors: RFIC, IMS

Organizers: Herbert Bennett, NIST, USA Pete Zampardi, RF Micro Devices, USA

Abstract: This workshop will focus on de-mystifying the process and results of the International Technology Roadmap for Semiconductors (ITRS) RF and Analog/Mixed-Signal (RF and AMS) Technologies Working Group and will discuss in more detail the Group's mm-wave device technology and circuit roadmapping activities. Device, circuit, and technology performance simulation, scaling, and experimental characterization metrics and techniques will be addressed in detail for the most advanced CMOS, SiGe BiCMOS, III-V HBT and III-V HEMT technologies. Intrinsic device structures as well as layout parasitics will be addressed as potential show stoppers to future scaling. The everincreasing gap between the intrinsic high frequency performance metrics of CMOS transistors and that of fully wired MOSFETs, not seen in other device types, will be explained.

- 1. "Roadmaps and Standards for RF and Analog/Mixed-Signal Technologies: International Roadmap for Semiconductors Perspectives", **Herbert Bennett**, *NIST, USA*
- "Ultimate Physical Limits of SiGeC HBTs and Technology Roadmap", Michael Schroter^{1,2}, 'Technical University Dresden, Germany, ²University of California at San Diego, USA
- 3. "III-V HBT and (MOS) HEMT Scaling", **Mark Rodwell**, *University of California at Santa Barbara, USA*
- 4. "RF and mm-Wave: The Nano-CMOS Perspective", Kenneth Yau, Broadcom, USA
- 5. "55nm SiGe BiCMOS Technology and Beyond. How Aggressively can the CMOS be Scaled?", **Pascal Chevalier**, *STMicroelectronics, France*
- 6. "mmWave RFCMOS Technology and Applications", David Harame, IBM, USA
- 7. "Beyond the Transistor. FET, HBT and FET-HBT mm-Wave Circuit Benchmarking and Scaling", **Sorin P. Voinigescu**, *University of Toronto, Canada*

WSH (Full Day): Sunday 08:00–17:00, 129B Nanopackaging: Multifunctional Nanomaterials and Devices Towards 3D System Miniaturization

Sponsor: RFIC, IMS

Organizers: Dominique Baillargeat, Université de Limoges, France Fabio Coccetti, Université de Toulouse, France

Abstract: Future nanoelectronics technology will face many challenges to match Moore and more than Moore Predictions. Going to nanometric dimensions is not only to apply a simple scale factor to current components, but also to overcome some limits due to 1) physical phenomena (quantum effects, property degradations of conventional materials such as Cu interconnect, ultralow k dielectric, high k dielectric, lead-free material,...), 2) technological capabilities, 3) packaging and assembly of circuits and system. Interconnecting, cooling, powering and protecting (nano) components are becoming major bottlenecks. Consequently, nanopackaging will play a crucial role for enabling future nanoelectronics to be consistent with future components, system and circuit board (or global level) requirements. Moreover, assembly approaches are moving toward three-dimensional integrated circuits (3D ICs) with through silicon via (TSV), wafer-thinning and bonding technologies, electro/optical integration, and 3D system integration and miniaturization. Many of these packaging and assembly requirements are triggering an unprecedented pace of innovation in terms of new technologies, new system integration techniques and new materials. For the latters, intensive research investigations are focused on carbon nano-tubes, graphen, 2D materials, nanowires, nanoparticles and macromolecules.

- "Carbon Based 3D Interconnect Technology", Johan Liu^{1,2}, Yifeng Fu³, Di Jiang¹, Shuangxi Sun¹, Jie Bao², Ning Wang², ¹Chalmers University of Technology, Sweden, ²Shanghai University, China, ³SHT Smart High Tech, Sweden
- 2. "Micro-Nano Interposer for Molecular Electronics and 3D Integrated Circuits", P. Reynaud, A. Thuaire, X. Baillin, S. Cheramy, G. Poupon, *CEA-LETI, France*
- "High Frequency Models for Multilayer Graphene Interconnects", V. Kumar¹, Shaloo Rakheja², Azad Naeemi¹, ¹Georgia Institute of Technology, USA, ²MIT, USA
- 4. "RF Nano Electromechanical Systems Based on Vertically Aligned Carbon Nanotubes", A. Ziaei, S. Xavier, *Thales RGT, France*
- "Nanopackaging: Multifunctional Nanomaterials and Devices Towards 3D System Miniaturization", D. Baillargeat¹, S Bila¹, P Coquet², BK Tay^{2,3}, ¹Université de Limoges, France, ²CINTRA UMI 3288 CNRS/NTU/Thales, Singapore, ³SEEE NTU, Singapore
- "Advanced Numerical Tools for the Multiscale-Multiphyiscs Modelling of Carbon-Based Interconnections", L. Pierantoni1¹, D. Mencarelli¹, F. Coccetti², ¹Università Politecnica delle Marche, Italy, ²LAAS-CNRS, France

WSI (Full Day): Sunday 08:00–17:00, 130 mmWave to THz, Which Applications with Which Technology

Sponsor: RFIC, IMS

Organizers: Didier Belot, CEA-LETI, France Pierre Busson, STMicroelectronics, France

Abstract: Millimeter Waves applications are becoming more and more used for civil markets in the infrastructures, automotive, mobile devices connectivity, and imaging domains while THz applications remain manly in the military domain, even if we can notice tentative for civil security and health imaging domain. The Workshop is organized in three levels of complexity: in a first time in order to target applications mentioned above, process technologies has to be defined, and we will have presentations covering SiGe and III-V processes; then we will address modeling issues for millimeter waves and THz frequencies, before having an overview on different design techniques in SiGe and III-V processes addressing mmW and THz applications. At the end of the day, we will have an open door on industrial systems and applications opportunities in Telecommunications infrastructures, mobile devices and connectivity.

Speakers:

- 1. "SiGe Technologies for mmW and THz Applications", **Pascal Chevalier**, *STMicroelectronics, France*
- 2. "III-V Technologies for mmW and THz Applications", **Mohamed Zaknoune**, *IEMN*, *France*
- 3. "RF Front-Ends for mm-Wave and THz Application in SiGe/CMOS", Ulrich Pfeiffer, University of Wuppertal, Germany
- "Multifunctional Circuits and Modules Based on III/V mHEMT Technology for (Sub-) Millimeter-Wave Applications in Space, Communication and Sensing", Michael Schlechtweg, Fraunhofer IAF, Germany
- 5. "Towards the Integration of Millimeter Wave Access Points in Future 5G HetNet: Stakes, Challenges, and Enabling Technologies", **Cedric Dehos**, *CEA-LETI, France*
- 6. "Enabling Backhaul and Access with mmWave Modular Antenna Array", *Ali Sadri, Intel, USA*
- 7. "SiGe mmW and THz Applications", Ali Hajimiri, CalTech, USA
- 8. "Coherent Sub-THz Transmission Systems in Silicon Technology: Design Challenges for Frequency Synthesis", **Alexandre Siligaris**, *CEA-LETI, France*

WSJ (Full Day): Sunday 08:00–17:00, 131AB Modern Radar Systems for High Resolution Ranging, Indoor Localization, and Vital Signs Detection

WSK (Full Day): Sunday 08:00–17:00, 131C RF System Miniaturization with Integrated-Passive-Device (IPD), Through-Silicon-Via (TSV), and System-in-Package (SiP) Technologies

Sponsor: IMS

WSL (Full Day): Sunday 08:00–17:00, 132A Wearable Electronics

Sponsor: IMS

WSM (Hlaf Day): Sunday 08:00–17:00, TBD Current Trends in GaN PA Packaging

Sponsor: IMS

WSN (Full Day): Sunday 08:00–17:00, 132B Technologies for Tunable and Reconfigurable RF/Microwave Filters

Sponsor: RFIC, IMS

Organizers: Domine Leenaerts, NXP Semiconductors, The Netherlands Mohyee Mikhemar, Broadcom, USA Pierre Blondy, Université de Limoges, France Xun Gong, University of Central Florida, USA

Abstract: The quest for more frequency spectrum to support the increasing demand for higher data rate communication has led to the adoption of a number of techniques such as: Multiband operation, Carrier aggregation, and MIMO, in addition to novel techniques such as in-band full-duplex communications. All these techniques impose stringent RF requirements on the antenna interface components, specially the RF Filters. As an example, the next generation multiband 4G smart phone would require about 16 duplexers for the main paths and 16 saw/BAW filters for the diversity paths to cover the cellular bands in the (700–2700)MHz range. The antenna interface also includes the inevitable RF switches and antenna tuners. All solutions today are based on fixed RF filtering. The antenna interface can be substantially simplified if a tunable RF filter with adequate performance can be practically realized. The advent of innovative switched capacitor array technologies such as stacked gate CMOS, Silicon on Sapphire, and MEMS technologies permits the development of a new generation of high linearity, low loss, and low power consumption tunable components. This workshop focuses on the area of tunable and reconfigurable RF/microwave filters by reporting recent research findings in this exciting field. This includes a large variety of novel planar/hybrid tunable circuit realizations for spectrum management and dynamic broadband filtering.

Speakers:

- 1. "The Promise and Limits of On-Chip Filtering and CMOS Wideband Receiver Design", **David Murphy**, *Broadcom*, *USA*
- 2. "Reconfigurable and Tunable Micromechanical Filter Technologies for Adaptive RF Systems", **Roy H. Olsson III**, *DARPA, USA*
- 3. "Cellular Terminal Antenna Impedance Tuners in CMOS-SOI Technology", **Henrik** Sjöland, *Lund University, Sweden*
- 4. "Tunable Filters Topologies for 0.7–3GHz Carrier-Aggregation Wireless Systems", **Gabriel M. Rebei**z, *University of California at San Diego, USA*
- 5. "Flexible RF & Spectrum Slicing", Sachin Katti, Stanford University, USA
- 6. "Linear Wideband Tunable Filters Using MEMS, SoS and GeTe Switches", **Pierre Blondy**, *Université de Limoges, France*
- 7. "Recent Advances in Single and Multi-Band Adaptive and Reconfigurable Filters", Andrew Guyette, Naval Research Laboratory, USA
- 8. "Solutions for Reconfigurable Mobile Device RF Front-Ends", Art Morris, WiSpry, USA
- 9. "Design Considerations of High-Q Tunable Filters", **Raafat R. Mansour**, *University* of Waterloo, Canada
- 10. "Micromachined Transfer Function Adaptive Filters", **Dimitrois Peroulis**, *Purdue University, USA*

WSO (Full Day): Sunday 08:00–17:00, 121C MIMO and Beamforming Techniques

Sponsor: RFIC, IMS

Organizers: James F. Buckwalter, University of California at Santa Barbara, USA Eric Klumperink, University of Twente, The Netherlands Jeyanandh Paramesh, Carnegie Mellon University, USA Huei Wang, National Taiwan University, Taiwan

Abstract: Nothing can grow exponentially forever except — perhaps — for wireless communications. To support the huge demand for gigabit-per-second data rates, much denser networks with smaller cells and millimeter-wave bands are foreseen for next generation 5G wireless systems. There is still room to define how 5G standards will evolve based on MIMO and mm-wave techniques and the new RFIC techniques that will be required. In particular, systems with multiple antennas exploiting MIMO and beamforming will likely play a big role to increase data capacity, reduce interference of RF transmitters, or suppress interference exploiting adaptive beamforming in the receiver. This workshop will bring together industry and academic experts to review the challenges of deploying 5G systems and several enabling mm-wave, RF, and mixed-signal techniques to meet 5G demands.

Speakers:

- 1. "The Best Future for Wireless: Fluid Standards", **Daniel W. Bliss**, *Arizona State University, USA*
- 2. "On the Path to Commercial mmWave Mobile Solutions", **Tom Kovarik**, *Nokia Solutions, USA*
- 3. "Filter Bank Multicarrier Techniques for Massive MIMO", **Behrouz** Farhang-Boroujeny, *University of Utah, USA*
- 4. "Interference Robust CMOS Beamforming Receivers in the Low-GHz Mobile Frequency Bands", **Bram Nauta**, *University of Twente, The Netherlands*
- 5. "Millimeter-Wave Phased-Array Systems for 5G Communications", **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
- 6. "Silicon-Based ICs and Organic Packaging/Antenna Solutions for Gb/s mmWave Communications", **Alberto Valdes-Garcia**, *IBM*, *USA*
- 7. "Wideband Millimeter-Wave Beamforming Receivers in Silicon", Jeyanandh Paramesh, *Carnegie Mellon University, USA*
- 8. "Next Generation Power Amplifier for 5G Handset Application", Bumman Kim, POSTECH, Korea
- 9. "1024-QAM MMW Transceiver for 5G Communications", **Tian-Wei Huang, Wei-Heng** Lin, Jeng-Han Tsai, Huei Wang, *National Taiwan University, Taiwan*

WSP (Half Day): Sunday 08:00–17:00, 132C Microwave Photonics for Broadband Measurement

Sponsor: IMS

SUNDAY SHORT COURSE - 17 MAY 2015

SSA (Half Day): Sunday 13:00–17:00, 132C Dynamic Power Supply Transmitter Design

Sponsor: IMS

MONDAY WORKSHOPS - 18 MAY 2015

WMA (Full Day): Monday 08:00–17:00, 127 Direct Extraction of FET Circuit Models from Microwave and Baseband Large-Signal Measurements for Model-Based Microwave Power Amplifier Design

Sponsors: ARFTG, IMS

WMB (Full Day): Monday 08:00–17:00, 128 Terahertz-Wave Wireless Communications

Sponsors: RFIC, IMS

Organizers: Ho-Jin Song, Korea University, Korea Jae-Sung Rieh, NTT, Japan

Abstract: The terahertz-waves exhibit various interesting unique properties such as the high absorption in water and the high transparency over paper, plastic, clothes, etc. as well as their correspondence to many molecular absorption lines and no harmful ionization effects on biological tissues. Because of these properties, the terahertz-waves have been attracting growing interests among scientific and engineering communities for possible adoption in various application fields such as imaging, spectroscopy, security, and so forth. Another recently emerging application that is more directly related to our daily life is the adoption of the terahertz- waves for broadband wireless communication, which exploits the much wider bandwidth available with the terahertz band compared to the traditional microwave and millimeter-wave bands. With the terahertz wireless communication systems, it is envisioned that extremely large throughputs of 100 Gbps or more will be available in the near future. The objective of this workshop is to provide a current snap shot on this exciting topic to MTT-s members by reviewing the recent progress in the terahertz wireless communications, ranging from the terahertz transceivers in various device technologies, successful demonstration of the tens of Gbps data transmission, up to the standardization activities in IEEE/ ITU-R. The workshop will also provide related discussions on the pending technical issues and future research directions in this field.

- 1. "InP-Based TMIC Development for Terahertz Wireless Communications", M. Kim, J. Jeong, S. Jeon, *Korea University, Korea*
- 2. "850GHz Wireless Link Demonstration Using InP HEMT", **William Bill Deal**, *Northrop Grumman, USA*
- 3. "Photonic Technologies for Terahertz Communications", **Tadao Nagatsuma**, *Osaka University, Japan*
- 4. "Terahertz Communications at 300GHz for KIOSK Data Downloading System", **Ho-Jin Song**, *NTT, Japan*
- 5. "240GHz Wireless Communication System Operating at up to 100Gbps", **Ingmar Kallfass**, *University of Stuttgart, Germany*
- 6. "Pushing CMOS to New Terahertz Heights", Ali M. Niknejad, University of California at Berkeley, USA
- 7. "Towards Wireless 100Gb/s for Switched-Point-to-Point Links", **Thomas Kürner**, *Technische Universität Braunschweig, Germany*
- 8. "Terahertz Band: Next Frontier for Wireless Communications", **Josep M. Jornet**, *University at Buffalo SUNY, USA*
- "Experimental Progresses on Terahertz Fronthaul for Future Mobile Systems, and Regulatory Issues Related to ITU-R", Iwao Hosako, Norihiko Sekine, Akifumi Kasamatsu, Atsusi Kanno, Tetsuya Kawanishi, Hiroyo Ogawa, NICT, Japan

WMC (Half Day): Monday 08:00–12:00, 129A Micro and Nanowatt Smart RF Transceiver ICs for Internet of Thing

Sponsors: RFIC, IMS

Organizers: Gernot Hueber, NXP Semiconductors, Austria R. Bogdan Staszewski, University College Dublin, Ireland

Abstract: Over the last years more and more application of lowest power RFICs are evolving, while at the same time advancements on technology level, as well as on design perspective enable radios for Internet-of-Things solutions. However, those impart unique challenges on the RF-transceiver design with the design goals of lowest power consumption, size and costs that are attractive for mass market applications. Scaled CMOS on the one hand features the possibility for implementing all RF and control functionality of an Internet-of-Things solution directly on a single IC, on the other hand it shows poor performance in RF circuits compared to other technologies. The focus of this workshop will be on the challenges RF transceiver design and architectures in low-power RFICs in CMOS, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration with a microcontroller in a SoC. Approaches include novel architectures, low-power analog circuit blocks, and digitally assisted and enhanced analog/RF modules.

Speakers:

- 1. "Low-Power 60-GHz CMOS Radios for Miniature Wireless Sensor Network Applications", **David Wentzloff**, *University of Michigan, USA*
- 2. "Low-Power Sub-GHz RF Transceivers for Smart-Metering", **Melina Apostolidou**, *NXP Semiconductors, The Netherlands*
- 3. "Low Power RF Generation", **R. Bogdan Staszewski**, *Delft University of Technology, The Netherlands*
- 4. "Low-Power Design Techniques for a Bluetooth Low Energy SoC", **Hiroki Sakurai**, *Toshiba, Japan*
- "Ultra-Low Power Phase-Domain RF Transceiver Design for Short-Range WPAN/IoT Standards", Yao-Hong Liu^{1,2}, *'imec, The Netherlands, ²Holst Centre, The Netherlands*

WMD (Full Day): Monday 08:00–17:00, 129B Emerging and Silicon Technologies for Bio-sensing from RF to Millimeter-wave Frequencies

Sponsors: RFIC, IMS

Organizers: Arnaud Pothier, XLIM, France Dietmar Kissinger, TU Berlin, Germany Mehmet Kaynak, IHP Microelectronics, Germany

Abstract: Electromagnetic fields from low to millimeter-wave frequencies are presenting lots of interests for biological and medical applications. Indeed the possibility of non-invasively investigation

on living cells at a very small scale stimulates currently a large research activities and technological developments. This workshop will consequently address the most promising current advances in microwave and millimeter-wave technologies dedicated to detection, sensing, control and analysis on micro/nano-scale bio-sample applications, focusing on all silicon integrated on a chip approaches and also on emerging technologies that address single cell characterization and detection of bio-molecules in tiny concentration.

- 1. "Silicon Based CMOS Integrated Microfluidic Platform for THz-Sensing Applications", **Mehmet Kaynak**, *IHP Microelectronics, Germany*
- 2. "CMOS Flow Cytometry Using Microwave Electric and Magnetic Measurement Techniques", **Ali M. Niknejad**, *University of California at Berkeley, USA*
- 3. "RF-Based Magnetic Sensing Platforms for Genomic and Proteomics", Ali Hajimiri, Hua Wang, Stephen Chapman, Costis Sideris, Alex Pai, *CalTech, USA*
- "Broadband RF/Microwave Complex Dielectric Spectroscopy Systems in CMOS", Kamran Entesari, Masoud Moslehi, Ahmed Helmy, Osama El-Hadidy, Sheirf Shakib, Hajir Hedayati, Samuel Palermo, *Texas A&M University, USA*
- 5. "Highly Integrated Microwave and Millimeter-Wave Analyzers for Emerging Biomedical Microsystems", **Dietmar Kissinger**, *University of Erlangen-Nuremberg, Germany*
- "Microwave Biosensors Dedicated for Label-Free Discrimination of Cancer Cells", Arnaud Pothier¹, L.Y. Zhang¹, C. Dalmay¹, A. Landoulsi¹, J. Leroy¹, P. Blondy¹, A. Lacroix², C. Mélin², F. Lalloué², S. Battu², M.O. Jauberteau², C. Bounaix Morand du Puch³, C. Lautrette³, S. Giraud³, 'XLIM-CNRS, France, ²Homéostasie Cellulaire et Pathologies, France, ³Oncomedics, France
- "Tunable Radio Frequency Interferometers for the Detection and Analysis of Molecules in Solutions", Y. Cui, C. Song, Y. He, Z. Chen, Y. Shao, D. Ye, J. Osterberg, S. Islam, Z. Wang, P. Wang, *Clemson University, USA*
- "Fast, Compact and Label-Free Microwave Detection of Single Cells", Cristiano Palego¹, Y. Ning², C.R. Multari², X. Ma², X. Cheng², J.C.M. Hwang², A. Denzi³, C. Merla³, F. Apollonio³, M. Liberti Sapienza³, 'Bangor University, UK, ²Lebigh University, USA, ³University of Rome, Italy
- "Microwave Dielectric Spectroscopy of Human Single Cells", T. Chen^{1,2}, W. Chen^{1,2}, D. Dubuc^{1,2}, K. Grenier^{1,2}, J. Fournie³, M. Poupot³, ¹LAAS-CNRS, France, ²Toulouse University, France, ³CRCT, France

WME (Full Day): Monday 08:00–17:00, 130 Emerging Systems, Methods, and Applications for Microwave and THz Imaging

Sponsors: RFIC, IMS

Organizers: Sherif S. Ahmed, Rohde & Schwarz, Germany Armin Arbabian, Stanford University, USA

Abstract: This workshop aims to introduce emerging applications and technologies in the area of microwave, mm-wave, and THz imaging. Experts will present their work on state-of-the-art systems for advanced imaging solutions in security, industrial, navigation, as well as medical domains. Our focus will be on end-to-end systems that combine new algorithms and methods with actual imaging demonstrations. The workshop will address new applications and areas of interest in light of emerging hardware capabilities, both in terms of high-frequency front-ends and arrays as well as post-processing and computation.

- 1. "Combing Active and Passive Terahertz Imaging Systems for Security", **Roger Appleby**, *InnovaSec, UK*
- 2. "THz Videocam A Passive Sub-Millimetre Wave Video Camera for Security Applications", **Torsten May, Erik Heinz**, *Leibniz Institute of Photonic Technology, Germany*
- "Imaging Radars Above 180GHz for Security and Science", K. Cooper, G. Chattopadhyay, R. Dengler, C. Jung, C. Lee, I. Mehdi, T. Reck, J. Siles, *Jet Propulsion Laboratory, USA*
- 4. "Automotive Radar Chipsets: An Overview, Requirements and Technological Challenges & Trends", **Nader Rohani**, *Freescale Semiconductor, USA*
- 5. "Millimeter-Wave Imaging for Non-Destructive Testing Application Possibilities & Challenges", **Sherif Ahmed**, *Rohde & Schwarz, Germany*
- 6. "Millimeter Wave Radar Imaging for Security and Industrial Applications", **Nils Pohl**, **Dirk Nuessler**, *Fraunhofer FHR, Germany*
- 7. "Contrast-Enhanced Microwave Breast Imaging", **Susan C. Hagness**, *University of Wisconsin-Madison, USA*
- 8. "RF-Acoustic Hybrid Imaging Techniques for Medical and Security Applications", **Amin Arbabian**, *Stanford University, USA*
- 9. "Computational and Performance Tradeoffs of Super-Resolution Techniques in FMCW Radar", **Murtaza Ali**, *Texas Instruments, USA*
- 10. "Next-Generation Information Theoretical mm-Wave Imaging Radar: Theory and Experiments", **Upamanyu Madhow, Amin Arbabian**, *University of California at Santa Barbara, USA*

WMF (Full Day): Monday 08:00–17:00, 131AB Application of Waveform Engineering in Design of High Power Doherty PAs

Sponsors: RFIC, IMS

Organizers: Justin Annes, Freescale Semiconductor, USA David Wu, Freescale Semiconductor, USA

Abstract: Since D. Snider presented the concept of waveform engineering in 1967, it has captured the imagination of power amplifier (PA) engineers. However, its use and application by researchers and practitioners in this field has been limited at best due to a number of factors, principally among them being a well-defined design methodology. The goals of this workshop are to bridge this gap and suggest a useful first order approach of applying waveform engineering in the design of high power Doherty amplifiers. Concepts covered include a review and explanation of waveform engineering concepts based on first order principles (for those attendees who are not experts in this field). Following presentations will tend toward more in-depth discussions on focused topics as it applies to high power amplification and modeling. In addition to the technical presentations, the workshop will include a laboratory simulation component where attendees will have an opportunity to explore many of the concepts using software tools in a series of instructor driven and guided mini-projects. This will enhance the interactivity of the workshop by including both presentation material coupled with "hands on" student CAD.

- "RF I-V Waveform Measurement and Engineering The Unifying Link Between Transistor Technology, Circuit Design and System Performance", Paul Tasker, Cardiff University, UK
- 2. "RFPA Design: A Personal View", S.C. Cripps, Cardiff University, UK
- 3. "Creating Models for Waveform Engineering", **Kevin Kim**, *Freescale Semiconductor*, *USA*
- 4. "Validating Models for Waveform Engineering", **Basim Noori**, *Freescale Semiconductor, USA*
- 5. "Bridging Theory and Practice When Adopting a Waveform Engineering Design Approach", **David Yu-Ting Wu**, *Freescale Semiconductor, USA*
- "Lab Tutorial 1 Designing Optimal Matching Networks for Various Modes of Operation Utilizing Waveform Engineering with a Compact Nonlinear Product Model", Justin Annes, Freescale Semiconductor, USA
- "Lab Tutorial 2 Visualizing Voltage and Current Waveforms for Optimization of Doherty PA with a Non-Linear, Compact Product Model", Rudy Gutierrez, Freescale Semiconductor, USA

	WMG (Full Day): Monday 08:00–17:00, 131C
	Antenna and Packaging Technologies for
	mmWave Frond-End Integration
Sponsors:	IMS
	WMH (Half Day): Monday 08:00-12:00 1320
	Minin (Indir Day), Monday 00.00-12.00, 152A Microwaye Backhaul: Trends and Enabling Technologies
Ch	merowave backnaar. Hends and Endbing recimologies
sponsors:	1/15
	WMI (Full Day): Monday 08:00–17:00, 132B
٨dv	ances of Microwave and Millimeter-Wave Technologies for Vehicular Communication and Safety Driving
Sponsors:	IMS
	WMJ (Half Day): Monday 13:00–17:00, 132A
	Measurement-Based Modeling in SI Applications
Sponsors:	IMS, ARFTG
	MONDAY SHORT COURSES — 18 MAY 2015
	SMA (Half Day): Monday 13:00–17:00, TBD
	Near Field Probes: Useful Tools for RF/MW Engineers
Sponsor:	IMS
	SMR (Euli Day): Monday 08:00–17:00 1320
	Theory and Design of Phase Locked Loons
Sponsor	
5001801.	
	FRIDAY WORKSHOPS – 22 MAY 2015
	WFA (Full Day): Friday 08:00–17:00, 121AB
T	/R Module Panel Architecture and Associated Technology

WFB (Full Day): Friday 08:00–17:00, 122AB Recent Advancements on Millimeter-Wave 3D Heterogeneous and Multilayer MCM Integrations

Sponsor: IMS

WFC (Full Day): Friday 08:00–17:00, 125 Non Linear RFID Systems, Characterization and Exploitations

Sponsor: IMS

WFD (Full Day): Friday 08:00–17:00, 126 Radar in a Communications-Driven Spectrum: Innovative System, Component, and Circuit Design for the Evolving Spectrum Environment

Sponsor: IMS

WFE (Half Day): Friday 08:00–12:00, 127 Thermal Management of High Power Density Electronic Assemblies

Sponsor: IMS

WFF (Full Day): Friday 08:00-17:00, 128 RF Acoustic for Mobile Communication: Challenges and Modern Solutions

Sponsor: IMS

WFG (Full Day): Friday 08:00–17:00, 129A Advances in Microwave Multiplexers and Combiners, Combiners for High Power Using Quasi-Optic, Radial, and SIW Structures

Sponsor: IMS

WFH (Full Day): Friday 08:00–17:00, 129B Wireless Power Transmission and Scavenging

WFI (Full Day): Friday 08:00–17:00, 130 EM-Based Tuning Techniques, Computer-Aided Tuning and Tuning Space Mapping

Sponsor: IMS

WFJ (Half Day): Friday 08:00–12:00, 131AB Nanosecond Pulsed Electric Fields (nsPEF) — From Modeling to Applications: Biology, Medicine, Plasma and Apparatus

Sponsor: IMS

WFK (Full Day): Friday 08:00–17:00, 131C New Technology Developments for Space

Sponsor: IMS

FRIDAY SHORT COURSES - 22 MAY 2015

SFA (Half Day): Friday 08:00–12:00, 132A A Hands-On Approach to Spectrum Regulation for Innovative Microwave Engineers

Sponsor: IMS

SFB (Half Day): Friday 08:00–12:00, 132B The Dynamics, Bifurcation, and Practical Stability Analysis/Design of Nonlinear Microwave Circuits and Networks

Sponsor: IMS

SFC (Half Day): Friday 08:00–12:00, 132C Flexible 5G mmWave Waveform Testbed and Active Device Characterization

REGISTRATION

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration. It begins Monday, 2 February 2015 and will last through Monday, 20 April 2015. Early Bird registration provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird is the 2nd tier or Advance Registration. It extends from Tuesday, 21 April 2015 through Friday, 15 May 2015, just prior to the start of Microwave Week. The 3rd and final tier is the On-site Registration, starting on Saturday, 16 May 2015, the first day of Microwave Week, and ending on Friday, 22 May 2015.

Early Bird Registration: 2 February – 20 April 2015 (through midnight Hawaii Standard Time) Advance Registration: 21 April – 15 May 2015 (through midnight Hawaii Standard Time) Onsite Registration: 16 May – 22 May 2015 (through midnight Hawaii Standard Time)

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit http://www.ieee.org/services/join or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Registration Categories

Register online: https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=188

Symposia

Microwave Week includes the IMS technical program and exhibit, as well as the RFIC Symposium (<u>http://rfic-ieee.org/</u>), ARFTG Conference (<u>http://www.arftg.org/</u>).

Select the conference(s) you wish to attend.

- **SUPERPASS** registrants can attend as many technical sessions as they can from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend **ONE** full-day workshop (or half-day workshops, to equal one full-day), the Proceedings for IMS, RFIC, ARFTG, Workshop Electronic Proceedings for all three days and admission to the exhibits. In addition, the SUPERPASS will allow you to attend the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, the Kick-Off Reception on Monday, and the Awards Banquet on Wednesday.
- **RFIC Technical Sessions** are held on Monday and Tuesday. Registration includes admission to the RFIC Plenary Session, Industry Showcase, and Reception on Sunday evening, exhibits, and the electronic proceedings.
- **IMS Technical Sessions** are held on Tuesday, Wednesday and Thursday. Registration includes admission to the exhibits, the electronic proceedings, and the Kick-Off Reception on Monday.
- **ARFTG Technical Sessions** are held on Friday. Registration includes breakfast, lunch, electronic proceedings, and admission to the ARFTG exhibition. ARFTG Conference member rates are available to both ARFTG and IEEE members.

REGISTRATION (continued)

Exhibit Only Registration

Microwave Week hosts the largest exhibition of its kind with over 550 companies. Exhibit only registration is available.

Additional Items to Add to Your Registration

1) Guest Registration

Attendees registered for the technical portion of the conference (SUPERPASS, IMS, RFIC and ARFTG) may add a Guest to their registration for an additional fee. Guest Registration includes access to the Hospitality Suite, Plenary Session, and Exhibit Hall, but does not allow access to Technical Sessions and Workshops. Select the Guest Registration tab below to add this to your registration. The name of the guest is added on the checkout page.

2) Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 20 May from 18:00–22:00 in the "Valley of the Sun Ballroom" at the Sheraton Hotel. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

3) Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

4) Two Full-Day Workshop Registration

Purchase two full-day workshops by selecting the option titled "TWO FULL-DAY WORKSHOP REGISTRATION" and receive the electronic proceedings for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop electronic proceedings are not available for individual sale.

5) Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. The workshop's printed notes may be added for a nominal fee.

Full-day workshops include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and a morning refreshment break. Afternoon workshops include a lunch and an afternoon refreshment break.

6) Short Courses

The short course fee includes access to the short course selected and any materials that the short course organizers may provide.

Full-day short courses include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning short courses include a continental breakfast, and a morning refreshment break. Afternoon short courses include a lunch and an afternoon refreshment break.

REGISTRATION (continued)

7) Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to "2015 IEEE IMS". Written requests for refunds will be honored if received by 20 April 2015. Refer to the Refund Policy for complete details.

8) Refund Policy

Written requests received by 20 April 2015 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email when requesting a refund. Address your requests to:

MTT-S Registration Nannette Jordan MP Associates 1721 Boxelder St., Ste. 107 Louisville, CO 80027, USA

nannette@mpassociates.com

ON-SITE REGISTRATION

On-Site registration for all Microwave Week events will be available in the Per Function Space outside the Exhibit Hall of the Phoenix Convention Center. Registration hours are:

Date	Time
Saturday, 16 May	08:00-18:00
Sunday, 17 May	07:00-19:00
Monday, 18 May	07:00-19:00
Tuesday, 19 May	07:00-18:00
Wednesday, 20 May	07:00-18:00
Thursday, 21 May	07:00-16:00
Friday, 22 May	07:00-10:30

Exhibit Only Registration

Exhibit only registration is available.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to IMS technical sessions and exhibits. Digests are not included. The Press Lounge will be available from Monday thru Thursday of Microwave Week and it located on the third level in room 31.

ARFTG Registration

Late on-site registration will be available in the Per Function Space outside the Exhibit Hall of the Phoenix Convention Center on Friday, 22 May from 07:00 to 10:30. If at all possible, please preregister earlier in the week.

Devictmetion Detect in IICD	Early Bird	(2 Feb-20 Apr)	Advance (21 Apr-15 May)	On-site (1	(6-22 May)
RESISTATION RATES IN USD	Member	Non-Member	Member	Non-Member	Member	Non-Member
Superpass						
Superpass	\$1,025	\$1,540	\$1,190	\$1,785	\$1,385	\$2,060
IEEE Life Member (Retiree)	\$610		\$715		\$865	
Student	\$610	\$640	\$715	\$745	\$865	\$895
RFIC						
RFIC Sessions	\$240	\$340	\$270	\$395	\$290	\$430
IEEE Life Member (Retiree)	\$165		\$185		\$205	
Student	\$165	\$190	\$185	\$210	\$205	\$230
SWI						
IMS Sessions	\$440	\$655	\$510	\$765	\$590	\$875
IEEE Life Member (Retiree)	\$80		\$90		\$105	
Student	\$80	\$140	\$90	\$150	\$105	\$165
Single Day Registration	\$225	\$330	\$260	\$380	\$300	\$450
ARFTG						
ARFTG Sessions	\$225	\$340	\$265	\$395	\$300	\$450
IEEE Life Member (Retiree)	\$155		\$180		\$200	
Student	\$155	\$185	\$180	\$210	\$200	\$230
Exhibit Only						
Exhibition Only Pass	\$25	\$25	\$25	\$25	\$30	\$30
Wednesday Exhibition Only Pass	free	free	free	free	free	free
Guest Badge	\$30	\$30	\$30	\$30	\$30	\$30

REGISTRATION RATES

	Early Bird	(2 Feb-20 Apr)	Advance (21 Apr-15 May)	On-site (1	6-22May)
Registration Rates III USD	Member	Non-Member	Member	Non-Member	Member	Non-Member
Full Day Short Course						
Full Day Short Course	\$295	\$440	\$345	\$515	\$405	\$605
IEEE Life Member (Retiree)	\$210		\$240		\$280	
Student	\$210	\$235	\$240	\$265	\$280	\$300
Half Day Short Course						
Half Day Short Course	\$205	\$310	\$240	\$365	\$275	\$420
IEEE Life Member (Retiree)	\$145		\$170		\$195	
Student	\$145	\$165	\$170	\$190	\$195	\$215
Full Day Workshop						
Full Day Workshop	\$170	\$250	\$185	\$275	\$230	\$345
IEEE Life Member (Retiree)	\$130		\$140		\$160	
Student	\$130	\$150	\$140	\$160	\$160	\$180
Half Day Workshop						
Half Day Workshop	06\$	\$130	\$100	\$145	\$120	\$180
IEEE Life Member (Retiree)	\$65		\$70		\$85	
Student	\$65	\$85	\$70	\$90	\$85	\$105
2 Full Day Workshops (includes all workshop USB: Sun Mon Fri)						
2 Full Day Workshops	\$445	\$655	\$485	\$715	\$605	\$895
IEEE Life Member (Retiree)	\$330		\$360		\$410	
Student	\$330	\$350	\$360	\$380	\$410	\$430
Printed Workshop Notes	included	included	\$20	\$30	\$30	\$45

REGISTRATION RATES (continued)

	Early Rird	(3 Feh-20 Anr)	Advance (21 Anr-15 Mav)	On-site (1	(-22 Mav)
Registration Rates in USD	n nor frame	(THIT A MATE)		/ former / a where -		(frames o
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Proceedings USB						
RFIC	\$50	\$75	\$60	\$90	\$70	\$105
IMS	\$50	\$75	\$60	\$90	\$70	\$105
ARFTG	\$50	\$75	\$60	\$90	\$70	\$105
Evening Events						
RFIC Sunday Evening Only (includes: RFIC Plenary Session, Industry Showcase and Reception)	\$50	\$75	\$60	\$90	\$70	\$105
Award Banquet (Wednesday Night)	\$55	\$55	\$65	\$65	\$75	\$75
Lunch						
Monday Boxed Lunch	\$25	\$25	\$25	\$25		
Tuesday Boxed Lunch	\$25	\$25	\$25	\$25		
Wednesday Boxed Lunch	\$25	\$25	\$25	\$25		
Thursday Boxed Lunch	\$25	\$25	\$25	\$25		

REGISTRATION RATES (continued)

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning if required and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 36 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Andorra	Hungary	New Zealand
Australia	Iceland	Norway
Austria	Ireland	Portugal
Belgium	Italy	San Marino
Brunei	Japan	Singapore
Czech Republic	Latvia	Slovakia
Denmark	Liechtenstein	Slovenia
Estonia	Lithuania	South Korea
Finland	Luxembourg	Spain
France	Malta	Sweden
Germany	Monaco	Switzerland
Greece	the Netherlands	United Kingdom

Currently, 36 countries participate in the Visa Waiver Program, as shown below:

For more information, see http://travel.state.gov/visa/temp/without/without_1990.html.

VISA INFORMATION (continued)

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, https://www.cbp.gov, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing. Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (information to be posted shortly).

Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing.

For additional visa assistance, please contact Zaher Bardai at <u>zb@ieee.org</u>.

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative sources of information are the U.S. Government website at http://travel.state.gov/content/visas/english.html.

SOCIAL EVENTS/GUEST PROGRAM

MONDAY, 18 MAY 2015

Welcome Celebration: 19:00-21:30

IMS2015 starts with a welcome celebration on Monday for all attendees, which will be hosted at the Arizona Science Center immediately following the IMS2015 Plenary Session.

TUESDAY, 19 MAY 2015

Women in Microwaves Reception: 18:00–19:30

The Women in Microwaves Reception will be held at the Sheraton Hotel, just a two minute walk from the Phoenix Convention Center.

Young Professionals/Student Reception: 18:30-20:30

The Young Professionals/Student (formerly Graduate of Last Decade (GOLD) reception will be hosted in Lucky Strikes located in Cityscape.

All three events are within the walking distance from the convention center, which are 0.2 mile (2 min), 0.4 mile (6 min), and 0.3 mile (4 min) away, respectively.

WEDNESDAY, 20 MAY 2015

Industry Hosted Cocktail Reception: 17:30–18:30

The Industry-Hosted Reception is scheduled on the exhibition floor on Wednesday, 20 May 2015 right before the MTT-S Awards Banquet.

Awards Banquet: 18:30-21:00

The MTT-S Awards Banquet will be hosted in the Sheraton Hotel and feature exciting entertainment from Global Roots.

Global Roots encompasses the soul of Spain and India in what we call Flamenco India. This show is the first true union of the melodic, spiritual grace of south India with the mesmerizing passionate rhythms of flamenco hailed from the Gypsy people.

THURSDAY, 21 MAY 2015

Closing Ceremony: 17:45–18:00

The closing ceremony will immediate follow the Thursday closing session at the Phoenix Convention Center.

MONDAY, 18 MAY – FRIDAY, 22 MAY 2015

Guest Lounge at Hyatt Regency Phoenix Hotel

The guest lounge will be located at the Hyatt Regency Phoenix Hotel. Continental Breakfast and refreshments will be provided for all guests. Several IPADs will be provided for the guest to browse internet or play games. The guest lounge serves as a hub for guests and a starting point for tours around the city.



CONVENTION CENTER MAPS



CONVENTION CENTER MAPS (continued)

Piscataway, NJ 08854, USA IEEE 445 Hoes Lane

2015 RFIC Symposium Phoenix, Arizona, USA 17–19 May 2015

