



2014 IEEE Radio Frequency Integrated Circuits Symposium

Tampa Bay, Florida, USA

1–3 June 2014



PROGRAM

Tampa Convention Center
and
Marriott Waterside Hotel and Marina

Sponsored by

IEEE Microwave Theory and Techniques Society
IEEE Electron Devices Society
and
IEEE Solid-State Circuits Society



RFIC Plenary Round-Table, Industry Showcase, and Reception

Sunday Evening, 1 June 2014
Marriott Waterside Hotel and Marina

After a busy day immersed in RFIC Workshops, enjoy a relaxing evening with your RFIC colleagues at these special Sunday night RFIC events, to be held in the Tampa Marriott Waterside Hotel and Marina, just across the street from the Tampa Convention Center (TCC).

17:30–19:00 Grand Ballroom — The Plenary Session kicks off the evening with the Student Paper Awards ceremony followed by two outstanding plenary speakers, Dr. Pieter Hooijmans, VP R&D and Strategy at NXP, and Prof. Lawrence Larson, Dean of School of Engineering, Brown University. Please see pages 7–11 for more details.

19:00–20:00 Grand Ballroom Foyer — “Hot Chips and Cold Drinks” Industry Showcase, and Reception Part 1: Immediately following the Plenary Session is the RFIC Reception held in the foyer just outside the ballroom (with a spectacular view of the marina). Cold drinks and appetizers will be provided while you connect with old friends, make new acquaintances, and catch up on the latest news in the wireless industry.

This year for the first time, the most innovative and highly-rated industrial papers will be highlighted in the Industry Showcase, held concurrently with the reception. Authors of these papers will be present for discussion of their work, summarized in poster format. Media will be present to cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. Please see pages 12–13 for more details.

20:00–21:00 Grand Ballroom — The Inaugural RFIC Plenary Round Table will feature luminaries from the RFIC community engaging in a lively discussion, in a casual, talk-show format, led by Prof. Hossein Hashemi, USC. Panelists include our two plenary speakers (listed above), along with Kamal Sahota, VP Qualcomm, Reza Rofougaran, SVP Broadcom, Zdravko Boos, Intel Fellow, and Peter Gammel, CTO Skyworks. Please see page 14 for more details.

21:00–22:00 Grand Ballroom Foyer — Reception Part 2

Admittance to all RFIC Sunday evening events is included with the RFIC Symposium registration and Superpass registration. Additionally, Sunday-night-only tickets can be purchased for those who cannot attend the rest of the RFIC Symposium but do not want to miss these great events. Please see <http://rfic-ieee.org/> for more details.

The RFIC Receptions are sponsored by the RFIC Steering Committee, and through the generous support of our cooperate sponsors:

Platinum



Gold



Silver



RFIC Symposium Schedule (31 May – 3 June 2014)

Event	Location	Saturday 31 May	Sunday 1 June	Monday 2 June	Tuesday 3 June
Registration	TCC 2 nd Lobby	08:00–18:00		07:00–19:00	07:00–18:00
Speakers' Breakfast	TCC Ballroom A			07:00–08:00	
Workshop Breakfast	TCC Ballroom D		07:00–08:00		
Workshops & Short Courses	TCC 10–25		08:00–17:00		
Workshop Lunch	TCC Ballroom D		12:00–13:00		
Panel Sessions	TCC Ballroom A (Monday) TCC Ballroom B (Tuesday)			12:00–13:30	
Steering Comm. Lunch Meeting	Marriott Florida Salon 4/5			13:00–14:30	
TPC Lunch Meeting	Marriott Florida Salon 4/5				13:00–14:30
Technical Sessions	TCC 10/11, 13/14, 15/16, 18			08:00–09:40 10:10–11:50 13:30–15:10 15:40–17:20	08:00–09:40 10:10–11:50
Interactive Forum	TCC Ballroom C/D				13:30–16:00
Plenary Session	Marriott Grand Ballroom		17:30–19:00		
Industry Showcase & Receptions	Marriott Grand Ballroom Foyer		19:00–20:00 21:00–22:00		
Plenary Round Table	Marriott Grand Ballroom		20:00–21:00		



photos courtesy of Visit Tampa Bay and Robert La Follette

TABLE OF CONTENTS

The RFIC Symposium is the premier IC conference focused exclusively on the latest developments in RF, Microwave, and mm-Wave Integrated Circuit technology and innovation from both industry and academia.

	Table of Contents	1
	Welcome Message from Chairs.....	2
	Steering Committee	4
	Executive Committee.....	4
	Advisory Board	4
	Technical Program Committee.....	5
	RFIC 2014 Schedule	6
	Plenary, Round-Table, Industry Showcase, and Reception Schedule	7
	Student Paper Award Finalists.....	8
	Plenary Speakers.....	10
	Industry Showcase.....	12
	Round Table Discussion	14
MONDAY	AM1 RMO1A: Energy-Efficient Wireless Transceivers	15
	AM1 RMO1B: Blocker-Tolerant and Low-Noise Front-Ends	17
	RMO2A: Mixed Signal Circuits at Gigahertz Frequencies	19
	AM2 RMO2B: K-Band Front-End ICs.....	21
	AM2 RMO2C: Advanced PLL Techniques.....	23
	AM2 RMO2D: Advancements in Distributive, Thermal, and Non-Linear Device Modeling	25
	PM1 RMO3A: Advances in Wireless Mobile ICs	27
	PM1 RMO3B: mm-Wave PAs: 60GHz and Beyond	29
	PM1 RMO3C: mm-Wave & Terahertz Frequency Generation Techniques	31
	PM1 RMO3D: Advances in Nano-Scale Devices and Novel Measurement Techniques for RFIC Designs	33
	PM2 RMO4A: Wireless Connectivity Transceivers and Multi-Standard Digital Transmitters	35
	PM2 RMO4B: Highly-Efficient Power Amplifiers	37
PM2 RMO4C: Quadrature and Multi-Mode VCOs	39	
PM2 RMO4D: High-Speed Data Transceivers	41	
TUESDAY	AM1 RTU1C: mm-Wave Integration Technologies	43
	AM2 RTU2A: Software-Defined and Cognitive Radio Techniques	45
	AM2 RTU2B: Multiband PAs and Power Mixers	47
	AM2 RTU2C: Sub-mm-Wave Transceivers	49
	PM RTU1F: Interactive Forum	51
	Panel Sessions.....	58
	Workshops and Short Courses	60
	Registration.....	79
	Registration Rates.....	83
	Visa Information.....	86
	Social Events/Guest Program.....	88
	Downtown Tampa Map.....	93
	Convention Center Maps	94

Welcome Message from Chairs

We invite you to participate in the 2014 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, to be held in Tampa, Florida on 1–3 June 2014. RFIC is the premier IC conference focused exclusively on the latest developments in RF, Microwave, and Millimeter Wave Integrated Circuit technology and innovation.

RFIC, the International Microwave Symposium (IMS), ARFTG, and the IMS Industry Exhibition make up “Microwave Week”, the largest worldwide RF/microwave meeting of the year. Come to Microwave week to learn from the world’s experts through a wide variety of technical sessions, interactive forums, panel sessions, workshops, short courses, industrial exhibits, application seminars, and historical exhibits. Share your knowledge with others by presenting your latest results. Expand your network. Catch up with old friends and colleagues. Return invigorated with new ideas and enthusiasm.

For the first time in 2014, RFIC will offer a number of new initiatives specifically geared towards the RFIC industry. First, a new 2-page industry brief format is introduced that allows the latest state-of-the-art RF IC design results to be presented, without requiring die photos and detailed schematics (as required in full-length, 4-page, submissions). Nevertheless, these 2-page briefs are subjected to the same technical criteria and rigorous review as full length papers. Secondly, the most innovative and highly-rated industrial papers, both 2- and 4-page, will be invited to present a poster (and optional demo) at a special Industry Showcase Session to held during the popular evening RFIC Reception on Sunday, 1 June 2014. In addition to all of the RFIC attendees, the media will be invited to cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs.

Another new initiative in 2014 is geared towards enhancing academic submissions through programs supporting students. All of the RFIC student paper finalists will now receive complementary RFIC registration. In addition, the lead authors of the top 3 student papers will receive \$500 honorariums along special recognition at the RFIC Plenary Session where these awards will be announced.

Students have even more ways to participate (and receive financial assistance) this year. Students may volunteer to help with RFIC (and/or IMS) conference logistics in exchange for complementary conference registration, meals, T-shirts, and other benefits. For the first time in 2014, first and second-year RFIC PhD students may also participate in the PhD Student Sponsorship Initiative Program, joint with IMS. This program, established and sponsored by the MTT-S Administrative Committee, aims to engage these PhD students in the conference by having them complete technical assignments during the conference and report on them later in the week. Sponsorship includes complementary conference registrations (RFIC and IMS), lodging, and meals.

The 2014 RFIC Symposium will open on Sunday, 1 June 2014 with a lineup of eight full-day and five half-day workshops, four of which will be co-sponsored by IMS. Three additional joint RFIC/IMS workshops will be held on Monday. RFIC workshops cover a wide array of topics with presentations from experts in their respective fields, and historically have been highly attended and well received. This year’s workshops cover some of the hottest topics in RFIC design. There are a number of workshops focused on power amplifier (PA) design including: silicon and GaN PAs for RF and mm-wave applications, highly-efficient power amplifiers and smart transmitters, power amplifiers for software defined radios, and critical supporting circuit designs such as GaN-based power supply modulators. In the frequency synthesis area, the “Frequency synthesis for 60-GHz and beyond: architectures and building blocks” workshop focuses on design techniques for low phase noise frequency synthesizers at mm-wave frequencies. Workshops focused on some of the emerging technologies in RF transceivers include techniques for handling interference and self-interference, RF and wideband data-converters for transmitters and receivers, and EMC/EMI-aware design practices for reducing coupling and interference in integrated circuits.

The RFIC Plenary Session will be held on Sunday evening, in the Marriott Hotel directly across from the Convention Center. The plenary will begin with some overall conference highlights, followed by

the student paper awards. The plenary continues with two outstanding keynote addresses, given by two renowned industry leaders in the RF/Microwave Community. The first speaker is Pieter Hooijman, Vice President R&D and Strategy at NXP Semiconductors, whose talk is entitled “*How to differentiate with RF Silicon Technologies in high volume applications?*” The second speaker is Prof. Lawrence Larson, Dean of the School of Engineering at Brown University, who will present a talk entitled “*The Next Era of Wireless Communications — Enabling Revolutions in Health Care, Transportation, Energy, and the Environment.*” Be sure not to miss these engaging presentations.

Immediately following the Plenary Session is the new Industry Showcase Session concurrent with the RFIC Reception, providing a mix of “hot chips” and cold drinks. These events will be held in the foyer just outside of the Plenary Session, with a wonderful view of the water and marina. You’ll want to be here.

The inaugural RFIC Plenary Round Table Discussion will be held next, with the stage set “talk show style”. Leaders from the RFIC community will engage in a lively discussion on “*Beyond 4G Wireless Communications: An RFIC Perspective.*” Audience participation will also be welcome. Once the Round Table adjourns, the Reception will continue where it left off, with plenty of cold beverages to keep everyone cool.

Technical papers will be presented during RFIC oral sessions throughout Monday and on Tuesday morning, followed by the RFIC Interactive Forum on Tuesday afternoon. The Interactive Forum features papers presented in poster format, giving the attendees a chance to speak directly with the authors regarding their work.

During lunchtime on both Monday and Tuesday, the conference features panel sessions that are sure to draw lively debate among the panelists and audience. Monday’s RFIC panel session is titled “*Fabless design: got any problem with that?*” and will debate the pros and cons of the fabless design model. The Tuesday panel session, held jointly with IMS, is titled “*Is Spectrum Explosion Muffled without Tunable RF?*” This panel brings together experts from across the wireless ecosystem to discuss the end user benefits, market opportunities, technical challenges and projected solutions surrounding the spectrum explosion and its impact on RF hardware, and whether or not tunable RF front-ends will step in to save the day.

Tampa offers a unique and exciting experience for everyone. A visit to the ever-growing downtown area, or the exciting Channelside and Ybor entertainment districts, will provide you with plenty to see. Tampa has a diverse selection of great restaurants and some of Florida’s best attractions, including the Florida Aquarium, Busch Gardens Tampa Bay, the Straz Center for the Performing Arts, and Lowry Park Zoo. Of particular note are the new Tampa Bay History Center and the recently opened Tampa Museum of Art.

On behalf of the entire RFIC Steering Committee, we would like to extend to all of you a warm welcome to attend the 2014 RFIC Symposium. We are looking forward to an exciting program and hope you can join us in Tampa! For more details, please visit our website <http://rfic-ieee.org>.



Lawrence Kushner
General Chair
BAE Systems



Bertan Bakkaloglu
TPC Co-Chairman
Arizona State University



Albert Wang
TPC Co-Chairman
UC Riverside

Steering Committee

- Lawrence Kushner, BAE Systems, *General Chair*
Bertan Bakkaloglu, Arizona State University, *TPC Co-Chair*
Albert Wang, University of California at Riverside, *TPC Co-Chair*
Kevin Kobayashi, RFMD, *Finance Chair*
Robert Alongi, IEEE, *Finances*
Walid Y. Ali-Ahmad, MediaTek, *Workshop Chair*
Li Lin, Marvell Technology Group, *Workshop Co-Chair*
Timothy M. Hancock, MIT Lincoln Laboratory, *Panel Sessions Chair*
Stefano Pellerano, Intel, *Digest & Publications Chair*
Domine Leenaerts, NXP Semiconductors, *RFIC Program Book*
Freek van Straten, NXP Semiconductors, *IMS Program Book*
Srenik Mehta, Qualcomm, *Session Organization*
Waleed Khalil, Ohio State University, *Transactions Special Issues*
Andre Hanke, Intel, *Student Paper Contest*
Brian Floyd, North Carolina State University, *Publicity Chair*
Amanda Scacchitti, *Publicity & Advisor*
Bob Stengel, SiriusXM, *Secretary*
Georg Boeck, Berlin Institute of Technology, *European Liaison*
Patrick Yue, HKUST, *Asia Pacific Liaison*
Fujiang Lin, USTC, *Asia Pacific Liaison*
Michael Oakley, Georgia Institute of Technology, *Webmaster*
Steven Turner, BAE Systems, *Paper Submission Website*
Tim Lee, Boeing, *Web Presence*
Elsie Cabrera, IEEE, *Conference Manager*
Zaher Bardai, IMN Epiphany, *VISAs*

Executive Committee

- Yann Deval, *University of Bordeaux*
David Ngo, *RFMD*
Jacques C. Rudell, *University of Washington*
Lawrence Kushner, *BAE Systems*

Advisory Board

- Natalino Camilleri, *RFWDS*
Joseph Staudinger, *Freescale Semiconductor*
Stefan Heinen, *RWTH Aachen University*
Luciano Boglione, *Naval Research Laboratory*
Jenshan Lin, *University of Florida*

Technical Program Committee

- Ali Afsahi, *Broadcom*
Walid Ali-Ahmad, *MediaTek*
Himanshu Arora, *Texas Instruments*
Edmund Balboni, *Analog Devices*
Jean-Baptiste Begueret, *University of Bordeaux*
Didier Belot, *STMicroelectronics*
Georg Boeck, *Technical University of Berlin*
Luciano Boglione, *Naval Research Laboratory*
Pierre Busson, *STMicroelectronics*
Natalino Camilleri, *Nitro*
Sudipto Chakraborty, *Texas Instruments*
Richard Chan, *BAE Systems*
Glenn Chang, *MaxLinear*
Jinghong Chen, *Southern Methodist University*
Nick Cheng, *Skyworks Solutions*
Yuhua Cheng, *Peking University*
Yann Deval, *University of Bordeaux*
Oren Eliezer, *Xtendwave*
Kamran Entesari, *Texas A&M University*
Ayman Fayed, *Iowa State University*
Brian Floyd, *North Carolina State University*
Eric Fogleman, *MaxLinear*
Ranjit Gharpurey, *University of Texas at Austin*
Danielle Griffith, *Texas Instruments*
Jane Gu, *University of California at Davis*
Aditya Gupta, *Northrop Grumman*
Timothy M. Hancock, *MIT Lincoln Laboratory*
Andre Hanke, *Intel*
Ramesh Harjani, *University of Minnesota*
Hossein Hashemi, *University of Southern California*
Gary Hau, *Anadigics*
Stefan Heinen, *RWTH Aachen University*
Mona Hella, *Rensselaer Polytechnic Institute*
Frank Henkel, *IMST*
Chun-Ming Hsu, *IBM*
Tian-Wei Huang, *National Taiwan University*
Gernot Hueber, *NXP Semiconductors*
Nobuyuki Itoh, *Okayama Prefectural University*
Reynold Kagiwada, *Northrop Grumman*
Waleed Khalil, *Ohio State University*
Jaber Khoja, *Qualcomm*
Sayfe Kiaei, *Arizona State University*
Bumman Kim, *POSTECH*
Jennifer Kitchen, *Arizona State University*
Eric Klumperink, *University of Twente*
Kevin Kobayashi, *RFMD*
Harish Krishnaswamy, *Columbia University*
Youngwoo Kwon, *Seoul National University*
Fred Lee, *Fairchild Semiconductor*
Tzung-Yin Lee, *Skyworks Solutions*
Chang-Ho Lee, *Qualcomm*
Domine Leenaerts, *NXP Semiconductors*
Salvatore Levantino, *Politecnico di Milano*
Donald Y.C. Lie, *Texas Tech University*
Jenshan Lin, *University of Florida*
Li Lin, *Marvell Technology Group*
Fujiang Lin, *USTC*
Danilo Manstretta, *University of Pavia*
Mozhgan Mansuri, *Intel*
Srenik Mehta, *Qualcomm*
Mohyee Mikhemar, *Broadcom*
Pedram Mohseni, *Case Western Reserve University*
Jyoti Mondal, *Northrop Grumman*
Arun Natarajan, *Oregon State University*
Kenjiro Nishikawa, *Kagoshima University*
Jeyanandh Paramesh, *Carnegie Mellon University*
Stefano Pellerano, *Intel*
Dennis Poulin, *Anritsu Company*
Madhukar Reddy, *MaxLinear*
Francois Rivet, *University of Bordeaux*
Francis Rotella, *Peregrine Semiconductor*
Chris Rudell, *University of Washington*
Derek Shaeffer, *InvenSense*
Osama Shanaa, *MediaTek*
Eddie Spears, *RFMD*
R. Bogdan Staszewski, *Delft University of Technology*
Joseph Staudinger, *Freescale Semiconductor*
Bob Stengel, *SiriusXM*
Noriharu Suematsu, *Toboku University*
Julian Tham, *Broadcom*
Steven Turner, *BAE Systems*
Leon van den Oever, *Radio Semiconductor*
Freek van Straten, *NXP Semiconductors*
Jeffrey Walling, *University of Utah*
Yanjie Wang, *Intel*
Hua Wang, *Georgia Institute of Technology*
David Wentzloff, *University of Michigan*
Magnus Wiklund, *Qualcomm Atheros*
James Wilson, *US Army Research Laboratory*
Renaldi Winoto, *Marvell Semiconductor*
Haolu Xie, *ZTE USA*
Li-Wu Yang, *Jiao-Tong University*
Chen Yang, *University of California at Berkeley*
Patrick Yue, *HKUST*
Gary Zhang, *Skyworks Solutions*

RFIC 2014 Schedule

Saturday, 31 May 2014

08:00–18:00 Registration — Tampa Convention Center (TCC) 2nd Lobby

Sunday, 1 June 2014

07:00–19:00 Registration — TCC 2nd Lobby

07:00–08:00 Speakers' Breakfast — TCC Ballroom A

07:00–08:00 Workshop Breakfast — TCC Ballroom D

08:00–17:00 Workshops and Short Courses, TCC 10–25

12:00–13:00 Workshops Lunch — TCC Ballroom D

17:30–19:00 RFIC Plenary — Marriott Grand Ballroom

19:00–20:00 Industry Showcase and Reception Part 1 — Marriott Grand Ballroom Foyer

20:00–21:00 RFIC Plenary Roundtable — Marriott Grand Ballroom

21:00–22:00 Reception Part 2 — Marriott Grand Ballroom Foyer

Monday, 2 June 2014

07:00–19:00 Registration — TCC 2nd Lobby

07:00–08:00 Speakers' Breakfast — TCC Ballroom A

07:00–08:00 Workshop Breakfast — TCC Ballroom D

08:00–17:00 Workshops and Short Courses — TCC 10–25

08:00–09:40 RMO1A — TCC 10–11: *Energy-Efficient Wireless Transceivers*

RMO1B — TCC 13–14: *Blocker-Tolerant and Low-Noise Front-Ends*

09:40–10:10 Break

10:10–11:50 RMO2A — TCC 10–11: *Mixed Signal Circuits at Gigahertz Frequencies*

RMO2B — TCC 13–14: *K-Band Front-End ICs*

RMO2C — TCC 15–16: *Advanced PLL Techniques*

RMO2D — TCC 18: *Advancements in Distributive, Thermal, and Non-Linear Device Modeling*

12:00–13:00 Workshops Lunch — TCC Ballroom D

12:00–13:30 RFIC Panel — TCC Ballroom A

13:00–14:30 RFIC Steering Committee Lunch Meeting — Marriott Florida Salon 4–5

13:30–15:10 RMO3A — TCC 10–11: *Advances in Wireless Mobile ICs*

RMO3B — TCC 13–14: *mm-Wave PAs: 60GHz and Beyond*

RMO3C — TCC 15–16: *mm-Wave & Terahertz Frequency Generation Techniques*

RMO3D — TCC 18: *Advances in Nano-Scale Devices and Novel Measurement Techniques for RFIC Designs*

15:10–15:40 Break

15:40–17:20 RMO4A — TCC 10–11: *Wireless Connectivity Transceivers and Multi-Standard Digital Transmitters*

RMO4B — TCC 13–14: *Highly-Efficient Power Amplifiers*

RMO4C — TCC 15–16: *Quadrature and Multi-Mode VCOs*

RMO4D — TCC 18: *High-Speed Data Transceivers*

Tuesday, 3 June 2014

07:00–19:00 Registration — TCC 2nd Lobby

07:00–08:00 Speakers' Breakfast — TCC Ballroom A

08:00–09:40 RTU1C — TCC 15–16: *mm-Wave Integration Technologies*

09:40–10:10 Break

10:10–11:50 RTU2A — TCC 10–11: *Software-Defined and Cognitive Radio Techniques*

RTU2B — TCC 13–14: *Multiband PAs and Power Mixers*

RTU2C — TCC 15–16: *Sub-mm-Wave Transceivers*

12:00–13:30 RFIC Panel — TCC Ballroom B

13:00–14:30 RFIC TPC Lunch Meeting — Marriott Florida Salon 4–5

13:30–16:00 RTU1F — TCC Ballroom C–D: *Interactive Forum*

Plenary, Round-Table, Industry Showcase, and Reception Schedule

Sunday Evening, 1 June 2014
Marriott Waterside Hotel and Marina

17:30

Marriott Grand Ballroom

RFIC Plenary

Chair: Lawrence Kushner, BAE Systems

Co-Chair: Bertan Bakkaloglu, Arizona State University

Co-Chair: Albert Wang, University of California at Riverside

- 17:30 Welcome Message from General and TPC Chairs, Student Paper Awards
18:00 *How to differentiate with RF Silicon Technologies in high volume applications?*
Pieter Hooijmans, NXP Semiconductors
18:30 *The Next Era of Wireless Communications —*
Enabling Revolutions in Health Care, Transportation, Energy, and the Environment
Lawrence Larson, Brown University

19:00

Marriott Grand Ballroom Foyer

“Hot Chips and Cold Drinks” Industry Showcase and Reception Part 1

20:00

Marriott Grand Ballroom

The Inaugural RFIC Plenary Round Table

Organizer and Moderator:

Hossein Hashemi, University of Southern California

Participants:

Zdravko Boos, Intel
Peter L. Gammel, Skyworks Solutions
Pieter Hooijmans, NXP Semiconductors
Lawrence Larson, Brown University
Reza Rofougaran, Broadcom
Kamal Sahota, Qualcomm

21:00

Marriott Grand Ballroom Foyer

Reception Part 2

Student Paper Award Finalists

One of the missions of RFIC Symposium is to encourage academic research and education. Best Student Award finalists nominated every year by RFIC Technical Program Committee benefit from a free RFIC registration. Among these, three Best Student Papers are further selected and awarded a \$500 honorarium during the plenary session. This year's best student finalists are:

A 2.5nJ/Bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 Based on a Hybrid Polyphase-MUX/ILO Based Modulator

Mustafijur Rahman, Mohammad Elbadry, Ramesh Harjani
University of Minnesota, USA
RMO1A-2 08:20

A Low-Power Digitally Controlled Wideband FM Transceiver

N. Saputra¹, John R. Long¹, John J. Pekarik²
¹Technische Universiteit Delft, The Netherlands, ²IBM, USA
RMO1A-3 08:40

A Compact 24–54GHz CMOS Band-Pass Distributed Amplifier for High Fractional Bandwidth Signal Amplification

V. Bhagavatula¹, M. Taghivand², Jacques C. Rudell¹
¹University of Washington, USA, ²Qualcomm, USA
RMO2B-1 10:10

A 0.6/1.2-V 14.1-mW 96.8GHz-to-108.5GHz Transformer-Based PLL with Embedded Phase Shifter in 65-nm CMOS

Yue Chao¹, Howard C. Luong¹, Zhiliang Hong²
¹HKUST, China, ²Fudan University, China
RMO2C-2 10:30

A Circuit-Level Model for Accurately Modeling 3rd Order Nonlinearity in CMOS Passive Mixers

Hazal Yüksel, Dong Yang, Alyosha C. Molnar
Cornell University, USA
RMO2D-5 11:30

Broadband CMOS Stacked Power Amplifier Using Reconfigurable Interstage Network for Envelope Tracking Application

Sunghwan Park, Jung-Lin Woo, Moon-Suk Jeon, Unha Kim, Youngwoo Kwon
Seoul National University, Korea
RMO3A-4 14:30

Spatially Power-Combined W-Band Power Amplifier Using Stacked CMOS

Jefy Jayamon, Ozan Gurbuz, Bassel Hanafi, Amir Agah, James Buckwalter, Gabriel M. Rebeiz, Peter Asbeck
University of California at San Diego, USA
RMO3B-1 13:30

A High-Power, Low-Loss W-Band SPDT Switch Using SiGe PIN Diodes

Peter Song, Robert L. Schmid, Ahmet Çağrı Ulusoy, John D. Cressler
Georgia Institute of Technology, USA
RMO3D-2 13:50

Sunday, 1 June 2014

17:30–18:00

Marriott Grand Ballroom

- A +27.3dBm Transformer-Based Digital Doberty Polar Power Amplifier Fully Integrated in Bulk CMOS*
 Song Hu¹, Shouhei Kousai², Jong Seok Park¹, Outmane Lemtiri Chlieh¹, Hua Wang¹
¹Georgia Institute of Technology, USA, ²Toshiba Corporation, Japan
 RMO4B-2 16:00
- A 26-GHz Low-Phase-Error In-Phase-Coupled QVCO Using Modified Bi-Directional Diodes*
 Jun-Chau Chien, Nai-Chung Kuo, Ali M. Niknejad
 University of California at Berkeley, USA
 RMO4C-1 15:40
- A 2.75–6.25GHz Low-Phase-Noise Quadrature VCO Based on a Dual-Mode Ring Resonator in 65nm CMOS*
 Masoud Moslehi Bajestan, Vahid Dabbagh Rezaei, Kamran Entesari
 Texas A&M University, USA
 RMO4C-4 16:40
- A 3-mW 25-Gb/s CMOS Transimpedance Amplifier with Fully Integrated Low-Dropout Regulator for 100GbE Systems*
 Yipeng Wang, Yan Lu, Quan Pan, Zhengxiong Hou, Liang Wu, Wing-Hung Ki, C. Patrick Yue
 HKUST, China
 RMO4D-2 16:00
- Dynamic Polarization Control of Integrated Radiators*
 Steven M. Bowers, Amirreza Safaripour, Ali Hajimiri
 California Institute of Technology, USA
 RTU1C-1 08:00
- A 79-GHz Bidirectional Pulse Radar System with Injection-Regenerative Receiver in 65nm CMOS*
 Pen-Jui Peng, Chiro Kao, Chin-Yang Wu, Jri Lee
 National Taiwan University, Taiwan
 RTU1C-4 09:00
- A Widely Tunable Active Duplexing Transceiver with Same-Channel Concurrent RX/TX and 30dB RX/TX Isolation*
 Dong Yang, Alyosha C. Molnar
 Cornell University, USA
 RTU2A-3 10:50
- A 1.8dB NF Blocker-Filtering Noise-Canceling Wideband Receiver with Shared TIA in 40nm CMOS*
 Hajir Hedayati¹, Wing-Fat Andy Lau², Namsoo Kim², Vladimir Aparin², Kamran Entesari¹
¹Texas A&M University, USA, ²Qualcomm, USA
 RTU2A-4 11:10



Plenary Speaker 1

Pieter Hooijmans
Vice President R&D and Strategy
NXP Semiconductors

How to Differentiate with RF Silicon Technologies in High Volume Applications?

Abstract: The presentation will start with an overview of functional and technology mapping of RF systems, ranging from RF amplifiers to System-on-Chips (SoC's), and from modules to Wafer-Level Chip-Scale Packaging (WLCSP).

We'll then discuss why (dedicated) Si-based component technologies are very price-performance competitive in volume markets, namely a combination of low-cost manufacturing in large volume Si fabs., as well as the right integration level.

Three RF application segments will be illustrated, including cellular and microwaves, and it will be shown how the technologies are applied for optimal solutions.

About Pieter Hooijmans

Pieter Hooijmans, currently Vice President R&D and Strategy for one of the five Business units of NXP Semiconductors from Eindhoven, the Netherlands, has spent a more than 25 year career in and around RF.

After an MSc and PhD (cum laude) in microwave and communication technology at the Technical University Delft, as well as a period as radar specialist with the Royal Netherlands Air Force, he started a long career with Philips Research, Philips Consumer Electronics, and finally Philips Semiconductors which became NXP in 2006. In these years he has covered a very broad range of RF applications, ranging from radio, TV and satellite reception, high speed optical storage, mobile and cordless phones, base stations and infrastructure, to today's Internet-of-Things.

Current activities include, next to other domains, driving technology and platform roadmaps for Base Station RF PA's, Wireless Connectivity Front ends, Si Tuners and low power RF (Zigbee and BTLE) for the Internet-of-Things.



Plenary Speaker 2

Lawrence Larson
Founding Dean of the School of Engineering
Brown University

***The Next Era of Wireless Communications
– Enabling Revolutions in Health Care,
Transportation, Energy, and the Environment***

Abstract: 2013 marked the 40th anniversary of the first cellular telephone call. The growth of personal portable wireless communications since then has created a global communications network unprecedented in human history. This anniversary gives us the opportunity to consider what the next forty years of wireless communication might look like. Further inevitable Improvements in semiconductor technology, with resulting improvements in processing power, transistor speed and complexity will result in exciting new applications of wireless devices.

Wireless technology has historically been focused on personal or data communications, but some of the most exciting new approaches will center on medical, energy, transportation and environmental applications. These include such areas as wireless medical and neural interfaces, networked personal transportation and infrastructure, and the “internet of things.”

This talk will summarize the emerging wireless technologies that will enable these new applications, and present some of the challenges to their widespread adoption.

About Lawrence Larson

Larry Larson received the BS in Electrical Engineering from Cornell University and a PhD from UCLA. From 1980–1996 he was at Hughes Research Laboratories in Malibu, CA, where he developed high-frequency microelectronics in GaAs, InP and Si/SiGe and MEMS technologies. He joined the faculty at the University of California at San Diego, in 1996, where he was the inaugural holder of the Communications Industry Chair. He was Director of the UCSD Center for Wireless Communications from 2001–2006 and was Chair of the Department of Electrical and Computer Engineering from 2007–2011.

He moved to Brown University in 2011, where he is Founding Dean of the School of Engineering. He was recipient of the Hughes Sector Patent Award in 1994 for his work on RF MEMS, co-recipient of the 1996 Lawrence A. Hyland Patent Award of Hughes Electronics, for his work on low-noise millimeterwave HEMTs, co-recipient of the 1999 IBM Microelectronics Excellence Award for his work in Si/SiGe HBT technology and co-recipient of the CICC Best Invited Paper Award in 2005. He has published over 300 papers, received over 40 US patents, co-authored four books, and is a Fellow of the IEEE.

Sunday, 1 June 2014

18:30–19:00

Marriott Grand Ballroom

“Hot Chips and Cold Drinks” Industry Showcase

Chair: Bob Stengel, SiriusXM

This year for the first time, the most innovative and highly-rated industrial papers will be highlighted in the Industry Showcase, held concurrently with the plenary reception. Authors of these papers will be present to discuss their work, summarized in poster format. Media will be present to cover this event, making it an excellent opportunity to announce the latest RFIC developments and breakthroughs. This year’s Industry Showcase papers are:

A 5th Order 0.8/2.4GHz Programmable Active Band Pass Filter for Power DAC Applications

HRL Laboratories, USA

Zhiwei Xu, Deborah Winklea, Thomas C. Oh, Samuel Kim, Steven T.W. Chen, Yakov Royter, Maggy Lau, Irma Valles, Donald A. Hitko, James C. Li
RMO2A-1 10:10

A 9.2–12.7GHz Wideband Fractional-N Subsampling PLL in 28nm CMOS with 280fs RMS Jitter

imec, Belgium

Kuba Raczkowski, Nereo Markulic, Benjamin Hershberg, Joris Van Driessche, Jan Craninckx
RMO2C-1 10:10

Variable Delay Transmission Lines in Advanced CMOS SOI Technology

¹IBM, Israel, ²IBM, USA

Shlomo Shlafman¹, Benny Sheinman¹, Danny Elad¹, Alberto Valdes-Garcia², Mihai A.T. Sanduleanu²
RMO2D-1 10:10

A HSPA+/WCDMA/EDGE 40nm Modem SoC with Embedded RF Transceiver Supporting RX Diversity

¹MediaTek, UK, ²MediaTek, Taiwan, ³MediaTek, Singapore, ⁴MediaTek, USA

Jon Strange¹, Hsiang-Hui Chang², Paul Muller¹, Walid Ali-Ahmad³, Christophe Beghein¹, Fahd Ben Abdeljelil¹, Wen-Chang Lee², Charles Chiu², Tze Yee Sin³, Ta-Hsin Lin², David Ivory¹, Hao-Tang Shih², Chris Beale¹, Dimitris Nalbantis¹, Ivan S.C. Lu⁴, Chi-Wei Fan², Shao-Hung Lin², Hsin-Hua Chen², Chih-Hao Sun², Li-Shin Lai², Jhy-Rong Chen², Sheng-Jui Huang²
RMO3A-1 13:30

A Multiband Power Amplifier Using Combination of CMOS and GaAs Technologies for WCDMA Handsets

Mitsubishi Electric Corporation, Japan

T. Shimura, S. Maki, S. Fujiwara, K. Fujii, Y. Takahashi, S. Suzuki, M. Miyashita, K. Yamamoto, H. Seki, M. Hieda, Y. Hirano
RMO3A-3 14:10

A 46.4–58.1GHz Frequency Synthesizer Featuring a 2nd Harmonic Extraction Technique That Preserves VCO Performance

IBM, USA

Bodhisatwa Sadhu, Mark Ferriss, Alberto Valdes-Garcia
RMO3C-1 13:30

mm-Wave Noise Characterization of 40nm CMOS Transistor for up to 67GHz

¹GLOBALFOUNDRIES, Singapore, ²Focus Microwaves, Canada

Xi Sung Loo¹, Hoang V. Nguyen², Zhihong Liu¹, Johnny Kok Wai Chew¹, Neven Misljenovic², Bryan Hosein², Christos Tsironis², Jen Shuang Wong¹, Wai Heng Chow¹
RMO3D-1 13:30

Sunday, 1 June 2014

19:00–20:00

Marriott Grand Ballroom Foyer

RF Power Transistor Characterization and Testing with Hybrid Harmonic Injection Source and Load Tuners

Focus Microwaves, Canada

Hoang V. Nguyen, Neven Misljenovic, Bryan Hosein

RMO3D-5 14:50

A 55nm CMOS 4-in-1 (11b/g/n, BT, FM, and GPS) Radio-in-a-Package with IPD Front-End Components Directly Connected to Antenna

¹MediaTek, Taiwan, ²MediaTek, Singapore, ³MediaTek, USA

Jing-Hong Conan Zhan¹, Yuli Hsueh¹, Min Chen¹, Meng-Hsiung Hung¹, Yi-An Li¹, Lan-Chou Cho¹, Hui-Hsien Liu¹,

Ming-Da Tsai¹, Ping-Yu Chen¹, Jui-Lin Syu¹, Yi-Chien Tsai¹, Tao-Yao Chang¹, Jen-Che Tsai¹, Sheng-Hao Chen¹,

Ping-Hsuan Tsu¹, Kuo-Hao Chen¹, Chun-Yi Wu¹, Sheng Jau Wong², Chun Geik Tan², George Chien³

RMO4A-1 15:40

A 23dBm Fully Digital Transmitter Using $\Sigma\Delta$ and Pulse-Width Modulation for LTE and WLAN Applications in 45nm CMOS

Texas Instruments, USA

Rahmi Hezar, Lei Ding, Joonhoi Hur, Baher Haroun

RMO4A-3 16:20

A 2x2 MIMO 802.11abgn/ac WLAN SoC with Integrated T/R Switch and On-Chip PA Delivering VHT80 256QAM 17.5dBm in 55nm CMOS

¹MediaTek, Taiwan, ²MediaTek, USA

Tsung-Ming Chen¹, Wei-Chia Chan¹, Chien-Cheng Lin¹, Jui-Lin Hsu¹, Wen-Kai Li¹, Pi-An Wu¹, Yen-Lin Huang¹,

Yen-Chuan Huang¹, TzungChuen Tsai¹, Po-Yu Chang¹, Chih-Lung Chen¹, Chih-Hou Tsai¹, Tao-Yao Chang¹,

I-Ching Huang¹, Wen-Hsien Chiu¹, Chun-Hao Liao¹, Chia-Hsin Wu¹, George Chien²

RMO4A-5 17:00

A 25dBm Outphasing Power Amplifier with Novel Non-Isolated Combining Network

Texas Instruments, USA

Lei Ding, Joonhoi Hur, Rahmi Hezar, Baher Haroun

RMO4B-1 15:40

A 2.4GHz Class-D Power Amplifier with Conduction Angle Calibration for -50dBc Harmonic Emissions

¹imec, The Netherlands, ²Renesas Electronics Corporation, Japan, ³Technische Universiteit Delft, The Netherlands

Ao Ba¹, Vamshi Krishna Chillara¹, Yao-Hong Liu¹, Hiromu Kato², Kathleen Philips¹, Robert Bogdan Staszewski³

RMO4B-3 16:20

A Compact Antenna-in-Package 60-GHz SiGe BiCMOS Radio

Peraso Technologies, Canada

Eric Juntunen, Alex Tomkins, Alan Poon, Jennifer Pham, Ahmed El-Gabaly, Mohammad Fakhrazadeh, Hatem Tawfik,

Yat-Loong To, Mihai Tazlauanu, Brad Lynch, Ron Glibbery

RMO4D-5 17:00

A 64QAM 94GHz CMOS Transmitter SoC with Digitally-Assisted Power Amplifiers and Thru-Silicon Waveguide Power Combiners

¹Northrop Grumman Aerospace Systems, USA, ²Space Micro, USA, ³University of California at Los Angeles, USA

Tim LaRocca¹, Yi-Cheng Wu¹, Khanh Thai¹, Rob Snyder¹, Naveen Daftari¹, Owen Fordham¹, Paul Rodgers²,

Monte Watanabe¹, Yeat Yang¹, Mohammad Ardakani¹, Waleed Namoos¹, Sumiko Poust¹, Mau-Chung Frank Chang³

RTU1C-2 08:20

A Multi-Mode Software-Defined CMOS BPSK Receiver SoC for the Newly Enhanced WWVB Atomic Clock Broadcast

Xtendwave, USA

O. Eliezer, T. Jung, R. Lobo, M. Appel, Y. Liang, D. Robbins, P. Nelsen, Z. Islam

RTUIF-3 13:30

Sunday, 1 June 2014

19:00-20:00

Marriott Grand Ballroom Foyer

Round Table Discussion

Beyond 4G Wireless Communications: An RFIC Perspective

Organizer and Moderator:

Hossein Hashemi, Associate Professor, University of Southern California

Participants:



Zdravko Boos
Fellow
Intel



Peter L. Gammel
Chief Technology Officer
Skyworks Solutions



Pieter Hooijmans
Vice President R&D and Strategy
NXP Semiconductors



Lawrence Larson
Dean, School of Engineering
Brown University



Reza Rofougaran
Senior Vice President Engineering & Fellow
Broadcom



Kamal Sahota
Vice President Engineering
Qualcomm

Sunday, 1 June 2014

20:00–21:00

Marriott Grand Ballroom

Monday, 2 June 2014

08:00–09:40

Room TCC 10–11

Session RM01A: Energy-Efficient Wireless Transceivers

Chair: David Wentzloff, University of Michigan

Co-Chair: Gernot Hueber, NXP Semiconductors

RM01A-1 08:00

A 2.3pJ/Bit Frequency-Stable Impulse OOK Transmitter Powered Directly by an RF Energy Harvesting Circuit with -19.5dBm Sensitivity

Hiroyuki Ito¹, Shoichi Masui², Youichi Momiyama², Atsushi Shirane¹, Motohiro Takayasu¹, Yoshihiro Yoneda¹, Taiki Ibe¹, Taisuke Hamada¹, Sho Ikeda¹, Daisuke Yamane¹, Noboru Ishihara¹, Kazuya Masu¹, ¹Tokyo Institute of Technology, Japan, ²Fujitsu Laboratories, Japan

Abstract: The proposed 2.5-GHz-band impulse transmitter technology realizes frequency-stable impulse generation against PVT variation and superior energy-per-bit operation, and it can be powered directly from a -19.5-dBm-sensitivity RF energy harvesting circuit without any regulators that are generally essential to power RF circuits. The transmitter occupies 0.38 mm² in a 65nm CMOS technology. The maximum frequency difference among measured output return-loss peak of 9 chips with 3 different process corners under 0.5 V supply is about 50 MHz without any frequency calibration. Our prototype achieves 1 Mb/s signal transmission under 2.3 μ W power consumption from 0.5 V supply thanks to pulse-level duty cycling operation of maximally digital architecture.

RM01A-2 08:20

A 2.5nJ/Bit Multiband (MBAN & ISM) Transmitter for IEEE 802.15.6 Based on a Hybrid Polyphase-MUX/ILO Based Modulator

Mustafijur Rahman, Mohammad Elbadry, Ramesh Harjani; University of Minnesota, USA

Abstract: This paper describes a 802.15.6 compliant 2360–2484MHz multiband transmitter that digitally multiplexes the appropriate phases from an 800MHz poly-phase filter output to generate $\pi/4$ DQPSK signals at 2.4GHz. Modulation at 1/3rd the RF frequency reduces the transmitter power consumption and enables channel selection using a PLL running at 800MHz. The prototype transmitter consumes 2.4mW while delivering -10dBm RF power at the TX output resulting in an energy efficiency of 2.5nJ/bit at 1.2Mbps. The measured RMS EVM for $\pi/4$ DQPSK modulation is 3.21%.

RM01A-3 08:40

A Low-Power Digitally Controlled Wideband FM Transceiver

N. Saputra¹, John R. Long¹, John J. Pekarik²; ¹Technische Universiteit Delft, The Netherlands, ²IBM, USA

Abstract: A frequency-agile, low-power 3–5GHz FM transceiver with on-chip calibration, and digital control of Rx gain, Tx power, and carrier frequency is described. The FCC-compliant transmitter incorporates a 3-phase CCO and frequency-tripling PA. A tunable LNA, envelope detector, limiter, and FSK demodulator comprise the receiver. Measured Rx sensitivity is -80.5dBm (10⁻³ BER) at 100kb/s.

The 0.9mm² IC fabricated in 90nm RF-CMOS dissipates 630μW in Tx and 580μW in Rx mode from a 1V supply.

RMO1A-4 09:00

A 700pJ/Bit, 2.4GHz, Narrowband, PLL-Free Burst Mode Transmitter Based on an FBAR with 5μs Startup Time for Highly Duty-Cycled Systems

Raghavasimhan Thirunarayanan¹, David Ruffieux², Franz Pengg², Nicola Scolari², Pascal Persechini², Christian Enz¹, ¹EPFL, Switzerland, ²CSEM, Switzerland

Abstract: This paper presents a PLL-free transmitter based on an FBAR achieving a 5μs startup time to reduce the crystal oscillator power overhead which degrades the energy efficiency for heavily duty cycled systems. The TX upconverts a FSK-modulated FBAR DCO signal with the IF output of a Phase Switching Divider (PSD) injection locked to the DCO. The PSD has a division step of 0.2 to circumvent the limited FBAR tuning range that prevents addressing all the channels in the various bands between 2.36 and 2.5 GHz. Integrated in a 65nm technology, the TX outputs -1dBm and consumes 9.2mA at 1.2V. Further, the TX is capable of data rates up to 16 Mbps leading to a peak energy efficiency of 700pJ/b as well as a multi-fold reduction in the mean power dissipation at lower mean data rates.

RMO1A-5 09:20

A 0.5-V 5.8-GHz Ultra-Low-Power RF Transceiver for Wireless Sensor Network in 65nm CMOS

Sho Ikeda, Sang-yeop Lee, Shin Yonezawa, Yiming Fang, Motohiro Takayasu, Taisuke Hamada, Yosuke Ishikawa, Hiroyuki Ito, Noboru Ishihara, Kazuya Masu; Tokyo Institute of Technology, Japan

Abstract: This paper proposes the RF CMOS transceiver that is suitable for wireless sensor network applications. To reduce the size of the antenna, target frequency is chosen to be 5.8GHz band, therefore proposed transceiver has potentiality to achieve ultra-small size wireless sensor module. Supply voltage of 0.5V can reduce the power consumption of overall RF transceiver. Current-reuse VCO and injection-locked frequency divider can enable ultra-low-power consumption of the PLL. In order to achieve both low power and high sensitivity, uncertain-IF and active mixer first architecture of the receiver are employed. Inverter-based topology of the transmitter is suitable for low supply voltage.

The prototype transceiver was fabricated in 65nm CMOS process, and the transmitter achieved EVM of 12.6% while consuming 2.86mW including the PLL, and the receiver realizes sensitivity of -75dBm while consuming 0.83mW including the local oscillator.

Monday, 2 June 2014

08:00–09:40

Room TCC 13–14

Session RM01B: Blocker-Tolerant and Low-Noise Front-Ends

Chair: Domine Leenaerts, NXP Semiconductors

Co-Chair: Frank Henkel, IMST

RM01B-1 08:00

A Noise Cancelling 0.7–3.8GHz Resistive Feedback Receiver Front-End in 65nm CMOS

Anders Nejdell, Markus Törmänen, Henrik Sjöland; Lund University, Sweden

Abstract: This paper presents a noise cancelling 0.7–3.8GHz receiver front-end implemented in 65nm technology. The circuit has a main path consisting of a high input impedance g_m -stage, current-mode passive mixers and baseband amplifiers, where the input match is provided by frequency translational negative feedback from baseband to RF input. An auxiliary path with tunable gain is introduced to cancel noise from the main path while maintaining linearity. The receiver front-end achieves a noise figure of 1.6–3.7dB and an IIP2 and IIP3 of >75dBm and >1dBm, respectively. The current consumption of the circuit is 22.8–34.9mA, from a 1.2V supply.

RM01B-2 08:20

A Blocker-Tolerant RF Front End with Harmonic-Rejecting N-Path Filtering

Yang Xu, Jianxun Zhu, Peter R. Kinget; Columbia University, USA

Abstract: A 0.2–1GHz RF front end with a harmonic-rejecting N-path filter (HR-NPF) features tunable narrow band filtering as well as high attenuation at the 3rd and 5th order LO harmonics at the LNA output. The B1dB-CP is -2.4dBm at a 20MHz offset, and remains high at the 3rd and 5th LO harmonics thanks to the HR-NPF configuration. The reverse isolation of the LNA helps to keep the LO emission below -90dBm. The two-stage harmonic rejection approach offers >51dB harmonic rejection ratio at the 3rd and 5th LO harmonics without calibration. The front end consumes 26–32mA while occupying an area of 0.77mm².

RM01B-3 08:40

An Integrated CMOS Passive Transmitter Leakage Suppression Technique for FDD Radios

Tong Zhang, Apsara Ravish Suvarna, V. Bhagavatula, Jacques C. Rudell; University of Washington, USA

Abstract: An integrated passive transmitter (TX) leakage suppression technique is proposed for FDD Radios. A Four Port Canceller (FPC) serves a dual function as a receiver (RX) input matching network, and provides an auxiliary path from TX to RX, used for leakage cancellation, without degrading the RX noise figure (NF). The FPC is integrated with a low noise amplifier (LNA) and an emulated power amplifier (PA) in 40nm CMOS process. A cancellation of 23dB is achieved with a negligible power consumption and noise penalty.

RM01B-4 09:00**A 2-Stage Recursive Receiver Optimized for Low Flicker Noise Corner**

Rangakrishnan Srinivasan, Wei-Gi Ho, Travis Forbes, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: Multi-frequency signal recursion allows for efficient reuse of transconductance in a radio receiver, which helps to reduce power dissipation. An I-Q receiver based on the recursive principle is demonstrated here. The design employs a self-biased load, with chopping at baseband in order to minimize low-frequency in-band flicker noise. The bias setting of the chopper devices is optimized to enhance the baseband load impedance and conversion gain of the receiver. An implementation in 130 nm CMOS provides 59.6 dB conversion gain for an RF of 960 MHz, and 8.2 dB DSB-NF. The measured flicker noise corner frequency is 100 kHz. The total current requirement is 2.6 mA from a 1.2 V supply.

RM01B-5 09:20**In-situ Noise Characterization of a 20–35GHz 32nm SOI CMOS Reconfigurable LNA Using a Broadband On-Chip Noise Source**

Mohammad Ghadiri-Sadrabadi, Ajay Subramanian, Ahmet H. Coskun, Joseph C. Bardin; University of Massachusetts at Amherst, USA

Abstract: A novel broadband current-mode noise source implemented in 32 nm SOI CMOS and appropriate for the in-situ testing of wide-band mm-wave low noise amplifiers is presented. The noise source was used to characterize a 20–35 GHz low noise amplifier and it was found that the noise source ENR is sufficiently repeatable to enable accurate noise measurements without the individual calibration of each integrated circuit. To the authors' knowledge, this work represents the first time that a CMOS integrated noise source has been used to characterize the noise performance of a mm-wave amplifier.

Monday, 2 June 2014

10:10–11:50

Room TCC 10–11

Session RMO2A: Mixed Signal Circuits at Gigahertz Frequencies

Chair: Jennifer Kitchen, Arizona State University

Co-Chair: Renaldi Winoto, Marvell Semiconductors

RMO2A-1 10:10

A 5th Order 0.8/2.4GHz Programmable Active Band Pass Filter for Power DAC Applications

Zhiwei Xu, Deborah Winklea, Thomas C. Oh, Samuel Kim, Steven T.W. Chen, Yakov Royter, Maggy Lau, Irma Valles, Donald A. Hitko, James C. Li; HRL Laboratories, USA

Abstract: A programmable active band pass filter (BPF) has been designed in a chip-scale heterogeneous integration technology, which intimately integrates InP HBTs on a deep scaled CMOS technology. Therefore, the active BPF can leverage both high performance of InP HBT and high density and programmability of CMOS. The BPF prototype consists of a programmable gain amplifier (PGA), a 5th order BPF core, and a buffer. The BPF center frequency is programmable from 0.8 GHz to 2.4 GHz with 150 MHz pass band and delivers >55 dB out-of-band rejection. Four gain steps: 0, 6, 12, and 16 dB, are enabled by the front PGA to trade off noise and linearity performances. Due to the > 300 GHz f_T of InP HBTs, the BPF core can leverage active-RC architecture for high linearity owing to the close-loop implementation. The prototype occupies 1.5×1.02 mm² area together with pads and draws 106/121 mA from a 3.3 V power supply for 0.8/2.4 GHz bands respectively. In addition, the prototype demonstrates out-of-band OIP₃s of 23.52/23.51 dBm for 0.8/2.4 GHz bands at the high gain mode.

RMO2A-2 10:30

A 6-b UWB Subsampling Track & Hold with 5.5-GHz ERBW in 40nm CMOS

Maarten Strackx¹, Emiliano D'Agostino², Paul Leroux¹, Patrick Reynaert¹; ¹Katholieke Universiteit Leuven, Belgium, ²SCK•CEN, Belgium

Abstract: This paper presents an ultra wideband track and hold (T/H) circuit using direct RF subsampling for radar applications. The circuit enables digitization of the whole received UWB pulse instead of a sole distance measurement used in correlating receivers. In this way, more target information is acquired for further digital processing. Subsampling was applied to achieve a low power consumption of 1.4 mW which includes the T/H core and clock generator. The circuit operates on a rail-to-rail input using the bootstrapping technique. To avoid reliability issues caused by bootstrapping the sampling switch, bulk switching and precharge techniques are introduced. An effective resolution bandwidth of 5.5-GHz was measured with an accuracy of 6-b. The track and hold circuit has been implemented in 40 nm CMOS.

RMO2A-3 10:50

An 8-Bit 100-GS/s Distributed DAC in 28-nm CMOS

Hao Huang, Johannes Heilmeyer, Markus Grözing, Manfred Berroth; Universität Stuttgart, Germany

Abstract: An 8-bit 100-GS/s digital-to-analog converter (DAC) using a distributed output topology in 28-nm low-power CMOS is presented. The ENOB and SFDR ranges from 5.3 bit and 41 dB to 3.2 bit and 27 dB from DC up to 24.9 GHz at 100 GS/s. The -3dB bandwidth is larger than 10 GHz. The 100 GS/s DAC is composed of two 50 GS/s time-interleaved sub-DACs and is operated from two 25 GHz clock signals with a phase shift of 90° . Due to this structure, the output frequency roll-off is comparable to a 50 GS/s DAC while the output frequency image rejection is comparable to a 100 GS/s DAC, easing the output frequency band utilization. With 1-kbyte on-chip memory the DAC can convert 1k symbols cyclically, which is sufficient for characterizing the DAC performance. The DAC consumes 2.5 W from a 1.1V/1.5V/2V power supply. The area of the test chip is 1.5mm^2 .

Monday, 2 June 2014

10:10–11:50

Room TCC 13–14

Session RMO2B: K-Band Front-End ICs

Chair: Danilo Manstretta, University of Pavia

Co-Chair: Li Lin, Marvell Technology Group

RMO2B-1 10:10

A Compact 24–54GHz CMOS Band-Pass Distributed Amplifier for High Fractional Bandwidth Signal Amplification

V. Bhagavatula¹, M. Taghivand², Jacques C. Rudell¹; ¹University of Washington, USA, ²Qualcomm, USA

Abstract: This paper describes a compact 24–54 GHz two-stage band-pass distributed amplifier (BPDA) utilizing dual mirror-symmetric Norton transformations to reduce inductor component values allowing an area-efficient layout. The BPDA, implemented in a 40nm CMOS process, occupies an active area of 0.15mm², has a 77% fractional-bandwidth, an overall gain of 7dB, a minimum in-band IIP₃ of 11dBm, in-band noise-figure less than 6.2dB while consuming 34mA from a 1V supply.

RMO2B-2 10:30

A K-Band 5-Bit Digital Linear Phase Rotator with Folded Transformer Based Ultra-Compact Quadrature Generation

Jong Seok Park, Hua Wang; Georgia Institute of Technology, USA

Abstract: This paper presents a K-band 5-bit vector modulator phase rotator. A fully differential based on a 6-port folded transformer I/Q generation passive network generates the quadrature signals at K-band with low loss, wide bandwidth and high precision, all within an ultra-compact foot-print; this makes the phase rotator design especially suitable for large-scaled high-density phased array systems. Two linear digital VGAs scale the quadrature signals to achieve the desired vector phase interpolation. As a proof-of-concept design, we implement the phase rotator in a SiGe BiCMOS process within a compact chip area of only 310 μm by 380 μm . It achieves -3 dB bandwidth of 6 GHz at the center frequency of 23.5 GHz. The maximum RMS phase error is only 2° for phase interpolation over the full 360° phase span. It consumes 4 mA from 2.5 V and the measured P_{1dB} and IIP₃ are -16 dBm and -5.5 dBm, respectively. Leveraging the dense phase interpolation points to calibrate undesired I/Q mismatch is also demonstrated, which shows the robustness of the design.

RMO2B-3 10:50

K-Band FMCW Radar CMOS Front-End ICs with 13.3dBm Output Power

Gitae Pyo¹, Jaemo Yang¹, Hyunji Ku¹, Choul-Young Kim², Songcheol Hong¹; ¹KAIST, Korea, ²Chungnam National University, Korea

Abstract: This paper presents CMOS front-end ICs with 13.3 dBm output power for K-band FMCW radar, which is integrated in 0.13- μm CMOS technology. The transmitter consists of a voltage controlled oscillator, divider chain, power amplifier, and additional buffers. The receiver consists of a low-noise amplifier, IQ mixers, an IQ generator, and buffers. The leakage problem can be mitigated

by adopting differential topology and ground shielding. As a result, the receiver achieves a conversion gain of 35.7 dB, a P1dB of -31.6 dBm, and a DSB noise figure of 5.5 dB. The transmitter achieves the tuning range of 23.8~24.5 GHz and the phase noise of -104 dBc/Hz @ 1MHz offset. The receiver and transmitter chips consume 121.5 mW and 373.5 mW from a 1.5 V power supply, respectively. Using these two chips, the K-band FMCW radar module is implemented and verified by measuring the distance of an object.

RMO2B-4 11:10

A 10–50GHz True-Time-Delay Phase Shifter with Max 3.9% Delay Variation

Qian Ma, Domine M.W. Leenaerts, R. Mahmoudi; Technische Universiteit Eindhoven, The Netherlands

Abstract: A fully integrated passive True Time Delay (TTD) phase shifter with 32ps continuous changing delay time has been realized in a 0.25 μ m SiGe:C BiCMOS technology. A new TTD architecture is proposed based on broadband matching technique, resulting in less than 4% delay variation over a very large, 10–50GHz frequency span, meanwhile maintaining an input return loss better than 10dB. The measured input 1dB compression point and input IP₃ are +15.5dBm and +24.7dBm at 30GHz, respectively. The phase shifter core occupies less than 0.22mm².

Monday, 2 June 2014

10:10–11:50

Room TCC 15–16

Session RM02C: Advanced PLL Techniques

Chair: Danielle Griffith, Texas Instruments

Co-Chair: Salvatore Levantino, Politecnico di Milano

RM02C-1 10:10

A 9.2–12.7GHz Wideband Fractional-N Subsampling PLL in 28nm CMOS with 280fs RMS Jitter

Kuba Raczkowski, Nereo Markulic, Benjamin Hershberg, Joris Van Driessche, Jan Craninckx; imec, Belgium

Abstract: This paper describes a fractional-N subsampling PLL in 28nm CMOS. Fractional lock is achieved by using a 10bit digital-to-time converter (DTC) that generates a delayed sampling clock with minimal impact on PLL performance. Background calibration guarantees appropriate DTC gain, reducing spurs. The system achieves -38 dBc of integrated phase noise (280 fs RMS jitter) at 10 GHz when a worst-case fractional spur of -43 dBc is present. In-band phase noise is at the level of -104 dBc/Hz. The class-B VCO used can be tuned from 9.2 GHz to 12.7GHz (32%). The total power consumption of the synthesizer, including the VCO, is 13mW from 0.9V and 1.8V supplies.

RM02C-2 10:30

A 0.6/1.2-V 14.1-mW 96.8GHz-to-108.5GHz Transformer-Based PLL with Embedded Phase Shifter in 65-nm CMOS

Yue Chao¹, Howard C. Luong¹, Zhiliang Hong²; ¹HKUST, China, ²Fudan University, China

Abstract: A low-voltage and low-power 96.8–108.5GHz transformer-based PLL is implemented in a 65nm CMOS technology. Consuming only 14.1mW from 0.6V/1.2V supply, the PLL measures phase noise of -84dBc/Hz at 100-kHz offset and -88dBc/Hz at 1-MHz offset from a 99.4GHz carrier while occupying a core chip area of 0.39mm². Moreover, with an embedded phase shifter, the PLL output phase can be shifted by 360° range with an average resolution of 3.9° and amplitude variation less than ±0.1dB.

RM02C-3 10:50

A Fractional-N DPLL with Adaptive Spur Cancellation and Calibration-Free Injection-Locked TDC in 65nm CMOS

Cheng-Ru Ho, Mike Shuo-Wei Chen; University of Southern California, USA

Abstract: A robust and low-cost fractional-N digital phase locked loop (DPLL) architecture is demonstrated via the proposed adaptive spur cancellation schemes and calibration-free time-to-digital converter (TDC). By leveraging the injection locked ring oscillator, the TDC achieves a fine resolution of ~7 ps that automatically tracks the period of digital controlled oscillator (DCO) and hence no TDC gain calibration is required over PVT. To suppress the spurious tones due to external or internal interferences, a gradient-based adaptive spur cancellation scheme is proposed and demonstrated more than 40dB improvement in the lab measurement. The proof-of-concept DPLL

prototype is implemented in 65nm CMOS and synthesizes frequencies between 2.7 to 4.8 GHz with fine frequency resolution of 610 Hz. The measured phase noise is -130dBc/Hz at 3MHz offset and the reference spur achieves -86.45 dBc.

RM02C-4 11:10

A 12GHz 67% Tuning Range 0.37pS RJ_{rms} PLL with LC-VCO Temperature Compensation Scheme in 0.13 μ m CMOS

Yang You¹, Deping Huang¹, Jinghong Chen¹, Sudipto Chakraborty²; ¹Southern Methodist University, USA, ²Texas Instruments, USA

Abstract: This paper presents a PLL designed in 0.13 μ m CMOS for multi-data rate serial link applications. A novel temperature compensation scheme is proposed to reduce the LC-VCO temperature frequency drift without sacrificing the tuning range. Thus, the PLL covers a 5.6GHz to 13.4GHz tuning range by using just two VCO cores while remaining locked from -40°C to 85°C. At 25°C, the PLL has an RMS random jitter (RJ_{rms}) of 0.37pS at 11.44GHz. The integrated jitter is less than 0.7pS over the tuning range and varies less than 50fS over temperature. The PLL consumes 50.88mW of power from a 1.2V supply at 12GHz and 25°C.

RM02C-5 11:30

A 60-GHz Sub-Sampling Frequency Synthesizer Using Sub-Harmonic Injection-Locked Quadrature Oscillators

Teerachot Siriburanon, Tomohiro Ueno, Kento Kimura, Satoshi Kondo, Wei Deng, Kenichi Okada, Akira Matsuzawa; Tokyo Institute of Technology, Japan

Abstract: This paper presents a 60-GHz sub-harmonic injection-locked quadrature frequency synthesizer with sub-sampling operation. This allows the proposed synthesizer to achieve relatively lower in-band phase noise through the use of sub-sampling operation, as well as good out-of-band phase noise through the use of sub-harmonic injection. The proposed synthesizer has been implemented in a standard 65nm CMOS technology. It can support all 60-GHz channels and achieves a phase noise of -115dBc/Hz at 10MHz offset. The sub-sampling operation helps reducing an integrated jitter from 12ps to 2.1ps. It consumes 20.2mW and 14mW from a 20GHz sub-sampling phase-locked loop (SS-PLL) and a quadrature injection-locked oscillator (QILO), respectively.

Monday, 2 June 2014

10:10–11:50

Room TCC 18

Session RM02D: Advancements in Distributive, Thermal, and Non-Linear Device Modeling

Chair: Francis M. Rotella, Peregrine Semiconductor

Co-Chair: Francois Rivet, University of Bordeaux

RM02D-1 10:10

Variable Delay Transmission Lines in Advanced CMOS SOI Technology

Shlomo Shlafman¹, Benny Sheinman¹, Danny Elad¹, Alberto Valdes-Garcia², Mihai A.T. Sanduleanu²; ¹IBM, Israel, ²IBM, USA

Abstract: Variable (Delay) Transmission Lines (VTL) offer digital tuning of fabricated transmission lines to compensate for process variation in active and passive devices of RF silicon design enabling self-healing and post-production circuit tuning. A novel compact semi-analytic single ended VTL model, enabling accurate RFIC circuit level simulation to enhance design flow, was developed. VTL structures were fabricated and measured in IBM 32nm CMOS SOI technology. The 30,50,80 Ohm VTL structures, consisting of metal crossing lines between the signal line and ground plane that are connected to ground through CMOS switches, exhibit over 11%, 15%, 18% delay tuning range respectively with low insertion loss and good agreement between measured results and developed model simulations.

RM02D-2 10:30

Analysis of Tunable Marchand Baluns

Luciano Boglione, Joel Goodman; Naval Research Laboratory, USA

Abstract: The paper tackles the issue of designing tunable Marchand baluns and provides an insight on available approaches for integrating the structure in a semiconductor process. Limitation of the approach and possible solutions are also discussed. The analysis is applied to a Marchand balun fabricated in IBM 8HP SiGe process to demonstrate the feasibility of the approach. A mix of measured and simulated data is used to support the analysis at Q band. State-of-the-art performance is achieved.

RM02D-3 10:50

Self-Heat Modeling of Multi-Finger n-MOSFETs for RF-CMOS Applications

Hitoshi Aoki, Haruo Kobayashi; Gunma University, Japan

Abstract: The purpose of this research is to characterize and model the self-heating effect of multi-finger n-channel MOSFETs. Self-heating effect (SHE) does not need to be analyzed for single-finger bulk CMOS devices. However, it should be considered for multi-finger n-channel MOSFETs that are mainly used for RF-CMOS applications. The SHE mechanism was analyzed based on a two-dimensional device simulator. A compact model, which is a BSIM6 model with additional equations, was developed and implemented in a SPICE simulator with Verilog-A language. Using the proposed model and extracted parameters excellent agreements have been obtained between measurements

and simulations in DC and S-parameter domain whereas the original BSIM6 shows inconsistency between static DC and small signal AC simulations due to the lack of SHE. Unlike the generally-used sub-circuits based SHE models including in BSIMSOI models, the proposed SHE model can converge in large scale circuits.

RM02D-4 11:10

The Thermal Scaling: From Transistor to Array

Tianbing Chen, Tzung-Yin Lee, Justin Allum, Mike McPartlin; Skyworks Solutions, USA

Abstract: The electrical and thermal performance scaling from transistor to array was studied in this paper to help improve the predictive modeling of the electrical-thermal behavior of bipolar arrays. The dc and ac performance scales well at low bias but not to the medium and high bias because thermal resistance does not scale to the total emitter area. It is demonstrated that after the correction of the R_{th} in array models, the simulation can predict the electrical-thermal behavior of power arrays.

RM02D-5 11:30

A Circuit-Level Model for Accurately Modeling 3rd Order Nonlinearity in CMOS Passive Mixers

Hazal Yüksel, Dong Yang, Alyosha C. Molnar; Cornell University, USA

Abstract: Many MOSFET models have discontinuities in the 2nd derivative of their drain current with respect to their drain-source voltage. Because these discontinuities occur at $V_{ds} = 0V$, they have little effect on simulations of active circuits, but matter when simulating transistors in deep triode, such as CMOS passive mixers. These discontinuities result in qualitatively incorrect simulations of the effects of third order nonlinearity, with the 3rd harmonic behaving proportional to the square of the input signal amplitude, A^2 , instead of A^3 . In this paper, we present a schematic-level modeling technique that can be easily implemented over any model that fails the Gummel Symmetry Test (e.g. BSIM4) without altering underlying physical equations. We then show how the model performs with respect to IM3 simulations ensuring correct magnitude and slope by comparing our model to measurements from an 8-phase passive mixer manufactured in a deep sub-micron process.

Monday, 2 June 2014

13:30–15:10

Room TCC 10–11

Session RM03A: Advances in Wireless Mobile ICs

Chair: Andre Hanke, Intel

Co-Chair: Magnus Wiklund, Qualcomm Atheros

RM03A-1 13:30

A HSPA+/WCDMA/EDGE 40nm Modem SoC with Embedded RF Transceiver Supporting RX Diversity

Jon Strange¹, Hsiang-Hui Chang², Paul Muller¹, Walid Ali-Ahmad³, Christophe Beghein¹, Fahd Ben Abdeljelil¹, Wen-Chang Lee², Charles Chiu², Tze Yee Sin³, Ta-Hsin Lin², David Ivory¹, Hao-Tang Shih², Chris Beale¹, Dimitris Nalbantis¹, Ivan S.C. Lu⁴, Chi-Wei Fan², Shao-Hung Lin², Hsin-Hua Chen², Chih-Hao Sun², Li-Shin Lai², Jhy-Rong Chen², Sheng-Jui Huang²; ¹MediaTek, UK, ²MediaTek, Taiwan, ³MediaTek, Singapore, ⁴MediaTek, USA

Abstract: A 40nm CMOS transceiver supports 10 bands of HSPA+ and quad-band GSM/EDGE occupying 6.2mm² of a Modem SoC. The TX supports up to 11Mb/s HSUPA with minimal analog filtering and <35mA battery current DG-09 weighted. Receive diversity with dual cell HSDPA supports up to 42Mb/s downlink. The RX path is inductorless and achieves -111dBm sensitivity using a low power synthesizer with <0.35deg-rms noise. This together with modem based impairment correction achieves >42dB SNR for receive levels >-60dBm.

RM03A-2 13:50

A 65nm 3G Femtocell Multiband Transceiver

Sofoklis Plevridis¹, Kostis Vavelidis¹, Nikos Haralabidis¹, Theodore Georgantas¹, Stamatis Bouras¹, Charalampos Kapnistis¹, Eleni Kytonaki¹, Yiannis Kokolakis¹, Theodoros Chalvatzis¹, Spyros Kavadias¹, Hamed Peyravi¹, Nikos Kanakaris¹, Christos Kokozidis¹, Spyridon Liolis¹, Kosmas Tsilipanos¹, Aris Kyranas¹, Chrysostomos Xesternos¹, Panagiotis Betzios¹, Ilias Bouras¹, Maryam Rofougaran²; ¹Broadcom, Greece, ²Broadcom, USA

Abstract: Last mile residential connectivity and the demand for increased indoor coverage and capacity in 3G cellular systems has led to the commercial introduction of femtocell (Home Node B) base stations. To achieve higher component integration, support additional functionality, and decrease power, there is a need to minimize component count, PCB area and power consumption without sacrificing performance, while also preserving backwards-compatibility with legacy 2G systems. In this paper, we present a 65nm CMOS 3G/HSPA+ femtocell transceiver with 350mW power consumption that eliminates the need for Tx SAW filters. The proposed solution supports 10 TX (Downlink) and 10+10 (Downlink+Uplink) RX UMTS bands from Band I to Band VI and Band VIII to Band XI, quad-band GSM sniffing and GPS band receive capability for soft GPS operation.

RM03A-3 14:10

A Multiband Power Amplifier Using Combination of CMOS and GaAs Technologies for WCDMA Handsets

T. Shimura, S. Maki, S. Fujiwara, K. Fujii, Y. Takahashi, S. Suzuki, M. Miyashita, K. Yamamoto, H. Seki, M. Hieda, Y. Hirano; Mitsubishi Electric Corporation, Japan

Abstract: A multiband power amplifier using combination of CMOS and GaAs technologies (Combo MB PA) which supports quad WCDMA bands (Band V, VIII, II, I) is described. With four chips — two GaAs-HBT chips, a GaAs-HEMT chip, and a CMOS chip — mounted on a $5.5 \times 5 \text{mm}^2$ laminate, the Combo MB PA comprises two amplifier chains and two SPDT HEMT band-select switches, covering 824–915MHz and 1850–1980MHz. Each amplifier chain has switchable signal paths corresponding to dual (high and low) power modes (HPM and LPM) for saving battery current in practical handset use. In the PA, driver stages, RF switches, and their bias- and switch-control circuits are integrated on the CMOS chip for cost reduction. Only the final power stages are fabricated in a GaAs HBT process. Measurements were carried out under the condition of a 3.4V supply voltage and a WCDMA (3GPP R99) modulated signal. Due to optimized broadband matching design, the Combo MB PA achieves a power-added efficiency (PAE) as high as 40% at a Pout of 28dBm over 824–915MHz in the HPM while keeping adjacent channel leakage power ratio (ACLR) less than -39dBc. In the LPM, PAE of 15% at a Pout of 17dBm is obtained with ACLR of less than -40dBc. For 1850–1980MHz, the PA shows 35% PAE with ACLR of less than -37dBc at 28dBm of Pout in the HPM and 14% PAE at 17dBm of Pout in the LPM.

RM03A-4 14:30

Broadband CMOS Stacked Power Amplifier Using Reconfigurable Interstage Network for Envelope Tracking Application

Sunghwan Park, Jung-Lin Woo, Moon-Suk Jeon, Unha Kim, Youngwoo Kwon; Seoul National University, Korea

Abstract: A 2-stage stacked-FET power amplifier with a reconfigurable interstage network is developed for broadband envelope tracking application using SOI CMOS. The wideband PA is based on Class-J mode of operation, where output matching is realized with two-section low-pass network. Miller capacitors are also employed across the FET stack to guarantee Class-J-like operation for inner FET stacks. To overcome the bandwidth limit due to high-Q interstage matching, reconfigurable matching network is employed using SOI switch, allowing dual frequency-mode operation. The fabricated PA shows CW efficiencies in excess of 60% from 0.65 to 1.0 GHz. When operated with an ET supply modulator, overall ET PA system shows W-CDMA efficiencies higher than 50% from 0.68 to 0.92 GHz and LTE efficiencies higher than 40% from 0.65 to 0.95 GHz.

Monday, 2 June 2014

13:30–15:10

Room TCC 13–14

Session RM03B: mm-Wave PAs: 60GHz and Beyond

Chair: Eddie Spears, RFMD

Co-Chair: Kevin Kobayashi, RFMD

RM03B-1 13:30

Spatially Power-Combined W-Band Power Amplifier Using Stacked CMOS

Jefy Jayamon, Ozan Gurbuz, Bassel Hanafi, Amir Agah, James Buckwalter, Gabriel M. Rebeiz, Peter Asbeck; University of California at San Diego, USA

Abstract: A spatially power-combined CMOS SOI power amplifier at 94 GHz is reported. The CMOS chip contains a 2×4 array of pseudo-differential power amplifiers, and is integrated with a microstrip antenna array on a quartz superstrate. A 13-stage amplifier chain is implemented to provide gain, using stacked NFETs in a 45-nm CMOS SOI process. The amplifier array outputs a power of 24 dBm (250 mW) and the chip-quartz assembly radiates an equivalent isotropic radiated power (EIRP) of 33 dBm at 94 GHz. This is the highest radiated power reported from a Silicon CMOS active array transmitter at W-band, and the highest W-band output power from a single CMOS chip.

RM03B-2 13:50

A Dual-Mode Highly Efficient 60GHz Power Amplifier in 65nm CMOS

Payam M. Farahabadi, Kambiz Moez; University of Alberta, Canada

Abstract: This paper presents a 60 GHz power amplifier utilizing a novel technique to achieve high efficiency at high output power levels. The proposed topology provides the capability of dual mode operation. The output power of a conventional class A power amplifier will be combined with the power provided by an amplifier operating at a different class to achieve higher efficiency at higher output levels. Driver stages to provide high power gain consist of an enhanced cascode stage followed by a common source amplifier with transformer-coupled impedance matching networks. Fabricated in 65 nm CMOS process, the measured gain of the 0.32 mm² power amplifier is 17.7 dB at 60 GHz with a wide 3dB band width of 12 GHz while consuming 378 mW from a 1.2V supply. A maximum saturated output power of 16.8 dBm is measured with the 14.5% peak power added efficiency at 60 GHz.

RM03B-3 14:10

A Digitally Modulated 60GHz Polar Transmitter in 40nm CMOS

K. Khalaf¹, V. Vidojkovic¹, K. Vaesen¹, John R. Long², W. Van Thillo¹, Piet Wambacq¹; ¹imec, Belgium, ²Technische Universiteit Delft, The Netherlands

Abstract: A 60GHz polar Tx prototype implemented in 40nm CMOS includes a two-stage PA with an RF-DAC, an I-Q upconversion mixer, a 60GHz LO hybrid and a digital synchronization interface. Saturated output power is approx. 10dBm, while RF output and baseband input bandwidths are 9GHz and 1.2GHz, respectively. The linear RF-DAC resolution is 5 bits. EVM degradation and spectral mask out-of-band distortion appear at input powers higher than 6dB above P_{-1dB}. EVM is -19dB and -16dB

at full rate, and -25.5dB and -22dB at reduced rates for QPSK and 16-QAM signals, respectively. The Tx consumes 75mW from 0.9V, and the core occupies 0.18mm² of the 2.38mm² testchip.

RM03B-4 14:30

A 112–134GHz SiGe Amplifier with Peak Output Power of 120mW

Hsin-Chang Lin, Gabriel M. Rebeiz; University of California at San Diego, USA

Abstract: A fully-integrated 8-way power combining amplifier for 120 GHz application in an advanced 90 nm SiGe HBT technology is presented. The single-ended PA breakout has a small-signal gain of 20 dB and P_{sat} of 12.5–13.8dBm at 114 to 130 GHz. The 8-way power combining PA achieves a small-signal gain of 15 dB and peak P_{sat} of 20–20.8dBm at 114–126GHz with a PAE of 7.6–6.3%. To our knowledge, this is the highest power silicon-based D-band amplifier to-date.

RM03B-5 14:50

E-Band Transformer-Based Doherty Power Amplifier in 40nm CMOS

Ercan Kaymaksut, Dixian Zhao, Patrick Reynaert; Katholieke Universiteit Leuven, Belgium

Abstract: This paper presents an 80 GHz Doherty power amplifier in 40 nm CMOS technology. The amplifier combines 4 push-pull amplifiers by using 2×2 parallel-series combiner. In addition, it employs additional LC impedance matching to enhance the back-off efficiency. The transformer-based Doherty amplifier demonstrates both high linearity and high back-off efficiency. Thus, it is tailored for high PAPR mm-wave applications such as E-band communication. The two stage Doherty power amplifier achieves 16.2 dBm output power at 0.9 V supply with a PAE of 12%. Thanks to the linearization feature of the Doherty topology the 1 dB compression point of the amplifier is as high as 15.2 dBm while the PAE at P_{1dB} is 11.1%.

Monday, 2 June 2014

13:30–15:10

Room TCC 15–16

**Session RM03C: mm-Wave & Terahertz Frequency Generation
Techniques**

Chair: Kamran Entesari, Texas A&M University

Co-Chair: Brian Floyd, NC State University

RM03C-1 13:30

**A 46.4–58.1 GHz Frequency Synthesizer Featuring a 2nd Harmonic
Extraction Technique That Preserves VCO Performance**

Bodhisatwa Sadhu, Mark Ferriss, Alberto Valdes-Garcia; IBM, USA

Abstract: This paper introduces a 2nd harmonic extraction technique in a 46.4–58.1 GHz frequency synthesizer. The frequency doubling approach is based on tapping second harmonic signals at the VCO supply and tail nodes and amplifying them to provide a differential output. Since the amplifiers do not load the VCO outputs, neither the tuning range nor the frequency of the VCO is affected. Moreover, a novel noise bypass technique is utilized to ensure that the amplifiers do not degrade the VCO phase noise. As a result, the frequency synthesizer achieves 22.4% tuning range (46.4–58.1 GHz) and phase noise below -118dBc/Hz while consuming 66mW power from a 1V supply. The synthesizer occupies 0.6mm×1mm in IBM 32SOI CMOS.

RM03C-2 13:50

**An 8th Sub-Harmonic Injection Locked V-Band VCO for Low Power LO
Routing in mm-Wave Beamformers**

Suman P. Sah, Deukhyoun Heo; Washington State University, USA

Abstract: This paper presents an 8th sub-harmonic injection locked V-band oscillator for low power LO routing in mm-wave beamformers. The VCO uses an inductively cross-coupled transformer for transconductance boosting. Injection is carried out through a customized three inductor transformer connected to achieve twice the coupling strength between any two inductors. The V-band sub-harmonic injection-locked oscillator (SILO) is implemented in a standard 0.13 μm BiCMOS process and occupies an active area of 200 μm \times 100 μm . The proposed SILO operates at 0.5 V supply and consumes a total power of 3.72 to 6.57 mW, including the injection source. The SILO shows a free-running tuning range of 17.9% centered at 53.5 GHz. In the injection locking mode, it achieves a minimum locking range of 450 MHz at high band and 1.4 GHz at low band with just -10 dBm input power. The proposed LO routing scheme shows minimum power consumption among state-of-the-art beamformers and thus is the most suitable candidate for LO routing in mm-wave beamformers.

RM03C-3 14:10

235–275GHz (×16) Frequency Multiplier Chains with up to 0dBm Peak Output Power and Low DC Power Consumption

Neelanjan Sarmah¹, Bernd Heinemann², Ullrich R. Pfeiffer¹; ¹Bergische Universität Wuppertal, Germany, ²IHP, Germany

Abstract: Wideband ×16 multiplier chains targeted for high speed communication and radar applications above 200 GHz are presented in this paper. The ×16 topology is based on 4 cascaded Gilbert-cell-based frequency doublers without any hybrids and intermediate drive amplifiers. The low external input frequency (14–17.5 GHz), enables the use of very low-power frequency dividers and also interfacing with commercial synthesisers below 20 GHz. Two versions of the circuit were implemented. Version 1 is a standalone ×16 chain and Version 2 is Version 1 plus wideband 3-stage PA. For Version 1, the measured peak output power is -8.5 dBm at 255 GHz with 40 GHz bandwidth (3 dB) and dc power consumption of 0.3 W. For Version 2, the peak output power is 0 dBm at 245 GHz with 30 GHz bandwidth (3 dB) and 0.7 W dc power consumption. These results are single ended on-wafer measurements without dembedding the 2.5 dB loss due to the output pad and balun. The available differential output power, to drive on-chip components like mixers, antennas etc, is -6 dBm for Version 1 and 2.5 dBm for Version 2. Additionally, break out structures for wideband PAs operating at 240 GHz were characterised. The peak power gain at 240 GHz was 7 and 10 dB for the 3 and 4 stages respectively over a 30 GHz bandwidth. The measured P_{sat} was 5 dBm at 240 GHz.

RM03C-4 14:30

A 5th Subharmonic, Inverter-Based Injection Locked Oscillator with 72–83GHz Locking Range

Qixian Shi¹, Davide Guermandi², Vito Giannini², Piet Wambacq¹; ¹Vrije Universiteit Brussel, Belgium, ²imec, Belgium

Abstract: This paper presents a 79GHz fifth sub-harmonic injection locked oscillator (ILO). Compared to classical ILOs which are based on the nonlinearity of coupling transistors, this work uses inverter chains for input pulse pre-shaping. Thanks to the harmonic rich square wave, the new ILO combines linear and nonlinear mechanisms which widen the locking range. A prototype chip is fabricated in 28nm CMOS technology. A locking range from 72 to 83GHz is measured under -2dBm input power. The total power consumption is 25mW. Besides, a peak detector is implemented to ensure the locked ILO operates near the free-running frequency where the output amplitude is higher.

Monday, 2 June 2014

13:30–15:10

Room TCC 18

**Session RM03D: Advances in Nano-Scale Devices and Novel
Measurement Techniques for RFIC Designs**

Chair: Aditya Gupta, Northrop Grumman

Co-Chair: Fujiang Lin, USTC

RM03D-1 13:30

**mm-Wave Noise Characterization of 40nm CMOS Transistor for up to
67GHz**

Xi Sung Loo¹, Hoang V. Nguyen², Zhihong Liu¹, Johnny Kok Wai Chew¹, Neven Misljenovic², Bryan Hosein², Christos Tsironis², Jen Shuang Wong¹, Wai Heng Chow¹; ¹GLOBALFOUNDRIES, Singapore, ²Focus Microwaves, Canada

Abstract: This noise modelling, characterization and measurement from 0.5 GHz to 67 GHz is reported for the first time in coaxial. RF CMOS devices fabricated on GLOBALFOUNDRIES' 40nm technology are measured with Focus Microwaves noise system for full frequency span of 67 GHz. Experimental results agree well with theoretical and modeling results.

RM03D-2 13:50

A High-Power, Low-Loss W-Band SPDT Switch Using SiGe PIN Diodes

Peter Song, Robert L. Schmid, Ahmet Çağrı Ulusoy, John D. Cressler; Georgia Institute of Technology, USA

Abstract: This paper presents a W-band SPDT switch implemented using PIN diodes in a new 90 nm SiGe BiCMOS technology. The SPDT switch achieves a minimum insertion loss of 1.4 dB and an isolation of 22 dB at 95 GHz, with less than 2 dB insertion loss from 77–134 GHz, and greater than 20 dB isolation from 79–129 GHz. The input and output return losses are greater than 10 dB from 73–133 GHz. By reverse biasing the off-state PIN diodes, the P_{1dB} is larger than +24 dBm. To the authors' best knowledge, these results demonstrate the lowest loss and highest power handling capability achieved by a W-band SPDT switch in any silicon-based technology reported to date.

RM03D-3 14:10

High-Q 3D RF Solenoid Inductors in Glass

Jitae Kim, Ravi Shenoy, Kwan-yu Lai, Jonghae Kim; Qualcomm, USA

Abstract: In this paper, we demonstrate the fabrication and characterization of various 3D solenoid inductors using a glass core substrate. Solenoid inductors were fabricated in glass by drilling through holes in glass and semi-additive copper plating for metallization. This topology is compared to similar solenoid structures in terms of Q-factor performance and inductance density. Inductances of 1.8–4.5nH with $Q \sim 60$ at 1GHz were demonstrated.

RM03D-4 14:30**A Cascade RF Power Sensor Based on GaAs MMIC for Improved Dynamic Range Application**

Zhenxiang Yi, Xiaoping Liao, Zhiqiang Zhang; Southeast University, China

Abstract: In this paper, a novel cascade power sensor with improved dynamic range is proposed. The terminating-type sensor and the coupling-type sensor are designed in series for low and high power detection, respectively. This device is designed and fabricated by GaAs MMIC process and MEMS technology. Impedance matching by increasing the slot width of the CPW transmission line is realized to optimize microwave performance. The measured return loss is close to -28dB and -26dB at 8GHz and 12GHz, respectively. For the incident power of 1mW to 100mW, the terminating-type sensor works and the measured sensitivity is close to 0.095mV/mW, 0.088mV/mW and 0.084mV/mW, at 8GHz, 10GHz and 12GHz, respectively. For the incident power with the improved dynamic range of 100mW to 150mW, the coupling-type sensor is adopted and the sensitivity is 9.2 μ V/mW, 8.6 μ V/mW and 9.0 μ V/mW at 8GHz, 10GHz and 12GHz, respectively.

RM03D-5 14:50**RF Power Transistor Characterization and Testing with Hybrid Harmonic Injection Source and Load Tuners**

Hoang V. Nguyen, Neven Misljenovic, Bryan Hosein; Focus Microwaves, Canada

Abstract: Recent work on hybrid harmonic injection source and load-pull system and tuning algorithm are presented. Measurement of RF power transistor shows a 10% increase in output power at fundamental when input is matched at second harmonic frequency.

Monday, 2 June 2014

15:40–17:20

Room TCC 10–11

Session RM04A: Wireless Connectivity Transceivers and Multi-Standard Digital Transmitters

Chair: Julian Tham, Broadcom

Co-Chair: Yanjie (Jay) Wang, Intel

RM04A-1 15:40

A 55nm CMOS 4-in-1 (11b/g/n, BT, FM, and GPS) Radio-in-a-Package with IPD Front-End Components Directly Connected to Antenna

Jing-Hong Conan Zhan¹, Yuli Hsueh¹, Min Chen¹, Meng-Hsiung Hung¹, Yi-An Li¹, Lan-Chou Cho¹, Hui-Hsien Liu¹, Ming-Da Tsai¹, Ping-Yu Chen¹, Jui-Lin Syu¹, Yi-Chien Tsai¹, Tao-Yao Chang¹, Jen-Che Tsai¹, Sheng-Hao Chen¹, Ping-Hsuan Tsu¹, Kuo-Hao Chen¹, Chun-Yi Wu¹, Sheng Jau Wong², Chun Geik Tan², George Chien³; ¹MediaTek, Taiwan, ²MediaTek, Singapore, ³MediaTek, USA

Abstract: This paper presents a 55nm 4-in-1 (11b/g/n, BT, FM, and GPS) radio assembled side-by-side with a 3-metal layer integrated-passive-device (IPD) chip in a QFN40 package. One 2.4GHz transceiver is area-efficiently shared between WiFi and Bluetooth systems. Including a 3dB IPD insertion loss, at chip output (antenna port) the saturated output power of the 11bgn integrated PA is 25dBm; the receiver noise figure is 6dB and 7dB in WiFi and BT modes, respectively. The shared synthesizer locks to within 4ppm target frequency during WiFi / BT channel switching in less than 23 μ sec. Tracking sensitivity of the GPS receiver and the sensitivity of the FM receiver (including IPD loss) are -162dBm and 2.7dBuVrms, respectively. The IPD chip contains a 2.4GHz WiFi/BT balanced tri-section filter and matching network; a 2.4GHz/1.6GHz diplexer; and a GPS 5th order elliptical filter and its matching network. The radio and IPD die sizes are 3.4mm² and 3.1mm², respectively.

RM04A-2 16:00

A 0.9dB NF 9mW 28nm Triple-Band GNSS Radio Receiver

Matteo Conta¹, Eric Rodal², Seema Anand¹, Henrik Jensen¹, Hu Huang¹, Yu-Wei Lin¹, Zhenhua Liu¹, Franco De Flaviis¹, Kamel Benboudjema¹; ¹Broadcom, USA, ²R2 Semiconductor, USA

Abstract: In order to achieve noise figure smaller than 1dB, the GNSS receivers require external LNA, which adds area, cost and current consumption. A 28nm CMOS sub-1dB NF 9mW GNSS receiver is presented, requiring no external components. This work takes advantage of symmetry in performance between NMOS and PMOS at 28nm node and demonstrates that low NF is possible on advanced CMOS at low power levels, with proper design of on-chip matching components.

RM04A-3 16:20

A 23dBm Fully Digital Transmitter Using $\Sigma\Delta$ and Pulse-Width Modulation for LTE and WLAN Applications in 45nm CMOS

Rahmi Hezar, Lei Ding, Joonhoi Hur, Baher Haroun; Texas Instruments, USA

Abstract: This paper presents a 23 dBm fully digital transmitter designed in a standard 45 nm CMOS process. The digital transmitter replaces the entire analog/RF signal chain in a traditional

transmitter architecture. It utilizes $\Sigma\Delta$ modulation and pulse-width modulation to turn high resolution baseband I and Q signals into switching signals, thereby allowing efficient Class-D PA stages to be used. In addition, cascaded $\Sigma\Delta$ stages and switched-capacitor combining are incorporated into the architecture to reduced out-of-band quantization noise while maintaining good efficiency. The proposed transmitter achieves peak output power of 23 dBm with 47% power added efficiency (PAE). For a OFDM signal with 8.2 dB peak-to-average power ratio (PAR), the PAE is 23%. The linearity of the digital transmitter meets WiFi spectral mask without any digital predistortion.

RM04A-4 16:40

A Digital Centric CMOS RF Transmitter for Multistandard Multiband Applications

Bastian Mohr, Jan Henning Mueller, Ye Zhang, Bjoern Thiel, Renato Negra, Stefan Heinen; RWTH Aachen University, Germany

Abstract: This work presents a digital centric transmitter in a 65 nm CMOS technology. The transmitter contains an RF-DAC frontend, a 3.2 Gbps interface, a fractional resampling pulse shape filter (PSF), LO feedthrough- and IQ-phase/gain-mismatch compensation. The PSF converts the XTAL based baseband clock to the independent LO clock domain. The 9 bit RF-DAC frontend occupies 0.18mm². The SSB sinusoid output power of the transmitter frontend reaches 11.9dBm at 2.4 GHz. The transmitter system fulfills all WLAN requirements at 2.4 GHz ISM band with an output power of 0.5dBm and a power dissipation of 92.6mW. It also enables WCDMA and LTE transmission, resulting in 4.7dBm / 89mW in WCDMA mode and 2.5dBm / 86.7mW in LTE mode respectively. In all cases the proposed design meets all ACLR requirements.

RM04A-5 17:00

A 2×2 MIMO 802.11abgn/ac WLAN SoC with Integrated T/R Switch and On-Chip PA Delivering VHT80 256QAM 17.5dBm in 55nm CMOS

Tsung-Ming Chen¹, Wei-Chia Chan¹, Chien-Cheng Lin¹, Jui-Lin Hsu¹, Wen-Kai Li¹, Pi-An Wu¹, Yen-Lin Huang¹, Yen-Chuan Huang¹, TzungChuen Tsai¹, Po-Yu Chang¹, Chih-Lung Chen¹, Chih-Hou Tsai¹, Tao-Yao Chang¹, I-Ching Huang¹, Wen-Hsien Chiu¹, Chun-Hao Liao¹, Chia-Hsin Wu¹, George Chien²; ¹MediaTek, Taiwan, ²MediaTek, USA

Abstract: This paper describes 2×2 MIMO 802.11ac Stage 1 WiFi + BT combo SoC chip with integrated dual-band PAs, LNAs, T/R switches, as well as a power management unit. The measured RX sensitivity of OFDM54M is -77.5dBm/ -77dBm in 2.4GHz and 5GHz, respectively. With the proposed broadband TX architecture, a high output power of 17.5dBm for 802.11ac Stage 1 VHT80 256QAM was achieved, and is extendable to the upcoming 802.11ac Stage2 VHT160. The maximum throughput achieved is 580Mbps in VHT80 MCS9 two-spatial stream mode, AWGN channel, with short GI. This chip occupies 27.8mm² in 55nm 1P6M CMOS technology in which the MIMO WiFi RF and analog circuits occupies 7.7mm².

Monday, 2 June 2014

15:40–17:20

Room TCC 13–14

Session RMO4B: Highly-Efficient Power Amplifiers

Chair: Jeff Walling, University of Utah

Co-Chair: Nick Cheng, Skyworks Solutions

RMO4B-1 15:40

A 25dBm Outphasing Power Amplifier with Novel Non-Isolated Combining Network

Lei Ding, Joonhoi Hur, Rahmi Hezar, Baher Haroun; Texas Instruments, USA

Abstract: This paper presents a 25 dBm outphasing power amplifier designed in a standard 45 nm CMOS process. Instead of using bulky quarter-wave transmission lines or transformers as non-isolated combiners, we propose a new combiner based on lump elements. The elements of the combiner act differently for in-phase and out-of-phase components, which allows additional resonant networks to be formed for improved backoff efficiency. The proposed PA design achieves 55% peak power added efficiency (PAE) at 900 MHz and 45% at 2.4 GHz. For an OFDM signal with 6 dB PAR, the PAE is 32% at 900 MHz and 22% at 2.4 GHz. The linearity of the PA meets WiFi spec without digital predistortion (DPD). With DPD, the linearity of the PA can be improved further to reach -53 dBc, -50 dBc, -42 dBc ACPR for 10 MHz, 20 MHz, and 2-carrier 20 MHz LTE signals.

RMO4B-2 16:00

A +27.3dBm Transformer-Based Digital Doherty Polar Power Amplifier Fully Integrated in Bulk CMOS

Song Hu¹, Shouhei Kousai², Jong Seok Park¹, Outmane Lemtiri Chlieh¹, Hua Wang¹; ¹Georgia Institute of Technology, USA, ²Toshiba Corporation, Japan

Abstract: This paper presents a digital Doherty polar power amplifier fully integrated in a 65nm bulk CMOS process. It achieves +27.3dBm peak output power and 32.5% peak PA drain efficiency at 3.82GHz and 3.60GHz, respectively. The PA demonstrates a maximum 7% back-off efficiency enhancement compared with a class-B PA and shows a robust Doherty PA operation against load variations. The 90° signal splitting at the Doherty input is realized by a compact folded transformer-based differential quadrature coupler. Active Doherty load modulation and output power combining are achieved by two transformers in a parallel configuration at the PA output. The transformer-based passive networks make the PA design ultra-compact (2.1mm²) and broadband (24.9% for -1dB bandwidth). Measurements with QPSK (1MSym/s)/16QAM (0.5MSym/s) signals show 3.5/4.7% rms EVM with +23.5/+22.1dBm average output power and 26.8/24.1% PA drain efficiency.

RM04B-3 16:20

A 2.4GHz Class-D Power Amplifier with Conduction Angle Calibration for -50dBc Harmonic Emissions

Ao Ba¹, Vamshi Krishna Chillara¹, Yao-Hong Liu¹, Hiromu Kato², Kathleen Philips¹, Robert Bogdan Staszewski³, imec, The Netherlands, ²Renesas Electronics Corporation, Japan, ³Technische Universiteit Delft, The Netherlands

Abstract: We present a digitally-controlled class-D power amplifier (PA) utilizing a new conduction angle calibration technique for harmonic suppression. The optimum conduction angle is derived to minimize chosen harmonics. The calibration circuit adjusts the conduction angle by changing the voltage transfer characteristic of the input buffer. Operating at 2.4GHz, this single-ended PA achieves a drain efficiency of 39% with an output power of 1.2dBm from a 1V supply. The even-order harmonics can be suppressed to below -49dBm. Integrated with an RF frequency modulator, the PA fully meets the spectral mask requirements for Bluetooth Smart applications.

RM04B-4 16:40

Wideband and Efficient Watt-Level SiGe BiCMOS Switching Mode Power Amplifier Using Continuous Class-E Modes Theory

Mustafa Özen¹, Mustafa Acar², Mark P. van der Heijden², Melina Apostolidou², Domine M.W. Leenaerts², Rik Jos², Christian Fager¹; ¹Chalmers University of Technology, Sweden, ²NXP Semiconductors, The Netherlands

Abstract: In this paper, a generic, wide-band switch mode power amplifier (SMPA) design approach is developed based on the continuous class-E modes theory. A watt level, 1.3–2.2 GHz SiGe BiCMOS class-E SMPA is realized for experimental verification. The prototype provides collector efficiencies higher than 70% and output power levels higher than 29 dBm across 1.3–2.2 GHz band, fully confirming the validity of the proposed design approach.

RM04B-5 17:00

A Fully-Integrated 18GHz Class-E Power Amplifier in a 45nm CMOS SOI Technology

Jing-Hwa Chen, Sultan R. Helmi, Alice Yi-Szu Jou, Saeed Mohammadi; Purdue University, USA

Abstract: A fully-integrated Class-E power amplifier (PA) operating at 18 GHz is implemented in a standard 45 nm CMOS SOI technology. The PA is designed using differential Cascode topology with cross-coupled capacitors for Gate-Drain capacitance neutralization. The measured single-ended saturated power (P_{SAT}) under a supply voltage of 2 V is 15.9 dBm (differential P_{SAT} of 18.9 dB) and the 1-dB single-ended compression power (P_{1dB}) is 13.3 dBm, with a peak power added efficiency (PAE) of 41.4%. The Gate-Drain capacitance neutralization technique facilitates the class-E operation and improves the PAE by ~20%.

Monday, 2 June 2014

15:40–17:20

Room TCC 15–16

Session RMO4C: Quadrature and Multi-Mode VCOs

Chair: Jane Gu, University of California at Davis

Co-Chair: Fred Lee, Fairchild Semiconductor

RMO4C-1 15:40

A 26-GHz Low-Phase-Error In-Phase-Coupled QVCO Using Modified Bi-Directional Diodes

Jun-Chau Chien, Nai-Chung Kuo, Ali M. Niknejad; University of California at Berkeley, USA

Abstract: This paper presents a new passive coupling technique for quadrature voltage-controlled oscillator (QVCO) with low phase error. The significance of the coupling devices nonlinearity is emphasized. Based on the phase error analysis, modified bi-directional coupling diodes are proposed with higher third-order nonlinearity while lowering the capacitive loading. The proposed prototype and a standard 26-GHz QVCO are fabricated in 65-nm CMOS for comparison. Measurements confirm that the phase error is reduced from 1.5° to 0.36° . Phase error immunity against LC-tank mismatch is significantly reduced.

RMO4C-2 16:00

Low-Phase-Noise 54GHz Quadrature VCO and 76GHz/90GHz VCOs in 65nm CMOS Process

Tianzuo Xi¹, Shita Guo¹, Ping Gui¹, Jing Zhang², Kenneth K. O², Yanli Fan³, Daquan Huang³, Richard Gu³, Mark Morgan³; ¹Southern Methodist University, USA, ²University of Texas at Dallas, USA, ³Texas Instruments, USA

Abstract: This paper presents new circuit topologies and design techniques for low-phase-noise CMOS mm-Wave Quadrature VCO (QVCO) and VCOs. A transformer coupling with extra phase shift is proposed in QVCO to decouple the tradeoff between phase noise (PN) and phase error and improve the PN performance. This technique is demonstrated in a mm-Wave QVCO with a measured PN of -119.2dBc/Hz at 10MHz offset of a 56.2GHz carrier and a tuning range of 9.1% (FOM_T of -179dBc/Hz). To our best knowledge, this QVCO has the lowest PN at 10MHz offset among all the QVCOs around 50–60GHz frequency range. In addition, an inductive divider feedback technique is proposed in VCO design to improve the transconductance linearity, resulting in larger signal swing and lower PN compared to the conventional LC VCOs. The effectiveness of this approach is demonstrated in a 76GHz VCO and a 90GHz VCO, both fabricated in a 65nm CMOS process, with an FOM_T of 173.6dBc/Hz and 173.1dBc/Hz , respectively.

RM04C-3 16:20

A 57-to-75GHz Dual-Mode Wide-Band Reconfigurable Oscillator in 65nm CMOS

Cheng-Hsien Hung, Ranjit Gharpurey; University of Texas at Austin, USA

Abstract: A dual-mode LC-tank based VCO for mm-wave applications is described. The design employs reconfiguration of the active negative resistance core around the LC tank, in order to provide two oscillation modes. The frequency spacing of the two modes is determined by an inductor ratio. The design is implemented in a 65nm CMOS process, with measured tuning ranges of 56.9 GHz to 65.4 GHz, and 64.6 GHz to 75.3 GHz in the two modes respectively, for a net tuning range of 28%. The oscillator consumes 13 mW from a 1 V supply. The minimum switch size that is required to ensure mode switching is analyzed.

RM04C-4 16:40

A 2.75–6.25GHz Low-Phase-Noise Quadrature VCO Based on a Dual-Mode Ring Resonator in 65nm CMOS

Masoud Moslehi Bajestan, Vahid Dabbagh Rezaei, Kamran Entesari; Texas A&M University, USA

Abstract: This paper presents a low-phase-noise wide-tuning-range quadrature voltage-controlled oscillator (QVCO) using a dual-mode ring resonator. In contrary to the conventional approaches that use transistor-coupled LC oscillators, the proposed resonator inherently provides quadrature signals by employing both magnetic and capacitive couplings in a ring structure, resulting in low phase noise performance and high quadrature accuracy. Additionally, it offers two oscillation modes which are exploited to realize a wide-tuning-range QVCO. The implemented prototype in a 65-nm CMOS process shows 2.75–6.25GHz continuous tuning range, phase noise figure-of-merit (FoM) of 188.2 dB at 3GHz and better than 184dB across the entire operating frequency range, 1.5° maximum phase error while consuming 9.7–15.6mA from 0.6-V supply. The QVCO occupies an active chip area of 0.35mm².

Monday, 2 June 2014

15:40–17:20

Room TCC 18

Session RM04D: High-Speed Data Transceivers

Chair: Mozghan Mansuri, Intel

Co-Chair: Steven Turner, BAE Systems

RM04D-1 15:40

A 25Gbps, 2×-Oversampling CDR Using a Zero-Crossing Linearizing Phase Detector

Zhongkai Wang¹, Rui Bai², Juncheng Wang¹, Xing Jing¹, Qi Nan², Li Sun³, C. Patrick Yue⁴, Zhiliang Hong¹, Patrick Yin Chiang¹; ¹Fudan University, China, ²Oregon State University, USA, ³University of California at Santa Barbara, USA, ⁴HKUST, China

Abstract: A 2×-oversampling 25Gbps clock and data recovery (CDR) circuit is proposed that employs a charge-based, zero-crossing linearizing phase detector (ZCL-PD). This technique linearizes the conventional bang-bang CDR system, resulting in low quantization jitter, improved loop bandwidth, and improved input sensitivity. To minimize the power consumption, an injection-locked inverter-based 1:2 divider reduces CML clocking power while maintaining low jitter. The 65nm-CMOS test-chip measurements demonstrate error-free operation for PRBS-7 and PRBS-31, an 120mV differential input sensitivity, a 9MHz jitter transfer bandwidth, 1.08ps/9.63ps (rms/pk-pk) of recovered clock jitter, and 65mW of power consumption.

RM04D-2 16:00

A 3-mW 25-Gb/s CMOS Transimpedance Amplifier with Fully Integrated Low-Dropout Regulator for 100GbE Systems

Yipeng Wang, Yan Lu, Quan Pan, Zhengxiong Hou, Liang Wu, Wing-Hung Ki, C. Patrick Yue; HKUST, China

Abstract: A novel inverter-based transimpedance amplifier (TIA) employing shunt-shunt inductive feedback and input series peaking is implemented in 65-nm CMOS for 100Gbit Ethernet (100GbE) receivers. The multiple peaking scheme provides an overall bandwidth enhancement ratio of 2.8 to deliver 42-dBΩ of gain up to 24 GHz. To suppress the wideband noise from the TIA power supply and to alleviate the loading effect due to the supply bond-wires, a low-dropout regulator (LDO) with full-spectrum power supply rejection (PSR) of at least -12 dB is co-designed and integrated with the TIA. Measurements at 25 Gb/s show that the data eye RMS and peak-to-peak (P-P) jitters are improved by 15% and 24%, respectively, with the LDO enabled. The measured TIA sensitivity is -7.3 dBm at 25 Gb/s with a BER < 10⁻¹² for a 2¹⁵-1 PRBS optical input. The TIA with LDO consumes 3 mW from a 1.2-V supply.

RM04D-3 16:20**A 23-mW 30-Gb/s Digitally Programmable Limiting Amplifier for 100GbE Optical Receivers**

Zhengxiong Hou, Quan Pan, Yipeng Wang, Liang Wu, C. Patrick Yue; HKUST, China

Abstract: A 30-Gb/s differential limiting amplifier (LA) composed of three cascaded stages is presented. Fabricated in 65-nm CMOS process, the proposed LA yields a typical gain of 31.1 dB and a -3-dB bandwidth of 22.1 GHz while consuming 23 mW from a 1-V supply. The measured gain tuning range is 10 dB with the maximum gain step size less than 1 dB. DC offset cancellation is implemented by a feedback loop consisting of a low-pass filter (LPF) and an amplifier. Optical measurements demonstrate that the degradation in RMS jitter for a 25-Gb/s PRBS due to supply variation from 1 V to 0.9 V can be improved from 37% to 22% using the LA's digital programmability. At 80°C, the RMS jitter can be improved by 16% with the optimal digital control. The core chip area is about 0.12 mm².

RM04D-4 16:40**A 25Gb/s 170μW/Gb/s Optical Receiver in 28nm CMOS for Chip-to-Chip Optical Communication**

Saman Saeedi, Azita Emami; California Institute of Technology, USA

Abstract: A low-power high-speed optical receiver in 28nm CMOS is presented. The design features a novel architecture combining a low-bandwidth TIA front-end, double-sampling technique and dynamic offset modulation. The low-bandwidth TIA increases receiver's sensitivity while adding minimal power overhead. Functionality of the receiver was validated and the design is compared with a conventional 3-stage TIA receiver via actual measurements. The proposed receiver architecture achieves error-free operation (BER<10⁻¹²) at 25Gb/s with energy efficiency of 170fj/b while the conventional receiver achieves error-free operation at 17.1Gb/s with energy efficiency of 260fj/b.

RM04D-5 17:00**A Compact Antenna-in-Package 60-GHz SiGe BiCMOS Radio**

Eric Juntunen, Alex Tomkins, Alan Poon, Jennifer Pham, Ahmed El-Gabaly, Mohammad Fakharzadeh, Hatem Tawfik, Yat-Loong To, Mihai Tazlauanu, Brad Lynch, Ron Glibbery; Peraso Technologies, Canada

Abstract: A small form-factor 60-GHz SiGe BiCMOS radio with two antennas-in-package is presented. The fully-integrated feature-rich transceiver provides a complete RF solution for mobile WiGig/IEEE 802.11ad applications.

Tuesday, 3 June 2014

08:00–09:40

Room TCC 15–16

Session RTU1C: mm-Wave Integration Technologies

Chair: Luciano Boglione, Naval Research Lab

Co-Chair: Georg Boeck, Berlin University of Technology

RTU1C-1 08:00

Dynamic Polarization Control of Integrated Radiators

Steven M. Bowers, Amirreza Safaripour, Ali Hajimiri; California Institute of Technology, USA

Abstract: Dynamic Polarization Control (DPC) ensures polarization matching to the receiving antenna regardless of its polarization or orientation in space. A fully integrated 105.5 GHz 2×1 DPC multi-port driven radiator array with beam steering radiates linear polarization across the full polarization angle range of 0° to 180° maintaining axial ratios above 10 dB, and controls the axial ratio from 2.4 dB (near circular) to 13 dB (linear) in various directions of radiation and a maximum EIRP of 7.8 dBm.

RTU1C-2 08:20

A 64QAM 94GHz CMOS Transmitter SoC with Digitally-Assisted Power Amplifiers and Thru-Silicon Waveguide Power Combiners

Tim LaRocca¹, Yi-Cheng Wu¹, Khanh Thai¹, Rob Snyder¹, Naveen Daftari¹, Owen Fordham¹, Paul Rodgers², Monte Watanabe¹, Yeat Yang¹, Mohammad Ardakani¹, Waleed Namoos¹, Sumiko Poust¹, Mau-Chung Frank Chang³; ¹Northrop Grumman Aerospace Systems, USA, ²Space Micro, USA, ³University of California at Los Angeles, USA

Abstract: A 94GHz 64QAM 1Gbps reconfigurable system-on-chip (SoC) CMOS transmitter with digitally-assisted power amplifiers (DAPA) and back-etched thru silicon waveguide power combiners is presented. The SoC includes a 7M gate ASIC with reconfigurable digital modulation and transmit pre-coding. The ASIC feeds two 10b 1.4GHz current-steering DACs followed by a direct conversion IQ modulator driving eight DAPAs. A 64QAM signal achieves 3.9% EVM with 50dBc ACPR at 94GHz. The data rate is 1.05Gbps and the output power exceeds 10dBm. DC power is 2.1W. The SoC uses IBM 12SOI CMOS.

RTU1C-3 08:40

An F-Band 20.6Gbp/s QPSK Transmitter in 65nm CMOS

Eli Bloch¹, Eran Socher²; ¹Technion, Israel, ²Tel-Aviv University, Israel

Abstract: We hereby report the design and measurements of a 101–118 GHz 65 nm CMOS transmitter. The transmitter architecture is based on a two-step upconversion using a single 80 GHz LO with the quadrature phases generated by injection locked frequency dividers. Both BPSK and QPSK modulations with a maximum data-rate of 20.6 Gbps are supported. A measured output power of -5 dBm at 115 GHz and an error-vector magnitude of 17.5% for 30 dB conversion-loss downconversion link are obtained. The chip core area is 0.21 mm^2 and a DC power consumption of 280 mW.

RTU1C-4 09:00**A 79-GHz Bidirectional Pulse Radar System with Injection-Regenerative Receiver in 65nm CMOS**

Pen-Jui Peng, Chiro Kao, Chin-Yang Wu, Jri Lee; National Taiwan University, Taiwan

Abstract: A 79-GHz fully-integrated bidirectional pulse radar system with injection-regenerative receiver is demonstrated in 65 nm CMOS. The novel design for the impedance transformation of PA/LNA improves the TX efficiency and RX noise figure significantly in comparison with the traditional RF switch. The injection-regenerative oscillator is proposed to increase the receiver gain as well as the system efficiency. The measured TX peak P_{out} and RX conversion gain are 9.2 dBm and 42 dB, respectively. Using an 8×8 patch antenna array with on board matching network to compensate bonding wire effect, the TX EIRP is 25 dBm with the beamwidth of 11.5° and 10° in E and H plane, respectively. The distance measurement for 0.3~1.5 m with the maximum error of less than 7.2 mm. The overall dc consumption is only 107 mW from a single 1.2 V supply under pulse modulation with 0.1% duty cycle.

RTU1C-5 09:20**A 9-pssec Differential Lens-Less Digital-to-Impulse Radiator with a Programmable Delay Line in Silicon**

M. Mahdi Assefzadeh, Aydin Babakhani; Rice University, USA

Abstract: In this paper, a lens-less digital-to-impulse radiator is implemented that radiates impulses with EIRP of 10dBm and a record pulse-width of shorter than 9pssec using an on-chip differential inverted cone antenna. It is shown that the starting time of the radiated impulses can be locked to the edge of the input trigger with high timing accuracy. A digitally programmable delay line is implemented and used at the input of the radiator. The delay line has a resolution step of 150fs and a dynamic range of 400ps. It is shown that by programming the delay line, the starting time of the radiated impulses in the air can be controlled.

Tuesday, 3 June 2014

10:10–11:50

Room TCC 10–11

Session RTU2A: Software-Defined and Cognitive Radio Techniques

Chair: Glenn Chang, MaxLinear

Co-Chair: Ali Afsahi, Broadcom

RTU2A-1 10:10

Dual-Mode 10MHz BW 4.8/6.3mW Reconfigurable Lowpass/Complex Bandpass CT $\Sigma\Delta$ Modulator with 65.8/74.2dB DR for a Zero/Low-IF SDR Receiver

Yang Xu, Zehong Zhang, Baoyong Chi, Qiongbing Liu, Xinwang Zhang, Zhihua Wang; Tsinghua University, China

Abstract: A dual-mode wideband reconfigurable lowpass /complex bandpass continuous-time sigma-delta (LP/CBP CT $\Sigma\Delta$) modulator with digitally-assisting integrated in a zero/ low-IF SDR receiver is presented. The proposed modulator is capable of switching in either 3rd-order LP or 2nd-order CBP with 10MHz bandwidth (BW) in each mode. The power-efficient amplifiers in active-RC integrators are implemented with active feedforward and anti-pole-splitting compensation schemes. The 2-bit digitally-switched current-steering DAC with gate-leakage compensation is proposed to cover the current variation in LP/CBP mode and solve the unavoidable gate-leakage issue in deep submicron CMOS. Fabricated in 65nm CMOS, the modulator achieves 65.8dB DR, 62.2dB peak SNDR in LP 10MHz BW mode and 74.2dB DR, 63.9dB SNDR across 10MHz signal-band with center frequency of 6MHz in CBP mode, occupying a core area of 0.39mm². Powered by a 1.2-V supply, the effective power consumption is only 4.8 and 6.3mW in LP and CBP mode respectively, resulting in measured FoMs of 0.23 and 0.25pj/conversion.

RTU2A-2 10:30

A Dual-Mode, Correlation-Based Spectrum Sensing Receiver for TV White Space Applications Achieving -104dBm Sensitivity

Xiao Xiao, Borivoje Nikolic; University of California at Berkeley, USA

Abstract: A spectrum-sensing receiver targeted at the UHF TV band is implemented in 65nm CMOS. Using known characteristics of the target signal, an efficient architecture employing subsampling downconversion and digital-analog hybrid correlation is implemented to achieve high sensitivity with low power. Fine and coarse detection modes enable both rapid sensing and the detection of very weak signals. For a 6MHz TV band channel, the system achieves -91dBm sensitivity with rapid energy detection, -104dBm sensitivity with correlation, and 84dB of full-scale dynamic range. The chip consumes only 28mW of power.

RTU2A-3 10:50

A Widely Tunable Active Duplexing Transceiver with Same-Channel Concurrent RX/TX and 30dB RX/TX Isolation

Dong Yang, Alyosha C. Molnar; Cornell University, USA

Abstract: We present a widely tunable passive mixer-first duplexing transceiver which employs baseband noise-canceling, duplexing LNAs. The LNAs buffer transmitted signals to the mixer while canceling those signals in receive path. The transmitted signals are up-converted by the same mixer used for receiver down-conversion. The transceiver operates over a frequency range of 0.1–1.5GHz with -18dBm transmitted power. A 33dB linear isolation between receive and transmit (separated by 135kHz) as well as suppression of transmit-induced noise and nonlinearity are achieved.

RTU2A-4 11:10

A 1.8dB NF Blocker-Filtering Noise-Canceling Wideband Receiver with Shared TIA in 40nm CMOS

Hajir Hedayati¹, Wing-Fat Andy Lau², Namsoo Kim², Vladimir Aparin², Kamran Entesari¹; ¹Texas A&M University, USA, ²Qualcomm, USA

Abstract: This paper presents a high performance two-path wideband receiver (RX) for mobile applications. The RX uses an extra gain stage after the LNA to significantly improve the noise figure (NF). Furthermore, different RF and baseband blocker rejection techniques are proposed to significantly improve the linearity of the RX. The blockers are first rejected after the LNA stage through an N-path filter. Then, a novel base-band blocker filtering (BBBBF) technique improves IIP₃ by 7 dB. A dual mixer architecture is also employed to attenuate blockers both before and after the mixer stage. The N-path filter noise is sensed out-of-phase by the main path and cancelled at the inputs of the shared TIA. The RX achieves 1.8 dB NF with 50 dB gain at 2 GHz in 40nm CMOS technology. The RX out-of-band IIP₃ is +5 dBm, which is improved by 20 dB by the proposed techniques, while consuming 36 mW.

RTU2A-5 11:30

A 50MHz–6GHz, 2×2 MIMO, Reconfigurable Architecture, Software-Defined Radio in 130nm CMOS

Behnam Analui¹, Timothy Mercer², Sam Mandegaran¹, Ankush Goel¹, Hossein Hashemi¹; ¹University of Southern California, USA, ²Broadcom, USA

Abstract: A monolithic 50 MHz – 6 GHz software-defined radio transceiver with two transmit (TX) and two receive (RX) channels to support 2×2 MIMO is implemented in 130nm CMOS. The transmitter's and receiver's frequency translation modes are reconfigurable to direct conversion or dual up-down conversion, featuring an on chip Q-enhanced 3 GHz 6-pole Chebyshev IF BPF in the dual conversion mode. The chip also includes two independent integrated wide-band frequency synthesizers for TX and RX paths to support Frequency Division Duplex (FDD) radios. Each frequency synthesizer has an integrated 50 MHz Direct Digital Synthesis (DDS) based reference into an integer-N PLL with integrated 3-tank VCOs, integrated loop-filter, and a zero-spur phase-frequency detector, to achieve low-spur and high resolution, simultaneously. The radio has >0 dBm TX P_{-1dB} and >70 dB RX blocker tolerance (in-band and out of band) with < 900 mW worst case total power consumption per transceiver channel.

Tuesday, 3 June 2014

10:10–11:50

Room TCC 13–14

Session RTU2B: Multiband PAs and Power Mixers

Chair: Leon van den Oever, Radio Semiconductor Corporation

Co-Chair: Joseph Staudinger, Freescale

RTU2B-1 10:10

A Dual Band CMOS Power Amplifier for an S/X Band High Resolution Radar System

Junhyuk Choi, Byungjoon Kim, Duksoo Kim, Jaeyong Ko, Sangwook Nam; Seoul National University, Korea

Abstract: This paper presents a dual band CMOS power amplifier (PA) for an S/X band high resolution radar system. Reconfigurable band-switchable matching networks and a dual band Wilkinson power combiner (impedance transformer) are used for an output matching network. The PA is fabricated using a UMC 0.13 μm CMOS process. It provides a saturated output power of 24.8 dBm and 25.3 dBm with the power-added-efficiency (PAE) of 27.2% and 36.4% at 8.4 GHz and 3.0 GHz, respectively. The 3-dB bandwidth is 2.5 GHz (7.4–9.9 GHz) and 2.3 GHz (2.7–5.0 GHz). This amplifier achieves a fractional bandwidth of 29% and 60% at each band, and shows suitable performance for use in a high resolution radar system.

RTU2B-2 10:30

A 9.5–18.5GHz Power Amplifier for Multi-Band Microwave Point-to-Point Backhaul Communication

Kefeng Han¹, Xun Luo²; ¹Huawei Technologies, China, ²Technische Universiteit Delft, The Netherlands

Abstract: A 9.5–18.5 GHz differential power amplifier (PA) with high linearity and low noise is proposed for multi-band microwave point-to-point (P2P) backhaul communication. Based on the emitter-degenerated hybrid cascode structure, input matching bandwidth is maximized without tuning. A high- f_T NPNs ($BV_{CEO}=1.8\text{V}$) with high breakdown (HB) NPNs hybrid cascode is utilized with a supply of 4.5V. A tunable broadside-coupled transformer with 2-bit switch-capacitor array is introduced to cover a wideband frequency range to meet the multi-band P2P standard. Then, the proposed PA is verified in IBM 8HP SiGe BiCMOS process. The PA shows the following measurements with merits: maximum gain of 8.6 dB (i.e., one-stage), OIP3 more than 29.3 dBm, noise figure less than 6 dB, and OP1dB greater than 19 dBm, total current of 98mA.

RTU2B-3 10:50**A 19.1dBm Segmented Power-Mixer Based Multi-Gbps mm-Wave Transmitter in 32nm SOI CMOS**

Kaushik Dasgupta, Kaushik Sengupta, Alex Pai, Ali Hajimiri; California Institute of Technology, USA

Abstract: A high-power, fully-integrated, mm-wave power mixer based transmitter capable of generating high-speed, complex non-constant envelope modulations is implemented in a 32nm SOI CMOS process. Segmented power generation approach is shown to be suitable for direct digital modulation as well as efficiency improvement at back-off power levels. The transmitter has a peak output power of 19.1dBm at 51GHz with a drain efficiency of 14.2% and a peak PAE of 10.1%. Measurements results show high-speed modulations for BPSK, QPSK, ASK, m-ASK and 16-QAM. Reliability of the transmitter has also been verified against worst case segmentation at 30% higher supply voltage.

RTU2B-4 11:10**A 200GHz Power Mixer in 130nm-CMOS Employing Nonlinearity Engineering**

Jahnvi Sharma, Tolga Dinc, Harish Krishnaswamy; Columbia University, USA

Abstract: CMOS high-mm-wave/sub-mm-wave sources leverage device nonlinearity, either in oscillators or frequency multipliers, to generate harmonics beyond the technology f_{\max} . We propose a power mixer topology that exploits nonlinearity engineering to enhance the output harmonic content. By engineering the amplitude and phase of the fundamental and second-harmonic content in the mixer device voltage waveforms, the output third harmonic power is enhanced significantly beyond that achievable in conventional frequency triplers. A 200GHz power mixer in 130nm CMOS generates 50 μ W of output power at a frequency 1.5 \times higher than f_{\max} .

Tuesday, 3 June 2014

10:10–11:50

Room TCC 15–16

Session RTU2C: Sub-mm-Wave Transceivers

Chair: Mona Hella, RPI

Co-Chair: Didier Belot, STMicroelectronics

RTU2C-1 10:10

A 240GHz Wideband QPSK Transmitter in 65nm CMOS

Shinwon Kang, Siva V. Thyagarajan, Ali M. Niknejad; University of California at Berkeley, USA

Abstract: This paper demonstrates a 240GHz wideband QPSK transmitter in 65nm bulk CMOS. The proposed transmitter employs an 80GHz local oscillator, a quadrature differential hybrid, and a QPSK modulator. Additionally, an 80GHz class-E switching power amplifier is used to efficiently boost the phase-modulated wideband signal. A frequency tripler then regenerates the modulated signal at 240GHz while preserving the QPSK constellation. By using on-chip slotted loop antennas, the transmitter achieves an EIRP of 1dBm. A maximum data rate of 16Gbps is achieved with a total power consumption of 220mW.

RTU2C-2 10:30

A 240GHz Wideband QPSK Receiver in 65nm CMOS

Siva V. Thyagarajan, Shinwon Kang, Ali M. Niknejad; University of California at Berkeley, USA

Abstract: This paper demonstrates a 240GHz wideband QPSK receiver in 65nm bulk CMOS. A direct-conversion mixer-first architecture is implemented with a 240GHz on-chip antenna. Wideband passive mixers at the front end employ a 240GHz LO and convert the received signal down to baseband. The baseband signal is then amplified using high gain, wide bandwidth amplifiers. The 240GHz LO chain consists of 27GHz/80GHz injection-locked oscillators, 80GHz amplifiers and a frequency tripler. The overall receiver gain is 25dB and the noise figure is 15dB from measurements. This receiver design achieves a data rate of 16Gbps with a power consumption of 260mW.

RTU2C-3 10:50

A 314GHz, Fully-Integrated SiGe Transmitter and Receiver with Integrated Antenna

Saeed Zeinolabedinzadeh¹, Mehmet Kaynak², Wasif Khan¹, Mahmoud Kamarei³, Bernd Tillack², John Papapolymerou¹, John D. Cressler¹; ¹Georgia Institute of Technology, USA, ²IHP, Germany, ³University of Tehran, Iran

Abstract: We present a 314 GHz transmitter and receiver chipset which is implemented in an advanced SiGe HBT platform, and which has on-chip antennas. The transmitter uses an active antenna structure, where the generated on-chip signal is directly fed into the antenna. The receiver consists of a novel sub-harmonic resistive mixer with an on-chip high-power differential signal source feeding the LO port. A test link which directly connects the transmitter to the receiver was also implemented as a reference for characterization. This reference circuit enables a simple and accurate measurement method for conversion loss and antenna gain by omitting external high

frequency signal sources. To further facilitate the characterization, the utilized on-chip signals were implemented and tested separately as well. The receiver achieves 22.5 dB conversion loss and the transmitter generates a signal power of -8 dBm at 314 GHz. On-die end-fire antennas were designed for both transmit and receive paths, and utilize a substrate etching technology to boost performance. This work demonstrates the feasibility of fully-integrated and compact sub-mmW transceiver implementations using SiGe technology.

RTU2C-4 11:10

A 155GHz 20Gbit/s QPSK Transceiver in 45nm CMOS

Y. Yang¹, S. Zahir¹, Hsin-Chang Lin¹, O. Inac², W. Shin³, Gabriel M. Rebeiz¹; ¹University of California at San Diego, USA, ²Intel, USA, ³Qualcomm, USA

Abstract: This paper presents a 155 GHz 20 Gbit/s quadrature phase-shift-keying (QPSK) transceiver front-end with modulator, demodulator, LO chain and an option for external LO feed. The transceiver can achieve a bit error rate (BER) $< 10^{-12}$ for an 19 Gbit/s $2^{31}-1$ pseudorandom binary sequence data at a received power of -20 dBm. The size of the chip is $2.8 \times 1.4 \text{ mm}^2$ and consumes 345 mW with the on-chip LO (290 mW without the on-chip LO). To our knowledge, this is the first demonstration of a single-chip QPSK transceiver in CMOS at frequencies above 100 GHz.

RTU2C-5 11:30

An Integrated Traveling-Wave Slot Radiator

Steven M. Bowers, Amirreza Safaripour, Ali Hajimiri; California Institute of Technology, USA

Abstract: A traveling-wave integrated slot radiator is designed using electromagnetic duality theory based off of the ring portion of a radial multi-port driven radiator to minimize the area required exclusively for the antenna. It is designed in 32 nm SOI CMOS and driven by a buffered quadrature VCO at 4 points to create the traveling wave that radiates out of the backside of the chip. It is measured to have a maximum EIRP of 6.0 dBm at 134.5 GHz with a total radiated power of -1.7 dBm while drawing 168 mW DC power.

Tuesday, 3 June 2014

13:30–16:00

Room TCC Ballroom C–D

Session RTUIF: Interactive Forum

Chair: Freek Van Straten, NXP Semiconductors

Co-Chair: Jennifer Kitchen, Arizona State University

RTUIF-1 13:30

A Low Power and High Linearity Dual Path Up-Down Converter for Wireless Telecommunication Repeater System

Hyo-Bin Jung¹, Won-Jae Jung¹, Se-mi Lim¹, Sung-woo Lim¹, Ji-hoon Lee¹, Kyu-Hyun Nam¹, Nam-Pyo Hong², Jong-Eun Jang², Jun-Seok Park¹; ¹Kookmin University, Korea, ²EPIC Solution, Korea

Abstract: This paper proposes low power and high linearity up-down frequency converter for wireless telecommunication repeaters. A wireless telecommunication repeater is typically required high linearity and certain system dynamic range for automatic gain control (AGC). Furthermore, the demand of low power repeaters is increasing recently for green IT purpose. Capacitor cross-couple and threshold voltage decreasing techniques are applied to each sub building block in order to achieve the lowest power consumption and the highest linearity in a given technology and power supply voltage. Also, an ultra-low power wake-up receiver is implemented to control the shut-down when no user exists in the repeaters' connection range. One path of the converter is composed of a wideband down-converting mixer, programmable gain amplifiers (PGA), and a wideband up-converting mixer. The total power consumption is 150mA at 3.3V power supply. The output IP_{3s} of the down-converting mixer and the up-converting mixer are 38dBm at 3dBm two tones output power and 25dBm at -10dBm two tones output power, respectively. The total dynamic gain range is more than 43dB with 1dB step resolution. Furthermore, 3mA wake-up receiver is designed and implemented. The up-down converter is fabricated on a 0.35 μ m SiGe Bipolar CMOS technology.

RTUIF-2 13:30

A 17-mW 5-Gb/s 60-GHz CMOS Transmitter with Efficiency-Enhanced On-Chip Antenna

Rui Wu¹, Wei Deng¹, Shinji Sato¹, Takuichi Hirano¹, Ning Li¹, Takeshi Inoue², Hitoshi Sakane², Kenichi Okada¹, Akira Matsuzawa¹; ¹Tokyo Institute of Technology, Japan, ²S.H.I. Examination & Inspection, Japan

Abstract: A 60-GHz CMOS transmitter with on-chip antenna for high-speed short-range wireless interconnection is presented. The radiation efficiency of the on-chip antenna is doubled using substrate loss improvement techniques. The transmitter fabricated in a 65-nm CMOS process achieves over 5 Gb/s data rate with an EVM performance of -12 dB for BPSK modulation. The whole transmitter consumes 17mW from a 1.2-V supply and occupies a core area of 0.64mm² including the on-chip antenna.

RTUIF-3 13:30**A Multi-Mode Software-Defined CMOS BPSK Receiver SoC for the Newly Enhanced WWVB Atomic Clock Broadcast**

O. Eliezer, T. Jung, R. Lobo, M. Appel, Y. Liang, D. Robbins, P. Nelsen, Z. Islam; Xtendwave, USA

Abstract: The first receiver system-on-chip (SoC) for the newly enhanced phase-modulation based WWVB broadcast is presented. Having an extensively digital architecture, and relying on the new features of the broadcast, it demonstrates 2–3 orders of receiver sensitivity superiority when compared to receiver ICs designed for the legacy WWVB broadcast. To allow for robust reception at very low signal levels, as well as in proximity to the station, it accommodates a dynamic range of over 130dB, representing the widest dynamic range found in any consumer-market receiver IC. The SoC is implemented in a 180nm CMOS process and has a die size of about 7mm².

RTUIF-4 13:30**Design and Implementation of an Analog Front-End Circuit for Semi-Passive HF RFID Tag**

Xuecheng Zou¹, Huan Lin¹, Hui Lin², Dongsheng Liu¹, Liang Guo¹, Ke Yao¹; ¹HUST, China, ²WUT, China

Abstract: This paper presents an analog front-end circuit for semi-passive HF RFID tag compatible to ISO/IEC 14443 Type A. System architecture is constructed. The proposed AFE has realized much longer recognition distance than passive tags and can work normally when the magnetic field is 0.3A/m. It was fabricated with HHNEC 0.13 μ m 1P4M CMOS technology with its layout area of 416 μ m \times 472 μ m. Measurement results show that this AFE can successfully demodulate the 100% ASK modulated signal and the index of the subcarrier modulation can achieve as high as 16.4%. Its power consumption is as low as 129.6 μ W. This chip met the demands of an HF semi-passive tag and made it possible to implant the temperature sensor in the tag.

RTUIF-5 13:30**A UHF-Band RFID Transmitter with Spur Reduction Technique Using a DLL-Based Spread-Spectrum Clock Generator**

Seungjin Kim¹, In-Young Lee¹, Sang-Sung Lee¹, Min Su Kil², Jeongki Choi², Jinho Ko², Sang-Gug Lee¹; ¹KAIST, Korea, ²PHYCHIPS, Korea

Abstract: This paper presents a UHF-band RFID transmitter with a robust spur reduction technique using a DLL-based SSCG. By adopting an 8-bit DLL and Hershey-kiss modulated profile together, the SSCG shows more than a 20dB EMI reduction while providing up-, down-, and center-spread modes. Implemented in a 0.18 μ m CMOS process, the proposed transmitter achieves < -80dBc spur suppression with 25dBm transmit power at 920MHz, which complies with the most stringent regulatory spectral mask without a SAW-filter.

RTUIF-6 13:30

A Fully Integrated 5.9GHz RF Frontend in 0.25 μ m GaN-on-SiC for Vehicle-to-Vehicle Applications

Pilsoon Choi¹, Sushmit Goswami¹, Chirn Chye Boon², Li-Shiuan Peh¹, Hae-Seung Lee¹; ¹MIT, USA, ²Nanyang Technological University, Singapore

Abstract: This paper presents the design of a high-efficiency and high-power RF frontend for the 802.11p standard, leveraging an embedded Tx/Rx switching scheme and a dual-bias power amplifier (PA) linearization technique. The fully integrated RF frontend is fabricated in 0.25 μ m GaN-on-SiC technology and occupies 2mm \times 1.2mm. In the Tx mode, the PA+Tx switch achieves 48.5% drain efficiency at 33.9dBm Psat with 28V supply. With OFDM-modulated signals, it achieves 30% average efficiency at 27.8dBm output power while meeting the -25dB EVM limit without predistortion. In the Rx mode, the LNA+Rx switch achieves +22dBm OIP₃ with 8dB power gain at 12V supply. The fully integrated high-efficiency and linear RF frontend is demonstrated at high output power for vehicular communications for the first time.

RTUIF-7 13:30

A Low Power 8th Sub-Harmonic Injection Locked Receiver for mm-Wave Beamforming Applications

Suman P. Sah, Pawan Agarwal, Deukhyoun Heo; Washington State University, USA

Abstract: This paper presents a single element V-band low power 8th sub-harmonic injection locked beamforming receiver. A significant savings in local oscillator (LO) routing power is achieved by using an 8th sub-harmonic injection locked oscillator (SILO) for frequency multiplication and phase-shifting. Power consumption of the LNA and mixer is lowered by means of transformer feedback techniques. The proposed receiver is implemented in a standard 0.13 μ m BiCMOS process and occupies an active area of only 630 μ m \times 400 μ m. The receiver consumes a minimum power of 11.4 mW and achieves a peak gain of 8.3 dB, IP_{1dB} of -33.5 dBm, minimum NF of 7.7 dB and an IF bandwidth of larger than 11 GHz. A total phase-shift of 144 $^\circ$ is measured. The proposed LO routing and phase-shifting scheme shows minimum power consumption among state-of-the-art receivers and is easily scalable to multiple elements.

RTUIF-8 13:30

A D-Band Transceiver Front-End for Broadband Applications in a 0.35 μ m SiGe Bipolar Technology

Abhiram Chakraborty¹, Saverio Trotta¹, Johann Wuertele¹, Robert Weigel²; ¹Infineon Technologies, Germany, ²FAU Erlangen-Nürnberg, Germany

Abstract: This paper presents a D-band transceiver front-end with twin quadrature receivers fabricated in a low cost 0.35 μ m SiGe bipolar production technology, featuring HBTs with f_{ν}/f_{\max} of 200/250 GHz. The receiver achieves a minimum single-sideband noise figure of 14 dB, conversion gain greater than 23 dB and an input-referred 1-dB compression point of -9 dBm, at an IF of 10 MHz for input signals between 121–126 GHz. A three stage LO buffer amplifier in the receiver allows operation with LO power as low as -10 dBm. The measured amplitude and phase imbalance at 122 GHz are 1 dB and 6 deg respectively. The transmitter can be tuned from 112 GHz to 140 GHz and delivers a maximum output power of -2.5 dBm. The measured phase noise at 1 MHz offset is -102

dBc/Hz at 140 GHz. The maximum suppression of the V-band signal at the transmitter output is better than -25 dBc. The chip consumes 300 mA from a 3.3 V power supply.

RTUIF-9 13:30

A 0.5–6GHz 25.6dBm Fully Integrated Digital Power Amplifier in 65nm CMOS

Hongrui Wang, Hossein Hashemi; University of Southern California, USA

Abstract: This paper presents a 0.5–6GHz fully-integrated Digital Power Amplifier (DPA) in 65nm CMOS technology. Transformer-based class-E/F power amplifiers with zero-voltage switching are designed to achieve high power and high efficiency across a wide frequency band. A Single-Pole Triple-Throw (SP3T) switch featuring low insertion loss and high isolation is implemented to select the output of one of the three sub-band DPAs covering approximately 0.5–1.3GHz, 1.3–3.2GHz, and 3.2–6GHz, respectively. Measurement results show a peak output power of 25.6–22.8dBm with a peak drain efficiency of 34%–20% across 0.5–6GHz.

RTUIF-10 13:30

A Watt-Level 2.4GHz RF I/Q Power DAC Transmitter with Integrated Mixed-Domain FIR Filtering of Quantization Noise in 65nm CMOS

Ritesh Bhat, Harish Krishnaswamy; Columbia University, USA

Abstract: This paper presents an S-band RF I/Q power DAC transmitter with embedded mixed-domain finite-impulse-response (FIR) filter to suppress out-of-band (OOB) quantization noise for FDD/co-existence. Watt-level output power and low output OOB noise level is achieved through (1) power combining (2) device stacking with thick oxide devices in a switching-class power amplifier (PA) and (3) embedded RF FIR filtering. To combat the strong conductance-to-amplitude/ phase nonlinearity of switching-class digital PAs, a transformer-based FIR architecture is proposed that ensures completion of filtering after the nonlinearity. Implemented in 65 nm CMOS, the transmitter has a measured peak output power of 29.1 dBm with 42% system efficiency at 2.25 GHz. The measured noise floor at 100 MHz offset from the 2.4 GHz carrier is -134 dBc/Hz for a 20 MHz 64-QAM signal at 200 MSa/s including 8 dB noise floor suppression from transformer-based two-tap third-order FIR filtering, yielding an ENOB of 8.18.

RTUIF-11 13:30

Design Strategy for High Performance 60GHz CMOS Power Amplifiers

Amin Hamidian, Andrea Malignaggi, Georg Boeck; Technische Universität Berlin, Germany

Abstract: This paper presents a systematic design procedure for compact and high performance mm-wave power amplifiers based on distributed-transformers. For this purpose scalable models for on-chip transformers and power combiners are introduced. The developed scalable models helped achieving a much faster design reiteration time and higher performances for the power amplifier. Finally, using these models a 60 GHz CMOS power amplifier has been designed. The measured results of the power amplifier show 17 dB gain, 18 dBm saturated output power, 15 dBm output power at 1 dB compression point with 0.5 mm² chip size.

RTUIF-12 13:30**Voltage Controlled Oscillator Area Reduction in Nano-Scale CMOS**

Amit Jha¹, Ken Liao², Geoffrey Yeap², Kenneth K. O¹; ¹University of Texas at Dallas, USA, ²Qualcomm, USA

Abstract: A 4.3–5.6 GHz (26% tuning range) voltage controlled oscillator (VCO) incorporating MOS bypass capacitors, MOS varactors, cross-coupled transistors, a current source and buffers underneath an inductor is demonstrated in 65-nm CMOS. Use of a simple inverter based buffer enables straightforward placement under an inductor. The bypass capacitors and other components are used to form a patterned ground shield that improves inductor Q. The measured phase noise of the VCO is -117dBc/Hz at 1 MHz offset from a 4.3GHz carrier. The VCO power consumption is 4 mW. The circuit occupies an area of 14,400 μm^2 , and exhibits FOM_A and FOM_{TA} of -202 and -210 dB, respectively. The FOM_{TA} is at least 10 dB better than the others in the literature. The area is $\sim 3X$ smaller compared to that of the VCO with all the components outside of the inductor.

RTUIF-13 13:30**Impact of Non-Quasi-Static Effects on $1/f^3$ Phase Noise in a 1.9-to-2.6GHz Oscillator**

Federico Pepe, Andrea Bonfanti, Salvatore Levantino, Andrea L. Lacaita; Politecnico di Milano, Italy

Abstract: This work provides a comprehensive discussion of flicker noise up-conversion in current-biased oscillators. It is shown that the excess phase noise mostly arises from an AM-to-PM conversion due to the presence of a large capacitance at the tail node. During the study, a significant discrepancy has also emerged between measurements and simulations. A first attempt to explain this discrepancy is proposed, which takes into account the distributed nature of the flicker-noise source in the switching transistor pair.

RTUIF-14 13:30**A 1.6GHz/4.8GHz Dual-Band CMOS Fractional-N Frequency Synthesizer for S-Band Radio Applications**

Masoud Moslehi Bajestan, Eugene Foli, Hajir Hedayati, Kamran Entesari; Texas A&M University, USA

Abstract: A 1.6GHz/ 4.8GHz fractional-N frequency synthesizer in 0.18- μm CMOS technology is presented in this paper. Its purpose is to generate the local oscillator (LO) signals for a fully integrated S-Band transceiver with a direct-conversion receiver (RX) and a dual up-conversion transmitter (TX) to avoid the frequency pulling problem. The synthesizer achieves phase noise of -141.3dBc/Hz at 1.62GHz and -132.6dBc/Hz at 4.86GHz (both at 3MHz offset), with reference spurs $< -70.2\text{dBc}$ for the lower band (LB) and $< -63.8\text{dBc}$ for the higher band (HB). Total power consumption is 18.2–22.7mW from a 1V supply for the VCO and 1.8V for the other synthesizer blocks.

RTUIF-15 **13:30****An RF Instantaneous-Hop Frequency Synthesizer Based on a Zero-Initial-Phase-Error Multi-Modulus Divider**

Tsung-Hao Chuang, Harish Krishnaswamy; Columbia University, USA

Abstract: In this paper, we propose an instantaneous-hop frequency synthesizer based on a zero-initial-phase-error multi-modulus divider that breaks the fundamental trade-off between hopping time, spectral purity and frequency resolution. In the proposed synthesizer, initial frequency error and phase error at the instant of hop are virtually eliminated through frequency presetting in the high-resolution voltage-controlled oscillator (VCO) and the proposed zero-initial-phase-error divider. This eliminates the acquisition process and enables “instantaneous hops” to within a frequency error that is only limited by the resolution of digital control. An IC prototype is implemented and fabricated in a standard 65nm CMOS technology. The implemented frequency synthesizer operates over 4–5.84 GHz with three discrete divider ratios (80, 88, 96) and achieves instantaneous hops to within an average of 3.64 MHz of the desired output frequency. The prototype dissipates 16.8 mW from 1.2V power supply.

RTUIF-16 **13:30****Variation-Aware X-Topology Architecture with Local Ground References for Broadband Characterization of Passives**

Farooq Mukhtar¹, Johannes A. Russer¹, Sidina Wane², Damienne Bajon³, An-Yu Kuo⁴, Peter Russer¹; ¹Technische Universität München, Germany, ²NXP Semiconductors, France, ³ISAE, France, ⁴Cadence Design Systems, USA

Abstract: X-Topology architecture accounting for distributed floating local ground references is proposed for variation-aware design and characterization of passives. The ability of the proposed solution to map physical design parameters into broadband physics-based equivalent circuit model extraction is demonstrated based on design of low-loss integrated coplanar strip (CPS) lines on anisotropic DTI (Deep-Trench Insulator) patterning realized in advanced SiGe BiCMOS technology. Perspectives for use of X-topology in enabling Q-controllable components with compact broadband equivalent circuit representation fully scalable with respect to the device geometry and architecture are drawn.

RTUIF-17 **13:30****Analysis of Crosstalk Delay Using Mixed CNT Bundle Based Through Silicon Vias**

Manoj Kumar Majumder, Archana Kumari, B.K. Kaushik, S.K. Manhas; IIT Roorkee, India

Abstract: This research paper presents a new method to reduce crosstalk of carbon nanotube (CNT) bundle based through silicon vias (TSVs). For this, a unique structure of mixed CNT bundled (MCB) TSV is proposed with specific arrangement of single- (SWCNT) and multi-walled CNTs (MWCNTs). An equivalent electrical model is presented for different MCB configurations wherein MWCNTs are placed at peripheral layers to the centrally located SWCNTs. A significant reduction in crosstalk induced delay is observed for higher number of peripheral layers containing MWCNTs. For different TSV heights, the overall reduction in crosstalk induced delay is 44.03% using novel MCB instead of conventional SWCNT bundle.

RTUIF-18 **13:30**

On the Reliability of SiGe HBT Cascode Driver Amplifiers

Michael A. Oakley, Brian Wier, Uppili S. Raghunathan, Partha S. Chakraborty, John D. Cressler;
Georgia Institute of Technology, USA

Abstract: This paper investigates the RF reliability of SiGe HBT cascode driver amplifiers. By subtracting capacitive currents internal to the common-base device from its collector waveform, a more accurate depiction of electrical stress in the I-V plane is achieved, and from this revised load line, RF stress data is better correlated to DC stress data. This novel analysis technique provides a framework for designers to simulate the effects of RF stress using DC data from both TCAD models and measurements, allowing for optimized performance in high power and high frequency applications where reliability concerns often lead to under-utilization of the transistor's capabilities.

RTUIF-19 **13:30**

A 4.7-Gb/s Imaging Receiver with Adaptive Spectrum Re-Balancing Equalizer for Wireless Optical Communications

Behrooz Nakhkoob, Mona M. Hella; Rensselaer Polytechnic Institute, USA

Abstract: Imaging Optical Receivers (IOR), in which a single photodiode (PD) is replaced by an array of small on chip PDs followed by a matrix of switches, can reduce the received ambient light noise, multi-path distortion, and allow electronic Line Of Sight (LOS) detection and tracking of the transmitted signal. However, such receivers experience a change in the total input capacitance introduced to the front-end circuitry depending on the number of activated PDs in LOS with the transmitter, mandating adaptive equalization in the receive side. In this work, a high speed imaging receiver is reported in IBM 130 nm CMOS technology. The receiver is formed of a 3×3 matrix of high speed Spatially Modulated Light detectors (SML) followed by a trans-impedance amplifier, an adaptive equalizer and a limiting amplifier. For one activated PD, the chip is capable of communicating at speeds up to 4.7-Gb/s with BER = 10^{-10} and sensitivity of -3.5dBm using $\lambda = 850$ nm modulated light. For 9 activated PDs, corresponding to an input capacitance of 11.5pF, the chip is capable of communicating at speeds up to 2-Gb/s for BER = 10^{-12} and an optical sensitivity of -5dBm. The power consumption of the imaging receiver is 97 mW from a single 1.5 V dc supply and the total die area is $1400\mu\text{m} \times 870\mu\text{m}$.

RFIC 2014 Panel Sessions

Monday, 2 June 2014

12:00–13:30

TCC Ballroom A

Fabless Design: Got Any Problem with That?

Panel Organizer and Moderator:

Luciano Boglione, *Naval Research Laboratory*

Panelists:

David Scagnelli, *IBM*

Samir Chaudhry, *TowerJazz*

Srenik Mehta, *Qualcomm*

Jon Strange, *MediaTek*

Frederic Giancesello, *STMicroelectronics*

Abstract: The past decade has seen a tremendous growth in fabless design companies which have been able to offer new products in the communication and electronic application market without bearing the high costs associated with a manufacturing infrastructure. On the other hand, foundries have been able to meet that demand with a large range of Silicon processes — from low cost to high performance devices. This relationship has worked out very well in the entire semiconductor industry as new demand has been met by new faster devices; and new faster devices have enabled more integration and more complexity, making Silicon the first choice in areas that were dominated by compound semiconductors just a handful of years ago.

Is this symbiotic relationship coming to an end or is it getting stronger? Moore's law has paced the speed in device innovation so far, but now improvements are getting harder and harder to achieve — and the fabrication cost for fabless innovators is sky-rocketing. Access to the latest technology can be prohibitive for many design teams and process innovation is becoming an ever more expensive proposition. The foundry business is dominated by a few large companies, whose operation and choices may affect the whole world. Further, the technological knowledge concentrates where the fabs are located, consolidating the manufacturing business to a limited number of locations. Is there still room for fabless start-ups to grow in this environment? Is this business for big players only? Or should the small players just resign to considering a foundry a commodity, focus on integration of more and more functionality and passively observe how the technology evolves? Our panelist will take this discussion from here and they will give the audience new perspectives on what the future may bring to the fabless design industry.

RFIC 2014 Panel Sessions

Tuesday, 3 June 2014

12:00–13:30

TCC Ballroom B

Is Spectrum Explosion Muffled without Tunable RF?

Panel Organizers and Moderators:

Jeff Hilbert, *WiSpry*

Joe Maden, *Mobile Experts*

Panelists: **Yuang Lou**, *AT&T*

Armin Klomdsorf, *Motorola*

Harish Krishnaswamy, *Columbia University*

David Whitefield, *Skyworks*

Steve Brown, *Qualcomm*

Jeff Hilbert, *WiSpry*

Abstract: The cellular network is rapidly evolving, driven by the immense global consumer appetite for data. Bandwidth across the spectrum is auctioned and then rolled out to support these needs. Effectively leveraging this bandwidth requires RF hardware that can operate across the current and future (LTE-A) multiple frequency ranges. Unfortunately, physical limitations in filters, amplifiers and antennas have greatly constrained the practical solutions to support this evolution. Today's standard approach utilizes separate filters for each band, and amplifiers over groups of bands while using antennas that attempt to cover the full bandwidth. While this architecture scales linearly, it is quickly becoming untenable. Replacing this approach with a tunable front end has been the 'holy grail' — always just out of reach. Evolution in the cost and performance of tuning technologies appears to be on the threshold of enabling this long-held dream. This panel brings together experts from across the wireless ecosystem to discuss the end user benefits, market opportunities, technical challenges and projected solutions surrounding this spectrum explosion.

WORKSHOPS AND SHORT COURSES

Workshops and Short Courses are offered on Sunday, Monday and Friday of Microwave Week. Please see daily handout on Sunday, Monday, and Friday in the registration area and from volunteers throughout the meeting floors to confirm room location.

SUNDAY WORKSHOPS – 1 JUNE 2014

WSA (Full Day): Sunday 08:00–17:00, TCC 13–14 **Silicon and GaN PA for RF and mm-Wave Applications**

Sponsors: **RFIC, IMS**

Organizers: **Didier Belot**, *STMicroelectronics, France*
Eric Kerhervé, *IMS Bordeaux, France*

Abstract: Silicon PAs, (in SiGe, High Voltage or High Frequency; in CMOS, High Voltage LDMOS or thin gate oxide High frequency; in SOI, Partially Depleted or Fully Depleted; also GaN technology), are dedicated for RF applications with “high” power and/or High linearity requirements, and for millimeter-wave applications with high Power added efficiency, medium linearity, and medium to “high” power requirements. At the same time, new “digital” like architectures for RF request class E, class F, RF-DAC power devices, while in mm-wave first mm-wave-DAC architectures are ongoing. Where is the limit? Can we imagine a pure digital Transmitter with such “PAs”? Which technology could answer to these challenges? Do we need multi-technologies module? What is the best cost/efficiency compromise? This workshop will overview state of the art technologies and design and system evolution, to address these questions.

Speakers:

1. “CMOS on SOI Power Amplifiers for Microwave and mm-Wave Applications”, **Peter Asbeck**, *University of California at San Diego, USA*
2. “CMOS SOI PA for Mobile Applications”, **Alexandre Giry**, *CEA-LETI, France*
3. “Towards the Best Compromise in CMOS PA Design, as a Complete System on Board Approach”, **Vincent Knopik**, *STMicroelectronics, France*
4. “Design Considerations of CMOS mm-Wave Power Amplifiers”, **Georges Boeck**, *Berlin University of Technology, Germany*
5. “mm-Wave PA-Antenna Co-Integration in CMOS SOI and BiCMOS SiGe Technologies”, **Eric Kerhervé**, *IMS Bordeaux, France*
6. “RF-DACs Replacing RF Power Amplifiers”, **R. Bogdan Staszewski**, *Delft University of Technology, The Netherlands*
7. “Interstage Matching Design for Broadband High Efficiency MMIC RFPAs”, **Steve C. Cripps**, *Cardiff University, UK*

WSB (Half Day): Sunday 08:00–12:00, TCC 15–16

Power Amplifiers for Software Defined Radios

Sponsor: **RFIC**

Organizers: **Jeffrey S. Walling**, *University of Utah, USA*
Hongtao Xu, *Intel, USA*

Abstract: Software-defined and cognitive radio backends are becoming more prevalent, while the RF front-end hardware used to transmit such SDR and CR signals are constrained to multi-band architectures with independent front-end gain and filtering. Bandpass data converters have proven adept at operating over multiple communications standards and a wide range of frequency, but the transmitter lags behind. The RF PA is a key element to enabling more portable solutions in SDR, but remains challenging to implement because most PAs use narrowband matching networks that limit their use over a wide range of frequencies. Furthermore, such PAs are not readily reconfigurable from one standard to the next due to differing fidelity requirements. This workshop presents techniques to improve efficiency over a wide range of modulation standards, using techniques such as DPA, SCPA, outphasing, etc. Pathways toward multiband PAs will also be presented using techniques such as wideband matching and new materials.

Speakers:

1. “Digital PAs: Switched Capacitor Circuits Pave the Way to Reconfigurability”, **Jeffrey S. Walling**, *University of Utah, USA*
2. “Marriage of Digital Bits and RF Power Amplifier — A Mixed-Signal Polar Power Amplifier for Reconfigurable Wireless Transmitters”, **Debopriyo Chowdhury**, *Broadcom, USA*
3. “Broadband Techniques for CMOS Power Amplifiers”, **Hua Wang**, *Georgia Institute of Technology, USA*
4. “RF Reconfiguration Using Phase-Change Switches”, **Jeyanandh Paramesh**, *Carnegie Mellon University, USA*
5. “Linearity and Efficiency Enhancement”, **Hongtao Xu**, *Intel, USA*
6. “mm-Wave Linearized PAs and TX in CMOS”, **Patrick Reynaert**, *KU Leuven, Belgium*

WSC (Half Day): Sunday 13:00–17:00, TCC 15–16

GaN-Based Power Supplies and Power Supply Modulators for Efficient Powering of RF PAs

Sponsor: **RFIC**

Organizers: **Ayman Fayed**, *Iowa State University, USA*
Jennifer Kitchen, *Arizona State University, USA*

Abstract: Efficient operation of RF PAs is a strong function of the power conversion efficiency of the power supplies used to deliver power to these PAs. Therefore, the design of highly-efficient switching

power supplies and power supply modulators for these PAs is of utmost importance. A key aspect of designing switching power supplies is the devices used to implement the power switches. GaN devices have great potential to fulfill that role, mainly due to their ability to handle high voltage and current levels while maintaining very low on resistance and relatively low gate capacitance compared to silicon counterparts. This makes GaN devices very attractive for building efficient switching power supplies, as well as wide-band power supply modulators for RF PAs. However, there continue to be many hurdles that must be overcome. These hurdles include better understanding of GaN device physics and operation, as well as its modeling and simulation techniques; the design of gate drive circuits of GaN power switches, especially normally-on depletion mode devices; and the utilization of GaN devices as both high-side and low-side power switches, especially with the lack of complementary GaN devices at this point. This workshop will cover four important aspects of designing switching power supplies using GaN devices: 1) the physics of GaN devices, how GaN devices compare to other technologies such as Si and SiC, when would using GaN make more sense, and modeling and simulation of GaN Devices, 2) the design of gate drive circuits for depletion-mode GaN power switches, 3) the design of static switching power supplies using enhancement-mode GaN power devices, and 4) the design of switching and hybrid power supply modulators using GaN devices.

Speakers:

1. “Device Physics Advantages of GaN for Power Switches”, **David Fanning, Vipin Kumar**, *Triquint, USA*
2. “Gate Drive Techniques for High-Power Switched-Mode Power Amplifiers”, **David Cripe, Don Landt**, *Rockwell Collins, USA*
3. “Linear and Switching Power Supplies for RF Applications Using eGaN FETs”, **Michael A. de Rooij**, *Efficient Power Conversion, USA*
4. “Innovative Use of Enhanced Mode GaN Power FETs in Medium Power Envelope Tracking Modulators”, **Dave McIntosh**, *KCB Signal Solutions, USA*

WSD (Half Day): Sunday 08:00–12:00, TCC 18

Techniques for Handling Interference and Self-Interference

Sponsor: **RFIC**

Organizers: **Danilo Manstretta**, *University of Pavia, Italy*
Eric Klumperink, *University of Twente, The Netherlands*

Abstract: Interference handling, but also self-interference handling, is increasingly becoming important in radio receivers. On the one hand this is because the number of wireless devices is steadily increasing, increasing the probability that a nearby strong interferer exists. On the other hand extra interference and also self-interference occurs because multiple radios have to co-exist in one user terminal, preferably with less external components. In systems that transmit at the same time but at different frequency, duplexer filters can be used to suppress self-interference. To maximize data throughput and spectral efficiency further, it might be beneficial to not only transmit and receive at the same time but also at the same frequency. However, such full-duplex communication causes very strong self-interference, and techniques to reduce this are very much wanted. Such techniques can also relax duplex filter requirements, also creating new possibilities

in half-duplex radio architectures. This workshop will review techniques to reduce interference and self-interference. Several recently proposed techniques that can contribute to improving interference and self-interference handling will be reviewed.

Speakers:

1. “Current-Mode Approach in High Dynamic Range Wireless Transceivers”, **Antonio Liscidini**, *University of Toronto, Canada*
2. “Harmonic Rejection Mixers for Wideband Interference Handling”, **Aslam A. Rafi**, *Silicon Labs, USA*
3. “Active Low-Noise Self-Interference Cancellation in Software-Defined Radios”, **Harish Krishnaswamy**, *Columbia University, USA*
4. “Tradeoffs in Full-Duplex Wireless”, **Ashutosh Sabharwal**, *Rice University, USA*
5. “Full Duplex Radios”, **Sachin Katti**, *Stanford University, USA*

WSE (Half Day): Sunday 13:00–17:00, TCC 18

Coupling and Self-Interference in Integrated Circuits: EMC/EMI-Aware Design Practices

Sponsors: **RFIC, IMS**

Organizers: **Rick Janssen**, *NXP Semiconductors, The Netherlands*
Oren Eliezer, *Xiendwave, USA*
Naveen Yanduru, *Peregrine Semiconductor, USA*

Abstract: With the integration of RF, mixed signal and digital building blocks on a single die, combined with the trend to go to higher frequencies to accommodate higher data rates, it is essential to consider various on-chip coupling effects during the design phases of the IC. Additionally, measures should be taken at the system/application level to reduce the impact of peripheral interactions (between chip, package, PCB, antenna, etc.), as well as the potential for self-interference, such that these are either eliminated or can be resolved on the fabricated product, thereby reducing the number of re-spins. Additionally, present-day products are often required to pass rigorous EMC tests to verify their compliance with standards and regulations. The focus of this workshop will be on addressing EMC/EMI problems by applying the proper methodologies during the design phase. This includes making use of dedicated EDA capabilities to predict EMC/EMI, as well as applying design methodologies and approaches that allow for the mitigation of self-interference effects.

Speakers:

1. “Methodology for Floor Plan Development and Verification of Isolation and Grounding Strategies”, **Rick Janssen, Jan Niehof**, *NXP Semiconductors, The Netherlands*
2. “A Practical Approach to Resolving Self-Interference Problems in Transceiver SoCs”, **Oren Eliezer**, *Xiendwave, USA*
3. “RF Switch Based Circuits for Systems Requiring Front-Ends with High Isolation and Linearity”, **Naveen Yanduru**, *Peregrine Semiconductor, USA*

4. “Electromagnetic Interference and Compatibility Analysis of Analog Integrated Circuits — An Approach Based on Measurement and Simulation Techniques”, **Christian Stockreiter**, *ams, Austria*
5. “Spur and Performance Degradation Mitigation in Free-Running XTAL Cellular Platforms”, **Nikos Haralabidis**, *Broadcom, Greece*

WSF (Full Day): Sunday 08:00–17:00, TCC 25

MEMS-CMOS Integration

Sponsors: **MTT-21 RF MEMS, RFIC**

Organizers: **James C.M. Hwang**, *Lehigh University, USA*
Joachim Oberhammer, *KTH, Sweden*

Abstract: This workshop focuses on the rapidly evolving field of MEMS-CMOS integration for commercialization of RF MEMS. The integration can be homogeneous or heterogeneous. Homogeneous integration on the wafer scale takes advantage of the mature CMOS backend processes to improve the yield, cost, robustness and reliability of MEMS. Alternatively, integration can be done heterogeneously in-package or at the circuit level, using CMOS circuits to intelligently control MEMS or using MEMS to switch CMOS circuits with high on/off ratios. Integration of MEMS and CMOS, on wafer, chip or package level, has been commercially successful in many MEMS applications. The development of RF MEMS can benefit from these experiences, which will be shared in this workshop. The limitations of CMOS-integrated RF MEMS will be critically reviewed and different approaches to overcome such limitations will be explored.

Speakers:

1. “CMOS-MEMS Integration and Beyond”, **Gary K. Fedder**, *Carnegie Mellon University, USA*
2. “Technical and Commercial Aspects of MEMS-CMOS Integration”, **Franz Larmer**, *Robert Bosch, Germany*
3. “Monolithic Integration of CMOS-MEMS for Digital Light Processing”, **Sean O’Brien**, *Texas Instruments, USA*
4. “Limitations of IC-Integration, and High-Performance Stand-Alone RF and Microwave MEMS”, **Joachim Oberhammer**, *KTH, Sweden*
5. “MEMS/CMOS Tradeoffs for Cell-Phone Antenna Tuners”, **Julio C. Costa**, *RFMD, USA*
6. “Monolithic Integration of RF MEMS in CMOS for High Volume and Low Cost Markets”, **Arthur S. Morris**¹, **Anthony K. Stamper**², *¹WiSpry, USA, ²IBM, USA*
7. “SiGe-Backend Integrated MEMS: RF Switches, Antennas, and Sensors”, **Mehmet Kaynak**, *IHP, Germany*
8. “Intelligent Bipolar Control of MEMS Capacitive Switches”, **James C.M. Hwang**¹, **Charles L. Goldsmith**², *¹Lehigh University, USA, ²MEMtronics, USA*

WSG (Full Day): Sunday 08:00–17:00, TCC 10–11

Advanced SiGe and CMOS Phased Arrays Systems from 3 to 100GHz

Sponsors: **IMS, RFIC**

Organizers: **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
Domine Leenaerts, *NXP Semiconductors, The Netherlands*

Abstract: SiGe and CMOS Technologies have permanently changed the way we build phased arrays by integrating the complex back-end functions into a single chip, and by integrating many channels on the same chip with high isolation. These complex back-end chips also allow the construction of multiple-beam arrays (2, 3, 4 simultaneous beams), something which was considered nearly impossible with GaAs T/R modules. This started at the university level but quickly transferred to industry, and today, there are several efforts in industry from 3GHz to >100GHz using silicon back-ends. Also, highly complex panel-based phased arrays have been demonstrated using this technology. This workshop will present some of the recent demonstrations of such systems, from an academia, industry and government perspective.

Speakers:

1. “Si/SiGe BiCMOS Transceiver ICs for Ka Band Phased Array Antennas”, **H. Schumacher¹, F. Tabarani¹, T. Purtova^{1,2}, T. Chaloun¹, W. Menzel¹**, *¹Ulm University, Germany, ²now with Triquint, Germany*
2. “Si-Based Phased Array Transmitter for Ka-Band Applications”, **Domine Leenaerts, Yu Pei, Ying Chen**, *NXP Semiconductors, The Netherlands*
3. “Enabling Mobile Communication at mm-Wave Using Phased Arrays”, **Farshid Aryanfar**, *Samsung Research America, USA*
4. “Low Cost Panel-Based Phased Arrays at X- and Ka-Band”, **Lee Paulsen, Michael Buckley, Russ Wyse, Michael Hageman, Jeremiah Wolf, James West**, *Rockwell Collins, USA*
5. “Circuits, Antennas, Packaging and Scalable Integration for W-Band Phased Arrays”, **Alberto Valdes-Garcia**, *IBM T.J. Watson Research Center, USA*
6. “SiGe and CMOS Millimeter-Wave Phased Arrays with Built-In-Self-Test Capabilities”, **Gabriel M. Rebeiz¹, Ozgur Inac², Bonhyun Ku¹, Fatih Golcuk³, Sangyoung Kim⁴**, *¹University of California at San Diego, USA, ²Intel, USA, ³MediaTek, USA, ⁴Marvell Semiconductors, USA*
7. “Novel Uses of Digitally Influenced Arrays”, **William Chappell**, *Purdue University, USA*
8. “Design Techniques for L- Through X-Band Phased-Array Transceivers”, **Frank E. van Vliet**, *TNO and University of Twente, The Netherlands*
9. “GaN and CMOS-Based T/R Chipset and Module for Phased Array Antennas”, **Jeong-Geun Kim¹, Sanghoon Sim², Moonkyu Cho¹, Laurence Jeon²**, *¹Kwangjuon University, Korea, ²RFcore, Korea*

WSH (Half Day): Sunday 08:00–12:00, TCC 20

How Digital Can RF Go?

Sponsor: **RFIC**

Organizers: **Gernot Hueber**, *NXP Semiconductors, Austria*

R. Bogdan Staszewski, *Delft University of Technology, The Netherlands*

Abstract: Advances in CMOS fabrication technology enabled the use of CMOS technology in today RF transceivers for wireless communications. Multi-band and multi-mode radios covering the diversity of communication standards from 2G GSM, 3G UMTS, to 4G LTE and LTE-advanced impart unique challenges on the RF-transceiver design due to limitations in terms of reconfigurable RF components that meet the demanding cellular performance criteria at costs that are attractive for mass market applications. Nanoscale CMOS, on the one hand, features the possibility for implementing a significant computational power and complex functionality directly on a single IC, and on the other hand, it shows poor performance in RF circuits compared to other technologies. The focus of this workshop will be on the challenges RF transceiver design and architectures in nanoscale CMOS, along with a thorough discussion of advanced techniques for receivers and transmitters towards integration in a multi-radio SoC or SiP. Approaches include novel architectures, highly configurable analog circuitry, digitally assisted and enhanced analog/RF modules and the integration of digital signal processing into the traditionally purely analog front-end.

Speakers:

1. “Modeling and Digital Suppression of Power Amplifier Unwanted Emissions at Receiver Band in FDD Transceivers”, **Mikko Valkama**, *Tampere University of Technology, Finland*
2. “Highly-Integrated Wireless Receiver Architectures Composed of Only Switches, Capacitors and Inverter-Based Amplifiers”, **Ahmad Mirzaei**, *Pennsylvania State University, USA*
3. “Coping with In-Band Interference in CMOS Radio Receivers”, **Eric Klumperink**, *University of Twente, The Netherlands*
4. “Challenges in Designing a Transceiver Carrier Aggregation”, **Charn Narathong**, *Qualcomm, USA*
5. “How Extreme ADCs Enable the Future of Nanoscale RF”, **Vito Giannini**, *imec, Belgium*
6. “A Digitally-Assisted Reciprocal-Mixing and Spurs Cancellation Technique for Modern Receivers”, **Mohyee Mikhemar**, *Broadcom, USA*

WSI (Full Day): Sunday 08:00–17:00, TCC 21
Wireless Power Transfer and Wireless Charging

Sponsor: **RFIC**

Organizers: **Gernot Hueber**, *NXP Semiconductors, Austria*
Magnus Wiklund, *Qualcomm Atheros, USA*

Abstract: Wireless power transfer and wireless charging is becoming a technology on the way to deployment in the high volume market from mobile devices (smartcards, phones, tablets) to electric vehicles and many other areas. The interest of the RFIC community is to explore technological challenges and boundaries of what our modern integrated circuit processes has to offer, which architecture and how to design on circuit level. RFIC development of circuits is a highly advanced topic and this workshop will address devices from both, system and circuit design level including testing.

Speakers:

1. “An Overview of Standards for Wireless Power Standards”, **Klaas Brink**, *NXP Semiconductors, The Netherlands*
2. “Essentials in Wireless Power Systems”, **Charles Wheatley**, *Qualcomm, USA*
3. “Heterogeneous Non Ohmic Coupling Between Antennas and Integrated Electronics: A Pace Along the IoT Way”, **Luca Roselli**, *University of Perugia, Italy*
4. “Numerical, Electromagnetic and Nonlinear Modeling of Entire WPT Links”, **Alessandra Costanzo**, *University of Bologna, Italy*
5. “WPT for Smartcards and NFC”, **Michael Gebhart**, *NXP Semiconductors Austria*
6. “Circuit Design for Highly Resonant Wireless Charging of Mobile Devices”, **Patrick Riehl**, *MediaTek, USA*
7. “Specially Designed Waveforms for Wireless Power Transmission Improvement”, **Nuno Carvalho**, *Universidade de Aveiro, Portugal*
8. “Novel Inkjet Printed Structures for Highly Efficient Wireless Power Harvesting, Transfer and Charging”, **Manos M. Tentzeris**, *Georgia Institute of Technology, USA*

WSJ (Full Day): Sunday 08:00–17:00, TCC 22
Reconfigurable Radio-Frequency Transceivers

Sponsor: **RFIC**

Organizers: **Hossein Hashemi**, *University of Southern California, USA*
William Chappell, *DARPA, USA*

Abstract: Modern commercial and military wireless systems should support various waveforms and standards under dynamically changing electromagnetic environments. A straight forward Software-

Defined Radio (SDR) enables changing the radio parameters, such as carrier frequency, modulation format, and signal bandwidth, in a fixed architecture, through software. A more advanced reconfigurable radio enables changing the architecture of the transceiver and/or the individual building blocks in order to optimize the performance while minimizing the power consumption. Architectural level reconfigurability reduces the Non-Recurring Engineering (NRE) cost associated with the design of a new transceiver tailored to a specific application. Moreover, dynamic adjustment of radio architecture and specifications can be in response to, for instance, varying signal, noise, and interference levels. This workshop covers the latest developments in the design and implementation of reconfigurable wireless transceivers.

Speakers:

1. “MATRICs: Microwave Array Technology for Reconfigurable Integrated Circuits”, **Douglas S. Jansen**, *BAE Systems, USA*
2. “A Broadband Reconfigurable Mixed-Signal CMOS/Interposer RF Transceiver”, **Elad Alon**, *University of California at Berkeley, USA*
3. “Time-Domain Analog and RF Signal Processing for Reconfigurable Transceivers”, **R. Bogdan Staszewski**, *Delft University of Technology, The Netherlands*
4. “Reconfigurable Radios Leveraging Discrete Time Signal Processing”, **Hossein Hashemi**, *University of Southern California, USA*
5. “Monolithic Frequency Agile Wideband RF Front-End Design Techniques”, **Lawrence Larson**, *Brown University, USA*
6. “Frequency-Division Duplexing and Co-Existence in Reconfigurable RF Radios”, **Harish Krishnaswamy**, *Columbia University, USA*
7. “Multi-Standard Transceiver Design for Ultra-Low Power Wireless Personal/Body Area Networks”, **Yao-Hong Liu**, *imec, The Netherlands*
8. “Fine-Grain Reconfigurable and Programmable FPAAs Towards Receiver Applications”, **Jennifer Hasler**, *Georgia Institute of Technology, USA*

WSK (Full Day): Sunday 08:00–17:00, TCC 23

Frequency Synthesis for 60-GHz and Beyond: Architectures and Building Blocks

Sponsor: **RFIC**

Organizers: **Stefano Pellerano**, *Intel, USA*
Jeyanandh Paramesh, *Carnegie Mellon University, USA*

Abstract: Synthesizing local-oscillator (LO) signals with high spectral purity within an integrated circuit can be quite a challenging task and it has been the focus of many researchers for decades. Moreover, other aspects as very high oscillation frequency (60GHz for wireless communications or even sub-THz for imaging applications), low-power consumption (for integration within mobile devices), very wide tuning range/frequency modulation (for radar applications), relatively low quality factor passives (to enable low-cost, high volume technologies like CMOS), make the design

even more daunting. This workshop focuses on the latest state-of-the-art advancements on how to efficiently synthesize LO signals from 60GHz all the way up to sub-THz frequencies for several applications like wireless communications, radar and imaging. Both overall synthesizer architecture and building block details will be considered, with particular attention to oscillator design. Techniques for reducing power consumption and phase noise while increasing tuning range will be addressed. Latest advancements in injection-locking and frequency division/multiplication will also be presented.

Speakers:

1. “Frequency Synthesis in Millimeter-Wave ICs: A System-Level Perspective”, **Bevin Perumana**, *Broadcom, USA*
2. “Design and Optimization of On-Chip Passive Components and Their Application to mm-Wave Frequency Synthesis”, **John R. Long**, *Delft University of Technology, The Netherlands*
3. “Insights into Circuits for Frequency Synthesis at mm-Waves”, **Andrea Mazzanti**, *University of Pavia, Italy*
4. “Injection-Locked Frequency Synthesizers and Building Blocks”, **Howard C. Luong**, *Hong Kong University of Science and Technology, China*
5. “Low-Noise mm-Wave Frequency Synthesis Techniques in Silicon”, **Bodhisatwa Sadhu**, *IBM T.J. Watson Research Laboratory, USA*
6. “60GHz WiGig Frequency Synthesizer Using Injection Locked Oscillator”, **Kenichi Okada**, *Tokyo Institute of Technology, Japan*
7. “Frequency Synthesis for High Volume Market 77GHz FMCW Automotive Radar in SiGe BiCMOS”, **Didier Salle**, *Freescale Semiconductor, France*
8. “All-Digital PLL Design for mm-Wave FMCW Radars”, **R. Bogdan Staszewski**, *Delft University of Technology, The Netherlands*
9. “Sub-Millimeter Wave Signal Generation and Phase Locking in CMOS”, **Kenneth K. O.**, *University of Texas at Dallas, USA*

WSL (Full Day): Sunday 08:00–17:00, TCC 19

Ultra Low Power, Low Cost Radios

Sponsor: **RFIC**

Organizers: **Sudipto Chakraborty**, *Texas Instruments, USA*
Oren Eliezer, *Xiendwave, USA*
Danielle Griffith, *Texas Instruments, USA*

Abstract: There has been a growing interest in minimizing the power/energy consumption and the cost of integrated radios for various applications that are battery operated and/or harvest energy from the environment. Successful development of ultra-low power and low cost radios requires that different aspects of the design are properly addressed. These include: (a) consideration of relevant standards, (b) overall system design and radio system architecture, (c) circuit design techniques, (d)

minimal external component count, and (e) low cost testing. Several standards, such as Bluetooth low energy (BLE), ZigBee, ANT, and BAN, have been proposed in the past years to address the growing needs of various personal area communication systems. These solutions primarily target sports monitoring, body area networking, remote structural health monitoring, wireless sensors, and various other emerging applications. This workshop addresses various system and circuit design techniques that serve to augment the dynamic range per unit power consumption of integrated radios, while achieving a low cost solution. Industry and academia experts will present a wide variety of topics, covering low-data-rate radios operating at sub-MHz frequencies and high data-rate radios operating at millimeter-wave frequencies.

Speakers:

1. “Ultra-Low Power, Multi-Standard SoCs for WBAN”, **Alan Wong**, *Toumaz, UK*
2. “Energy Efficient Radios with Sub nJ/Bit Efficiency”, **Xiongchuan Huang**, *imec and Holst Centre, The Netherlands*
3. “Low Power Design Techniques of UHF CMOS Wake-Up Receivers”, **Heinrich Milosiu**, *Fraunhofer IIS, Germany*
4. “Low Power Transceiver Design for Battery Free Wireless Powered Systems”, **Raymond Barnett**, *Texas Instruments, USA*
5. “Energy Efficient Low-Cost Millimeter-Wave Transceiver”, **Elad Alon**, *University of California at Berkeley, USA*
6. “Low Voltage Design Techniques for Low Power Radios”, **Peter Kinget**, *Columbia University, USA*
7. “Low Power Sleep Timers for Wireless Networks”, **Danielle Griffith**, *Texas Instruments, USA*
8. “Design/Test Synergy in RF Built-In Self Calibration to Realize Ultra Low Power, Low Cost Radios”, **Sudipto Chakraborty**, *Texas Instruments, USA*
9. “Efficient Wide Dynamic Range Receivers for the New WWVB Broadcast”, **Oren Eliezer**, *Xtendwave, USA*

WSM (Full Day): Sunday 08:00–17:00, TCC 24

RF and Wideband Data-Converters for Transmitters and Receivers

Sponsor: **RFIC**

Organizers: **Gaurav Chandra**, *MaxLinear, USA*
Harish Krishnaswamy, *Columbia University, USA*
Oren Eliezer, *Xtendwave, USA*

Abstract: As RF transceivers continue to be integrated into extensively digital SoCs, in which multiple radio standards and frequency bands are covered, there is increased motivation in realizing the digital-to-RF and RF-to-digital conversions in ways that are more amenable to integration in such environments. More specifically, the preferred implementations are extensively digital in nature, since digital resources, such as processing and memory, can be assumed to be readily available in

such SoCs, and can serve for digital-signal-processing based calibration and compensation. This workshop, involving experts from industry and academia, will cover various architectures and techniques for digital-to-RF conversion, that are to be used at the transmitter end, as well as efficient and configurable RF-to-digital converters to be used at the receiver end. Additionally, wideband data-converters, such as pipelined ADCs and interleaved DACs, which may serve in wideband transceivers, will be covered.

Speakers:

1. “RF-to-Digital Conversion by Continuous-Time Bandpass Delta-Sigma ADC”, **Hajime Shibata**, *Analog Devices, USA*
2. “High Speed Time Interleaved ADCs for Software Defined Radios”, **Gaurav Chandra**, *MaxLinear, USA*
3. “A High Resolution RF-DAC for a Multi-Mode Polar Transmitter”, **Zdravko Boos**, *Intel (previously with Infineon Technologies), Germany*
4. “Asynchronous Compressive RF-Sampling for Radar with In-Band Communication Interference”, **Sebastian Hoyos**, *Texas A&M University, USA*
5. “Evolution of ADCs and its Role in Enabling Software Defined Radio Architectures”, **Kush Gulati**, *Maxim Integrated Products, USA*
6. “Watt-Level RF Power-DAC Transmitters in Nanoscale CMOS”, **Harish Krishnaswamy**, *Columbia University, USA*
7. “Fully-Digital Self-Compensated RF-DAC Based Transmitter Architectures”, **Oren Eliezer**, *Xtendwave, USA*
8. “Power Efficient ADC Topologies Towards RF Sampling”, **Mike Shuo Wei Chen**, *University of Southern California, USA*

WSN (Half Day): Sunday 13:00–17:00, TCC 20

Characterizing the Impact and Benefits of Millimeter Waves on Biomaterial

Sponsor: **MTT-10 Biological Effects and Medical Applications**

SUNDAY SHORT COURSES – 1 JUNE 2014

SC-1 (Half Day): Sunday 08:00–12:00, TCC 12

Integrated Multi-Technology Physical RF Design Flow

Sponsor: **IMS**

SC-2 (Half Day): Sunday 13:00–17:00, TCC 12

Near Field Probes: Useful Tools for RF/MW Engineers

Sponsor: **MTT-17 HF-VHF-UHF Technology**

MONDAY WORKSHOPS – 2 JUNE 2014

WMA (Full Day): Monday 08:00–17:00, TCC 19

Modern RF-Module Design: Integrated Forms of Silicon and Gallium Nitride

Sponsors: **RFIC, MTT-6 Microwave and Millimeter Wave Integrated Circuits,
MTT-16 Microwave Systems,
MTT-20 Wireless Communications**

Organizers: **Ruediger Quay, Fraunhofer IAF, Germany**
Frank Sullivan, Raytheon, USA
John Pierro, Telephonics, USA
Tim Lee, Boeing, USA

Abstract: This workshop is focused on recent developments of transmit and receive modules and integration based on the advances in Silicon and Gallium Nitride IC technology. The technologies emerging for this application in various substantial research programs such as SiGe — as BICMOS — and CMOS, in combination with more integrated and higher functional GAN enable significant architectural changes in the race for performance and cost so far limiting the applications space. Innovative TRX modules, which may or may not be free of GaAs, are discussed allowing for new concepts at applications such as radar, counter measures and communication. The workshop will address the progress, design, trade-offs, and remaining issues arising from the combinations of GaN and the use of Si as well as the resulting possible improvements in array technology starting from technology to system aspects.

Speakers:

1. “Semiconductor Materials and Integration Strategies for Modern RF-Module Designs”, **Daniel S. Green¹, Avinash S. Kane², Carl L. Dohrman²**, ¹DARPA, USA, ²Booz Allen Hamilton, USA
2. “Advanced T/R Modules Based on SiGe and GaN MMICs”, **Patrick Schuh, Ralf Rieger, Martin Oppermann**, *Cassidian, Germany*
3. “SiGe and CMOS Chips for Phased Arrays with High Linearity GaN Front-Ends”, **Gabriel M. Rebeiz**, *University of California at San Diego, USA*
4. “New Generations of T/R Modules for Tile Antennas”, **Yves Mancuso**, *Thales Systèmes Aéroportés, France*

5. “High Performance RF Circuits Enabled by the Heterogeneous Integration of GaN HEMTs with Si CMOS on a Silicon Substrate”, **Thomas E. Kazior**, *Raytheon, USA*
6. “Switch Mode Power Amplifier for Base Stations — Raising the Bar for Reconfigurability and Efficiency”, **Mustafa Acar, M.P. van der Heijden**, *NXP Semiconductors, The Netherlands*
7. “Impacts of Scaled Silicon on Modern Module Designs”, **William Chappell**, *Purdue University, USA*
8. “Very High Efficiency SiGe and GaN High Power Amplifiers for Tile Modules”, **Victor Dupuy, Eric Kerhervé**, *IMS Bordeaux, France*

WMB (Full Day): Monday 08:00–17:00, TCC 20

Highly Efficient Power Amplifiers and Smart Transmitters

Sponsors: **RFIC, WAMICON, MTT-23 RFIC**

Organizers: **Renato Negra**, *RWTH Aachen University, Germany*
Georg Boeck, *Berlin Institute of Technology, Germany*

Abstract: The wireless communication community has always been looking for efficient linear amplification systems. This full-day workshop combines international academic specialists to outline the most recent activities, achievements and future possibilities in the area of highly efficient microwave power amplifiers and advanced transmitter architectures for wireless applications. The talks will span from circuit design to system level and introduce both progresses in the design of highly efficient power stages using harmonic matching, supply modulation and load modulation concepts, as well as their application in digital-centric flexible transmitter architectures. Special emphasis is on transmitters beyond the state-of-the-art technology of envelop tracking. The principles of pulse shaping, outphasing and active load-pulling transmitter architectures will be introduced and their potential and characteristics will be illustrated through practical implementations and measurement results. An emphasis on critical issues and limitations in realising these amplifiers and systems will be given.

Speakers:

1. “Supply-Modulated X-Band MMIC Power Amplifiers and Transmitters for Communications and Radar”, **Zoya Popovic**, *University of Colorado at Boulder, USA*
2. “Advanced Operation of Envelope Tracking Power Amplifier for Handset Applications”, **Bumman Kim**, *POSTECH, Korea*
3. “Continuous-Mode Broadband Power Amplifiers”, **Saeed Rezaei, Fadhel M. Ghannouchi**, *University of Calgary, Canada*
4. “Fully Integrated Doherty PAs in Nanometer CMOS”, **Patrick Reynaert**, *KU Leuven, Belgium*
5. “Highly Efficient PA Architectures in the Presence of High Peak-to-Average Signals”, **Souheil Ben Smida, Kevin Morris**, *University of Bristol, UK*

6. “Multilevel Outphasing Transmitter in Standard CMOS”, **Ahmed F. Aref**, *RWTH Aachen University, Germany*
7. “Efficient and Wideband Digital Transmitters Based on New Class-E Theory”, **Christian Fager**, *Chalmers University of Technology, Sweden*
8. “Microwave and Millimeter-Wave MMIC Power Amplifiers Using 3-D Dual-Radial Combining Technique”, **Tian-Wei Huang**, *National Taiwan University, Taiwan*
9. “Delta-Sigma and Pulse-Width Modulation Power Amplifiers for High Peak-to-Average Power (PAPR) Signals”, **Donald Kimball**, *University of California at San Diego, USA*

WMC (Full Day): Monday 08:00–17:00, TCC 21

Efficient RF Design Using Practical Behavioral Models — Bridging the Gap Between Measurements and Simulations

Sponsors: ARFTG, MTT-11 Microwave Measurements

WMD (Full Day): Monday 08:00–17:00, TCC 22

Recent Developments in Low Noise and Front-End Technology, Design, Circuits, Measurement Techniques, and State-of-the-Art Applications

Sponsors: MTT-14 Microwave Low Noise Techniques,
MTT-17 HF-VHF-UHF Technology,
MTT-22 Signal Generation and Frequency Conversion

WME (Full Day): Monday 08:00–17:00, TCC 23

Recent Advances in Radar Indoor Sensors, Wireless Implantable Devices and Biosensors

Sponsors: WAMICON,
MTT-10 Biological Effects and Medical Applications,
MTT-20 Wireless Communications

WMF (Full Day): Monday 08:00–17:00, TCC 12

Physics-Based Nonlinear Compact Transistor Modeling for mm-Wave Applications

Sponsor: MTT-14 Microwave Low Noise Techniques

WMG (Half Day): Monday 08:00–12:00, TCC 25

Current Trends in mm-Wave Integrated Circuits and Integration Techniques

Sponsors: **MTT-6 Microwave and Millimeter-Wave Integrated Circuits,**
MTT-12 Microwave and Millimeter-Wave Packaging and Manufacturing

WMH (Half Day): Monday 13:00–17:00, TCC 25

System-on-Chip and System-on-Package for mm-Wave Communication and Imaging

Sponsors: **IMS, RFIC**

Organizers: **Arun S. Natarajan, Oregon State University, USA**
Pierre Busson, STMicroelectronics, France

Abstract: Several communication and imaging applications at mm-wave require large element arrays for increased data rates and resolution. The feasibility of silicon integration of large number of elements at mm-wave has been shown in recent years. Packaging and measuring such multiple-antenna systems in V-band and W-band, particularly at low cost for widespread commercial applications, presents interesting challenges. Several approaches are being explored — antenna in package, on-chip antennas with off-chip dielectric slabs/lenses. This workshop will focus on design and measurement techniques for co-integration of mm-wave ICs with mm-wave antennas and packages. State-of-the-art system level integration and testing of multiple antenna mm-wave systems for 60GHz communication and W-band imagers will be presented, and challenges and benefits of different technologies and approaches will be discussed.

Speakers:

1. “Supply-Modulated X-Band MMIC Power Amplifiers and Transmitters for Communications and Radar”, **Zoya Popovic**, *University of Colorado at Boulder, USA*
2. “High-Efficiency On-Chip Antennas for Millimeter-Wave/THz Wafer-Scale Phased Arrays and Imaging Systems”, **Gabriel M. Rebeiz¹, Jen Edwards², Ozan Gurbuz¹, Yu-Chin Ou³, Mehmet Uzunkol³, Woorim Shin³, Kevin Ho¹, Fatih Golcuk⁴, Ramadan Al-Halabi⁵**, ¹*University of California at San Diego, USA*, ²*Apple, USA*, ³*Qualcomm, USA*, ⁴*MediaTek, USA*, ⁵*Cavendish Kinetics, USA*
3. “mm-Wave Antennas and Front Ends on Multilayer Organic Packaging Technology”, **John Papapolymerou**, *Georgia Institute of Technology, USA*
4. “Designs of Organic Package with Embedded Antennas for 60GHz and W-Band Phased-Array Applications”, **Xiaoxiong Kevin Gu**, *IBM Research, USA*
5. “60GHz Packaging & Antenna Technologies: From WiGig to Backhaul”, **Fred Gianesello**, *STMicroelectronics, France*
6. “Advanced Technologies for Millimeter-Wave System Integration”, **Maciej Wojnowski, K. Pressel**, *Infineon Technologies, Germany*

WMI (Full Day): Monday 08:00–17:00, TCC 24

**Challenges and Advances in Wafer-Level Calibration and
Characterization of Millimeter and Sub-Millimeter Wave Devices and
Systems**

Sponsors: ARFTG,
MTT-11 Microwave Measurements,
MTT-14 Microwave Low-Noise Techniques

FRIDAY WORKSHOPS – 6 JUNE 2014

WFA (Full Day): Friday 08:00–17:00, TCC 18

**Revisiting Equivalent Circuit Models for Emerging Technologies: From
Microwaves to THz**

Sponsor: MTT-15 Microwave Field Theory

WFB (Half Day): Friday 08:00–12:00, TCC 19

**Frequency Agile Antennas and Sensors Using Advanced Control
Materials**

Sponsor: MTT-13 Microwave Control Materials and Devices

WFC (Half Day): Friday 13:00–17:00, TCC 19

**Microwave Photonic Integrated Circuits and Systems: Opportunities
and Challenges Offered by Graphene and Silicon**

Sponsor: MTT-3 Microwave Photonics

WFD (Full Day): Friday 08:00–17:00, TCC 20

Statistical Modeling of Microwave Circuits and Systems

Sponsors: MTT-1 Computer-Aided Design,
MTT-15 Microwave Field Theory

WFE (Full Day): Friday 08:00–17:00, TCC 12

Recent Advances in Space Mapping Modeling and Optimization

Sponsors: MTT-1 Computer-Aided Design,
MTT-8 Filters and Passive Components,
MTT-15 Microwave Field Theory

WFF (Full Day): Friday 08:00–17:00, TCC 22

MIMO Radar Techniques and Frontends for Localization and Imaging

Sponsors: MTT-9 Digital Signal Processing,
MTT-16 Microwave Systems,
MTT-27 Wireless-Enabled Automotive and Vehicular Applications

WFG (Full Day): Friday 08:00–17:00, TCC 13–14

**Efficient PAs and Transmitters for High Peak-to-Average Power Ratio
Signals**

Sponsor: MTT-5 Microwave High-Power Techniques

WFH (Half Day): Friday 08:00–12:00, TCC 21

Terahertz Interconnects

Sponsors: MTT-4 Terahertz Technology and Applications,
MTT-12 Microwave and Millimeter-Wave Packaging and Manufacturing

WFI (Full Day): Friday 08:00–17:00, TCC 15–16

**Recent Advances in Digital Pre-Distortion for Wireless
Communications**

Sponsor: MTT-5 Microwave High-Power Techniques

WFJ (Full Day): Friday 08:00–17:00, TCC 23

**Inkjet-Printing: The Next Generation of Multi-Layer Fabrication,
Integration & Packaging for RF and mm-Wave Systems**

Sponsor: IMS

WFK (Full Day): Friday 08:00–17:00, TCC 24

Beyond Graphene: Electronic Devices and Their Potential for High-Frequency Applications

Sponsor: **MTT-7 Microwave and Millimeter-Wave Solid-State Devices**

FRIDAY SHORT COURSES – 6 JUNE 2014

SC-3 (Full Day): Friday 08:00–17:00, TCC 10–11

Fundamentals of Device Modeling for Nonlinear Circuit Simulation and Microwave Design

Sponsors: **MTT-1 Computer-Aided Design,
MTT-11 Microwave Measurements**

SC-4 (Full Day): Friday 08:00–17:00, TCC 25

Frequency Synthesizer Design Techniques

Sponsor: **MTT-22 Signal Generation and Frequency Conversion**

REGISTRATION

The Registration process is split into three tiers in order to better serve membership needs. The 1st tier is the Early Bird Registration. It begins Monday, 3 February and will last through Monday, 5 May. Early Bird registration provides an opportunity to register for the Symposium at the lowest possible cost. Immediately following the Early Bird is the 2nd tier or Advance Registration. It extends from Tuesday, 6 May through Friday, 30 May, just prior to the start of Microwave Week. The 3rd and final tier is the On-site Registration, starting on Saturday, 31 May, the first day of Microwave Week, and ending on Friday, 6 June.

Early Bird Registration: 3 February – 5 May (through midnight Hawaii Standard Time)

Advance Registration: 6 May – 30 May (through midnight Hawaii Standard Time)

On-Site Registration: 31 May – 6 June (through midnight Hawaii Standard Time)

Membership

Check the boxes of all organizations of which you are a member. To receive IEEE member rates, enter your member number and present your IEEE card upon check in at the conference. Registrants who do not have a current IEEE membership card at check in will be charged non-member rates. If you are not a member and would like to learn about the advantages of being a member and receiving the conference member rate, please visit <http://www.ieee.org/services/join> or call 1-800-678-IEEE. Please note that you must be a member at the time of registration to receive the member rate.

Registration Categories

Register online: <https://reg.mpassociates.com/reglive/PromoCode.aspx?confid=173>

Symposia

Microwave Week includes the IMS technical program and exhibit, as well as the RFIC Symposium (<http://rfic-ieee.org/>), ARFTG Conference (<http://www.arftg.org/>) and WAMICON (<http://wamicon.org/>).

Select the conference(s) you wish to attend.

- **SUPERPASS** registrants can attend as many technical sessions as they can from any of the three contributing organizations, IMS, RFIC, and ARFTG, as well as attend **TWO** full-day workshop (or half-day workshops, to equal two full-days), the Proceedings for IMS, RFIC, ARFTG, Workshop Electronic Proceedings for all three days and admission to the exhibits. In addition, the SUPERPASS will allow you to attend the RFIC Plenary Session, Round Table, Industry Showcase, and Reception on Sunday evening, the Kick-Off Reception on Monday, and the Awards Banquet on Wednesday. **WAMICON** is also included in the SUPERPASS registration.
- **RFIC Technical Sessions** are held on Monday and Tuesday. Registration includes admission to the RFIC Plenary Session, Round Table, Industry Showcase, and Reception on Sunday evening, the Kick-Off Reception on Monday, exhibits, and the electronic proceedings. The hard copy Digest is NOT included in the base registration but can be added to your registration for a nominal fee.
- **IMS Technical Sessions** are held on Tuesday, Wednesday and Thursday. Registration includes admission to the exhibits, the electronic proceedings, and the Kick-Off Reception on Monday.

REGISTRATION (continued)

- **ARFTG Technical Sessions** are held on Friday. Registration includes breakfast, lunch, electronic proceedings, and admission to the ARFTG exhibition. NEW this year, ARFTG registration will also allow access to the WAMICON technical sessions also being held on Friday. ARFTG Conference member rates are available to both ARFTG and IEEE members.
- **WAMICON 2014 will be on Friday.** The conference is co-located with the IEEE MTT-S International Microwave Conference (<http://www.ims2014.org/>) and ARFTG (<http://www.arftg.org/>). The conference will address up-to-date multi-disciplinary research needs and interdisciplinary aspects of wireless and RF technology. The program includes both oral and poster presentations. Registration includes breakfast, lunch, electronic proceedings. WAMICON registration will also allow access to the ARFTG technical sessions and exhibition that are also being held on Friday.

Exhibit Only Registration

Microwave Week hosts the largest exhibition of its kind with over 400 companies.

Exhibit only registration is available.

Additional Items to Add to Your Registration

1) Guest Registration

Attendees registered for the technical portion of the conference (SUPERPASS, IMS, RFIC, ARFTG and WAMICON) may add a Guest to their registration for an additional fee. Guest Registration includes access to the Hospitality Suite, Plenary Session, and Exhibit Hall, but does not allow access to Technical Sessions and Workshops. Select the Guest Registration tab below to add this to your registration. The name of the guest is added on the checkout page.

2) Awards Banquet

The MTT Awards Banquet will be held on Wednesday, 4 June from 18:00–22:00 at the Tampa Marriott Waterside Hotel in the Grand Ballroom. The evening will include fine dining, an awards presentation, and excellent entertainment. Major Society Awards will be presented.

3) Boxed Lunches

Optional boxed lunches are available for purchase by all attendees but are especially convenient for those attending the panel sessions or exhibit hall during lunchtime. It is encouraged to purchase boxed lunches before Microwave Week, as orders will not be available on-site. Refunds for lunches will not be available since these are ordered in advance.

4) Workshops

The workshop fee includes electronic proceedings for all the workshops being presented on that particular day. **For Early bird registration ONLY**, the workshop's printed notes are also included for the workshop you are registered for with the workshop's fee. For Advanced and On-site registration, the workshop's printed notes are **NOT** included in the workshop's fee and must be purchased separately.

REGISTRATION (continued)

Full-day workshops include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning workshops include a continental breakfast, and a morning refreshment break. Afternoon workshops include a lunch and an afternoon refreshment break.

5) Short Courses

The short course fee includes access to the short course selected and any materials that the short course organizers may provide.

Full-day short courses include a continental breakfast, a morning refreshment break, a lunch, and an afternoon refreshment break. Morning short courses include a continental breakfast, and a morning refreshment break. Afternoon short courses include a lunch and an afternoon refreshment break.

6) Two Full-Day Workshop Registration

Purchase two full-day workshops by selecting the option titled “TWO FULL-DAY WORKSHOP REGISTRATION” and receive the electronic proceedings for all three days of workshops (Sunday, Monday, and Friday). The All-Workshop electronic proceedings are not available for individual sale.

7) Payment

Individual payment must accompany the registration form and is payable in U.S. dollars only, using a personal check drawn on US bank or credit card (VISA, MasterCard, or American Express) or bank wire transfer. Personal checks must be encoded at the bottom with the bank account number and check number. Bank drafts, cash, international money order and purchase orders are UNACCEPTABLE and will be returned. Please make checks payable to “2014 IEEE IMS”. Written requests for refunds will be honored if received by 5 May 2014. Refer to the Refund Policy for complete details.

8) Refund Policy

Written requests received by 5 May 2014 will be honored. Refund requests postmarked after this date and on-site refunds will be generated only if an event is cancelled. This policy applies to the registration for the symposium sessions, workshops, digests, extra electronic proceedings, awards banquet and boxed lunches. Please state the pre-registrants name and provide an email when requesting a refund. Address your requests to:

MTT-S Registration
Nannette Jordan
MP Associates
1721 Boxelder St., Ste. 107
Louisville, CO 80027, USA
nannette@mpassociates.com

ON-SITE REGISTRATION

On-Site registration for all Microwave Week events will be available at the Tampa Convention Center Second Lobby. Registration hours are:

Date	Time
Saturday, 31 May	08:00–18:00
Sunday, 1 June	07:00–19:00
Monday, 2 June	07:00–19:00
Tuesday, 3 June	07:00–18:00
Wednesday, 4 June	07:00–18:00
Thursday, 5 June	07:00–16:00
Friday, 6 June	07:00–09:00

Exhibit Only Registration

Exhibit only registration is available.

Press Registration

Credentialed press representatives are welcome to register without cost, receiving access to IMS technical sessions and exhibits. Digests are not included. The Press Lounge will be available from Monday through Thursday of Microwave Week and it located on the third level in room 31.

ARFTG and WAMICON Registration

Late on-site registration will be available at the Tampa Convention Center Second Lobby on Friday, 6 June from 07:00 to 09:00. If at all possible, please pre-register earlier in the week.

REGISTRATION RATES

Registration Rates in USD	Early Bird (3 Feb–5 May)		Advance (6–30 May)		On-site (31 May–6 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Superpass						
Superpass	\$1,175	\$1,685	\$1,340	\$1,925	\$1,530	\$2,200
IEEE Life Member (Retiree)	\$765		\$870		\$1,015	
Student	\$765	\$795	\$870	\$900	\$1,015	\$1,045
RFIC Symposium						
RFIC Sessions	\$240	\$340	\$270	\$390	\$290	\$425
IEEE Life Member (Retiree)	\$160		\$180		\$200	
Student	\$160	\$190	\$180	\$210	\$200	\$230
IMS						
IMS Sessions	\$435	\$650	\$505	\$755	\$585	\$865
IEEE Life Member (Retiree)	\$80		\$90		\$105	
Student	\$80	\$150	\$90	\$160	\$105	\$175
Single Day Registration	\$220	\$325	\$255	\$375	\$295	\$445
ARFTG Conference or WAMICON						
ARFTG or WAMICON Sessions	\$225	\$335	\$260	\$390	\$295	\$445
IEEE Life Member (Retiree)	\$155		\$180		\$200	
Student	\$155	\$185	\$180	\$210	\$200	\$230
Exhibit Only						
Exhibition Only Pass	\$25	\$25	\$25	\$25	\$30	\$30
Wednesday Exhibition Only Pass	free	free	free	free	free	free
Guest Badge	\$20	\$20	\$20	\$20	\$20	\$20

REGISTRATION RATES (continued)

Registration Rates in USD	Early Bird (3 Feb–5 May)		Advance (6–30 May)		On-site (31 May–6 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Full Day Short Course						
Full Day Short Course	\$295	\$445	\$345	\$510	\$400	\$600
IEEE Life Member (Retiree)	\$210		\$240		\$275	
Student	\$210	\$235	\$240	\$265	\$275	\$300
Half Day Short Course						
Half Day Short Course	\$205	\$305	\$240	\$360	\$275	\$415
IEEE Life Member (Retiree)	\$145		\$170		\$195	
Student	\$145	\$165	\$170	\$190	\$195	\$215
Full Day Workshop						
Full Day Workshop	\$170	\$250	\$185	\$270	\$230	\$345
IEEE Life Member (Retiree)	\$130		\$140		\$160	
Student	\$130	\$150	\$140	\$160	\$160	\$180
Half Day Workshop						
Half Day Workshop	\$90	\$130	\$100	\$145	\$120	\$175
IEEE Life Member (Retiree)	\$65		\$70		\$85	
Student	\$65	\$85	\$70	\$90	\$85	\$105
2 Full Day Workshops or Equivalent (includes 3 USBs)						
2 Full Day Workshops or Equivalent	\$445	\$655	\$485	\$715	\$605	\$895
IEEE Life Member (Retiree)	\$330		\$360		\$410	
Student	\$330	\$350	\$360	\$380	\$410	\$430
Printed Workshop Notes	included	included	\$20	\$30	\$30	\$45

REGISTRATION RATES (continued)

Registration Rates in USD	Early Bird (3 Feb–5 May)		Advance (6–30 May)		On-site (31 May–6 June)	
	Member	Non-Member	Member	Non-Member	Member	Non-Member
Proceedings						
RFIC USB	\$50	\$75	\$60	\$90	\$70	\$105
RFIC Digest (Hard Copy)	\$50	\$75	\$60	\$90	\$70	\$105
IMS USB	\$50	\$75	\$60	\$90	\$70	\$105
ARFTG USB	\$50	\$75	\$60	\$90	\$70	\$105
Evening Events						
RFIC Sunday Evening Only (includes: RFIC Plenary Session, Round Table and Reception)	\$50	\$75	\$50	\$75	\$65	\$85
Award Banquet	\$55	\$55	\$65	\$65	\$75	\$75
Lunch						
Monday Boxed Lunch	\$25	\$25	\$25	\$25		
Tuesday Boxed Lunch	\$25	\$25	\$25	\$25		
Wednesday Boxed Lunch	\$25	\$25	\$25	\$25		
Thursday Boxed Lunch	\$25	\$25	\$25	\$25		

VISA INFORMATION

United States Visa Advisory

The United States has updated its visa policy for increased security. As a result, it now takes longer to obtain a visa. Advance planning by travelers is essential to avoid frustration and disappointment.

- Review your visa status to find out if you need a U.S. visa or a visa renewal.
- Plan to submit your visa application well in advance of your intended departure date.
- Contact your nearest U.S. embassy or consulate for current time estimates and recommendations.
- Visit the embassy or consular section website to find important information on how to schedule an interview appointment, finger scanning — if required — and pay fees. An interview is required as a standard part of processing for most visa applicants.

Visa Waiver Program (VWP)

The Visa Waiver Program (VWP) enables nationals of 36 participating countries to travel to the United States for tourism or business (visitor [B] visa purposes only) for stays of 90 days or less without obtaining a visa. The program was established to eliminate unnecessary barriers to travel, stimulating the tourism industry, and permitting the Department of State to focus consular resources in other areas. VWP eligible travelers may apply for a visa, if they prefer to do so. Nationals of VWP countries must meet eligibility requirements to travel without a visa on VWP, and therefore, some travelers from VWP countries are not eligible to use the program. VWP travelers are required to have a valid authorization through the Electronic System for Travel Authorization (ESTA) prior to travel, are screened at the port of entry into the United States, and are enrolled in the Department of Homeland Security's US-VISIT program.

Currently, 36 countries participate in the Visa Waiver Program, as shown below:

Andorra	Hungary	New Zealand
Australia	Iceland	Norway
Austria	Ireland	Portugal
Belgium	Italy	San Marino
Brunei	Japan	Singapore
Czech Republic	Latvia	Slovakia
Denmark	Liechtenstein	Slovenia
Estonia	Lithuania	South Korea
Finland	Luxembourg	Spain
France	Malta	Sweden
Germany	Monaco	Switzerland
Greece	the Netherlands	United Kingdom

For more information, see http://travel.state.gov/visa/temp/without/without_1990.html.

VISA INFORMATION (continued)

Passports

A passport with a validity date of at least six months beyond the applicant's intended period of stay in the U.S. is required. If more than one person is included in the passport, each person desiring a visa must make a separate application. Please check with the website, <https://www.cbp.gov>, to confirm that your passport is compliant. Temporary Passports will likely merit special scrutiny. To avoid complications, check with your local US consular offices, well ahead of your intended departure dates.

Visa Letters

A visa support letter can be provided for authors and registered attendees upon request. Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing. Spouses and guests requiring visa assistance must be registered for an IMS Guest Program Event (information to be posted shortly).

Please submit your requests for letters of support well in advance of your interview dates to allow sufficient time for processing.

For additional visa assistance, please contact Zaher Bardi at imn.epiphany@gmail.com.

Disclaimer

This information is provided in good faith but travel regulations do change. The only authoritative sources of information are the U.S. Government website at http://travel.state.gov/visa/visa_1750.html.

SOCIAL EVENTS/GUEST PROGRAM

MONDAY, 2 JUNE 2014

Welcome Celebration: 19:00–20:30

IMS2014 starts with a welcome celebration on Monday for all attendees, which will be hosted at the convention center immediately following the IMS2014 Plenary Session. A water ski show will be the highlight of this event.

MONDAY, 2 JUNE – FRIDAY, 6 JUNE 2014

Guest Lounge at Tampa Marriott Waterside Hotel

The guest lounge will be located in a big room with bright windows inside the Tampa Marriot Hotel Waterside. Continental Breakfast and refreshments will be provided for all guests. Several IPADs will be provided for the guest to browse internet or play games. The guest lounge serves as a hub for guests and a starting point for tours around the city.

TUESDAY, 3 JUNE 2014

Ham Radio Social: 17:30–19:00

Ham Radio Social will take place in the conference headquarter hotel, Tampa Marriot Hotel Waterside.

Women in Microwaves Reception: 18:00–19:30

The Women in Microwaves Reception will be held in Tampa Bay History Center, just a five minute walk from the Marriott Tampa Waterside Hotel.

Young Professionals/Student Reception: 18:30–20:30

The Young Professionals/Student (formerly Graduate of Last Decade — GOLD) reception will be hosted in the Florida Aquarium.

All three events are within the walking distance from the convention center, which are 250 ft (1 min), 0.3 mile (6 min), and 0.7 mile (14 min) away, respectively.

WEDNESDAY, 4 JUNE 2014

Industry Hosted Cocktail Reception: 17:30–18:30

The Industry-Hosted Reception is scheduled right outside the exhibition floor on Wednesday, 4 June 2014 right before the MTT-S Awards Banquet.

SOCIAL EVENTS/GUEST PROGRAM (continued)

Awards Banquet: 18:30–21:00

The MTT-S Awards Banquet will be hosted in the headquarter hotel and feature exciting entertainment.

THURSDAY, 5 JUNE 2014

Closing Ceremony: 17:45–18:00

The closing ceremony will immediately follow the Thursday closing session at the Tampa Convention Center.

IMS2014 COMPANION TOURS

Tours will be departing from the Marriott Waterside Hotel & Spa. Guests should be ready to depart from the Marriott Hotel lobby 15 minutes prior to scheduled departure time.

To register for the following tours, please visit <http://eventionsfl.com/2014IMSReg>

* Tour pre-registration cut-off is Monday, 26 May 2014 at 17:00 EDT.

MONDAY, 2 JUNE 2014

Florida Aquarium & Dolphin Eco-Tour

09:30–14:30

(\$68 per adult, \$56 per child up to 11 years old, free for 3 and under)

The Florida Aquarium combines education and fun for guests of all ages in this one-of-a-kind facility. You will be introduced to more than 4,300 fascinating aquatic animals and plants that call Florida home and even some unique species from exotic lands...all in air-conditioned comfort. You will explore the wondrous journey of water from its quiet underground source out to the deep, dark realms of the open sea.

Includes: Deluxe Round Trip Transportation, Uniformed Tour Guide, Admission to Aquarium, 90 minute Eco-tour Cruise, liability insurance, all applicable taxes and driver gratuities.

TUESDAY, 3 JUNE 2014

Neighborhoods of Tampa

09:15–13:00

(Price: \$48 per adult, \$43 per child up to 12 years old, free for 3 and younger)

A city rich in history, abundant with architecture and bountiful ethnic charm: TAMPA BAY. Today you will board the coach at the hotel and embark on a narrative tour of Tampa. You will have the opportunity to enjoy all that TampaBay has to offer, such as Bayshore Boulevard, Hyde Park, Henry Plant Museum and Ybor City.

SOCIAL EVENTS/GUEST PROGRAM (continued)

Includes: Deluxe Round Trip Transportation, Uniformed Tour Guide, Narrative City Tour, Walking tour of Ybor City, Admission and Docent Tour of the Henry Plant Museum and Ybor State Museum, Bottled Waters, liability insurance, all applicable taxes and driver gratuities..

TUESDAY 3 JUNE, WEDNESDAY 4 JUNE & THURSDAY 5 JUNE 2014 Busch Gardens and Lowry Park Zoo (round trip transportation only)

09:00–16:00

(Price per person: \$24)

This 360-acre African-Themed family entertainment park ranks among the top zoos in North America. Featuring thrilling rides, shopping and restaurants with zoological habitats interwoven amongst lush landscaping and other park attractions. Your trip to Busch Gardens is filled with possibilities, which include ongoing shows ranging from the Dolphins to Exotic Birds and musicals. For the daring a ride on the Southeast's largest not to mention fastest roller coaster is a must or experience SheiKra which carries riders up 200 feet at 45 degrees, then hurtles them 70 mph back toward the ground at a 90-degree angle. It is the first coaster of its kind in the Americas and only the third in the world. Or Launch into the ultimate excitement of Cheetah Hunt, the newest roller coaster experience that coaster enthusiasts can't stop talking about. Hold tight as this thrill machine takes riders through a wild adventure just like a Cheetah on the hunt for his prey over towering rises, breathtaking plunges and a trio of launches at speeds pushing 60 mph. We recommend comfortable, casual clothing, as many of the rides are wet ones!

WEDNESDAY, 4 JUNE 2014

Clearwater Beach Shuttle (round trip transportation only)

09:00–16:30

(Price per person: \$37)

Rated the Best Beach Town in Florida by USA Today readers, Clearwater Beach has many offerings to make your day perfect. With miles of pristine white sands, a pedestrian path right off the beach features shops and restaurants to keep hunger away during a day of fun and sun. You'll be sure to have a day in paradise as you drift to sleep with the sound of crashing waves or play Frisbee with friends under the warm Florida sun.

Big Cat Rescue

10:00–13:30

(Price: \$63 per adult/child, *children under 10 not allowed on tour)

You will be visiting one of the world's largest sanctuaries for wild cats. Big Cat Rescue is a 501(c)(3) non-profit. They receive no government funding and rely on the generosity of thousands of individual donors to support the cats. They are an educational sanctuary, which means that their dual mission is both to take care of the cats and to educate the public so they can eliminate the abuse and abandonment that causes them to need a sanctuary. You will enjoy a one hour walking tour and will learn about the cats and enjoy seeing them from distances as close as 3–6 ft away. Cameras and Video Recorders are allowed (no tripods allowed).

SOCIAL EVENTS/GUEST PROGRAM (continued)

- * Driving time to/from Big Cat is approximately 20–30 minutes each way;
- * This is a walking tour on non-paved roads, so comfortable walking shoes recommended;
- * A waiver release form will be provided prior to the tour;
- * A waiver release form must be signed by all guests before entering the sanctuary;
- * Extra time has been allotted for guests to shop in the gift shop at the sanctuary.

Lunch and Cooking Demo by the StoneChef

11:00–14:00

(Price: \$75.00 per person, price does not include wine)

The heart of StoneChef Catering complex has a state of the art Theatre Kitchen which Chef Anthony custom designed to accommodate maximum productivity while sharing the drama of seeing his haute cuisine come to life. A specially designed lunch will be created and enjoyed by all.

THURSDAY, 5 JUNE 2014

Discover Art & History on Tampa's Riverwalk

09:45–13:45

(Price: \$49 per adult, \$45 per child up to 12 years old, free for 3 and younger)

Tampa's Riverwalk is the newest addition to the downtown area and houses numerous museums for guests to enjoy. Today guests will explore two of the most popular museums, Tampa History Museum and the Florida Museum of Photographic Art.

Includes: Deluxe Round Trip Transportation, Uniformed Tour Guide, Admission to the Florida Museum of Photographic Art and Admission to the Tampa History Museum, Free time to Shop at both museum gift shops, liability insurance, all applicable taxes and driver gratuities.

Westchase Golf Club

Minimum # of guests: 4

(Price per person: \$119, estimated time: 6 hours)

Since opening in the fall of 1992, Westchase Golf Club has established itself as one of Tampa Bay's upscale golf facilities. The 6,710 yard, Par-72 Westchase course was designed by nationally known architect Lloyd Clifton. The Westchase course takes full advantage of its natural setting and the well-manicured fairways and greens of this course surrounded by natural wetlands, wooden bridges and bulkheads are what set it apart. With its 9,500 sq. ft. clubhouse, full-service dining room, and fully stocked pro shop, Westchase offers a country club atmosphere along with first-class service. Located in northwest Tampa, the golf club has established itself as one of Tampa Bay's best upscale golf facilities.

Includes: Round Trip Transportation, Uniformed Golf Escort, Green Fees, Cart Rental, individual tee time play, liability insurance, all applicable taxes and driver gratuities.

SOCIAL EVENTS/GUEST PROGRAM (continued)

Tournament Players Club of Tampa Bay

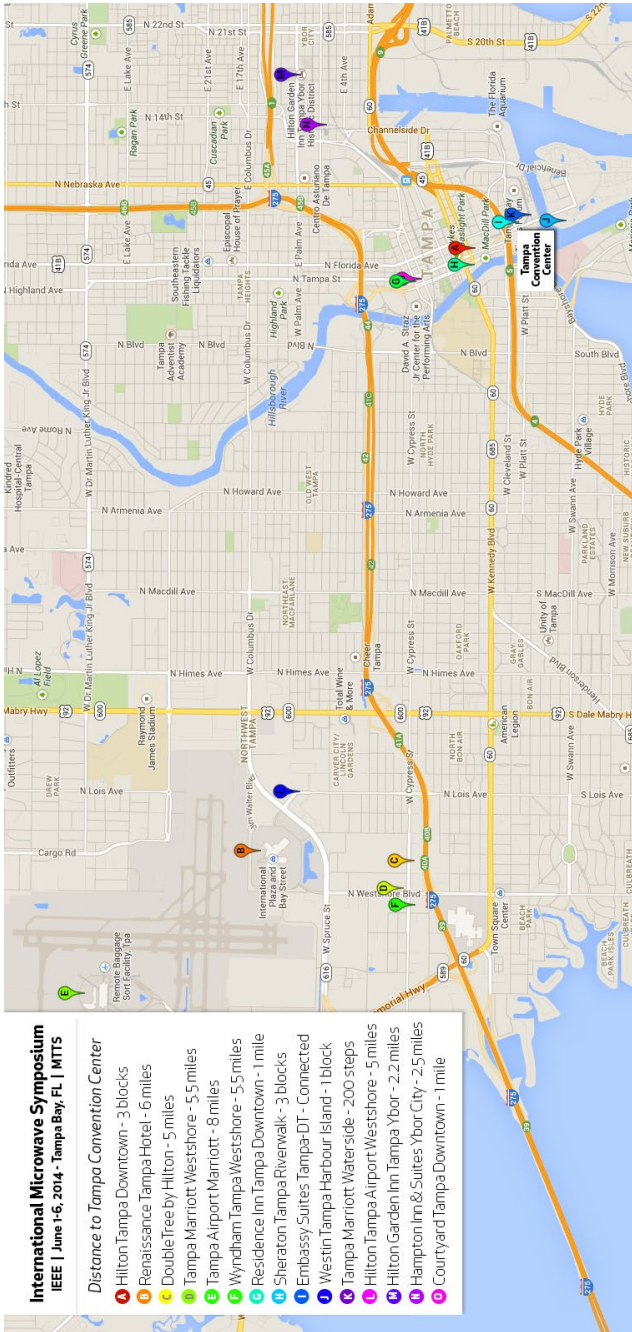
Minimum # of guests: 4

(Price per person: \$165, estimated time: 6 hours)

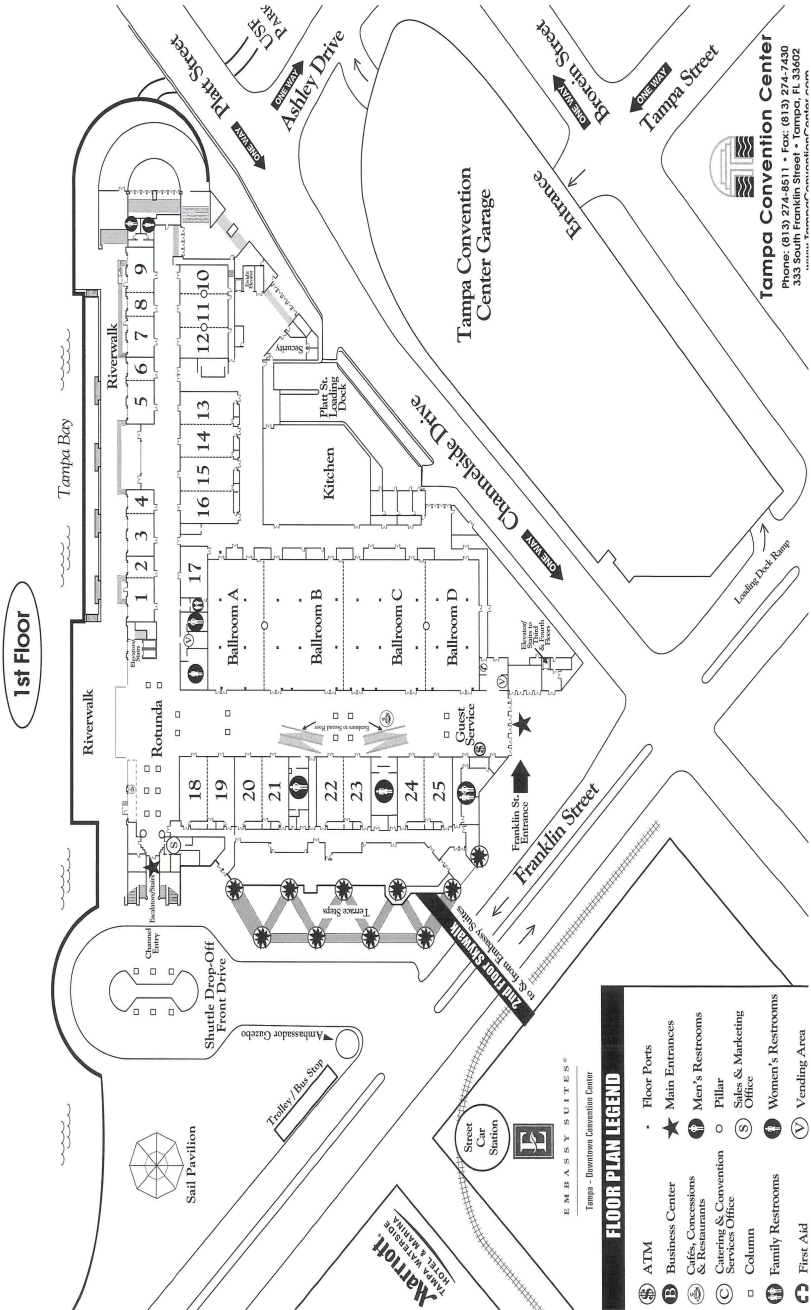
The area's premier daily fee facility, the TPC of Tampa Bay is conveniently located 20 minutes northwest of Tampa International Airport. Part of a network of courses owned and operated by PGA TOUR Golf Course Properties, the course is home to the Verizon Classic, one of the most successful Senior PGA TOUR events.

Includes: Round Trip Transportation, Uniformed Golf Escort, Green Fees, Cart Rental, individual tee time play, liability insurance, all applicable taxes and driver gratuities.

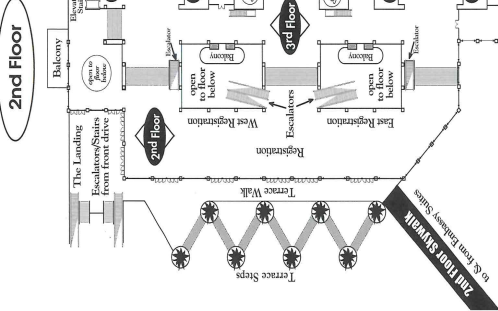
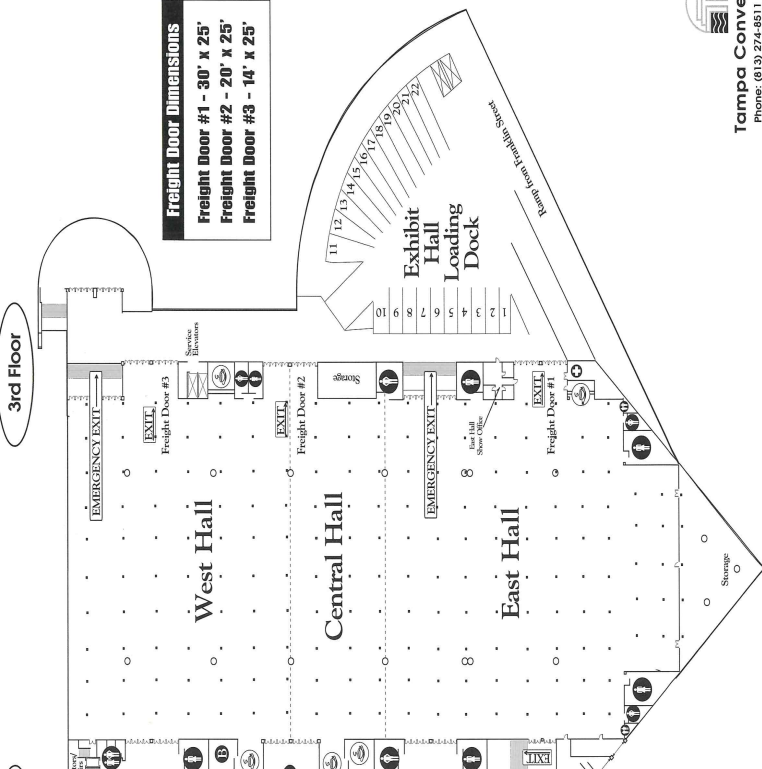
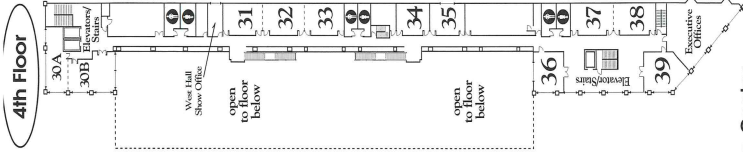
DOWNTOWN TAMPA MAP



CONVENTION CENTER MAPS



CONVENTION CENTER MAPS (continued)



- FLOOR PLAN LEGEND**
- Ⓐ ATM
 - Ⓑ Business Center
 - Ⓒ Conventions & Restaurants
 - Ⓓ Catering & Convention Services
 - Ⓔ Family Restrooms
 - Ⓕ First Aid
 - Ⓖ Floor Ports
 - ★ Main Entrances
 - Ⓗ Men's Restrooms
 - Ⓘ Pillar
 - Ⓢ Sales & Marketing Office
 - Ⓥ Vending Area
 - Ⓗ Women's Restrooms



Tampa Convention Center
 Phone: (813) 274-8383 Fax: (813) 277-3500
 305 East Bay Street, Tampa, FL 33602
 www.TampaConventionCenter.com

IEEE

445 Hoes Lane
Piscataway, NJ 08854, USA

2014 RFIC Symposium
Tampa Bay, Florida, USA
1–3 June 2014



PROGRAM